Network Server Hardware Developer Notes

Chapter 1 Network Server Overview

1. Introduction

Network Servers are the first servers from Apple to be designed as high performance, scalable, reliable, and serviceable servers targeted at Unix accounts serving Macintosh Desktops. This specification is unfortunately not one-stop shopping, owing to the architectural origins of the Network Servers in the PowerMac 9500 family. Therefore much of the hardware detail which is fully documented in the PowerMac family is not repeated here. Instead, unique hardware interfaces are described

1.1 Product Family

1.1.1 Not 64-bit ready

The Apple Network Server is not meant to accomodate a 64-bit implementation based on the 620 microprocessor.

1.1..2 Network Server Differentiation

The Network Server will be differentiated into two product price points, distinguished by:

- More drive Bays
- Redundant Power Supplies
- Higher Clock frequency
- More Cache memory

1.2 Product Position

1.2.1 Target Operating System

AIX 4.1, keeping pace with IBM updates as soon as practical.

1.2.2 Target Customers

Publishing customers and others who are already using Unix to serve Macintosh desktops.

1.2.3 Target Competition.

Sun Microsystems, SGI, and to some extent Windows NT encroachments.

1.2.4 Target Performance

Best price performance in the industry running a supported, full featured Unix. Validated by running Appletalk and IPT uShare and/or Helios Ethershare; database; webstones.

1.3 Network Server FCS Features

- 604 µP at 132 MHz or 150 MHz
- Seven half-height fast/wide drive bays
- Two “Geo Ports” (9 pin serial)
- Dual SCSI Fast and Wide
- Six Slots PCI 32-bit 5 Volt
- 100 Mb/s 100BaseT card and 10BaseT card
- Expandable Main Memory to 512 Mbyte
- Internals physically secured with lock
- Optional 425W redundant power supply
- New product design with "30 second component access"
- Hot swap fans
- Standard 1.44 M Floppy
- Ethernet (AAUI)
- Mac Compatible SCSI-1
- ADB
- LCD display for diagnostics
- 325 Watt modular power supply
- On Board video to 1024x768 @ 8-bits
- Optional RAID card
- Rack Mount capability

1.4 Collateral Documentation

Power PC Architecture Books 1-3
Books 4--601, 603, 604
Technical Documentation for PowerMac 9500 Family
Designing Cards and Drivers for the Network Server
Open Firmware Specification for the Network Server

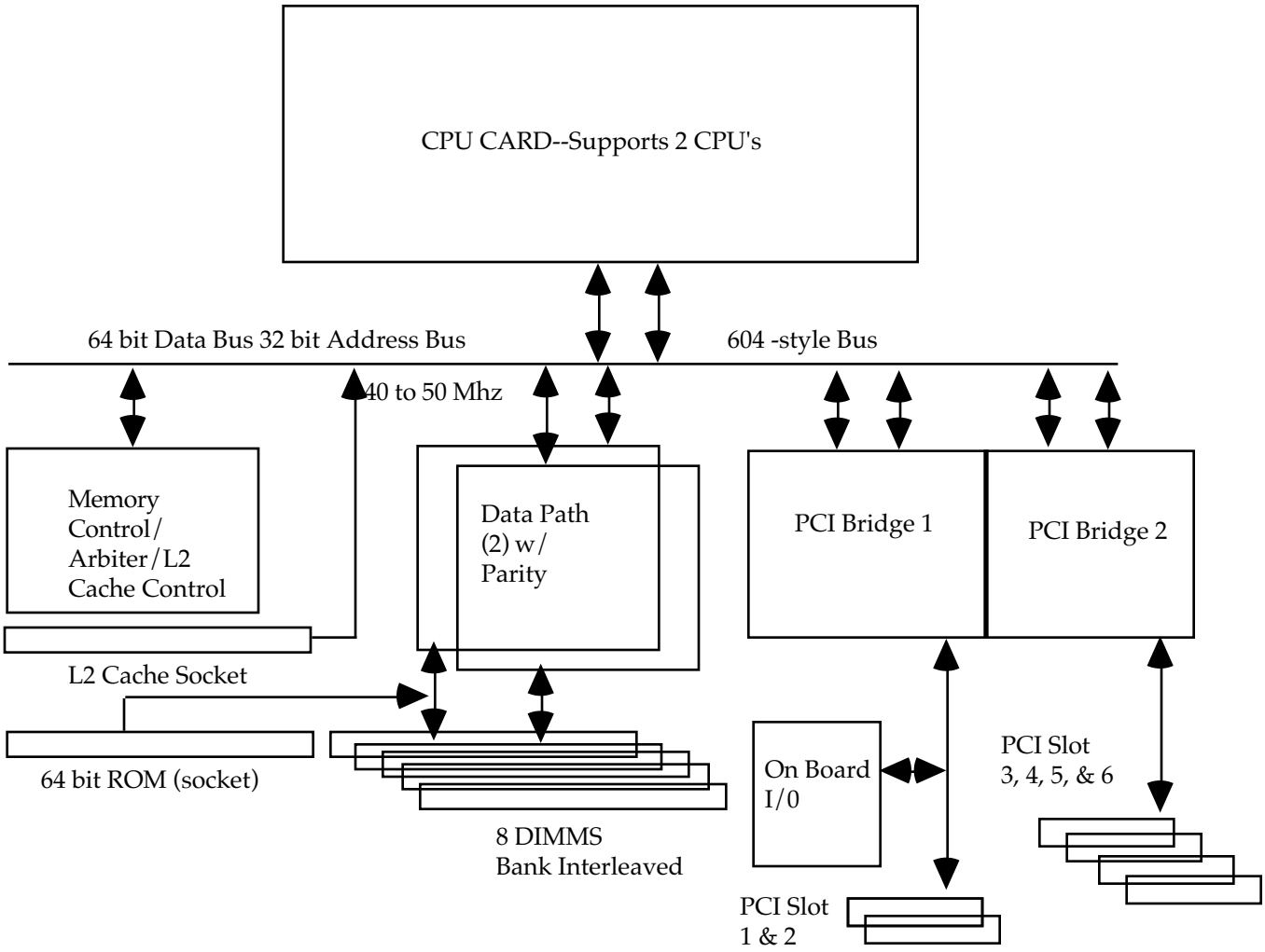
Chapter 2 Functional Description

2. Network Server Architecture

This chapter details the salient features of the Network Server vis a vis the PowerMac 9500 architecture machines.

2.1 Block Diagram

The block diagram of Figure 1 maps out the essential functional blocks for Network Server and their interconnections across various interfaces. For greater detail refer to PowerMac 9500 family documentation.



Programmability follows the MacRISC architecture with enchancements made for server needs. This document focuses mainly on the differences.

2.2 Network Server Quick I/0 Primer

Network Server will use Grand Central to provide non-critical I/O. This is justified by reasons of cost, and commonality with MacRisc. Use of DBDMA will provide some software commonality that may reduce software port time.

Note that Grand Central appears as a PCI 2.x-compliant device. System initialization code must provide a base address to PCI devices via configuration cycles. Grand Central addresses live within a 128Kbyte space set up from the initialized base address; refer to the Network Server memory map.

All register accesses will be default swapped by Bandit. Multi-byte data structures (such as DBDMA commands) will need to be be byte reversed by software for consistency.

The only exception to this is for 16 bit audio samples transferred through Grand Central; a register bit can be written which will do a byte lane swap so that the data will appear correctly in a big endian main memory system.

2.2.1 DBDMA

The following is provided as a quick reference.

Grand Central implements only the base DB DMA architecture. The following optional features are not implemented:

- 64-bit addressing. (CommandPtrHi, DataPtrHi registers are not implemented.)
- Memory to memory transfers. (OffsetHi, OffsetLo registers are not implemented.)
- Multiple "transfer-modes". (Memory addresses always increment, block transfer size is always system defined, transfers are always coherent.)
- Special "Event" and "Management" channels. (Device registers, and interrupts are used to implement these functions.)

2.2.1.1 Descriptor Basics

Descriptors are memory resident data structures which provide commands to DBDMA channels within Grand Central (or other future device that supports the architecture). They are succintly described by the following diagram:

Operation:	Command	Count	Address
Result:	Pointer to some status location		

2.2.1.2 Register Format

Channels that access descriptors in main memory must be explicitly programmed to do so. This is accomplished through the DBDMA Channel Register. Grand Central supports 10 such channels for on-board devices.

Register Address	Description	Interface
Device1 Base Addr	Control register	Device1
+ 4 bytes	Status register	Device1
+ 8 bytes	CCL Pointer High	Device1
+12 bytes	CCL Pointer Low	Device1
	[etc.]...	

2.2.1.3 DBDMA commands

The following is a brief description of the important commands supported by DBDMA channels.

Output_more, Output_last
These commands are used to transfer data from memory to the particular interface.

Input_more, Input_last
Complementary to the Output_more and Output_last commands are the Input_more and Input_last. These commands are used to transfer data in from the particular interface into memory.

Store_Immediate command
This command provides a mechanism to allow the CCL to store a 32/64 bit value into a memory mapped location like a controller's register(s). This command can be functionally equivalent to writing the device with the processor except that it is precisely tied to the activities of the CCL

Command (16)	Count (16 bits)	Address (32 bits)
Store_Immediate	Count	&Somewhere
data[0..7]		

Stop command
The Stop command is defined to simply end the CCL. It does NOT return any status, interrupt, or other information except that the Run bit in the Status register will be cleared.

Jump command
This is an abbreviated version of the "full-up" one in the DBDMA document. The Jump command is used to change the CCL Pointer value.

Command (16)	Count (16 bits)	Address (32 bits)
Jump	0000	newCCLPtr
status pointer		

2.2.2 Grand Central Register Map

For details please refer to the PowerMac 9500 documentation. For a list externally attached Grand Central devices see the Network Server Address Map below.

Note that Grand Central implements a Generic Bus (GBUS) which provides six chip selects and write enable which the Network server uses for devices such as NVRAM, Ethernet PROM, board registers, and the LCD.

2.3 Network Server Protection Devices (Safe Server)

Network Server has several thermal trips which software can use to:
- Provide warning of impending shutdown;
- Shutdown gracefully on its own;
- Ignore and hope for the best.

2.3.1 Thermal Sensor

The processor card contains a thermal management device, which has two settable trip points. These trip points are read as bits in a GBUS register. Normally the first trip point is set prior to hardware

vulnerability, at a point that would normally correspond to either a blocked airflow or a slowing fan. Software would normally issue warnings to console, or send email for example. The second trip point is set slightly beyond worst case thermal ratings for the normal operation of hardware and would require software-initiated shut down.

2.3.2 Power Supply

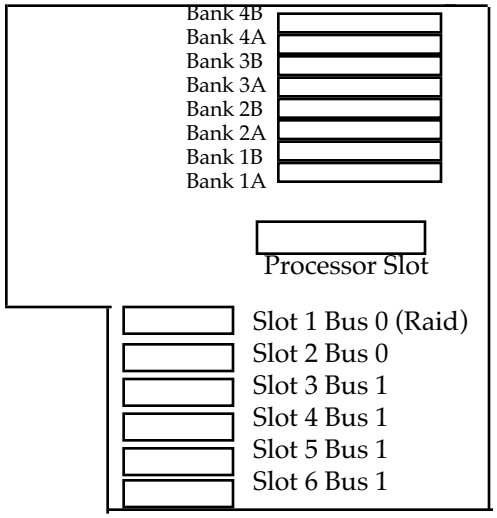
Network Server has the hooks to accept a Network Server Redundant Power Supply. With this power system, Network Server has thermal trips and fault signals for two power supplies. With the standard Network Server supply, only a thermal trip signal is provided. These also are provided as bits in a GBUS register.

2.3.3 Fan Fail

Network Server provides failure signals for its two fans. Software can notify the administrator of fan failure, however it is likely that operation will not continue for very long. A common fan failure mode is decreased air flow, which can be detected separately through the thermal sensor trip.

2.4 Logic Board

The following is representational only. For mechanical drawings contact Developer Support.



Note that in the following section Main Logic Boards should consume a minimum of 3 A @ 5 volts for start up conditions. This could be a special requirement on 3 volt logic boards moving forward.

2.4.1 Parity Memory

Parity memory is supported by a modification of the PowerMac 9500 data path chip. It writes and reads byte-wide parity for memory accesses only. ROM and SRAM are not parity protected. The boot ROM sets DRAM timing based on two factors: the detected bus speed and detected parity. If parity is detected, 60 ns timing is set.. If parity is not detected, 70 ns timing is set. At 50 MHz, 70 ns timing is approximately a 20% memory bandwidth penalty.

Eight DIMM slots are provided; production ROMs through (TBD) August 1996? provide decoding of up to 512 Mbytes (Eight 64 Mbyte or four 128 Mbyte DIMM's). Sixty-four megabit technology is recommended for DIMMs of this size to reduce bus loading at 60 ns timing. FCT technology should be used for buffers; ACT is specifically not supported.

2.4.2 Cache Memory

Network Serves support the cache DIMM pinout of the PowerMac 8500. However, the ROM will turn on "fast L2" mode for bus speeds 44 MHz and below, which decreases latency to the L2 by one cycle. Tag and cache memory speeds need to be 8ns and 11 ns or better, respectively.

2.5 Power Supply Budgeting

2.5.1 Network Server 500 Power Supply

Load Conditions	+5 V	-12V	+12 V	+3.3 V	Total Power
Minimum currents:	3 A	0 A	0 A	0 A	15 W
Maximum currents:					
Maximum load #1:	28 A	0.6A	11 A	10 A	325 W
Maximum load #2:	18 A	0.6 A	11 A	25 A	325 W
Peak load:			16 A		

Note that internal SCSI hard drives should perform delayed spin up. There is adequate margin in the +12 V output for peak load, however, so that there is little chance of start up problems should the customer ignore this recommendation. Remote start enabled is the desired configuration for drives. For many highly configured Network Server systems, the power supply needs might exceed the capabilities of the 325 W device. Engineering rules should be developed to help explain these limitations.

2.5.2 Network Server 700 Power Supply

Network Server 700 provides an optional redundant supply system. This provides higher power and a power backplane. The specifications for load are as follows:

Load Conditions (v)	5	-12	12	3.30	Total Power
Minimum currents:	3	0	0	0.00	15 W
Maximum currents:					
Maximum load #1:	44	0.6	13	13.00	425 W
Maximum load #2	19	0.6	13	50.00	425 W
Peak load:			18		

Note that the installation of an optional redundant power supply does NOT increase these limits. The redundant supply system will current share to increase longevity. Power supplies are hot swappable.

2.6 Keyswitch

Network Servers provide a keyswitch function which both Open Firmware and the Operating System interact with to set a boot path, as well as provide some lock-out of functionality.

Open Firmware detects both the service and the locked positions of the key. If the key is in the locked position, Open Firmware prevents all parameter and NVRAM resets (CMD-OPT-P-R). In the Service mode only, Open Firmware will erase all AIX-related booting parameters with CMD-OPT-P-R. In the normal mode, this keyboard combination will erase the Macintosh parameter RAM only.

2.7 NVRAM

The non-volatile RAM is used by Open Firmware, POST, and the operating system. Boot Paths, POST results, Open Firmware patches, and much other information is stored here. Removal of a battery from the Main Logic Board will reset all parameter and NVRAM to default values. Parameter RAM is a separate part of a Power Monitor IC, and this is where date, time, and boot beep volume are stored. The fail-safe red button on the logic board resets parameter RAM but not NVRAM; it will also clear all pending power messages and set the Power Monitor IC to ide.

2.8 On-Board Video

The Network Server implements a Cirrus Logic 54M30 video controller, which provides a bit-mapped 1Mbyte DRAM frame buffer. This controller implements only a little-endian window into the packed-pixel frame buffer, hence Big Endian operating systems are limited to 8 bits per pixel unless low-level transformation routines are written. The buffer will support 1024x768 at 8 bits, however many monitor modes are supported. Extended RAS is configured with adequate DRAM speed to accomplish 68 MHz clocking. Hardware acceleration and cursors are available requiring software implementation. Pure bit-mapped mode will undoubtedly be visibly slow and require signficant CPU utilization. Screen savers should be discouraged for maximum system performance.

The external hardware interface is standard VGA with DDC-2 monitor sense. However the operating system may or may not interact with DDC. Care must be taken to assure the monitor is multi-sync and compatible with the selected resolution and refresh rate.

2.9 Fast/Wide SCSI

The network servers implement two fast/wide SCSI channels (up to 40 Mbytes/sec) using the Symbios Logi 53C825A. These devices use SCRIPTS based DMA for high performance with low overhead. For details on the phyical implementation of SCSI on the Main Logic Board refer to Chapter 7.

2.10 Low-Skew Clocking

Network Server processors and Network Server motherboards need to be designed to minimize skewing of the various clocks as the system bus behaves as a synchronous design. To enable processor daughtercard upgrades, a means is required by which the motherboard acquires clocking from the processor card. Processor clocking is synchronous to ASICs on the main logic board. Current and future 604 processors have needed a delay line to accomodate the 604's 0 ns output hold time, which is inadequate for the system ASICs. Supported system speeds are 40-50 MHz.

Network Server processor cards need to provide system clock to the main logic board. This should be from a fast transition device (F family or better). The form factor is described in the mechanical specifications.

2.11 Processor Cards

Network server processor cards are implemented on a large form factor to accomodate multipe CPU's and greater power dissipaton. Power and cooling for up to about 70 Watts is achievable, given adequate heat sinking. An approximate rule of thumb for 40 degrees C ambient is 200 linear feet/minute of air flow with the standard fan. Note that thermal design is complex with many variables like processor die temperature, peak vs. average dissipation, heat sink position in the airflow, etc. Rules of thumb do no substitute for a complete analysis.

Chapter 3 Network Server Initialization

3. Network Server Initialization

This chapter is a very concise statement of the function of POST and Open Firmware in Network Server. Please refer to the Open Firmware specification for Network Server.

The basic flow for Network Server Initialization is as follows:

A processor comes out of hardware reset and fetches the reset vector FFF00100. Hammerhead maps this to ROM space and non-cacheable accesses to the ROM begin. The first code executed will determine whether the processor is the primary processor, in which case it will continue with machine initialization, power-on self-test (POST) and then launching Open Firmware; or if the processor is the secondary it will enter a spin-wait for an interprocessor interrupt. Note that the way software accesses the dual processor hardware implementation is the same as in the PowerMac 9500 family , although the physical connector and card form factor are specific to the Network Server.

POST and Open Firmware will attempt:

- To map and test main memory in conjunction with Hammerhead Registers
- To map, zero, and eventually enable L2 cache
- To map and configure a device tree for handoff to an Operating System
- To find a bootable device
- To detect keywsitch service position and prompt to console if applicable
- To detect and report system hardware failures to both the LCD panel and to the device tree.

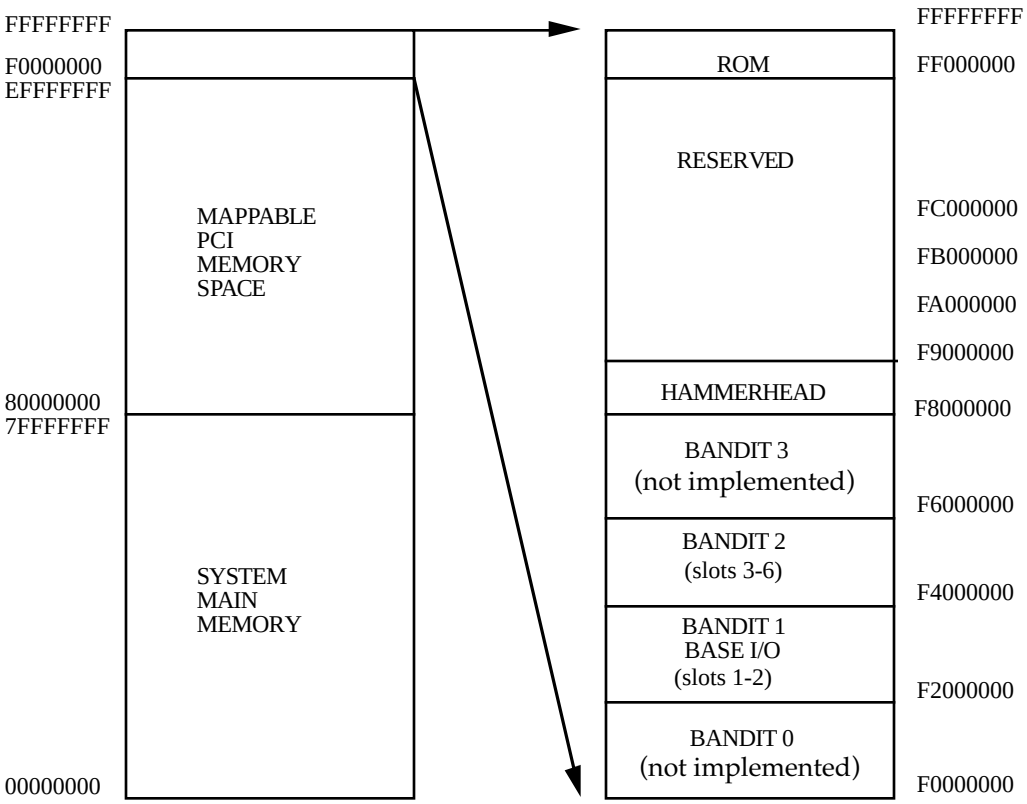
Enabling of the second processor in a two processor system will be operating system dependent.

Chapter 4 Network Server Address Map

4. Network Server Address Map

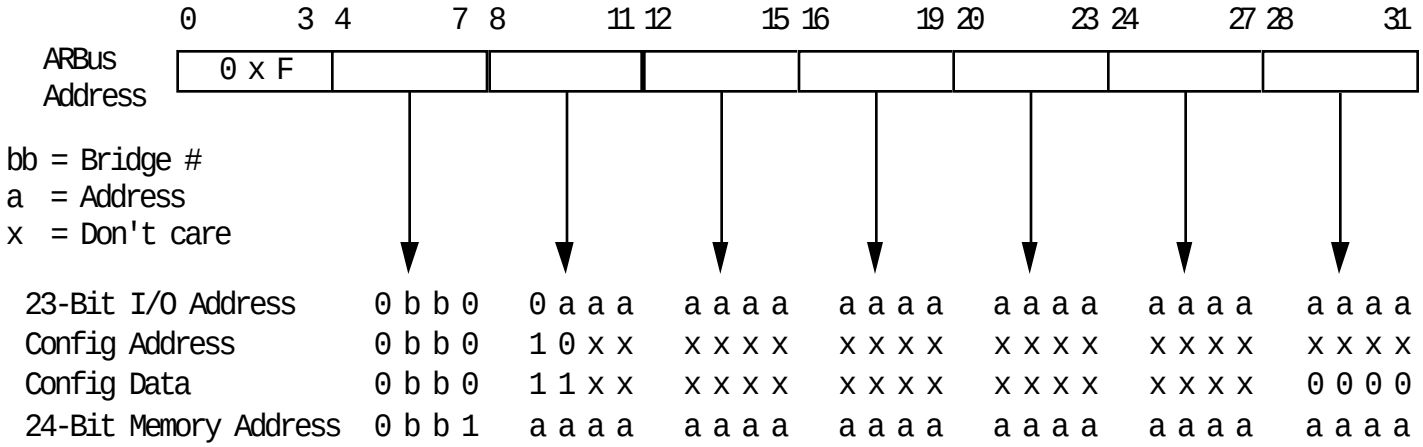
The address map for Network Server significantly leverages the MacRISC address Map. In particular, since the base I/O using Grand Central is very similar, much of the map is identical to the PowerMac 9500 series. We expect some reduction in software effort to support both machines as a result, and we would also hope to get some early bring up payback on TNT motherboards without too much duplication of effort.

The simplest view of the address map is shown in the following diagram:



4.1 PCI I/O Space

The Network Server uses two separate PCI buses for on-board I/0 (and two slots) and card expansion (four slots). The above table shows the major allocation of space for 4 ARBus-PCI bridges. This section shows how these ranges are further sub-allocated to allow the production of all possible PCI cycles from the processor. The upper 7 bits of an address are determined by the PCI Bridge number in the set of 0xF0, 0xF2, 0xF4, 0xF6. The next 3 bits are used to encode the desired PCI cycle type as shown in Figure 3.



4.2 Pass-Through Memory Cycles

A Pass-Through Memory Cycle is made when an ARBus address has A[7] == 0b1. In this case, the bridge passes the original ARBus address during the Address Phase. This effectively defines an 8 MB Pass-Through Memory region per ARBus-PCI bridge.

4.2.1 Grand Central Device Registers

Grand Central implements a large number of registers to control the various I/O devices. Additionally, to support backwards compatibility for VIA register offsets, 128KBytes of address space is consumed. To accommodate these requirements while not consuming large amounts of PCI memory space, Grand Central uses the pass-through memory space defined in Section 2.4.1 on page 23.

TNT Grand Central Device Register Mapping

Start Address	End Address	Name	Comments
0xF3000000	0xF301FFFF	Grand Central Device Registers	Grand Central Device registers. Mapped to 0F3000000 to 0xF301FFFF on PCI1 for memory commands.

Grand Central Base Address

Grand Central is fully PCI compliant and therefore can re-position its memory space response to anywhere in PCI memory space. The addresses defined in Table 9 are defined for convention only (defined by the current OpenFirmware and Expansion Manager code for the TNT ROM releases). Grand Central may be mapped anywhere in PCI Memory space.

4.3 I/O Cycles

PCI I/O Cycles are made when a PCI bridge is accessed with an address with A[7:9] == 0b000. An access to this address generates an I/O cycle on the PCI side of the bridge passing the low-order 23 bits from the ARBus address. Software should guarantee that the relevant, device specific upper bits (other than the bridge select bits) are zeros. Architecturally, the PCI spec defines PCI I/O cycles to have only the lower 16 bits of the address be significant. The extra bits are provided for architectural expansion and hardware simplicity.

ARBus read or write accesses by the CPU to the PCI I/O space defined in Table 7 are serviced by the appropriate Bandit/Control/Kaos chips and forwarded onto the appropriate PCI as I/O read/write commands. Bandit/Control/Kaos drives the a low-order 16-bits of the ARBus address onto the PCI during the command cycle to access up to 64K worth of PCI I/O space. Access to PCI I/O space must occur after each PCI node has been configurated via the PCI configuration space. TNT system, behavior is undefined if PCI I/O space is accessed BEFORE the PCI nodes are properly configured.

4.4 Configuration Cycles

Configuration Cycles are generated in an indirect manner, similar to mechanism #1 suggested in the PCI specification for x86 class processors. This mechanism uses two registers (Config Address and Config Data), accessed using normal ARBus Cache-Inhibited, single-beat Reads and Writes using 32-bit operands. These registers are located in the bridges PCI I/O Space as shown in Table below.

PCI Bridge Config Address and Config Data Locations

ARBus Address	PCI Bridge	Register
0xF0800000	reserved	reserved
0xF0C00000	reserved	reserved
0xF2800000	Bandit PCI 1	PCI1 Config Address
0xF2C00000	Bandit PCI 1	PCI1 Config Data
0xF4800000	Bandit PCI 2	PCI2 Config Address
0xF4C00000	Bandit PCI 2	PCI2 Config Data

The first register is the Config Address register. This register contains the address to be used during the Address Phase of a subsequent PCI Config cycle. Two types of config cycles are defined for the PCI. For config cycles that are destined for the PCI directly defined by Bandit, Type 0 Config cycles are generated. For Config cycles that are destined for a hierarchical bridge via a PCI to PCI bridge chip, Type 1 Config cycles are generated. In both cases, the same register in Bandit/Control/Kaos is used. Bandit/Control/Kaos drives the contents of the Config Address register directly on the PCI AD lines, un-modified.

The second register involved with Config Cycles is the Config Data register. This is actually a “pseudo-register” in the sense that it does not physically exist within the bridge. An access to this “register” causes a Config (or, Special) Cycle to be made on the PCI side, using the address contained within the Config Address register.

The type of Config cycle (Config Read / Config Write) depends upon the cycle accessing the Config Data “register”. The data for a PCI Config Write Cycle is specified by the data being written to the Config Data “register”. Data read from the during a PCI Config Read Cycle is the value returned for a read of the Config Data “register”.

Open Firmware maps devices for their requested spaces in discovery order. Order of discovery is in slot order; on board inpu-output devices are configured prior to slots.

4.6 Network Server Device Address Map

4.6.1 GrandCentral

Grand Central decodes 128 Kbytes of memory space and is configured by Open Firmware to live at xF300000. For detail on register function refer to the Grand Central ERS. Note that Grand Central's registers live on 4 or 16 byte strides and can be accessed as 32- bit words modulo the SCC compatibility port.

The 128KByte space is allocated to device registers, central DMA controller registers and individual DMA channel registers as indicated below in Figure 2. Writes to unmapped portions of the 128K space will have no affect. Reads of unmapped locations will return zeros.

Grand Central Register Space Map

Offset (binary)	Space
0_0000_0000_RRRR_RRRR	DMA Controller Register Space **RRRR_RRRR** selects controller register
0_1000_cccc_RRRR_RRRR	DMA Channel Register Space cccc selects DMA channel **RRRR_RRRR** selects channel register

1_dddd_RRRR_RRRR_rrrr	Device Register Space **dddd** selects device **RRRR_RRRR** selects device register **rrrr** selects register for SCC compatibility port, otherwise, **rrrr** is 0

DMA Channel Number Assignments
Grand Central contains ten DMA channels. The channel number assignments are illustrated in below. Note that these numbers correspond to the "cccc" channel select values in the table above.

DMA Channel Number Assignments

Channel Number	Channel Name
0x00	SCSI
0x01	Floppy
0x02	Ethernet Transmit
0x03	Ethernet Receive
0x04	SCC Channel A Transmit
0x05	SCC Channel A Receive
0x06	SCC Channel B Transmit
0x07	SCC Channel B Receive
0x08	Audio Out
0x09	Audio In

Device Number Assignments
Grand Central provides access to several sets of device registers. The device number assignments are illustrated below. Note that these numbers correspond to the "dddd" device select values above.

Device Number Assignments

Device Number	Device Name
0x00	SCSI
0x01	MACE
0x02	SCC - "Compatibility" Port
0x03	SCC - "MacRISC" Port
0x04	Audio
0x05	SWIM3
0x06-0x07	VIA
0x9	Ethernet Address PROM
0xA	GBus Device 1 (Board Register 1)
0xB	GBus Device 2 (Reserved)
0xC	GBus Device 3 (LCD & Time Base Enable)
0xD	GBus Device 4 (NVRAM High Address)
0xE	GBus Device 5 (Board Register2)
0xF	GBus Device 6 (NVRAM Data)

4.1.1.1 Gbus Registers

Ethernet Prom

Address xF0319000 +	**Size**	**Field Name**
00	byte	highest byte of Group ID
10	"	middle byte of Group ID

20	"	lowest byte of Group ID
30	"	highest byte of sequencing address
40	"	middle byte of sequencing address
50	"	lowest byte of sequencing address
60	"	'AA' (signifies normal bit ordering)
70	"	/cx (xor cs inverted of above 7 bytes)
80	"	/highest byte of Group ID
90	"	/middle byte of Group ID
A0	"	/lowest byte of Group ID
B0	"	/highest byte of sequencing address
C0	"	/middle byte of sequencing address
D0	"	/lowest byte of sequencing address
E0	"	'55' (signifies reverse bit ordering)
F0	"	cx (xor cs of above 7 bytes)

Board Registers 1 and 2: These are the same locations as in the 9500, x1A000 and x1E000, and ETH10BT_Link is not supported. The PCIPRSNT bits are unchanged. In the top byte of board register 1 is where the **active Low** Keyswitch bits are located. In the following tables, bits not mentioned are the same asin 9500.

Location	Function
b10	not connected
b11	BoxId0=1
b12	BoxId1=0
b13	Keyswitch ServiceL
b14	Keyswitch LockedL
b15	TwoSuppliesH

Board Register 2 is now a 16 bit register. The top byte of this 16 bit register is where the Network Serverspecific server monitoring status bits are located. These are all **active Low** signals.

Location	Function
b8	FanFailDrive
b9	FanFailProcessor
b10	TempFailProcessor
b11	TempWarnProcessor
b12	FailPowSupplyLeft
b13	FailPowSupplyRight
b14	powSupply HotLeft
b15	powSupplyHotRight

IMPORTANT PROGRAMMATIC NOTE: Network Server does not implement an interrupt for these functions. Software can implement a daemon that does background reads of this register (say every 30 seconds or so).

LCD Interface: Network Servers provides a WRITE ONLY LCD interface as two registers on GBUS device 3. Software will have to provide a 1 microsecond (or longer) timer between write accesses. Register 0 at address offset x1C000 is the R (Command) register for the device; register 1 at address offset x1C010 is the S (Data) register for the device.

The Network Server has also implemented the Synchronize_TimeBase function on the LCD GBUS device. Synchronize_TimeBase allows software to lock-step the timebases of the two processors. This may or may not be useful in two processor configurations. Software would have to write a 0 to this register, implemented at bit 15 of Register 2 at offset x1C020. This disables the 604 timebase. It would then write a "0" value to each processor's timebase. It would then write a 1 to bit 15 of Register 2 at offset x1C020, re-enabling the timebases.

4.6.2 Other PCI devices

Fast/Wide SCSI buses (Symbios Logic 53C825A) occupy the IDSEL positions 17 and 18. Slots 1 and 2 in the Network Server remain at IDSEL 13 and 14. The Cirrus Logic 54M30 Video Controller occupies IDSEL 15.

For PCI Bus 2, PCI Slot 3 is moved to the second Bandit. Config cycles start at IDSEL(13) =Slot 3, (14)= Slot 4, (15) = Slot5, (16) = Slot6.

4.2 Network Server External Interrupt Map

The Network Server keeps the critical positions of PowerMac 9500; however, F/W SCSI interrupts are moved to Bandit's positions. Bandit 1 and 2 have their interrupts wired together and moved to the Error_Int. Bandit only interrupts on bus timeouts (see the Bandit spec section 2.5); as this is an error response, this should not impact much of anything. Note that the 54M30 video controller has no interrupt line. Note that the internal Grand Central interrupt mapping is unchanged.

Signal On GC	9500	Network Server
EXT0	Cuda_NMI	Cuda_NMI
EXT1	Reserved	Error_Int*
EXT2	Ban1_Int	FW0_Int
EXT3	SlotA_Int	Slot1_Int
EXT4	SlotB_Int	Slot2_Int
EXT5	SlotC_Int	Slot3_Int
EXT6	Ban2_Int	FW1_Int
EXT7	SlotD_Int	Slot4_Int
EXT8	SlotE_Int	Slot5_Int
EXT9	SlotF_Int	Slot6_Int
EXT10	SecToPri_Int	SecToPri_Int

Note that the programmatic way for a second processor to interrupt the first processor (seen as EXT10 on Grand Central) is through accesses to the Ethernet Prom Gbus Device address space. Hence SecToPri_Int is tied to Enet ROM Chip Select (at offset x19_000) on GBUS.

Chapter 5 Network Server System Bus

5. System Bus Definition

The system bus is a modified, multiple master version of the 60x system bus. It is essentially identical to the 9500 system bus, with the addition of hooks for more than one caching agent. The pinout and form factors are not compatible with the 9500 however.

5.1 Signal Definitions

Network Server's system bus is a multiple master, multiple caching agent shared bus running at up to 50 MHz. Signal definitions are identical to PowerMac 9500 which in turn are essentially those of the 604 bus. Arbitration defintions are brought out separately for completeness.

Coherence granularity unit is 32 bytes. Level 2 caching agents force inclusion on the L1 of the 60x processors. There are four types of agents on the Network Server system bus: masters (M), slaves (S), snooping masters (sM), and a single arbiter (A).

5.1.1 System Bus Arbitration

Mnemonic	Dir.	Pins	R	Name and Description
master BusReqL	M:Out S: na A:In	1 7	Y N Y	**Address Bus Request:** These active low, point to point signals indicate to the arbitration logic that a master is requesting the bus. A bus request is kept asserted until the master has received a qualified bus grant (*master* BusGrantL asserted and sysAbbL deasserted). Each master drives only one of the *master* BusReqL lines.A later section describes address arbitration and the flexibility and restrictions on the use of *master* BusReqL.
master BusGrantL	M:In S:na A:Out	1 7	Y N Y	**Address Bus Grant:** These active low signals indicate that the arbitration logic has granted a master the address bus. Each master only receives one of the *master* BusGrantL signals. All masters must qualify *master* BusGrantL with the deassertion of sysAbbL There is bus parking on the address bus. A later section describes the flexibility and restrictions on the use of *master* BusGrantL.
slave RddaL	M:na S:Out A:In	 1 11	N Y Y	**Read Data Available:** These active low, point to point signals indicate that slave[S] has read data available. Each slave returns data in the order it is requested; however, within a request the critical word is returned first. Each slave drives only one of the *slave* RddaL signals, whereas, the arbiter receives all of the *slave* RddaL signals.

master DbgL	M:In S:na A:Out	1 7	Y N Y	**Data Bus Grant:** These active low, point to point signals indicate that the arbitration logic has granted a master the data bus. Each master only receives one of the DbgL signals. This signal has the same timing as SsdL.
slave SsdL	M:na S:In A:Out	 1 11	N Y Y	**Slave Source/Sink Data:** These active low, point to point signals indicate that the arbitration logic has granted a slave the data bus. Each slave only receives one of the *slave* SsdL signals. This signal has the same timing as *master* DbgL.
sysDBWOL	M:I S: I A:Out	1 1 1	Y Y Y	**Data Bus Write Only** This active low, shared tristate signal is asserted by the arbiter to indicate to the master that its next tenure will be a write. This signal has the same timing as DbgL.

5.2 Parity Handling

Memory parity errors generate MCP to the 60x. This may or may not be gracefully handled by the operating system, however it should normally prevent further execution.

Chapter 6 Network Server Interconnects

6. Network Server Physical Interconnects

This chapter provides the signal information carried across the major interconnect points for the logic boards in Network Server.

6.1 Processor Slot Definition

This will be a surface mount version of the AMP high speed edge connector in a Dual 90 position form factor. The pinout is as follows:

Connector is 180 signal contact AMP 0.025 pitch surface mount dual 90, part 94-7831-08.

(pins not specified are reserved)

ArAdr(31)	5	SecInt_l	93
ArAdr(29)	6	ArAdr(30)	95
ArAdr(27)	7	ArAdr(28)	96
ArAdr(25)	8	ArAdr(26)	97
ArAdr(23)	9	ArAdr(24)	98
ArAack_l	10	ArAdr(22)	99
ArAdr(21)	12	ArArtry_l	101
ArAdr(19)	13	ArAdr(20)	102
ArAdr(17)	14	ArAdr(18)	103
ArAdr(15)	15	ArAdr(16)	104
ArAdr(13)	16	ArAdr(14)	105
ArAdr(11)	17	ArAdr(12)	106
ArAdr(9)	18	ArAdr(10)	107
ArAdr(7)	19	ArAdr(8)	108
ArAdr(5)	20	ArAdr(6)	109
ArTea_l	21	ArAdr(4)	110
ArAdr(3)	22	ArTA_l	111
ArAdr(1)	23	ArAdr(2)	112
ArDBWO_l	25	ArAdr(0)	113
ArTSIZ(1)	26	ArTSIZ(2)	115
ArTS_l	27	ArTSIZ(0)	116
ArDBB	28	ArTbst_l	117
ArTT(3)	29	ArTT(4)	118
ArTT(1)	30	ArTT(2)	119
ArGbl	31	ArTT(0)	120
ArSync	32	ArShd	121
ArCI	33	tempTripWarnH	122
ArTC(0)	34	tempTripHotH	123
DBDIS_l	35	ParityErrL	124
SecDBG_l	36	PriDBG_l	125
SecBG_l	37	PriBG_l	126
SecBR_l	38	PriBR_l	127
clkToProc0	40	clkToProc1	130

ArDat(32)	41	ArDat(0)	131
ArDat(33)	42	ArDat(1)	132
ArDat(34)	43	ArDat(2)	133
ArDat(35)	44	ArDat(3)	134
ArDat(36)	46	ArDat(4)	135
ArDat(37)	47	ArDat(5)	137
ArDat(38)	48	ArDat(6)	138
ArDat(39)	49	ArDat(7)	139
ArDat(40)	52	ArDat(8)	141
ArDat(41)	53	ArDat(9)	143
ArDat(42)	54	ArDat(10)	144
ArDat(43)	55	ArDat(11)	145
ArDat(44)	56	ArDat(12)	146
ArDat(45)	58	ArDat(13)	147
ArDat(46)	59	ArDat(14)	149
ArDat(47)	60	ArDat(15)	150
ArDat(48)	62	ArDat(16)	152
ArDat(49)	64	ArDat(17)	153
ArDat(50)	65	ArDat(18)	155
ArDat(51)	66	ArDat(19)	156
ArDat(52)	67	ArDat(20)	157
ArDat(53)	68	ArDat(21)	158
ArDat(54)	70	ArDat(22)	159
ArDat(55)	71	ArDat(23)	161
ArDat(56)	73	ArDat(24)	163
ArDat(57)	74	ArDat(25)	164
ArDat(58)	76	ArDat(26)	165
ArDat(59)	77	ArDat(27)	167
ArDat(60)	78	ArDat(28)	168
ArDat(61)	79	ArDat(29)	169
ArDat(62)	80	ArDat(30)	170
ArDat(63)	82	ArDat(31)	171
+12	84	sRst	174
CLKID(2)	85	procReset	175
CLKID(1)	86	timeBaseEn	177
CLKID(0)	87	PriInt_l	178
refClk	92		

OffSenseOut	176, 3
+5V	1, 136, 180, 267, 268, 269, 270, 357, 358, 359, 360, 51, 89, 94
+3_3V	100, 11, 114, 142, 148, 154, 160, 166, 172, 179, 2, 217, 218, 219, 220, 24, 307
+3_3V	308, 309, 310, 4, 45, 57, 63, 69, 75, 81, 88, 90, 91
GND	129, 181, 182, 183, 184, 185, 186, 187, 188, 189, 190, 191, 192, 193, 194, 195
GND	196, 197, 198, 199, 200, 201, 202, 203, 204, 205, 206, 207, 208, 209, 210, 211
GND	212, 213, 214, 215, 216, 221, 222, 223, 224, 225, 226, 227, 228, 229, 230, 231
GND	232, 233, 234, 235, 236, 237, 238, 239, 240, 241, 242, 243, 244, 245, 246, 247
GND	248, 249, 250, 251, 252, 253, 254, 255, 256, 257, 258, 259, 260, 261, 262, 263
GND	264, 265, 266, 271, 272, 273, 274, 275, 276, 277, 278, 279, 280, 281, 282, 283
GND	284, 285, 286, 287, 288, 289, 290, 291, 292, 293, 294, 295, 296, 297, 298, 299
GND	300, 301, 302, 303, 304, 305, 306, 311, 312, 313, 314, 315, 316, 317, 318, 319
GND	320, 321, 322, 323, 324, 325, 326, 327, 328, 329, 330, 331, 332, 333, 334, 335

GND	336, 337, 338, 339, 340, 341, 342, 343, 344, 345, 346, 347, 348, 349, 350, 351
GND	352, 353, 354, 355, 356, 39

The ground plane pins (181-360) are split to provide a greater number of +3.3 and +5 voltage pins. Pins 217-220, 307-320 are +3.3V, and pins 267-270, 357-370 are +5.

Processor connector notes:
+12 current consumption must not exceed 0.4 A. +5 current consumption must not exceed 12 A; +3.3 current consumption must not exceed 24 A. Offsense Out must not connect to anything and need not connect to each other; these are used to detect unseated processor cards and prevent the power supply from powering on. refClk needs to be a fast transition signal (min 1v/ns); clkToProc's are returned asynchronous to refClk but synchronous to the system ASICs but in advance by approximately 700 ps (4" typical trace) Processors with 0 hold time will require inserted clock delay of at least 1 ns. tineBaseEn is a signal that allows software to synchronize MP timebases. For 601 processors, a local timebase is required. Processor card hard reset de-asserts approximately 500 ms after Main Logic Board hard reset. ParityErrL would normally be routed to MCP on the processor. ArSync, ArGbl, ArShd are not used by the current Main Logic Board but may be used in dual connector versions in the future.

6.2 Network Server Cache DIMM

The cache DIMM connector is fit, form and function compatible with the PowerMac 8500 cache slot. However, it must be noted that early versions of burst SRAM from Motorola may cause signal integrity issues within the DIMM itself, resulting in clocking glitches that cause failed burst writes. Use of later generation 5 Volt parts, or 3.3 volt parts from Motorola, Micron, or IBM is preferred. Also, Network Server ROM enables "fast L2" mode for bus speeds of 44 Mhz or less. Do not use slower than 8 ns tag ram, 7 ns preferred.

6.3 Network Server Power Supply Connector

Network Server 500 does not implement a power backplane, and its hardwired interface to the blind mate motherboard connects to a subset of the pins, based on the difference in the levels of current delivered to the main logic board. The Network Server 700 power interconnect system pinout is available from Developer Support.

6.4 Network Server Mezzanine Interconnect

In order to allow immediate serviceability and upgrade of the motherboard, Network Server and Network Server will support a standard edge interconnect for devices which live inside the box. This includes: Floppy, LCD Panel,Reset and Programmer's Switches, Fan, Speaker, and SCSI interfaces. These will be implemented across a single 132 position edge. Mezzanine pin list is availabe from Devleoper Support.

Chapter 7 Network Server Expansion Buses

7. Network Server Expansion Buses

Network Server has two major expansion buses: The built-in dual fast and wide SCIS backplane buses, and six slots of PCI.

7.1 PCI Definition

Network Server will use a 32-bit card to motherboard 5 Volt implementation for six slots of PCI expansion. For complete PCI information refer to the various documents published by the Special Interest Group. These are available through many channels.

Network Servers attempts to be PCI 2.1 compliant. Open issues surrounding this compliance are: Special Cycle support and discontiguous byte enables.

Network Server will support the PCI PRSNT signals. See the discussion on the Board Register above. For best performance PCI cards in the Network Server need to implement the Cache Line Size register (32 bytes, 8 DWORDS), and Write with Invalidate for burst writes, and Read Multiple or Read Line for burst reads; otherwise the bridge will perform single beats to memory which decreases bandwidth significantly and also increases system utilization.

7.1.1 PCI Device Configuration

Fast/Wide SCSI buses (Symbios Logic 53C825) occupy the IDSEL positions 17 and 18. Slots 1 and 2 are at IDSEL 13 and 14. The 54M30 Video Controller occupies IDSEL 15. For PCI Bus 2, PCI Slot 3 is moved to the second Bandit. Config cycles start at IDSEL(13) =Slot 3, (14)= Slot 4, (15) = Slot5, (16) = Slot6. See the discussion on device addresses in Chapter 4.

7.1.2 PCI Power Dissipation

Based on a reasonable level of reserve power for processor upgrades and SCSI devices, the following guidelines pertaining to all six cards taken in aggregate will generally prove successful.

Network Server	Voltage	Current	Total Power
500	+3.3 +5	10 A 10 A	Not to exceed 50 watts in any combination
	+12	2 A	

Network Server	Voltage	Current	Total Power
700	+3.3 +5	18 A 18 A	Not to exceed 90 watts in any combination
	+12	2 A	

The above tables are meant to communicate the fact that 3.3 and 5 volts trade off and that an assortment of cards that draw from both 3.3 and 5 can be supported at the overall power rating of the unit. The per card rating for PCI 2.1 of no more than
25 watts always applies.

7.2 Network Server SCSI Expansion

Network Server implements a unique SCSI backplane which provides unparalleled ease of use for both Main Logic Board SCSI and add-in card RAID.

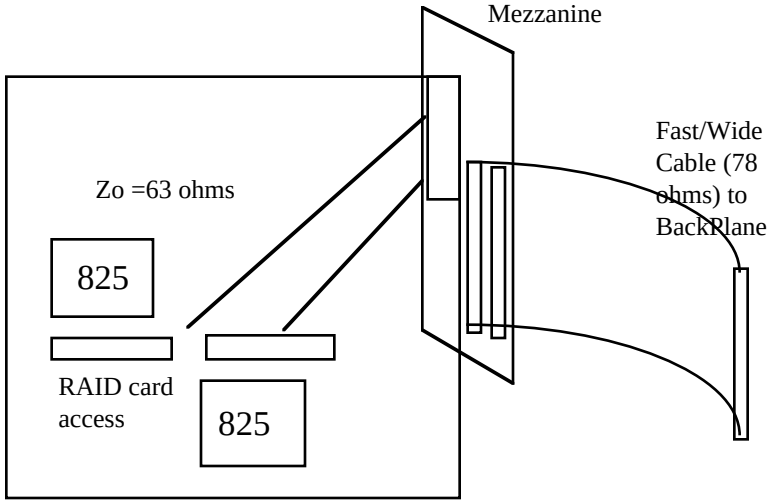
The Network Server SCSI backplane consists of seven slots with hot swap. It is expected(but not required) that slot 0 will be a CD ROM.

7.2.1 Theory of Operation

Network Server's backplane is organized as a pair of fast and wide buses with narrow compatibility. These are driven through a pair of NCR 825A single-ended SCSI controllers residing on the Network Server Main Logic Board. These buses leave the Main Logic Board through the blind mate Mezzanine interface and are cabled therefrom. Active terminators are used on the Main Logic Board for signal integrity.

For RAID card access, the RAID card sits in PCI BUS 0 Slot 1 and cables into the Main Logic Board. A separate 26 pin control interface allows the RAID card to drive LED's on the front panel of the drives in the backplane.

Note that the SCSI traces will be approximately 12" long on the Main Logic Board at an impedance of approximately 63 ohms. The cables on the mezzanine will be standard 78 ohm single-ended. These will be under 24"; including the backplane, the total extent of the SCSI bus should be under 6 feet. For the 820, the "glitch eating" period far exceeds the total settling time on this short, controlled bus. Furthermore, the 820 device has a forgiving 9.7 ns minimum rise time.



7.2.2 Main Logic Board to RAID card interface

Network Server implements the industry standard Wide SCSI pinout on the RAID access connectors, with the exception that pin 19 is stolen to disable the Main Logic Board termination, and TERMPOWER is not implemented. The RAID card will need to connect pin 19 to ground (which is normal).

7.2.2.1 _____ 26 PinRAID Control Interface

Unlisted pins are reserved. ledOE must be driven to ground by the mating interface to enable the LED function. Bus0 Strobe L latches the state of the drive LEDs 0-3; Bus1StrobeL latches the state of drive LED's 4-6.

Pin #	Function
5	FailDrive0
6	Bus0StrobeL
7	FailDrive1
9	FailDrive2
11	FailDrive3
12	Bus1StrobeL
13	FailDrive4
15	FailDrive5
17	FailDrive6
18	ledOE
24	armO
26	armI

SCSI BUS 0

Pin #	Function	Pin #	Function	Pin #	Function	Pin #	Function
1	gnd	18	nc	35	FW0(12)	52	nc
2	gnd	19	nc	36	FW0(13)	53	nc
3	gnd	20	gnd	37	FW0(14)	54	gnd
4	gnd	21	gnd	38	FW0(15)	55	FW0Atn
5	gnd	22	gnd	39	FW0P1	56	gnd
6	gnd	23	gnd	40	FW0(0)	57	FW0Bsy
7	gnd	24	gnd	41	FW0(1)	58	FW0Ack
8	gnd	25	gnd	42	FW0(2)	59	FW0Reset
9	gnd	26	gnd	43	FW0(3)	60	FW0Msg
10	gnd	27	gnd	44	FW0(4)	61	FW0Sel
11	gnd	28	gnd	45	FW0(5)	62	FW0CD
12	gnd	29	gnd	46	FW0(6)	63	FW0Req
13	gnd	30	gnd	47	FW0(7)	64	FW0IO
14	gnd	31	gnd	48	FWP0	65	FW0(8)
15	gnd	32	gnd	49	gnd	66	FW0(9)
16	disableTermL	33	gnd	50	gnd	67	FW0(10)
17	nc	34	gnd	51	nc	68	FW0(11)

nc = no connection

SCIS BUS 1

Pin #	Function	Pin #	Function	Pin #	Function	Pin #	Function
1	gnd	18	nc	35	FW1(12)	52	nc
2	gnd	19	nc	36	FW1(13)	53	nc
3	gnd	20	gnd	37	FW1(14)	54	gnd
4	gnd	21	gnd	38	FW1(15)	55	FW1Atn
5	gnd	22	gnd	39	FW1P1	56	gnd

6	gnd	23	gnd	40	FW1(0)	57	FW1Bsy
7	gnd	24	gnd	41	FW1(1)	58	FW1Ack
8	gnd	25	gnd	42	FW1(2)	59	FW1Reset
9	gnd	26	gnd	43	FW1(3)	60	FW1Msg
10	gnd	27	gnd	44	FW1(4)	61	FW1Sel
11	gnd	28	gnd	45	FW1(5)	62	FW1CD
12	gnd	29	gnd	46	FW1(6)	63	FW1Req
13	gnd	30	gnd	47	FW1(7)	64	FW1IO
14	gnd	31	gnd	48	FW1P0	65	FW1(8)
15	gnd	32	gnd	49	gnd	66	FW1(9)
16	disableTermL	33	gnd	50	gnd	67	FW1(10)
17	nc	34	gnd	51	nc	68	FW1(11)

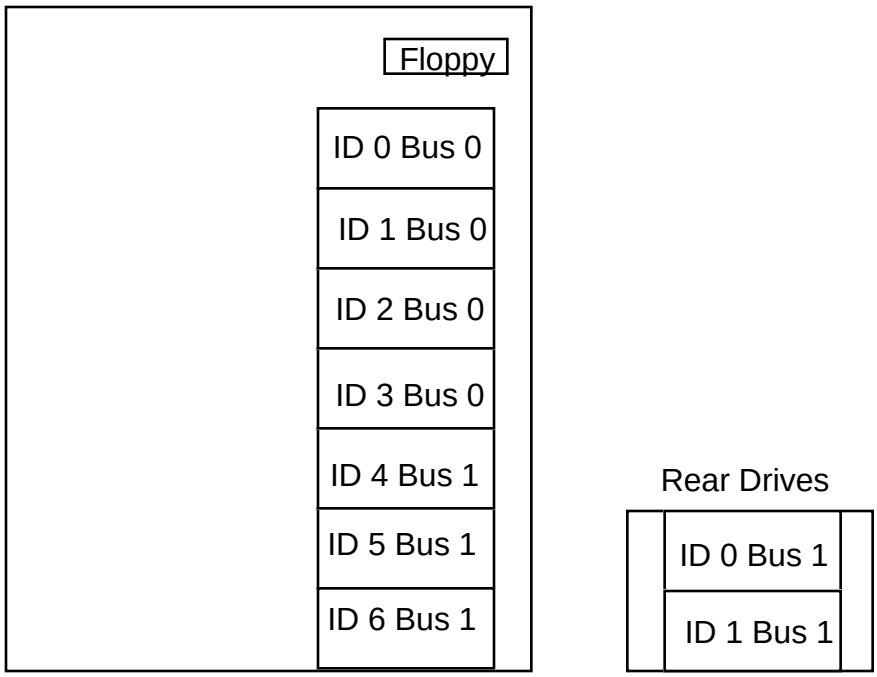
nc = no connection

7.2.2.2 Mezzanine to Backplane Interface

Internally Network Server uses ribbon contact (not pin and socket) 68-pin headers with 0.05 pitch 75 ohm ribbon. Pinouts are available for legitimate use from Developer Support.

7.2.3 SCSI ID

Drives assume their SCSI ID through the backplane. Custom drive carriers provide a cable breakout from the backplane connector to the specific drive. Apple will provide connectors for Apple labeled fast/wide drives and for quad speed CD ROM. amd a connector kit for third parties.



As in the above diagram, the backplane has four drives on one bus and 3 drives on another. In the Network Server 700, a rear drive bracket will support two more drives which are cabled to the bottom bus.

A stuffing option allows this backplane to appear as one bus. This may be useful in supporting a low end configuration. The terminators in the middle are automatically disabled by stealing a ground signal from the mating ribbon cable. This concept is also used to support the optional internal drives in the rear of Network Server.

7.2.4 Hot Swap

Hot swap is accomplished through:

1) a mechanically timed assertion, implemented through the use of long and short pins, of SCSI reset; and
2) advance power and ground, also through long pins.

Operating systems may or may not support the use of SCSI reset to hot swap drives. Typically this function is reserved for RAID card use.

Network Server's backplane uses a FutureBus backplane connector in a 4 x 18 configuration. This is a very low cost solution that allows 3 pin lengths and blind mateability. The pinout for the drive carriers is as follows:

Pin No.	Function	Pin No.	Function	Pin No.	Function	Pin No.	Function
A1	gnd	B1	Data11	C1	gnd	D1	fail1
A2	Data9	B2	gnd	C2	Data10	D2	gnd
A3	gnd	B3	ScsiI0	C3	gnd	D3	Data8
A4	ScsiCD	B4	gnd	C4	ScsiReq	D4	gnd
A5	gnd	B5	ScsiMsg	C5	gnd	D5	ScsiSel
A6	ScsiAck	B6	gnd	C6	ScsiRst	D6	gnd
A7	gnd	B7	ScsiAtn	C7	gnd	D7	ScsiBsy
A8	Data7	B8	gnd	C8	DataP0	D8	gnd
A9	gnd	B9	Data5	C9	gnd	D9	Data6
A10	Data3	B10	gnd	C10	Data4	D10	gnd
A11	gnd	B11	Data1	C11	gnd	D11	Data2
A12	DataP1	B12	gnd	C12	Data0	D12	gnd
A13	gnd	B13	Data14	C13	gnd	D13	Data15
A14	Data12	B14	gnd	C14	Data13	D14	gnd
A15	delay gnd	B15	gnd	C15	+5	D15	ScsiID2
A16	adv +5	B16	+5	C16	gnd	D16	ScsiID1
A17	adv gnd	B17	+12	C17	+5	D17	ScsiID0
A18	+12	B18	+12	C18	+12	D18	+12

Pins A17, A16, and A13 are long power /ground pins on the drive carrier and are tied through series resistors on the backplane. These series resistors minimize any power transient to existing drives upon hot plug of a drive. A15 is a short pin. It is tied to ground as above on the Drive carrier. XOR logic on the backplane detects changes in the state of this pin, which is pulled up on the backplane. Insertion or removal of the drive will cause a SCSI Reset for the time it takes to unmate or mate the long vs. short pins. RAID or higher level software will use this to blow away outstanding transactions, reconstruct the state of the bus, and start repair or notify authorities as needed. For typical long/short pin lengths, the SCSI reset assertion is found to be a minimum of 5 ms.

7.2.5 Narrow Device Compatibility

A narrow drive carrier simply connects to the appropriate subset of signals on the backplane connector.

7.3 SCSI Device Requirments

Network Server will expects its fast and wide drives to be configured to meet the following requirements: Remote start, single-ended, full SCSI-2 with tag-queuing optimization.

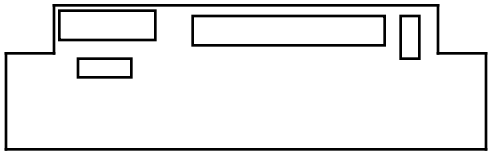
7.3.1 SCSI Device Power Limits

Drives should not exceed 1.1 Amps at +5 and 1.3 Amps at +12 thermal (average) power consumption. Full height drives double the power limits.

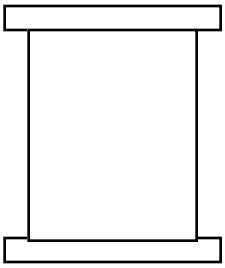
7.3.2 Installing Drives

To get a flavor of how a third party drive is configured into the Network Server, the break out of the adapter kits is shown below:

50 pin interface kit -

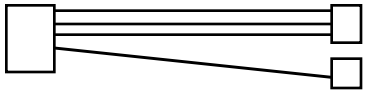


50 Pin Interface PCB P/N 820-0716

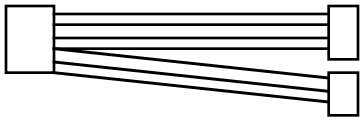


50 Pin Data Cable P/N 590-0666

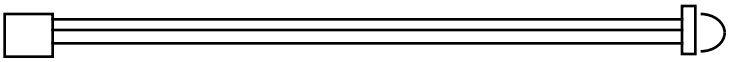
Power Cable P/N 590-0665



DDS Tape SCSI ID Cable P/N 590-1508

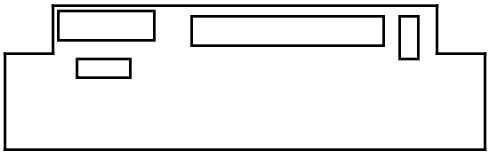


CD SCSI ID Cable P/N 590-1509

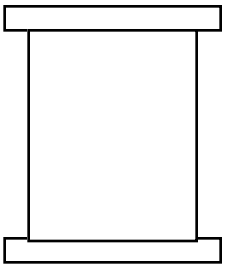


LED Cable P/N 590-0637

68 pin interface kit -



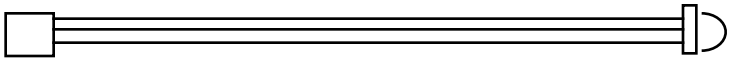
68 Pin Interface PCB P/N 820-0717



68 Pin Data Cable P/N 590-0636

Power Cable P/N 590-0665

68 Pin SCSI ID Cable P/N 590-1507



LED Cable P/N 590-0637

To take advantage of the tray portability and LED functions built into the Network Server , it is necessary to cable non-Apple-qualified peripherals to the interface PCB. To do this, a special cable may be necessary The pinouts for the two interface PCB connectors are as follows.

50 pin interface SCSI ID Connector (J2 on P/N 820-0716):

Pin	Function
1	CD Audio Common
2	CD Audio Right
3	CD Audio Left
4	No Connect
5	LED Drive Signal
6	SCSI ID 0
7	SCSI ID 1
8	SCSI ID 2

Note that the CD Audio connection is only for a CD-ROM drive in Slot 0. Operating systems may or may not support this use of the CD Audio connection.

68 pin interface SCSI ID Connector (J13 on P/N 820-0717):

Pin	Function
1	LED Drive Signal (Active HIGH)
2	No Connct
3	LED Drive Signal (Active LOW)
4	SCSI ID 0
5	SCSI ID 1
6	SCSI ID 2

The provider of the peripheral provides information on the connection of these signals at the peripheral.

NOTE: The SCSI address of a peripheral device can be “hardwired” by setting jumpers on the peripheral, itself. If this is done, care must be taken to set the address corresponding to removable tray slot in which the peripheral is placed. Slots in the Network Server 500/700 are address 0-6 with 0 being the address of the uppermost slot and 6 being the address of the lowermost slot.

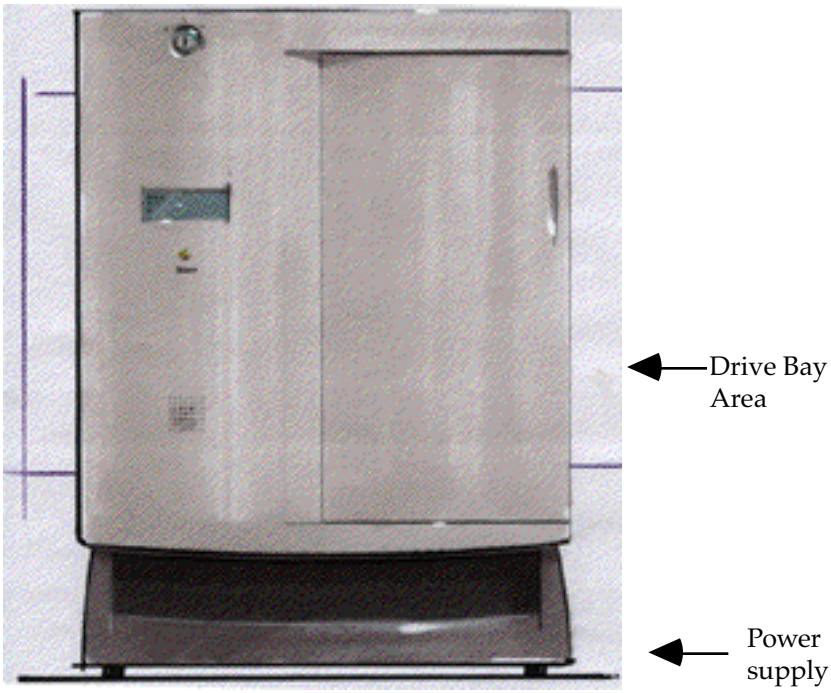
Chapter 8 Network Server Mechanicals

8. Product Design

The chapter is only intended to give a flavor of the product design forthcoming from ABS. Formal drawings are available through the normal mechanical drawing channels.

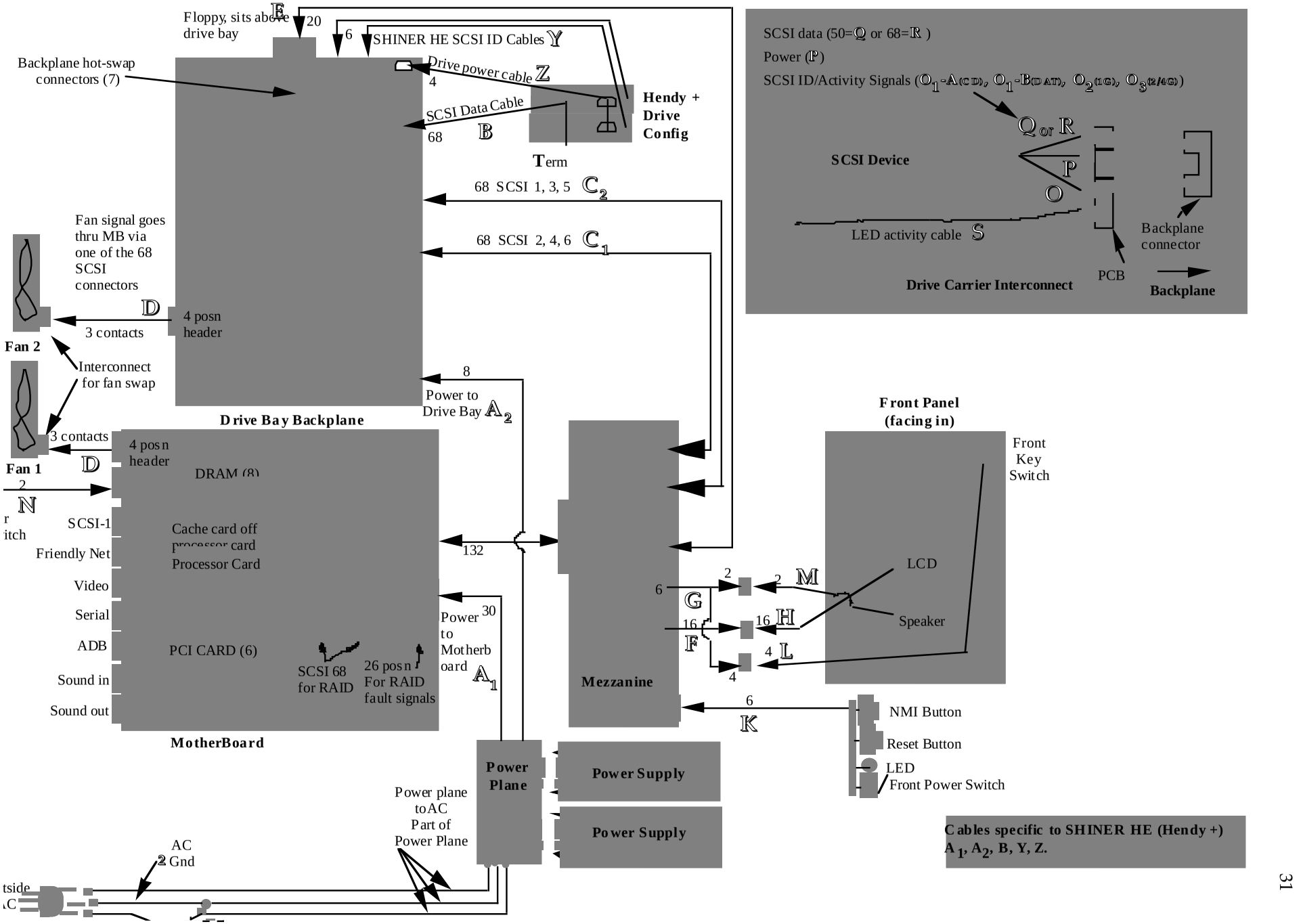
8.1 Network Server Box (Hendy)

The following diagram shows the current product design view, known as Hendy. Dimensions are approximately 17"W x 23"H x 18" D. Weight with 1 hard drive is approximately 60 pounds.



8.2 Network Server Mechanical Interconnect Matrix

The following diagram shows the overall interconnect matrix for off-Main Logic Board devices.


Floppy, sits above drive bay
E
20
6
SHINER HE SCSI ID Cables Y
Backplane hot-swap connectors (7)
Drive power cable Z
4
SCSI Data Cable
68
B
Hendy + Drive Config
Term
68 SCSI 1, 3, 5 C2
68 SCSI 2, 4, 6 C1
Fan signal goes thru MB via one of the 68 SCSI connectors
D
4 posn header
3 contacts
Fan 2
Interconnect for fan swap
8
Power to Drive Bay A2
Drive Bay Backplane
3 contacts
4 posn header
Fan 1
DRAM (8)
SCSI-1
Friendly Net
Video
Serial
ADB
Sound in
Sound out
Cache card off processor card
Processor Card
PCI CARD (6)
SCSI 68 for RAID
26 posn For RAID fault signals
132
Power to Motherboard A1
30
MotherBoard
Mezzanine
Front Panel (facing in)
Front Key Switch
LCD
Speaker
6
G
2
2
M
16
F
16
H
4
4
L
6
K
NMI Button
Reset Button
LED
Front Power Switch
Power Plane
Power Supply
Power Supply
Power plane to AC Part of Power Plane
AC
2 Gnd
SCSI data (50=Q or 68=R)
Power (P)
SCSI ID/Activity Signals (O1-A(CD), O1-B(DAT), O2(LG), O3(2/4G))
Q or R
P
O
SCSI Device
LED activity cable S
Backplane connector
PCB
Drive Carrier Interconnect
Backplane
Cables specific to SHINER HE (Hendy +)
A1, A2, B, Y, Z.

The following table details vendor connector types used in the various positions. Note that these are subject to change without notice.

Interconnect Type			
Location	Generic Descr	Splr(s)	Supplier
			P/N
Chassis			
AC Power Recepacle -			
internally wired to AC internal w/interlock			
Main Logic Board I/O			
SCSI-1			
	25-pin/apple style	Fox Conn	DE11322-11
		AMP	748957
Friendly Net			
		Fox Conn	QB11073-S2
		AMP	7488761-1
		MOLEX	52515-1410
Video			
	DSUB 15	Fox Conn	DE11222-12
		AMP	748876
Serial			
	9 pin mini-DIN	Fox Conn	MH11093-K
		AMP	786767-1
		MOLEX	87418-0002
ADB			
	4-pin mini-din	Fox Conn	MH11043-K0
		AMP	749181-2
		MOLEX	87220-1410
Sound In			
	Stereo Jack 4 leads	MOLEX	87370-2702
		PAN	70462-T06
Sound Out			
	Stereo Jack 3 leads	Pan	70462-T05
		Molex	87370-2502
Main Logic Board Signal & Power			
Power			
	30 R/A m w/cust bkt	Positronic	PLC30M4BNA2-152.0
Fan out/SMT compatible shrouded			
	4 contacts	Molex	22-11-2042(equiv)

Rear Switch/SMT compatible shrouded			
	2 contacts	Molex	22-11-2022(equiv)
			Can use for EVT1
Main Logic Board			
PCI			
	64 bit-5 V (184)	Burndy-TH (1)	CEE2X92SCV35Z48W
		Foxconn (2)	EH09201-PB-W
		AMP (3)	646254-1
Internal SCSI cabled to RAID card			
	68 contacts	AMP	1-557102-7
	SMT compatible	MOLEX	71661-1068
Fault Signal connector			
	26 pos FR header (SMT comp)	MOLEX	70246-2620
		w. Holls	WH#6202-0090
MB-Processor card			
	90 Dual posn, high speed	AMP	94-7831-08
DRAM connector			
	168position SMT,JEDEC,72ECC	Burndy	ELF168EGC3Z50
		AMP	N/A
		Molex	71251-0008
Processor card			
Cache connector			
	200 cache card	Burndy	ELF200DGC3Z50
Mezzanine Card			
Floppy			
	20 contacts		existing parts
LCD			
	16 contacts	Molex	22-11-2162
Speaker, Front Keyswitch			
	6 contacts	Molex	22-11-2062
Powerswitch			
	2 contacts header	Molex	22-11-2022
Internal SCSI			
	68 contacts	AMP	1-557102-7
		Molex	71661-1068
Mezzanine connector			
	132 connector, Press-fit style	Burndy	CEE2X66PF-102FE
NMI, Reset	termination that can be soldered.		
	4 contacts	Molex	22-11-2042

SCSI backplane/ 2-sided			
Hot plug connector, contacts need with 1A			
current carrying capacity	Futurebus, 72 posn-receptacle	Burndy	HM1S49FPR971H9
	3 levels of sequence for hot swap Advance ground,		
	signals/ground, short pin for 1st break		
Internal SCSI			
	68 contacts Same as the SCSI	AMP	1-557102-7
	conn on the mezzanine card	Molex	71661-1068
Power connector			
	Mate-N-Lock, 4 contacts	AMP	641967-1
Fan out/SMT compatible shrouded			
	4 contacts	Molex	22-11-2042
Drive Carrier Mini-Board			
Hot plug connector, contacts need with 1A			
current carrying capacity	Futurebus, 72 posn-plug	Burndy	HM1W49ZZR970H9
50 position SCSI connector			
		Foxconn	HL03252-K3
		W. Holls	6202-9001
68 position SCSI connector			
	NO AMPLIMITE	Molex	71661-1068
		AMP	1-557102-7
Power connector			
	PC mt power connector	AMP	350211-1
SCSI ID connector	Add amp p/n to existing Apple avl		
	10 contacts		515-0186
LED fault signal			
	4 contacts		22-11-2042

Chapter 9 Environmental Specs

9. Environmental Specification

9.2.1 Operating Temperature

The operating temperature range shall be from +10°C (50°F) to +40°C (104°F).
For DAT and other tape media, a derating to +35 degress C may be applied.

9.2.2 Storage Temperature

The storage temperature range shall be from -40°C (-40°F) to +47°C (116.6°F).

Network Server shall pass a modified Class 1 Storage Temperature Test, as referenced in the Apple Corporate Specifications 062-0089-C, section 4.0.

9.2.3 Transit Temperature

The transit temperature range shall be from -40°C (-40°F) to +65°C (149°F).

Network Server shall pass the Class 1 Transit Temperature Test, as referenced in the Apple Corporate Specifications 080-0033A, section 7.0.

9.2.33 Altitude

The operating altitude shall be 0 to 3000 meters. However, this will not be tested.

9.1 Network Server Safety Requirements

The overall product will be evaluated and certified to accepted National and International Product Safety Standards, based on IEC 950 (Safety of Information Technology Equipment, Including electrical business equipment). Where appropriate, national deviations will be taken into account.

The overall product will bear the approval marks for the United States (UL or NRTL-Mark), Canada (CSA or C-Mark) and Europe (CE-Mark, self-Certification based on CB Report by accepted safety test agency). Most of the rest of the world will accept some or all of these marks. Some specific regions may require extra paperwork, samples, fees, etc., in order to sell product. Based on projected sales figures, this extra effort may or may not be justified.

Certain components within the overall product are required to have limited product safety certifications. The most important of these components is the power supply(-ies). The power supply specification(s) details the safety certifications that the power supply manufacturer(s) must obtain and maintain.

The safety approvals will be based on early samples of the product. The agencies will expect the product to remain the same unless they are advised otherwise and have a chance to evaluate and approve the changes (for example changing a model number or label or adding a new fan or changing the vent opening sizes).

9.2 Network Server EMC Requirements

Network Server shall meet the following Apple EMC standards listed below;

Apple Standard	**Description**	**Test Level**
062-0719-A	Domestic Emissions	Class A
062-0718-A	International Emissions	Class A
062-0302-C	Electrostatic Discharge	Level 2
062-0976-A	RF Immunity	3v/m 80% AM
062-0974-A	Electrical Fast Transients	Level 2
063-0175-B	Surge	1kV line to line 2kV line to ground

Welcome to The Developer CD for AIX® and Apple Network Server

On this CD you will find a collection of documents related to AIX and the Apple Network Server, as well as sample code and third-party drive mecanical CAD information.They have been provided in PDF and HTML formats. To read the PDF files, just click on the title listed below. To read the HTML files, just point your browser, or the included Mosaic browser, at the file "contents.html" located in the HTML folder at the root level.

Developer's Reference Guide for the Apple Network Server

AIX Application Binary Compatability and the Apple Network Server

Network Server 500 & 700 Data Sheet

Network Server Hardware Developer Notes

Network Server Hardware Troubleshooting Guide

Mechanical CAD Information for Third-Party Drives

Sample Code