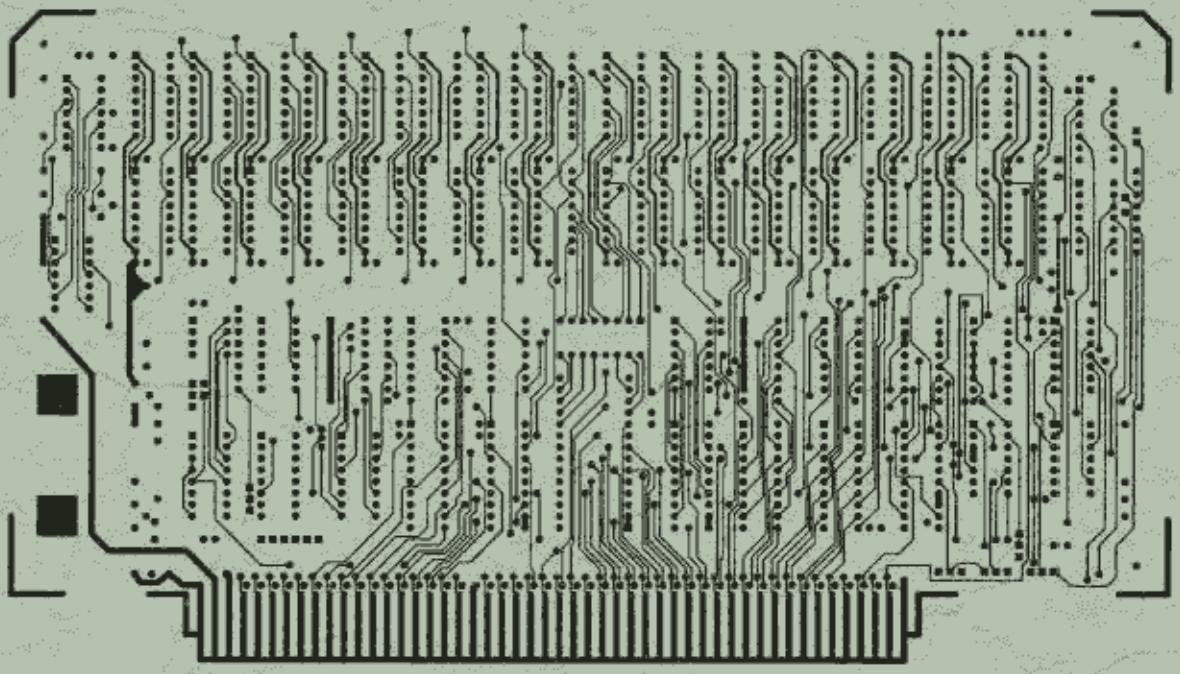
64K-DQ
OPERATION MANUAL



- FULLY BANK SELECTABLE
- I.O. PORT 40 (CROMEN CO) COMPATIBLE BANK SELECT
- DISABLE ON 16K BOUNDRIES
- ON BOARD REFRESH
- DMA COMPATIBLE
- EXTENDED ADDRESS LINES A16, A17, A18, A19
- FOUR LAYER CONSTRUCTION SUPER QUIET
- IEEE S-100

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BOARD SELECT (MODE ONE) **********

I.O. port 40H may be written into, to select up to eight different boards. Each bit of the byte written to this port will represent a board selected. Only one bit may be set low at a time.

There is a relationship between the bits of dip switch SW2 and the bits of the byte written to I.O. 40. If you wish the board in question to be 'on' when data bit 0 is low, then the lowest switch of SW2 must be ON. If this board is to respond when data 03 is set low, switch 4 (counting up from the bottom) must be on.

EXAMPLES:

OFF	ON				
X		07			
X		06	F	E	(HEX)
X		05			
X		04	1111	1110	(BINARY)
X		03			
X		02			
X		01			
	X	00			
SW2			BYTE		

NOTE: Jumper E-4 E-5 (permanent enable) must be removed for I.O. port 40 select to work. Jumper E & 8 should be installed, T & S removed.

BOARD SELECT (MODE II) **********

S-100 EXTENDED ADDRESS lines A16 thru A23 (8 lines) are brought onto the board to switch SW1. The board may be selected by the logical comparing of the 8 bits of A16-A23 and the individual switches of SW1. Assume A16 to be switch one.

Note that this mode differs from I.O. port 40 select in that the switches here are set in a binary fashion, allowing two or more to be on at the same time. If two switches in I.O. 40 mode were on at the same time, there would be a data clash on the bus.

In this extended address mode the bits are decoded allowing up to 256 boards (?) to be separately addressed.

EXAMPLES:

	off	on	off	on	off	on	off	on
A16---	|	X|	|X	|	|	X|	|X	|
A17---	|	X|	|	X|	|X	|	|X	|
A18---	|	X|	|	X|	|	X|	|	X|
A19---	|	X|	|	X|	|	X|	|	X|
A20---	|	X|	|	X|	|	X|	|	X|
A21---	|	X|	|	X|	|	X|	|	X|
A22---	|	X|	|	X|	|	X|	|	X|
A23---	|	X|	|	X|	|	X|	|	X|
	0-64K		64K-128K		128K-192K		292K-256K	

NOTE: To enable extended address mode,
Jumper T-S must be removed and
Jumper E-B must be removed.

BANK DISABLE **********

This board is configured as 4 contiguous 16K memory banks. The banks are clearly marked BANK 0,1,2,3, on the artwork. Any 16K cell may be removed from responding when the rest of the board is selected by the appropriate setting of the bits on switch SW#. Bit switch 1 corresponds with bank number 3 (highest 16K) and switch number 2 is for the next lower bank.

EXAMPLES:

off	on	off	on	off	on	off	on
|	X|	|X	|	|	X|	|	X|
|	X|	|	X|	|X	|	|	X|
|	X|	|	X|	|	X|	|X	|
|	X|	|	X|	|	X|	|X	|
ALL BANKS ENABLED		48K-64K DIS-ABLED		32K-48K DIS-ABLED		0K-32K DIS-ABLED	

PHANTOM LINE **********

All memory banks will become disabled when S-100 bus pin 67 is pulled low. To disable this feature, cut the trace between F - H.

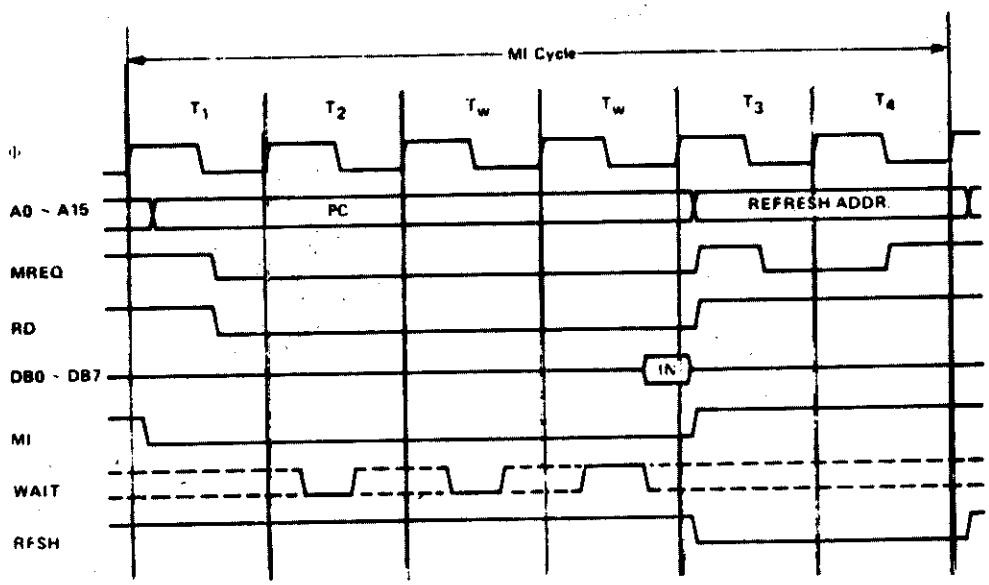
M-1 WAIT STATE GENERATION **********

In normal operation with a Z-80 CPU, no wait states will be generated.

There are certain asyncronous events that can cause the on board refresh circuitry to take over the job of periodically refreshing the dynamic memory chips. (i.e. DMA disk reads or other bus requests, or extended waits.)

When normal operation is resumed, (re-syncronization) a wait state may be automatically injected if the CPU should do a memory read while the board refresh circuitry is in midstate of a refresh cycle.

For further details of on/off board refresh timing, see theory of design and operation.



INSTRUCTION OP CODE FETCH WITH WAIT STATES

REFRESH CYCLE **********

A dynamic memory cell must be refreshed every 2ms. If not, the data bit in that cell will be lost. Refreshing a memory cell in a 4116 compatible RAM is done by placing the row address of the cell on the address inputs of the memory chip and pulsing the row address strobe (ras). Actually 128 cells are addressed and refreshed by one row address. There are 128 rows that must be refreshed, therefore a refresh cycle must occur every 2ms/128 or15.6 us.

64K REFRESH CYCLE USING Z-80 TIMING **********

The Z80 CPU provides a time period for refresh cycles, (so that wait states are not needed) refresh pulse and a 7 bit refresh address after every instruction op code fetch (M1 cycle). The 64KDQ memory uses the timing and refresh pulses provided by the Z80 for its refresh cycles. There must be a connection between the Z80's refresh output and the 64KDQ refresh input (pin 66). the 64KDQ has its own refresh address counter inside the 3242 (IC U18). The refresh address provided by the Z80 CPU is ignored.

The refresh circuit (IC-U2) on the 64KDQ uses the falling edge of phi 2 (Z80 phi not) clock and refresh not to generate one 250 ns (at 4MHZ, 500 ns at 2 MHZ) ras refresh pulse. This pulse will coincide with T4 of the Z80's M1 cycle. At the end of the refresh cycle the on board refresh counter is incremented to the next row to be refreshed.

AUTOMATIC REFRESH CYCLES **********

The Z80 CPU does not always provide refresh cycles within the 15.6 us margin, therefore automatic refresh cycles must be inserted to maintain memory integrity. There are 3 cases where the Z80 may not provide refresh cycles. They are:

RESET STATE
WAIT STATE
DMA CYCLES

The 64KDQ treats reset and wait states in the same way. If a reset or wait state occurs, an interval counter (IC U11) clocked by phi 2 is enabled. If the counter reaches a count of 14, the PRDY line (S-100 pin72) is pulled low by an open collector driver (IC U4). A refresh cycle is done during count 15. At the end of the refresh cycle the PRDY line is released, the refresh address is incremented and the interval counter starts over at zero. This continues until the reset or wait state ends.

NOTE: XRDY (S-100 BUS pin 3) is not monitored by the 64KDQ. If XRDY is pulled low the 64K will forget everything in 2ms.

DMA CYCLE **********

No automatic refresh cycles can occur during a DMA cycle. The current temporary bus master must either provide refresh pulses that are synchronized with phi 2 and that look like the refresh pulses provided by the Z80, or it must release control of the bus back to the Z80 in less than 14 us (DMA cycles must be less than 14 us total). Temporary masters must also provide MREQ on S-100 bus pin 60.

INTERFACING THE 64KDQ TO A CPU **********

The 64KDQ comes jumpered from the factory to run with the XOR CPU. Other Z80 CPU cards must provide, besides the normal S-100 bus signals, memory request/not and refresh cycle not to run with the 64KDQ. These two signals are present on all Z80 CPU chips, but may not be brought out to the S-100 bus. If your CPU does not have these signals you need to find two spare non-inverting buffers and connect the inputs to the Z80 chip pin 19 (MREQ) and pin 28 (RFSH). The buffered MREQ should be connected to S100 bus pin 60. The buffered RFSH should be connected to S100 bus pin 66. Note: you should have good technical experience before attempting to add these modifications to your cpu.

FACTORY INSTALLED JUMPERS **********

JUMPER	INSTALLED	OPEN	FUNCTION IF INSTALLED
B-C		X	NO MEMORY MANAGEMENT
B-E		X	I/O PORT MEMORY MANAGE
S-T	X		ENABLE EXTENDED ADDRESS
F-H	X		ENABLE PHANTOM PIN 67
F-J	X		PULL UP PHANTOM
M-K	X		MREQ NO INVERSION
M-L		X	INVERT MREQ
P-N	X		USE MREQ TO START MEMORY CYCLE
P-R		X	USE MWRT+SMEMR TO START CYCLE
V-U	X		IGNORE A20,21,22,23 ADD LINES
V-W		X	USE ALL EXTENDED ADDRESS LINES
E8-E9	X		RESET I/O PORT LATCH ON PR75
E8-E10		X	RESET I/O PORT LATCH ON SLV 54
E16-E15	X		RFSH NO INVERSION
E16-E14		X	INVERT RFSH
E19-E18	X		RFSH ON PIN 66
E19-E17		X	RFSF ON PIN 66
E22-E21	X		NO INVERSION OF PHI TO COUNTER
E22-E20		X	INVERT PHI 2 TO AUTO RFSH
E23-E20	X		INVERT PHI TO RFSH CYCLE FLOP
E23-E21		X	NO INVERSION OF PHI 2 TO RFSH

64K - DQ PARTS LIST

PART NO.	DESCRIPTION	QTY.	PART NO.	DESCRIPTION	QTY.
I-0000-06	HTSNK-B	2	I-7000-10	ZEN+5.1	1
I-0000-13	NUT 4-40	2	I-7000-54	74S138	1
I-0000-27	SCREW 4-40	2	I-7400-15	4116-200NS	32
I-1000-22	S164KBD	1	I-7400-28	7438	1
I-2000-05	14PSOC	10	I-7400-50	74109	1
I-2000-06	16PSOC	39	I-7400-57	74161	1
I-2000-08	20PSOC	6	I-7400-71	74LS00	1
I-2000-10	28PSOC	1	I-7400-74	74LS04	1
I-3000-11	33 OHM RES	5	I-7400-79	74LS11	1
I-3000-28	10KSIP	3	I-7400-82	74LS85	1
I-3000-51	4DIPSW	1	I-7400-87	74LS74	1
I-3000-54	8DIPSW	2	I-7400-88	74LS85	2
I-3000-58	.1MF50VR	44	I-7401-07	74LS175	1
I-3000-59	1KRESC	1	I-7401-09	74LS244	1
I-3000-68	220RES	1	I-7401-10	74LS240	5
I-3000-81	33R-PAK	1	I-7401-20	3242	1
I-3001-17	4.7MF25VR	10	I-7401-22	74LS30	1
I-7000-02	REG+5	1	I-7401-39	PE21199	1
I-7000-03	REG+12	1			

TROUBLESHOOTING

If the memory board has been in service for some time and a problem with it is suspected, a memory test should be run.

There are many faults that can occur on a memory board. Not all errors can be found by running any single memory test. We have supplied two tests that were created from years of manufacturing experience.

The first test ('MEMTEST') when run in its fundamental mode (executed under CP/M by typing M (cr) then (cr) (cr) in response to the start and stop questions,) will calculate the system size and begin a typical pattern of tests to uncover the most common problems first and the most uncommon ones last.

Typing a 'P' along with the address in the address field will PAUSE the test program after the memory fill passes. After the operator has waited an appropriate amount of time he may hit (cr) to continue the test. This feature will test for the existence of Phantom-bits. These are memory cells that change after being left un-accessed for a period of time. Initiating the test with M<sp>R<cr> will exclude the address and data tests and drop immediately into the random numbers test.

A second test called 'WORM' is designed to find memory cells that cannot stand rapid cycle time demands placed on them by some of the Z80 block move and math routines. While these chips will pass all standard memory tests for hours on end, they randomly fail during program execution time for seemingly unexplained reasons. The reason is that there is a difference between a chips ACCESS time and its CYCLE time. We generally only rate a memory board by its access time, (i.e. 450ns or 250ns.)

Worm starts itself at the load address and relocates itself repeatedly, reporting its current location periodically. It 'tests' by simply moving itself and constantly doing instruction fetches. A RAM failure is evidenced by the program crashing. The last reported address on the CRT should be interpreted to be the bank in which the errant chip resides. Binary replacing of chips, one half at a time, watching to see when the problem moves to the new bank, will uncover the bad device.

S100 BUS LINE ASSIGNMENTS

Preliminary — Subject to Revision

X = Recommended lines to terminate

	LINE	NAME	TYPE	POLARITY
	1	+8v	Bus	
	2	+15v	B	
X	3	XRDY	B	P
	4	VI0	Slave	N
	5	VI1	S	N
	6	VI2	S	N
	7	VI3	S	N
	8	VI4	S	N
	9	VI5	S	N
	10	VI6	S	N
	11	VI7	S	N
	12	NMI	S	N
	13	PWRFAIL	B	N
	14	DMA3	Master	N
	15	A18	M	P
	16	A16	M	P
	17	A17	M	P
X	18	STAT DSB	M	N
	19	C/C DSB	M	N
	20	GND	B	
	21	RFU		
X	22	ADD DSB	M	N
X	23	DO DSB	M	N
X	24	Ø2	B	P
X	25	pSTVAL	M	N
X	26	pHLDA	M	P
	27	RFU		
	28	RFU		
X	29	A5	M	P
X	30	A4	M	P
X	31	A3	M	P
X	32	A15	M	P
X	33	A12	M	P
X	34	A9	M	P
X	35	DO1/D1	M,M/S	P
X	36	DO0/D0	M,M/S	P
X	37	A10	M	P
X	38	DO4/D4	M,M/S	P
X	39	DO5/D5	M,M/S	P
X	40	DO6/D6	M,M/S	P
X	41	DI2/D10	S,M/S	P
X	42	DI3/D11	S,M/S	P
X	43	DI7/D15	S,M/S	P
X	44	sM1	M	P
X	45	sOUT	M	P
X	46	sINP	M	P
X	47	sMEMR	M	P
	48	sHLTA	M	P
X	49	CLOCK	B	N
	50	GND	B	

	LINE	NAME	TYPE	POLARITY
	51	+8v	B	
	52	-15v	B	
	53	GND	B	
	54	SLV CLR	B	N
	55	DMA0	M	N
	56	DMA1	M	N
	57	DMA2	M	N
	58	SXTRQ	M	N
	59	A19	M	P
	60	SIXTN	S	N
	61	A20	M	P
	62	A21	M	P
	63	A22	M	P
	64	A23	M	P
	65	MRQ	TTL	
	66	REFRESH	TTL	
	67	PHANTOM	B	N
X	68	MWRITE	B	P
	69	RFU		
	70	GND	B	
	71	RFU		
	72	pRDY	S	P
	73	PINT	S	N
	74	pHOLD	M	N
	75	pRESET	B	N
X	76	pSYNC	M	P
	77	PWR	M	N
X	78	pDBIN	M	P
X	79	A0	M	P
X	80	A1	M	P
X	81	A2	M	P
X	82	A6	M	P
X	83	A7	M	P
X	84	A8	M	P
X	85	A13	M	P
X	86	A14	M	P
X	87	A11	M	P
X	88	DO2/D2	M,M/S	P
X	89	DO3/D3	M,M/S	P
X	90	DO7/D7	M,M/S	P
X	91	DI4/D12	S,M/S	P
X	92	DI5/D13	S,M/S	P
X	93	DI6/D14	S,M/S	P
X	94	DI1/D9	S,M/S	P
X	95	DI0/D8	S,M/S	P
X	96	sINTA	M	P
X	97	sWO	M	N
	98	ERROR	M/S	N
	99	POC		N
	100	GND	B	

RFU = Reserved for future use.

PIN NO.	SIGNAL & TYPE	POLARITY	DESCRIPTION
1	+8 volts (B)		Instantaneous minimum greater than 7 volts, instantaneous maximum less than 25 volts, average maximum less than 11 volts.
2	+16 volts (B)		Instantaneous minimum greater than 14.5 volts, instantaneous maximum less than 35 volts, average maximum less than 21.5 volts.
3	XRDY (S)	P	One of two ready inputs to the current bus master. The bus is ready when both these ready inputs are true.
4	$\overline{VI\emptyset}$ (S)	N	Vectored interrupt line 0.
5	$\overline{VI1}$ (S)	N	Vectored interrupt line 1.
6	$\overline{VI2}$ (S)	N	Vectored interrupt line 2.
7	$\overline{VI3}$ (S)	N	Vectored interrupt line 3.
8	$\overline{VI4}$ (S)	N	Vectored interrupt line 4.
9	$\overline{VI5}$ (S)	N	Vectored interrupt line 5.
10	$\overline{VI6}$ (S)	N	Vectored interrupt line 6.
11	$\overline{VI7}$ (S)	N	Vectored interrupt line 7.
12	$\overline{NMI}$ (S)	N	Non-maskable interrupt.
13	$\overline{PWR\ FAIL}$ (B)	N	Power fail bus signal.
14	$\overline{DMA_3}$ (M)	N	Direct memory access device address at bit 3.
15	A18 (M)	P	Extended address bit 18.
16	A16 (M)	P	Extended address bit 16.
17	A17 (M)	P	Extended address bit 17.
18	$\overline{STAT\ DSB}$ (M)	N	The control signal to disable the 9 status signals.
19	$\overline{C/C\ DSB}$ (M)	N	The control signal to disable the 6 command/control signals.

PIN NO.	SIGNAL & TYPE	POLARITY	DESCRIPTION
20	GND		
21	RFU		Reserved for future use.
22	$\overline{\text{ADD DSB}}$ (M)	N	The control signal to disable the 16 address signals.
23	$\overline{\text{DO DSB}}$ (M)	N	The control signal to disable the 8 data output signals.
24	ϕ_2(B)	P	The master timing signal for the bus.
25	p$\overline{\text{STVAL}}$ (M)	N	Status valid strobe.
26	pHLDA (M)	P	A command/control signal used in conjunction with PHOLD to coordinate bus master transfer operations.
27	RFU		Reserved for future use.
28	RFU		Reserved for future use.
29	A5 (M)	P	Address bit 5.
30	A4 (M)	P	Address bit 4.
31	A3 (M)	P	Address bit 3.
32	A15 (M)	P	Address bit 15 (most signficant for non-extended addressing).
33	A12 (M)	P	Address bit 12.
34	A9 (M)	P	Address bit 9.
35	DO1 (M)/DATA 1 (M/S)	P	Data out bit 1, bidirectional data bit 1.
36	DOØ (M)/DATA Ø (M/S)	P	Data out bit Ø, bidirectional data bit Ø.
37	A10 (M)	P	Address bit 10.
38	DO4 (M)/DATA 4 (M/S)	P	Data out bit 4, bidirectional data bit 4.
39	DO5 (M)/DATA 5 (M/S)	P	Data out bit 5, bidirectional data bit 5.
40	DO6 (M)/DATA 6 (M/S)	P	Data out bit 6, bidirectional data bit 6.
41	DI2 (S)/DATA 1Ø (M/S)	P	Data in bit 2, bidirectional data bit 1Ø.

PIN NO.	SIGNAL & TYPE	POLARITY	DESCRIPTION
42	DI3 (S)/DATA 11 (M/S)	P	Data in bit 3, bidirectional data bit 11.
43	DI7 (S)/DATA 15 (M/S)	P	Data in bit 7, bidirectional data bit 15.
44	sM1 (M)	P	The status signal which indicates that the current cycle is an op-code fetch.
45	sOUT (M)	P	The status signal identifying the data transfer bus cycle of an OUT instruction.
46	sINP (M)	P	The status signal identifying the data transfer bus cycle of an IN instruction.
47	sMEMR (M)	P	The status signal identifying bus cycles which transfer data from memory to a bus master which are not interrupt acknowledge instruction fetch cycle(s).
48	sHLTA (M)	P	The status signal which acknowledges that a HLT instruction has been executed.
49	$\overline{\text{CLOCK}}$ (B)		2 MHz (2%) 40-60% duty cycle. Not required to be synchronous with any other bus signals.
50	GND		
51	+8 volts (B)		See comments for pin no. 1.
52	-16 volts (B)		Instantaneous maximum less than -14.5 volts, instantaneous minimum greater than -35 volts, average minimum greater than -21.5 volts.
53	GND		
54	$\overline{\text{SLAVE CLR}}$ (B)	N	A reset signal to reset bus slaves. Must be active with $\overline{\text{POC}}$ and may also be generated by external means.
55	$\overline{\text{DMA}}_0$ (M)	N	Direct memory access device address bit Ø.
56	$\overline{\text{DMA}}_1$ (M)	N	Direct memory access device address bit 1.
57	$\overline{\text{DMA}}_2$ (M)	N	Direct memory access device address bit 2.

PIN NO.	SIGNAL & TYPE	POLARITY	DESCRIPTION
58	$\overline{\text{SXTRQ}}$ (M)	N	The status signal which requests 16-bit slaves to assert $\overline{\text{SIXTN}}$.
59	A19	P	Extended address bit 19.
60	$\overline{\text{SIXTN}}$ (S)	N	The signal generated by 16-bit slaves in response to the 16-bit request signal $\overline{\text{SXTRQ}}$.
61	A20 (M)	P	Extended address bit 20.
62	A21 (M)	P	Extended address bit 21.
63	A22 (M)	P	Extended address bit 22.
64	A23 (M)	P	Extended address bit 23.
65	MRQ		Undefined; restricted to TTL levels.
66	REFRESH		Undefined; restricted to TTL levels.
67	$\overline{\text{PHANTOM}}$ (B)	N	A bus signal which disables normal slave devices and enables phantom slaves – primarily used for boot-strapping systems without hardware front panels.
68	MWRITE (B)	P	$\sim$ (p$\overline{\text{WR}}$ + sOUT) This signal must follow p$\overline{\text{WR}}$ by not more than 30ns.
69	RFU		Reserved for future use.
70	GND		
71	RFU		Reserved for future use.
72	PRDY (S)	P	See comments for pin no. 3.
73	$\overline{\text{PINT}}$ (S)	N	The primary interrupt request bus signal.
74	p$\overline{\text{HOLD}}$ (M)	N	The command/control signal used in conjunction with pHLDA to coordinate bus master transfer operations.
75	p$\overline{\text{RESET}}$ (B)	N	The reset signal to reset bus master devices. This signal must be active with $\overline{\text{POC}}$ and may also be generated by external means.

PIN NO.	SIGNAL & TYPE	POLARITY	DESCRIPTION
76	pSYNC (M)	P	The command/control signal identifying BS.
77	$\overline{\text{pWR}}$ (M)	N	The command/control signal signifying the presence of valid data on DO bus or DATA bus.
78	pDBIN (M)	P	The command/control signal that requests data on the DI bus or DATA bus from the currently addressed slave.
79	AØ (M)	P	Address bit Ø (least significant).
80	A1 (M)	P	Address bit 1.
81	A2 (M)	P	Address bit 2.
82	A6 (M)	P	Address bit 6.
83	A7 (M)	P	Address bit 7.
84	A8 (M)	P	Address bit 8.
85	A13 (M)	P	Address bit 13.
86	A14 (M)	P	Address bit 14.
87	A11 (M)	P	Address bit 11.
88	DO2 (M)/DATA2 (M/S)	P	Data out bit 2, bidirectional data bit 2.
89	DO3 (M)/DATA3 (M/S)	P	Data out bit 3, bidirectional data bit 3.
90	DO7 (M)/DATA7 (M/S)	P	Data out bit 7, bidirectional data bit 7.
91	DI4 (S)/DATA12 (M/S)	P	Data in bit 4 and bidirectional data bit 12.
92	DI5 (S)/DATA13 (M/S)	P	Data in bit 5 and bidirectional data bit 13.
93	DI6 (S)/DATA14 (M/S)	P	Data in bit 6 and bidirectional data bit 14.
94	DI1 (S)/DATA9 (M/S)	P	Data in bit 1 and bidirectional data bit 9.

PIN NO.	SIGNAL & TYPE	POLARITY	DESCRIPTION
95	DIØ (S)/DATA8 (M/S)	P	Data in bit Ø (least significant for 8 bit data) and bidirectional data bit 8.
96	sINTA (M)	P	The status signal identifying the bus input cycle(s) that may follow an accepted interrupt request presented on pINT.
97	sWO (M)	N	The status signal identifying a bus cycle which transfers data from a bus master to a slave.
98	ERROR (S)	N	The bus status signal signifying an error condition during a present or previous bus cycle.
99	POC (B)	N	The power-on clear signal for all bus devices; when this signal goes low, it must stay low for at least 3 bus states.
100	GND		

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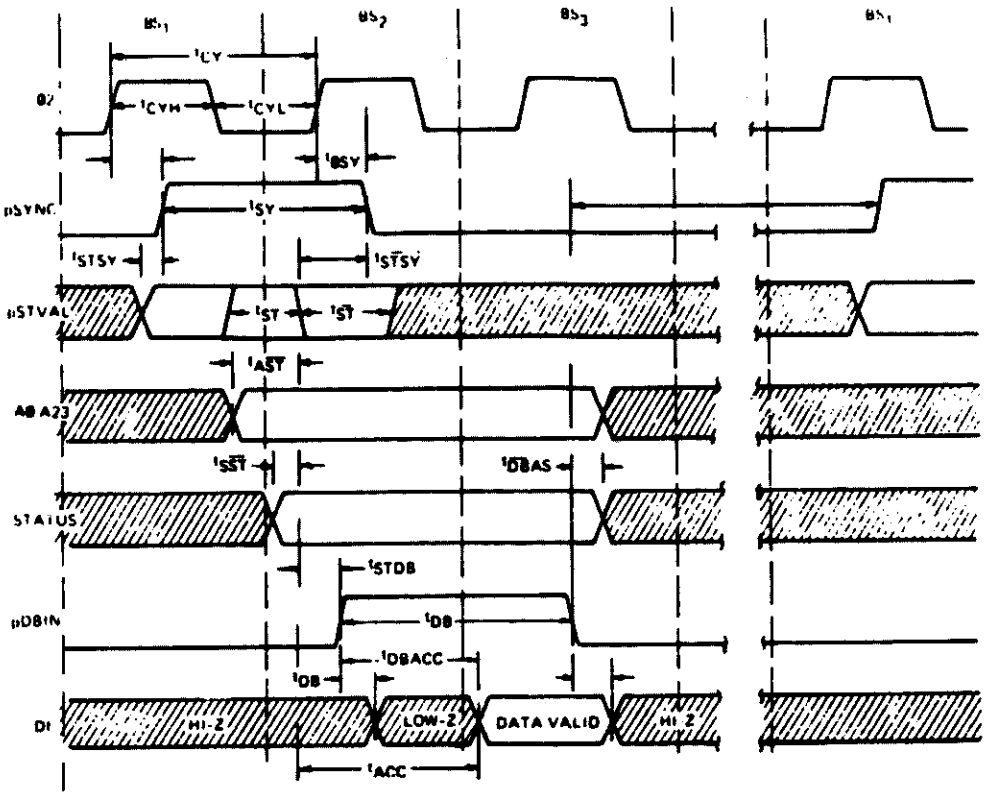
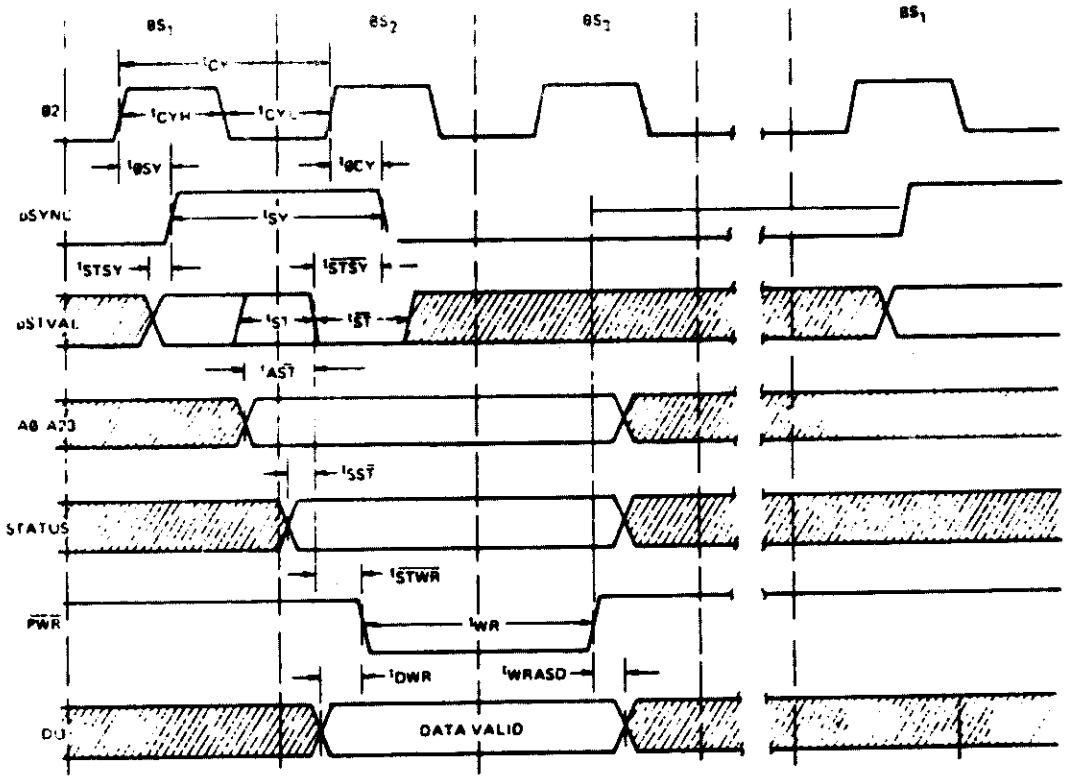
		MIN.	MAX. (nsec.)
t_{CY}	Ø2 period	166	2000
t_{CYH}	Ø2 pulse width high	$.4t_{CY}$	$.6t_{CY}$
t_{CYL}	Ø2 pulse width low	$.4t_{CY}$	$.6t_{CY}$
$t_{ØSY}$	delay Ø2 high to pSYNC high; delay Ø2 low to pSYNC low	10	$.25t_{CY}+5$
t_{SY}	pSYNC pulse width high	$.9t_{CY}$	
$t_{\overline{STSY}}$	$\overline{\text{pSTVAL}}$ low prior to pSYNC low	0	$t_{SY}-50$
t_{ST}	$\overline{\text{pSTVAL}}$ pulse width high	50	
$t_{\overline{ST}}$	$\overline{\text{pSTVAL}}$ pulse width low	50	
t_{STSY}	$\overline{\text{pSTVAL}}$ falling edge prior to pSYNC high	0	
$t_{A\overline{S}T}$	Addresses stable prior to $\overline{\text{pSTVAL}}$ low during pSYNC high	70	
$t_{S\overline{ST}}$	Status stable prior to $\overline{\text{pSTVAL}}$ low during pSYNC high	50	
t_{DB}	pDBIN pulse width high	$.9t_{CY}$	$1.1t_{CY}$
$t_{\overline{ST}DB}$	delay $\overline{\text{pSTVAL}}$ low to pDBIN high	30	
$t_{\overline{DB}SY}$	delay pDBIN low to pSYNC high	0	
$t_{\overline{DB}AS}$	hold time for addresses and status after pDBIN low	0	
$t_{\overline{DB}Z}$	delay pDBIN low to slave DI drivers Hi-Z		$25+.1t_{CY}$
$t_{DB\overline{Z}}$	delay pDBIN high to slave DI drives active	10	$25+.1t_{CY}$
t_{ACC}	delay $\overline{\text{pSTVAL}}$ low to data valid	Specified by manufacturer. Worst case maximum for all slaves and worst case minimum for all masters.	
t_{DBACC}	setup time pDBIN high td data valid	$40+.1t_{CY}$	

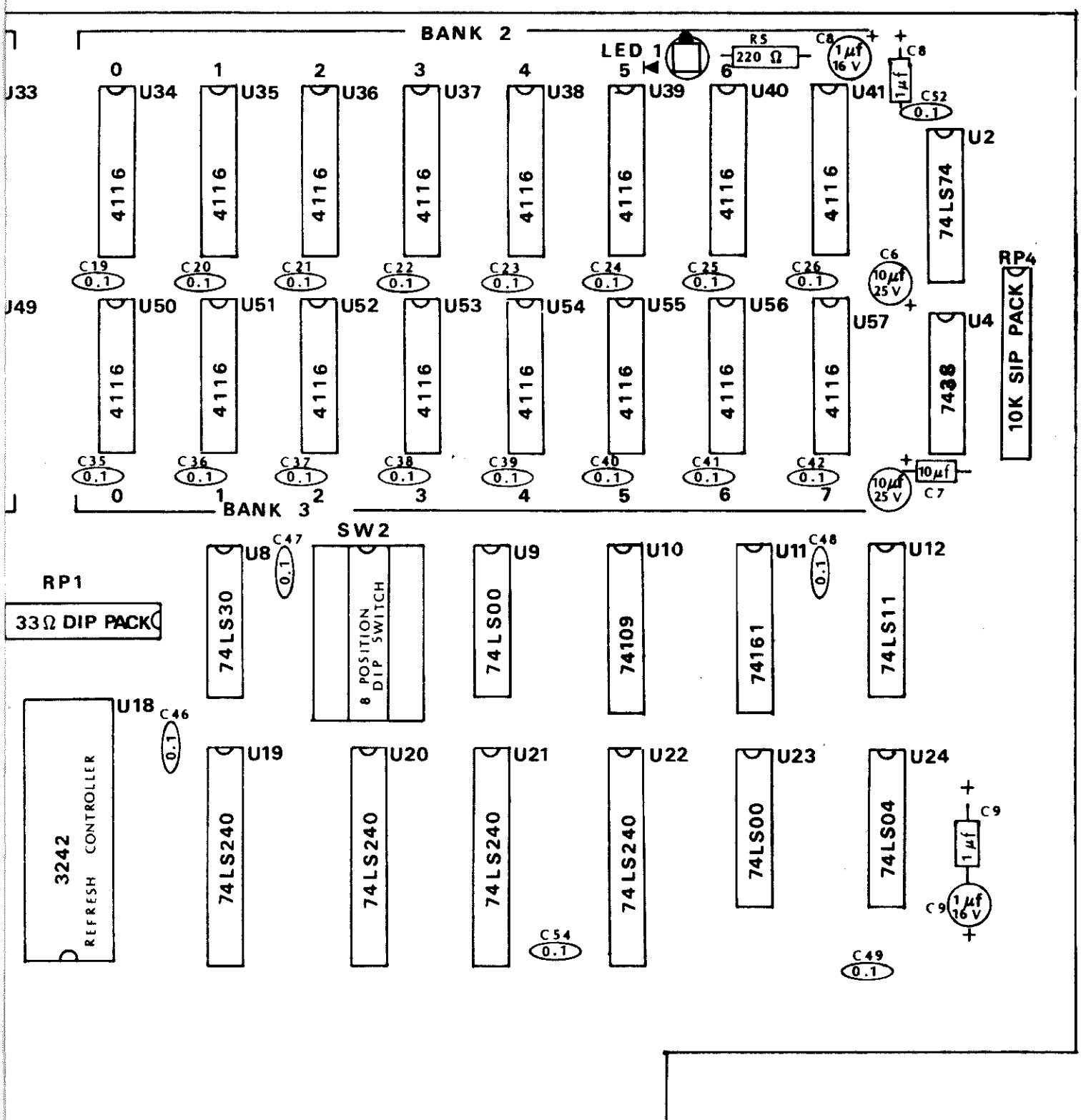
		MIN.	MAX. (nsec.)
$t_{\overline{WR}}$	$\overline{pWR}$ pulse width low	$.9t_{CY}$	$1.1t_{CY}$
$t_{\overline{STWR}}$	delay $\overline{pSTVAL}$ low to $\overline{pWR}$ low	30	
t_{WRSY}	delay $\overline{pWR}$ high to pSYNC high	0	
$t_{D\overline{WR}}$	setup time DO valid to $\overline{pWR}$ low	$.1t_{CY}$	
t_{WRASD}	hold time addresses, status, and DO to $\overline{pWR}$ high	$.2t_{CY}$	
t_{WRMR}	delay $\overline{pWR}$ low to MWRITE high; delay $\overline{pWR}$ high to MWRITE low		30
$t_{\overline{WR}SIX}$	access time $\overline{pWR}$ low to $\overline{SIXTN}$ valid		$40+.1t_{CY}$
$t_{WR\overline{SIX}}$	delay $\overline{pWR}$ high to $\overline{SIXTN}$ Hi-Z	10	$40+.1t_{CY}$

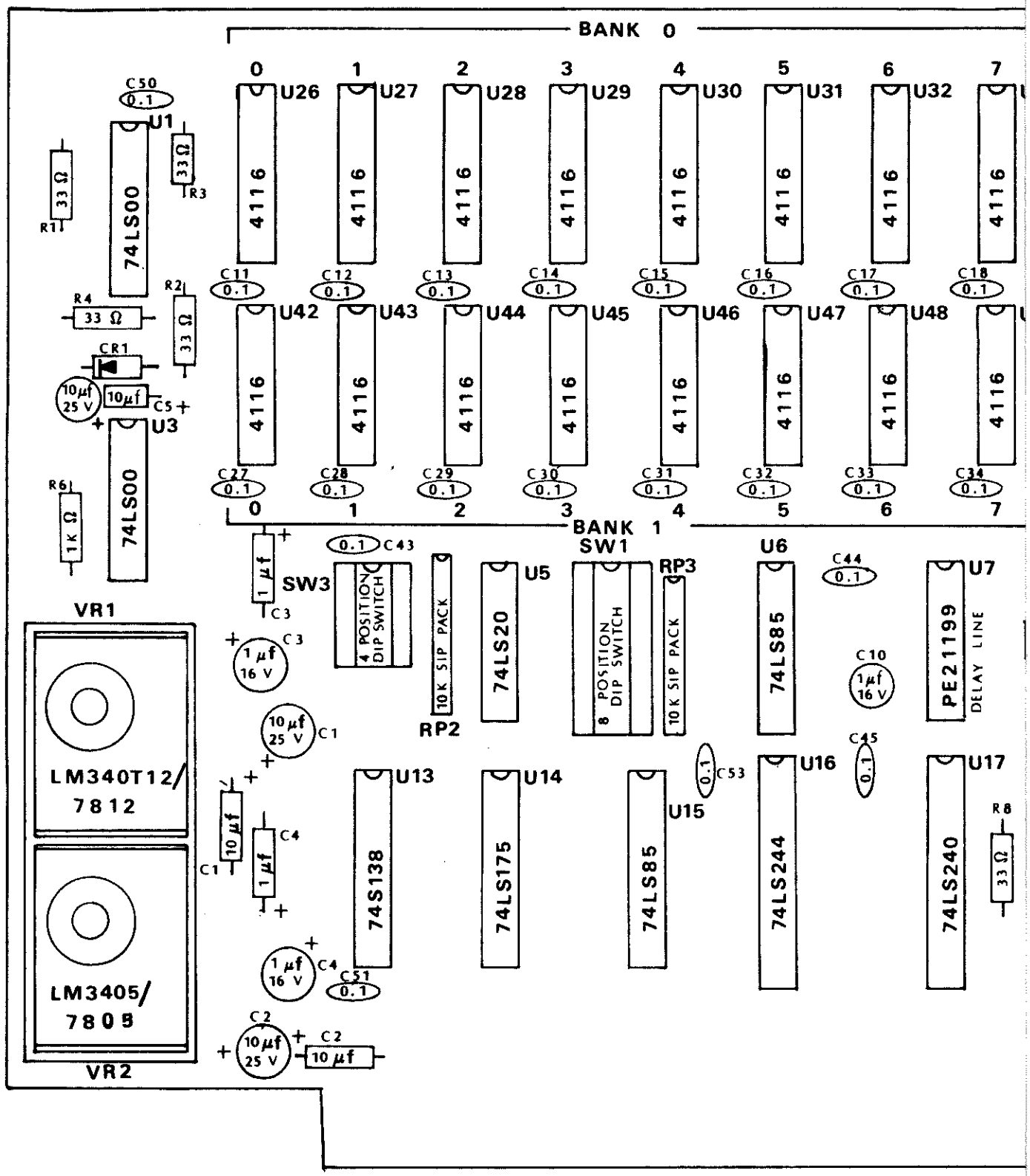
READ CYCLE

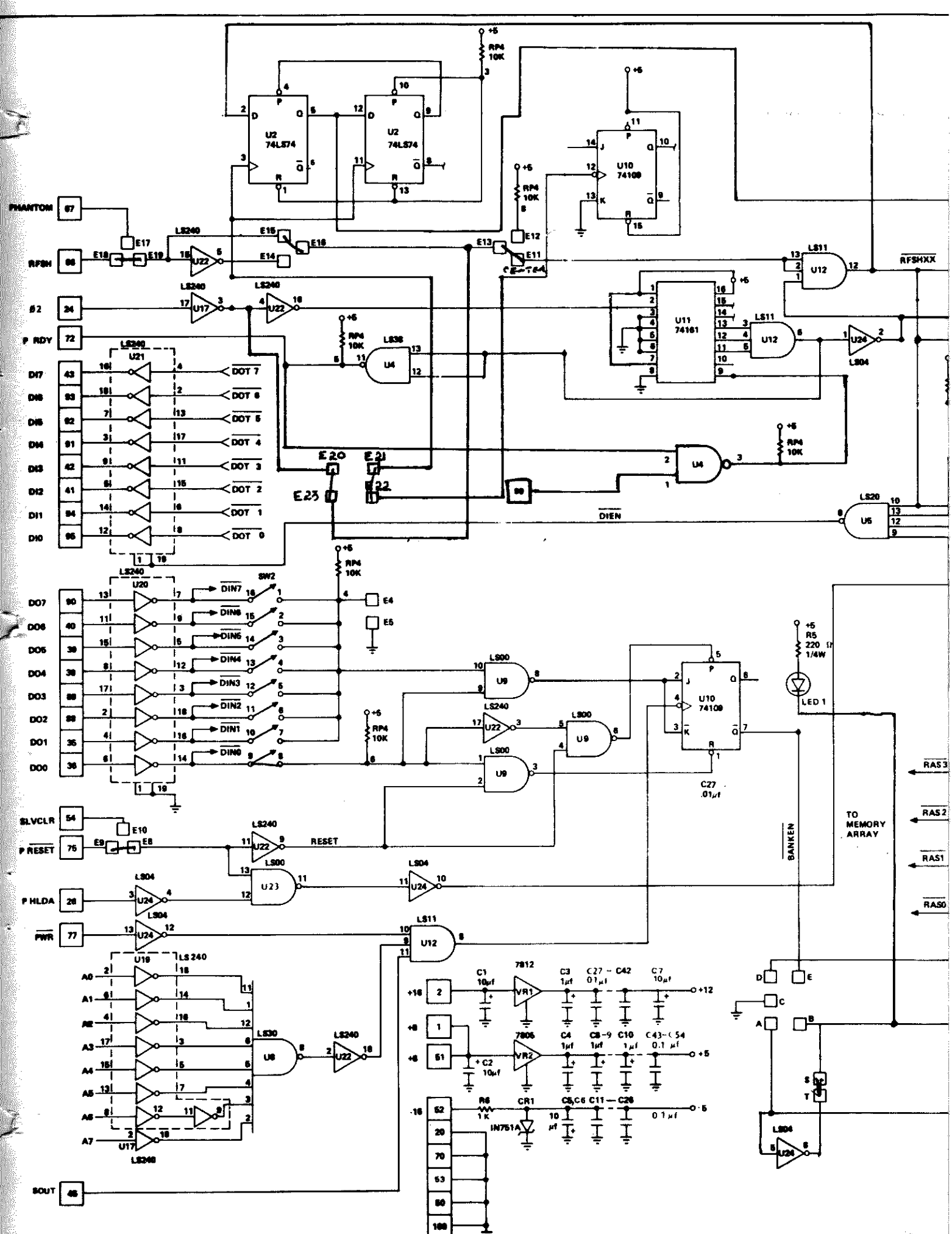


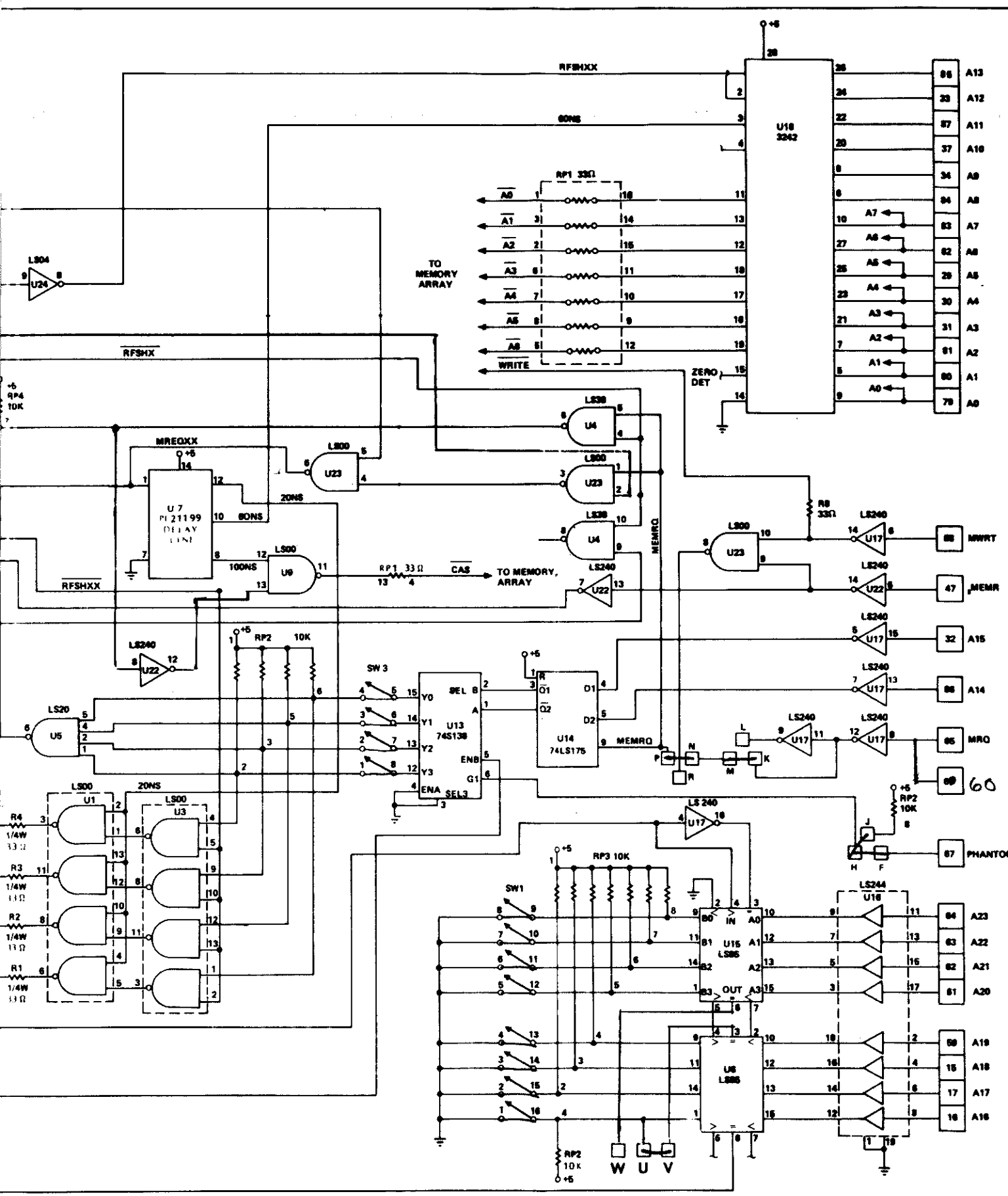
WRITE CYCLE

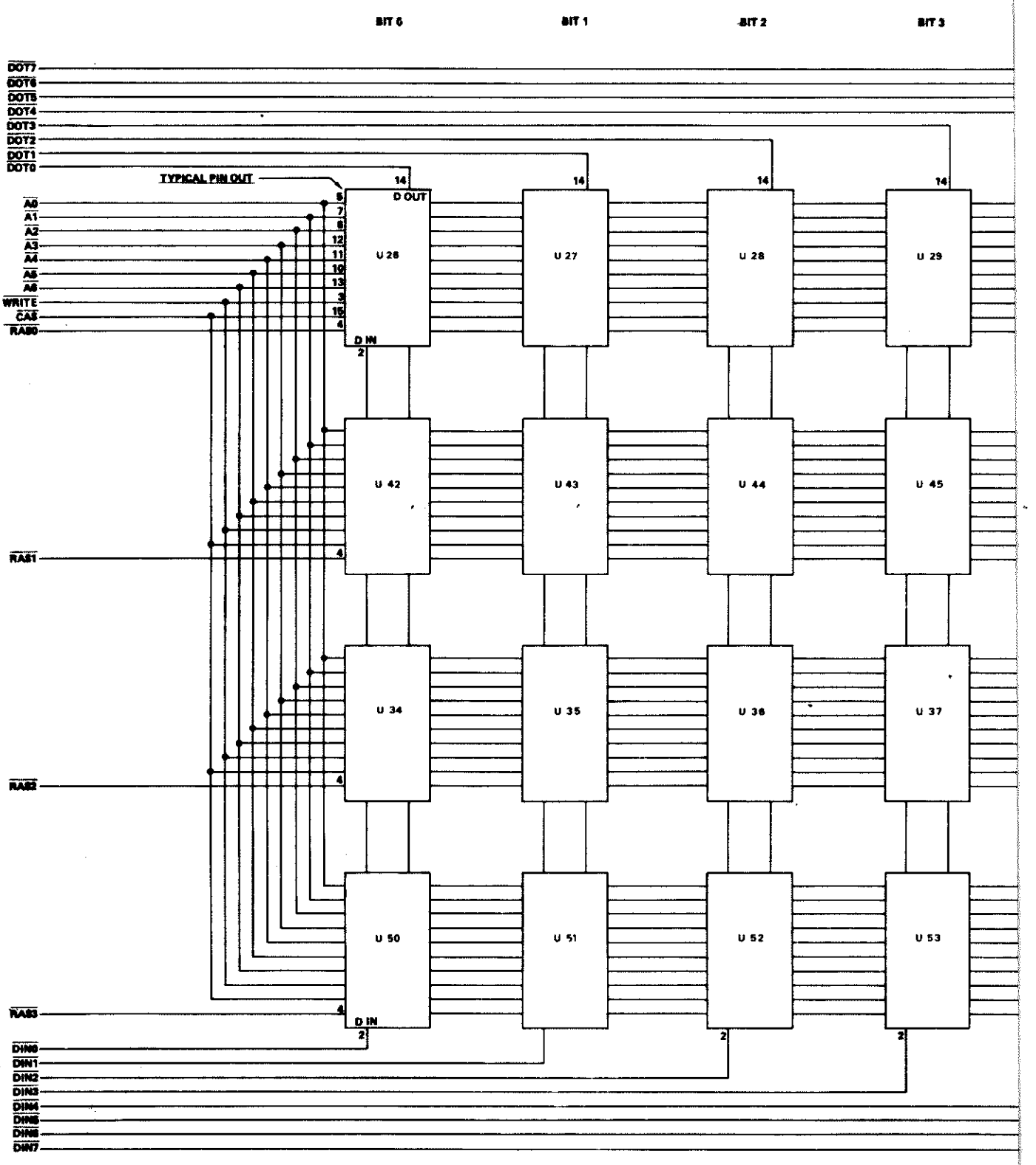


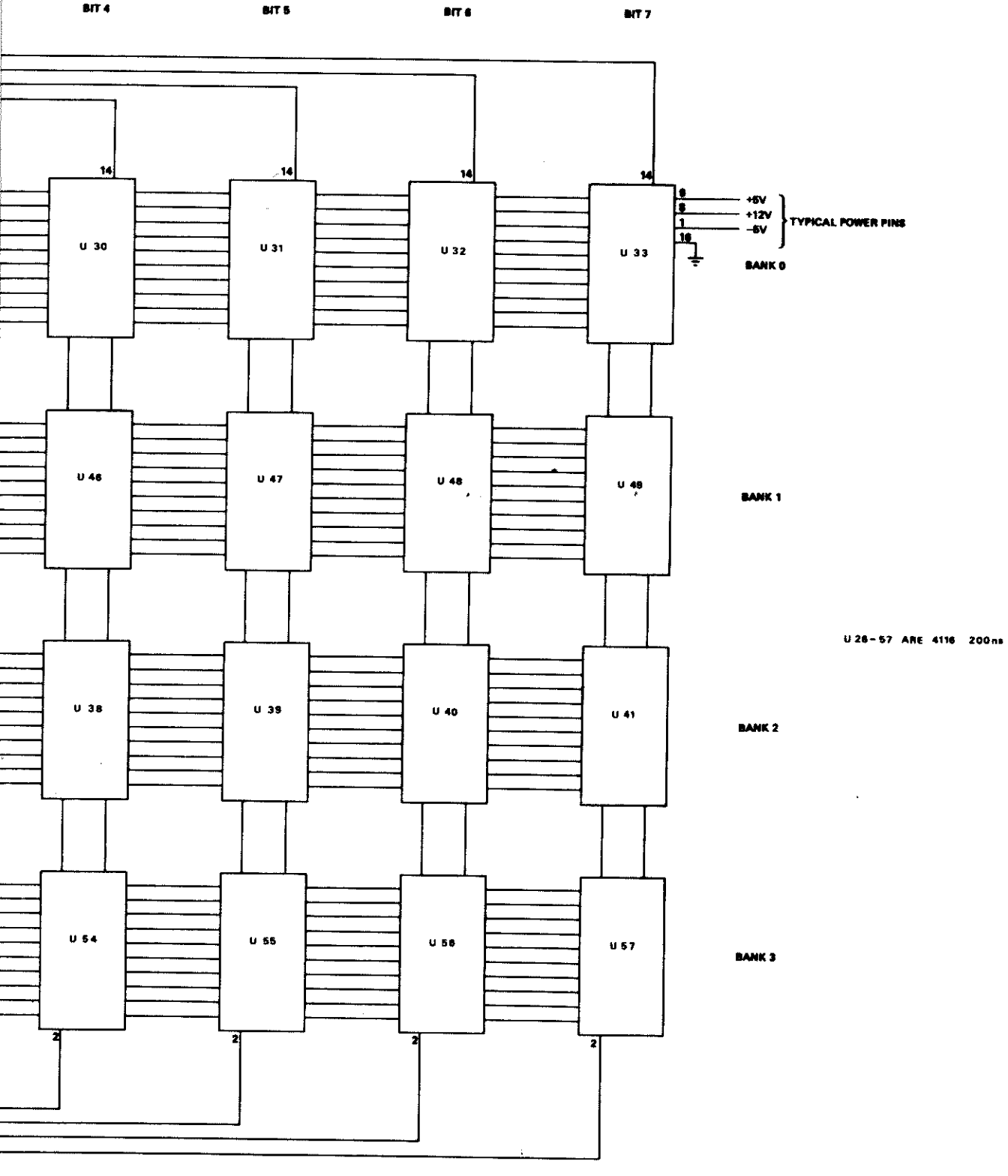

BANK 2
LED 1
R5
220 Ω
C8
1 µf 16 V
C52
0.1
U2
74LS74
RP4
10K SIP PACK
U33
U34
U35
U36
U37
U38
U39
U40
U41
4116
C19
C20
C21
C22
C23
C24
C25
C26
C6
10µf 25 V
U49
U50
U51
U52
U53
U54
U55
U56
U57
U4
7438
C35
C36
C37
C38
C39
C40
C41
C42
C7
BANK 3
SW2
8 POSITION DIP SWITCH
RP1
33Ω DIP PACK
U8
74LS30
C47
U9
74LS00
U10
74109
U11
74161
C48
U12
74LS11
U18
3242
REFRESH CONTROLLER
C46
U19
74LS240
U20
74LS240
U21
74LS240
C54
U22
74LS240
U23
74LS00
U24
74LS04
C9
C49


BANK 0
BANK 1
U26
U27
U28
U29
U30
U31
U32
U42
U43
U44
U45
U46
U47
U48
4116
74LS00
U1
U3
R1
R2
R3
R4
R6
CR1
C50
C11
C12
C13
C14
C15
C16
C17
C18
C27
C28
C29
C30
C31
C32
C33
C34
C5
C3
C1
C4
C43
C51
C53
C44
C45
C10
C2
SW3
SW1
RP2
RP3
4 POSITION DIP SWITCH
8 POSITION DIP SWITCH
10K SIP PACK
74LS20
74LS85
74S138
74LS175
74LS244
74LS240
PE21199
DELAY LINE
U5
U6
U7
U13
U14
U15
U16
U17
R8
VR1
VR2
LM340T12/
7812
LM3405/
7805
33 Ω
1K Ω
10µf
25 V
1 µf
16 V
0.1


PHANTOM
RFSH
Ø2
P RDY
DI7
DI6
DI5
DI4
DI3
DI2
DI1
DI0
DO7
DO6
DO5
DO4
DO3
DO2
DO1
DO0
SLVCLR
P RESET
P HLDA
PWR
SOUT
A0
A1
A2
A3
A4
A5
A6
A7
U2 74LS74
U10 74109
U11 74161
RP4 10K
LS240
LS00
LS04
LS11
LS20
LS30
DOT 7
DOT 6
DOT 5
DOT 4
DOT 3
DOT 2
DOT 1
DOT 0
DIN7
DIN6
DIN5
DIN4
DIN3
DIN2
DIN1
DIN0
SW2
RESET
DIEN
RFSHXX
BANKEN
TO MEMORY ARRAY
RAS3
RAS2
RAS1
RAS0
LED 1
R5 220 1/4W
7812
7805
VR1
VR2
IN751A
C1 10µf
C2 10µf
C3 1µf
C4 1µf
C7 10µf
C10 1µf
C27 - C42 .01µf
C43-C54 0.1 µf
R6 1K
CR1
+16
+12
+8
+5
-16
-5


RFSHXX
80NS
U18
3242
RP1 33Ω
TO MEMORY ARRAY
WRITE
ZERO DET
A13
A12
A11
A10
A9
A8
A7
A6
A5
A4
A3
A2
A1
A0
LS04
U24
RFSHX
+5
RP4
10K
MREQXX
U7
PL21199
DELAY LINE
20NS
80NS
100NS
U9
LS00
U23
U4
LS38
RP1 33Ω
CAS
TO MEMORY, ARRAY
MEMRQ
R8
33Ω
LS240
U17
U22
MWRT
MEMR
A15
A14
MRQ
60
PHANTOM
RP2
10K
SW 3
U13
74S138
SEL B
SEL3
ENB
G1
ENA
U14
74LS175
MEMRQ
LS20
U5
LS00
U1
U3
20NS
R4
R3
R2
R1
1/4W
RP3 10K
SW1
LS244
U16
U15
LS885
U6
LS885
IN
OUT
A23
A22
A21
A20
A19
A18
A17
A16
W
U
V


BIT 0
BIT 1
BIT 2
BIT 3
DOT7
DOT6
DOT5
DOT4
DOT3
DOT2
DOT1
DOT0
TYPICAL PIN OUT
A0
A1
A2
A3
A4
A5
A6
WRITE
CAS
RAS0
RAS1
RAS2
RAS3
D OUT
D IN
U 26
U 27
U 28
U 29
U 42
U 43
U 44
U 45
U 34
U 35
U 36
U 37
U 50
U 51
U 52
U 53
DIN0
DIN1
DIN2
DIN3
DIN4
DIN5
DIN6
DIN7



U 26 - 57 ARE 4116 200 ns


XOR