HP 1000 M/E/F-Series

Firmware Installation and Reference Manual

The following products are covered:

HP 13304A Firmware Accessory Board
HP 12791A Firmware Expansion Module
HP 13197A Writable Control Store Board
HP 13305A Dynamic Mapping System
HP 12731A Memory Expansion Module
HP 13307A Dynamic Mapping Instruction Firmware
HP RTE IV A/B Extended Memory Area Firmware
HP 13306A E-Series Fast FORTRAN Processor Firmware
HP 1000 F-Series Fast FORTRAN Processor Firmware
HP 1000 F-Series Scientific Instruction Set Firmware
HP 12824A Vector Instruction Set Firmware
HP 91740B Distributed System (DS/1000) Firmware
HP 1000 E-Series Base Set and EIG/Floating Point Firmware
HP 1000 F-Series Base Set and EIG/Floating Point Firmware

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New editions are complete revisions of the manual. Update packages contain replacement pages or write-in instructions to be merged into the manual by the customer. Manuals will be reprinted as necessary to incorporate all prior updates. A reprinted manual is identical in content (but not in appearance) to the previous edition with all updates incorporated. No information is incorporated into a reprinting unless it appears as a prior update. The edition does not change.

First Edition ..... June 1979	
Second Edition ..... Sept 1979	Update SIS ROM part numbers
Update 1 ..... Mar 1980	Add E/F-Series Base Set sections. Change Base Set ROM numbers for 12823F. Update F-Series FFP to reflect installation of 4K ROMs on the FEM.
Reprinted ..... Mar 1980	Incorporate Update 1

LIST OF EFFECTIVE PAGES

The List of Effective Pages gives the most recent update number on which the technical material on any given page was altered. If a page is simply re-arranged due to a technical change on a previous page, it is not listed as a updated page. Within the manual, changes are marked with a vertical bar in the margin. When a update is incorporated in a reprinted manual, the update number and vertical bar in the margin is removed but the update number will remain on this List of Effective Pages page.

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PREFACE

The firmware described in this manual is standard or optional firmware for the HP 1000 E/F-Series Computer. The 13304A FAB, 12791A FEM, and 13197A WCS are options for M/E/F-Series Computers. M-Series firmware options are not included in this manual, information for these can be found in the following manuals.

a. *HP 21MX Computer Series Installation and Service Manual,* part no. 02108-90006.

b. *HP 21MX Computer Series Reference Manual,* part no. 02108-90002.

c. *HP 21MX Computer Series Operator's Manual,* part no. 02108-90004.

d. *HP 21MX M-Series Computer HP 2108B and HP 2112B Operating and Reference Manual,* part no. 02108-90037.

e. *HP 1000 M-Series Computer HP 2108B and HP 2112B Installation and Service Manual,* part no. 02108-90035.

f. *HP 12945A M-Series User Control Store Board Installation Manual,* part no. 12945-90001.

g. *HP 12978A M-Series Writable Control Store Board Reference Manual,* part no. 12978-90007.

h. *HP 12976B M-Series Dynamic Mapping System Installation Manual,* part no. 12976-90005.

i. *HP 12977B M-Series Fast Fortran Processor Installation Manual,* part no. 12977-90008.

j. *HP 91740A M-Series Distributed System (DS/1000) Firmware Installation Manual,* part no. 91740-90007.

Additional information for E/F-Series Computers is provided in the following manuals.

a. *HP 1000 E-Series or F-Series Operating and Reference Manual.*

b. *HP 1000 E-Series or F-Series Installation and Service Manual.*

c. *HP 1000 E/F-Series Computer Microprogramming Reference Manual,* part no. 02109-90001.

d. *HP 12892A Memory Protect Installation Manual,* part no. 12892-90007.

CONTENTS

HP 13304A FIRMWARE ACCESSORY BOARD

SECTION I

1-1. INTRODUCTION

This section provides installation instructions and service information for the HP 13304A Firmware Accessory Board (FAB) which is standard on HP 1000 E/F-Series Computers. Installation and reference information for the various HP firmware options which can be installed on the FAB can be found in the appropriate section of this manual. Additional information is provided in the manuals listed in the preface.

1-2. DESCRIPTION

The 16,384 words of addressable control store in the HP 1000 E/F-Series Computer are divided into sixty-four 256-word modules (0 through 63). See figure 11-2 or 11-3 in section XI for the allocation of Control Memory. The computer base instruction set is not available to the user microprogrammer. Any other control store module not filled by microprogrammed Hewlett-Packard options are available to the user microprogrammer. It is recommended that the user microprogrammer only use modules which are not HP reserved or specified for HP microprogrammed options.

The HP 13304A Firmware Accessory Board (FAB) includes space for 3,584 words of addressable control memory and consists of 30 integrated-circuit (IC) sockets to accommodate up to 14 modules of control memory. These 14 modules are arranged into four addressable blocks (A, B, C, and D) of control memory. Each addressable block has its own jumper configuration which will determine its associated control memory module addresses.

BLOCK ADDRESSING

Block A (sockets A1 through A12) consists of twelve 1K (256 word by 4 bit) read-only-memory (ROM) IC's which include space for 512 words (two modules) of addressable control memory. ROM IC's to be installed in block A must be configured as two contiguous modules; e.g., modules 46 (sockets A1 through A6) and 47 (sockets A7 through A12). The least significant module (LSM) corresponds to the lower number IC sockets (A1 through A6). The most significant module (MSM) corresponds to the higher number IC sockets (A7 through A12). (See figure 1-2 and table 1-1).

Blocks B, C, and D (sockets B1 through B6, sockets C1 through C6, and sockets D1 through D6, respectively) each consist of six 4K (512 word by 8 bit) ROM IC's; each of these three blocks includes space for 1,024 words (four modules) of addressable control memory. ROM IC's to be installed in blocks B, C, or D must be configured as four contiguous modules; e.g., modules 60, 61, 62, and 63. If block B is used, the least significant module pair (LSMP) corresponds to the lower number IC sockets (B1 through B3) and the most significant module pair (MSMP) corresponds to the higher number IC sockets (B4 through B6). (See figure 1-2 and table 1-2.) Each ROM IC must be tested, burned, and verified according to the user's need, or purchased from Hewlett-Packard as an option.

PRIORITY

Control Store modules installed on the FAB assembly have lower priority than the HP 13197A Writable Control Store (WCS), the HP 12791A Firmware Expansion Module (FEM), and the base instruction set located on the CPU PCA (modules 0-3). In other words, if the instruction set or the optional WCS, or FEM is enabled and then addressed, control store installed on the FAB assembly is disabled.

KIT CONTENTS

The HP 13304A Firmware Accessory Board Kit consists of the following:

Description	HP Part No.	Quantity
Screw, machine, panhead, no. 6-32, 1/4 in. (with external toothed lockwasher)	2360-0113	4
Jumper, plug	1258-0124	14
Firmware Accessory Board Assembly	5061-1339	1
Ribbon Cable Assembly	5061-1336	1
M/E/F-Series Firmware Installation and Reference Manual	12791-90001	1

MODULE NO.	ADDRESSES		JUMPER PREFIX				UPPER/ LOWER 8K JUMPER
	DECIMAL	OCTAL	NOTE 1 9	10	11	12	NOTE 2 13
0	0-00255	00000-00377	0	0	0	0	0
1	00256-00511	00400-00777	1				
2	00512-00767	01000-01377					
3	00768-01023	01400-01777					
4	01024-01279	02000-02377	0	1	0	0	0
5	01280-01535	02400-02777	1				
6	01536-01761	03000-03377					
7	01762-02047	03400-03777					
8	02048-02303	04000-04377	0	0	1	0	0
9	02304-02559	04400-04777	1				
10	02560-02815	05000-05377					
11	02816-03071	05400-05777					
12	03072-03327	06000-06377	0	1	1	0	0
13	03328-03583	06400-06777	1				
14	03584-03849	07000-07377					
15	03850-04095	07400-07777					
16	04096-04351	10000-10377	0	0	0	1	0
17	04352-04607	10400-10777	1				
18	04608-04863	11000-11377					
19	04864-05119	11400-11777					
20	05120-05375	12000-12377	0	1	0	1	0
21	05376-05631	12400-12777	1				
22	05632-05887	13000-13377					
23	05888-06143	13400-13777					
24	06144-06399	14000-14377	0	0	1	1	0
25	06400-06655	14400-14777	1				
26	06656-06911	15000-15377					
27	06912-07167	15400-15777					
28	07168-07423	16000-16377	0	1	1	1	0
29	07424-07679	16400-16777	1				
30	07680-07935	17000-17377					
31	07936-08191	17400-17777					
32	08192-08447	20000-20377	0	0	0	0	1
33	08448-08703	20400-20777	1				
34	08704-08959	21000-21377					
35	08960-09215	21400-21777					
36	09216-09571	22000-22377	0	1	0	0	1
37	09572-09727	22400-22777	1				
38	09728-09983	23000-23377					
39	09984-10239	23400-23777					
40	10240-10495	24000-24377	0	0	1	0	1
41	10496-10751	24400-24777	1				
42	10752-10917	25000-25377					
43	10918-11263	25400-25777					
44	11264-11519	26000-26377	0	1	1	0	1
45	11520-11775	26400-26777	1				
46	11776-12031	27000-27377					
47	12032-12287	27400-27777					
48	12288-12543	30000-30377	0	0	0	1	1
49	12544-12799	30400-30777	1				
50	12800-13055	31000-31377					
51	13056-13311	31400-31777					
52	13312-13557	32000-32377	0	1	0	1	1
53	13558-13823	32400-32777	1				
54	13824-14079	33000-33377					
55	14080-14335	33400-33777					
56	14336-14591	34000-34377	0	0	1	• 1	1
57	14592-14847	34400-34777	1				
58	14848-15103	35000-35377					
59	15104-15359	35400-35777					
60	15360-15615	36000-36377	0	1	1	1	1
61	15616-15871	36400-36777	1				
62	15872-16127	37000-37377					
63	16128-16383	37400-37777					

1. Jumper 9 applies to block A only.
2. Jumper 13 selects upper or lower 8K of control store.
3. See figure 1-2 for jumper locations.

Figure 1-1. FAB Assembly Jumper Configurations

RECOMMENDED PROMs

One of the following recommended PROMs must be used to ensure reliable operation.

4K PROMs		1K PROMs	
HP Part No.	1816-1142	HP Part No.	1816-0782
Signetics	N82S141F	Signetics	N82S129F
Harris	HMI-7641-5	Harris	HMI-7611-5
		Monolithic Memories	6301

1-3. INSTALLATION/REMOVAL

Figure 1-2 shows the locations of the addressable block jumpers and ROM IC sockets. The shaded areas show the location of each ROM IC socket. Jumpers are designated 9A through 12A, 10B through 12B, 10C through 12C, 10D through 12D, and 13. The numerical jumper notations represent the ROM address register bits 9 through 13. The alphabetical jumper notations represent the associated block of addressable control store. In other words, jumper notations A, B, C, and D correspond to blocks A, B, C, and D, respectively.

INSTALLATION PROCEDURE

CAUTION

ROM IC's may be permanently damaged if oriented incorrectly when installed and power is applied.

a. Consult with the system programmer and determine the starting address and length of control store required for the microprogram.

b. For block A configuration, use table 1-1 and figure 1-1 for ROM location and jumper configuration requirements, respectively. Use the following example as a guide:

1. Assuming the microprogram operates between 27000_8 and 27777_8, figure 1-1 shows that modules 46 and 47 are required.

2. Determine if the microprogram operates in the least significant module (LSM) or the most significant module (MSM). Module 46 is the LSM and module 47 is the MSM.

3. If part of the microprogram operates in the LSM (27000_8 to 27377_8) install the corresponding six 1K ROM IC's in sockets A1 through A6. If part of the microprogram operates in the MSM (27400_8 to 27777_8), install the corresponding six 1K ROM IC's in sockets A7 through A12. (Refer to table 1-1 and figure 1-2.) Ensure that the IC's are oriented correctly as shown in figure 1-2 by matching pin 1 of each IC with the white dot of each IC socket.

4. Determine the jumper requirements to match the module(s) selected. For modules 46 and 47, install jumpers 9A, 10A, 11A, 12A, and 13 as 1, 1, 1, 0, and 1, respectively. (See figure 1-1.)

Table 1-1. ROM Locations for Block A

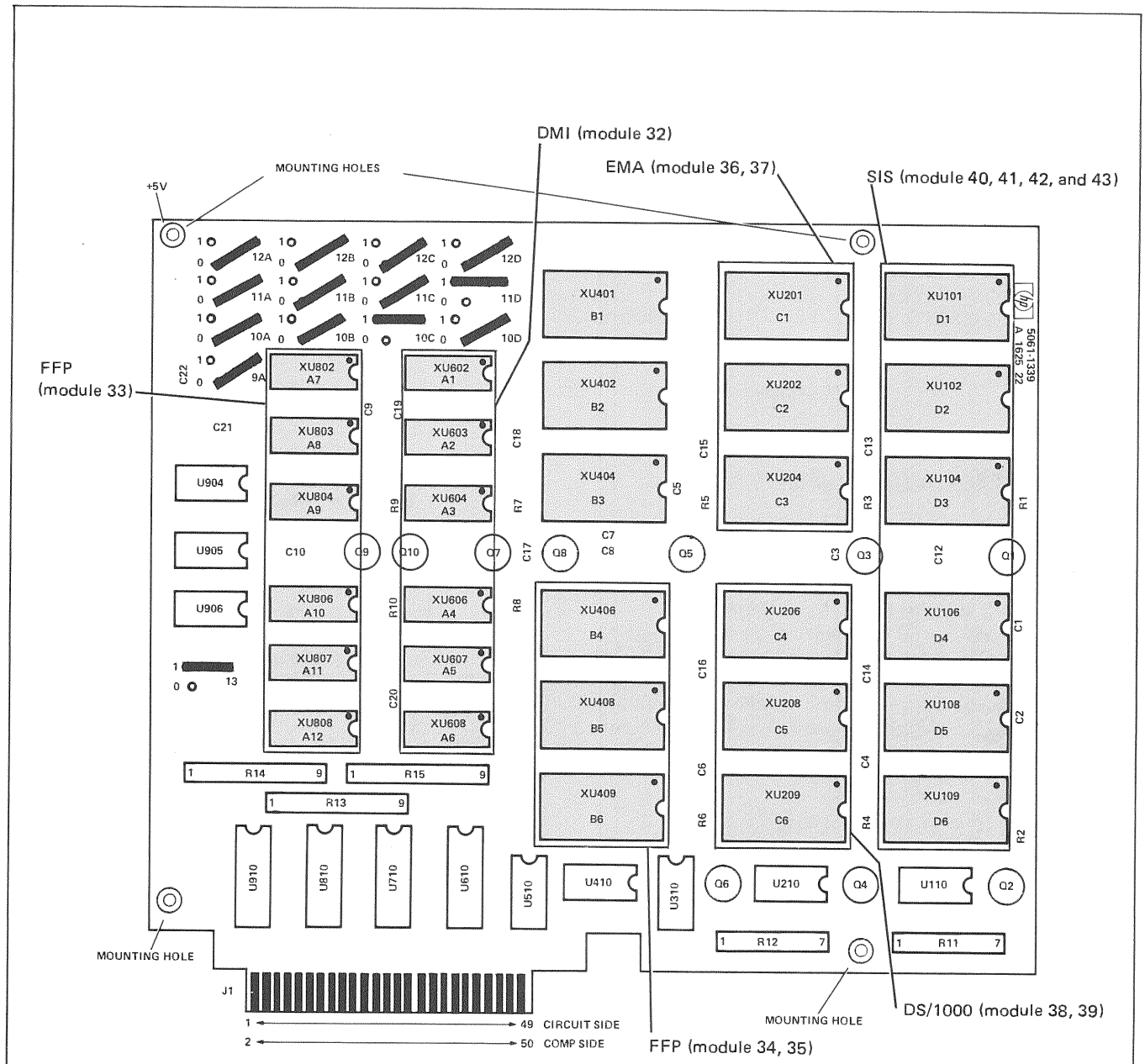
4-BIT SET	ROM PACKAGE LOCATION	
	LEAST SIGNIFICANT MODULE (LSM)	MOST SIGNIFICANT MODULE (MSM)
23-20 MSB	A6 (XU608)	A12 (XU808)
19-16	A5 (XU607)	A11 (XU807)
15-12	A4 (XU606)	A10 (XU806)
11-8	A3 (XU604)	A9 (XU804)
7-4	A2 (XU603)	A8 (XU803)
3-0 LSB	A1 (XU602)	A7 (XU802)

Notes:
1. Locations A1-A6 are selected first (the lower 1/4K configuration).
2. Locations A7-A12 are selected last (the upper 1/4K configuration).
3. See figure 1-2 for ROM locations.

Table 1-2. ROM Locations for Blocks B, C, and D

8-BIT SET	ROM PACKAGE LOCATION	
	LEAST SIGNIFICANT MODULE PAIR (LSMP)	MOST SIGNIFICANT MODULE PAIR (MSMP)
23-16 MSB	B3 (XU404) C3 (XU204) D3 (XU104)	B6 (XU409) C6 (XU209) D6 (XU109)
15-8	B2 (XU402) C2 (XU202) D2 (XU102)	B5 (XU408) C5 (XU208) D5 (XU108)
7-0 LSB	B1 (XU401) C1 (XU201) D1 (XU101)	B4 (XU406) C4 (XU206) D4 (XU106)

Notes:
1. Locations suffixed 1, 2, and 3 are selected first (the lower 1/2K configuration).
2. Locations suffixed 4, 5, and 6 are selected last (the upper 1/2K configuration).
3. See figure 1-2 for ROM locations.



NOTES:
1. SHADED AREA SHOWS ROM IC SOCKET LOCATIONS.
2. SEE TABLES 1 AND 2 FOR DESIGNATED ROM LOCATIONS.
3. JUMPERS 9A, 10A, 11A, 12A, AND 13 SHOWN CONFIGURED FOR BLOCK A MODULES 32 AND 33. JUMPERS 10B, 11B, 12B, AND 13 SHOWN CONFIGURED FOR BLOCK B MODULES 32, 33, 34, AND 35 (DMI AND FFP).
4. JUMPERS 10C, 11C, 12C, AND 13 SHOWN CONFIGURED FOR BLOCK C MODULES 36, 37, 38, AND 39 (EMA AND DS/1000). JUMPERS 10D, 11D, 12D, AND 13 SHOWN CONFIGURED FOR BLOCK D MODULES 40, 41, 42, AND 43 (SIS).
5. SEE FIGURES 1 AND 2 FOR OTHER JUMPER CONFIGURATIONS.

Figure 1-2. Firmware Accessory Board

c. For block B, C, or D configuration, use table 1-2 and figure 1-1 for ROM location and jumper configuration requirements, respectively. Use the following example as a guide:

   1. Assuming the microprogram operates between 34000_8 and 35777_8, figure 1 shows that modules 56, 57, 58, and 59 are required.

   2. Determine if the microprogram operates in the least significant module pair (LSMP) or the most significant module pair (MSMP). Modules 56 and 57 are the LSMP and modules 58 and 59 are the MSMP.

   3. If part of the microprogram operates in the LSMP (34000_8 to 34777_8), install the corresponding three 4K ROM IC's in sockets B1 through B3. (Refer to table 1-2 and figure 1-2.) If part of the microprogram operates in the MSMP (35000_8 to 35777_8), install the corresponding three 4K ROM IC's in sockets B4 through B6. Although blocks B, C, or D may be used, it is recommended that block B be used first, block C second, and block D last. Ensure that the IC's are oriented correctly as shown in figure 1-2 by matching pin 1 of each IC with the white dot of each IC socket.

   4. Determine the jumper requirements to match the modules selected. For modules 56 through 59, install jumpers 10B, 11B, 12B, and 13 as 0, 1, 1, and 1, respectively. (See figures 1-1 and 1-2.)

WARNING

Hazardous voltages are present inside the computer mainframe! Before installing the FAB, set the ~LINE and BATTERY switches to OFF and DISCONNECT THE POWER CORD!

d. Set ~LINE and BATTERY switches to OFF and disconnect the power cord.

e. Disconnect I/O extender cable assembly (if present) from CPU PCA edge connector.

f. Loosen screw located in rear fold of bottom cover; slide cover toward rear and remove.

g. Position FAB assembly over the CPU PCA standoffs and fasten it securely with the four screws and lockwashers. (See figure 1-3.) Note that the FAB assembly obtains its dc power from the CPU PCA standoffs.

h. Connect FAB connector assembly between FAB assembly connector J1 and CPU PCA connector J2.

i. Replace bottom cover.

j. Connect I/O extender cable assembly (if present) to CPU PCA connector J3.

k. Connect power cord to the computer and set ~LINE and BATTERY switches to ON.

l. Check that the +5V CPU voltage, when measured at the crossover board test point is 5.15 Volts. Adjust if necessary. The adjustment procedure is located in the appropriate Installation and Service Manual.

Installation is now complete and ready for the user's control store microprogramming application.

REMOVAL PROCEDURE

a. Set ~LINE and BATTERY switches to OFF and disconnect the power cord.

b. Disconnect I/O extender cable assembly (if present) from CPU PCA edge connector.

c. Loosen screw located in rear fold of bottom cover; slide cover toward rear and remove.

d. Remove FAB ribbon connector assembly between FAB assembly connector J1 and CPU PCA connector J2.

e. Remove the four screws and lockwashers (see figure 1-3) which fasten the FAB to the CPU standoffs.

Removal is now complete, refer to the previous section for configuration and installation procedures.

1-4. SERVICE INFORMATION

Because of its design, the FAB assembly is field replaceable as an assembly. However, a system failure can be isolated to the FAB-ROM combination by running the appropriate self test and/or diagnostic corresponding to the firmware that is installed on the FAB.

a. If Scientific Instruction Set (SIS), Extended Memory Area (EMA), Dynamic Mapping Instructions (DMS), Fast Fortran Processor (FFP), or Distributed System Firmware (DS/1000) is installed on the FAB, run the associated selftest and/or diagnostic. Self tests are described in the appropriate section of this manual. For diagnostic operation, the appropriate diagnostic manual must be consulted.

b. If a particular test fails, verify that the address jumpers on the FAB are configured correctly. Ensure that the ribbon cable is correctly seated.

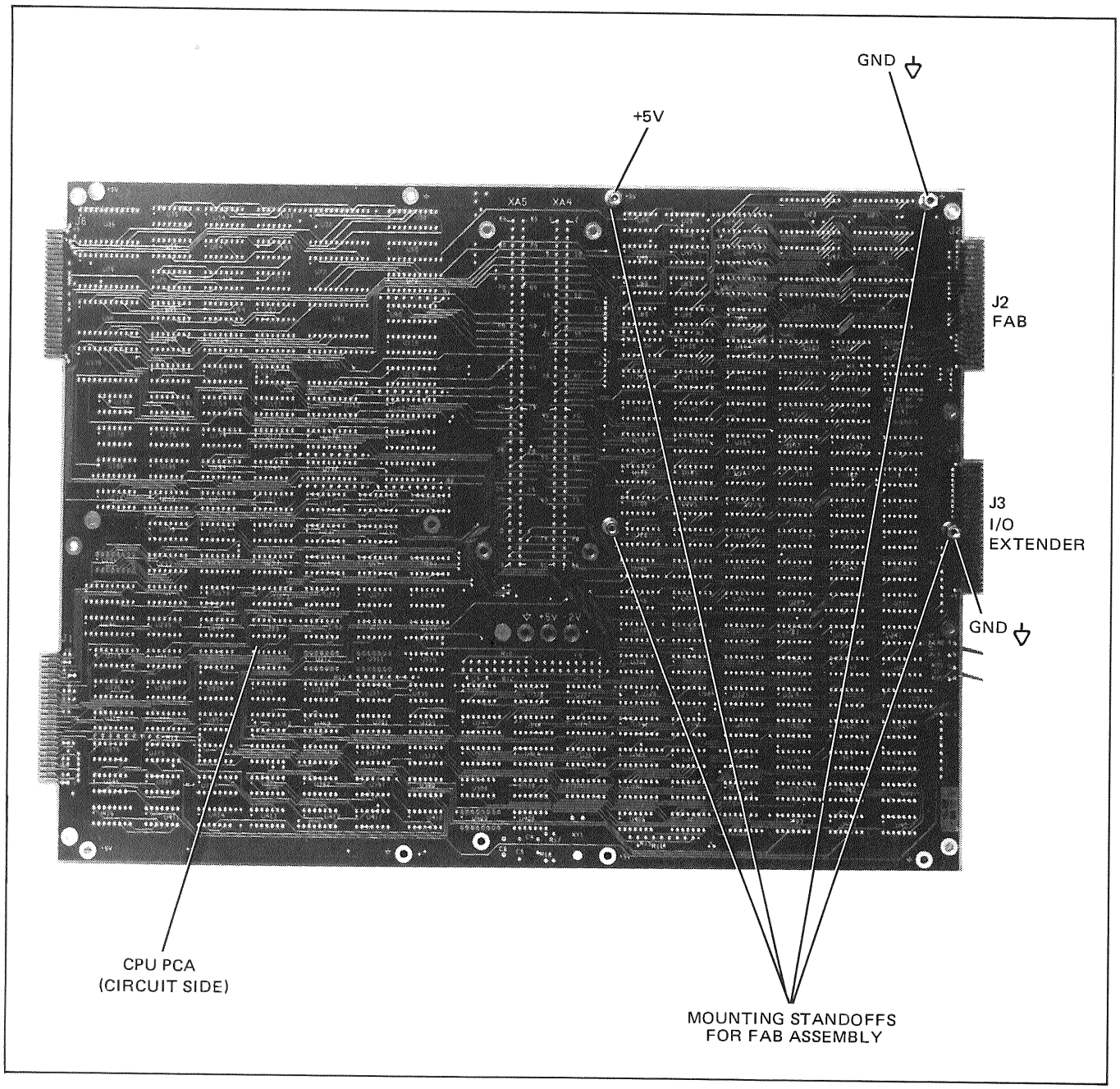


Figure 1-3. Firmware Accessory Board Mounting Details

c. Verify that the +5V CPU voltage is set at the recommended setting of 5.15 volts when measured at the crossover PCA test point. Refer to the appropriate installation and service manual for the power supply voltage adjustment.

d. If the test still fails, insert a known good set of ROMs in the failing locations and re-run the diagnostic and/or self test.

e. If the test now passes, defective ROMs are indicated. Change one ROM at a time to isolate the defective ROM(s).

If after installing a new FAB, the test still fails, install a new ribbon cable assembly and run the tests again.

If the test still fails, a defective FAB or ribbon cable assembly is indicated. Install a new FAB and run the tests.

f. If a failure still exists, contact your nearest Hewlett-Packard Sales and Service Office. A list of HP Sales and Service Offices is provided in the appropriate HP 1000 Series Computer Installation and Service Manual.

HP 12791A FIRMWARE EXPANSION MODULE

SECTION II

2-1. INTRODUCTION

This section provides installation and service information for the HP 12791A Firmware Expansion Module (FEM) which is an accessory for HP 1000 M/E/F-Series Computers. Installation and reference information for the various HP firmware options which can be installed on the FEM can be found in the appropriate section of this manual. Additional information is provided in the manuals listed in the Preface.

NOTE

Terminology may differ somewhat between the M-Series and E/F-Series computers. The E/F-Series terminology will be used, but the M-Series user should note that the following are synonomous.

E/F-Series	M-Series
Control Memory	Control Store
Control Memory Address Register (CMAR)	ROM Address Register (RAR)
Microinstruction Register (MIR)	ROM Instruction Register (RIR)

2-2. DESCRIPTION

The 16,384 words of addressable Control Memory in the HP 1000 E/F-Series computers are divided into sixty-four 256 word modules (0 through 63). The 4,196 words of addressable Control Memory in the HP 1000 M-Series computer are divided into sixteen 256 word modules (0 through 15). See the appropriate figure, 11-1, 11-2, or 11-3 in section XI for the allocation of Control Memory. The modules which hold the computer base instruction set are not available to the user microprogrammer (modules 0,1,14,15 in M-Series and modules 0,1,2,3 in E/F-Series computers). Any other Control Memory modules not filled by microprogrammed Hewlett-Packard options are available to the user microprogrammer. It is recommended that the user microprogrammer only use modules which are not HP reserved, or specified for HP microprogrammed options. If the user microprogrammer uses modules which are specified for HP firmware options or HP reserved, he will not be able to use present or future HP microprogrammed options which reside in those Control Memory modules.

The HP 12791A Firmware Expansion Module (FEM) contains 24 integrated-circuit (IC) sockets which are divided into eight sets of three sockets each (see figure 2-1). Each set of three 24 pin sockets can accommodate 4k (512 × 8) or 8k (1024 × 8) read-only-memory (ROM) ICs. Since each set is individually addressable, up to eight discrete sections (or blocks) of Control Memory can be installed on the FEM. Each set of sockets has a corresponding 10 rocker switch DIP pack which is configured to enable or disable the set, specify the size of ROMs used, and specify the Control Memory modules which will be addressed by these sockets (see table 2-1 for switch configuration settings).

BLOCK ADDRESSING

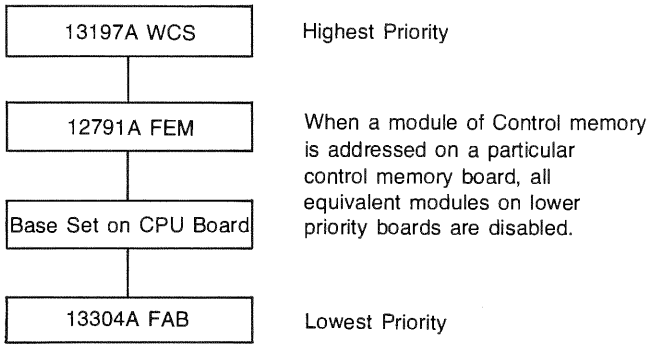
The eight sets of three 24-pin sockets are identified as SETA, SETB, SETC, SETD, SETE, SETF, SETG, and SETH. Within each set, the sockets are designated as sockets 1, 2, or 3 (e.g. A1, A2, and A3). Socket A1 contains the least significant bits (bits 0-7) of the microinstruction, socket A2 contains bits 8-15, and socket A3 contains the most significant bits (bits 16-23). The corresponding 10 rocker switch DIP packs are identified as SWA, SWB, SWC, SWD, SWE, SWF, SWG, and SWH.

If 4k ROMs (512 word by 8 bit) are used in a set, the set contains 512 words (two contiguous modules) of Control Memory. The two contiguous modules begin on an even module number (e.g., 36 and 37, or 52 and 53). If 8k ROMs (1024 word by 8 bit) are used in a set, the set contains 1024 words (four contiguous modules) of Control Memory. The four contiguous modules begin on a module number which is an even multiple of 4 (e.g., 24 through 27, or 48 through 51). Both 4k and 8k ROMs can be used on the FEM at the same time, since each set of 3 sockets can be individually configured for ROM size. Switch settings and part locations are shown in table 2-1 and figure 2-1 respectively.

PRIORITY

Control Memory modules installed on the FEM assembly have lower priority than the 13197A Writable Control Store (WCS) but higher priority than the base instruction set located on the CPU PCA or the FAB board.

In an E/F-Series Computer the priority is as follows:



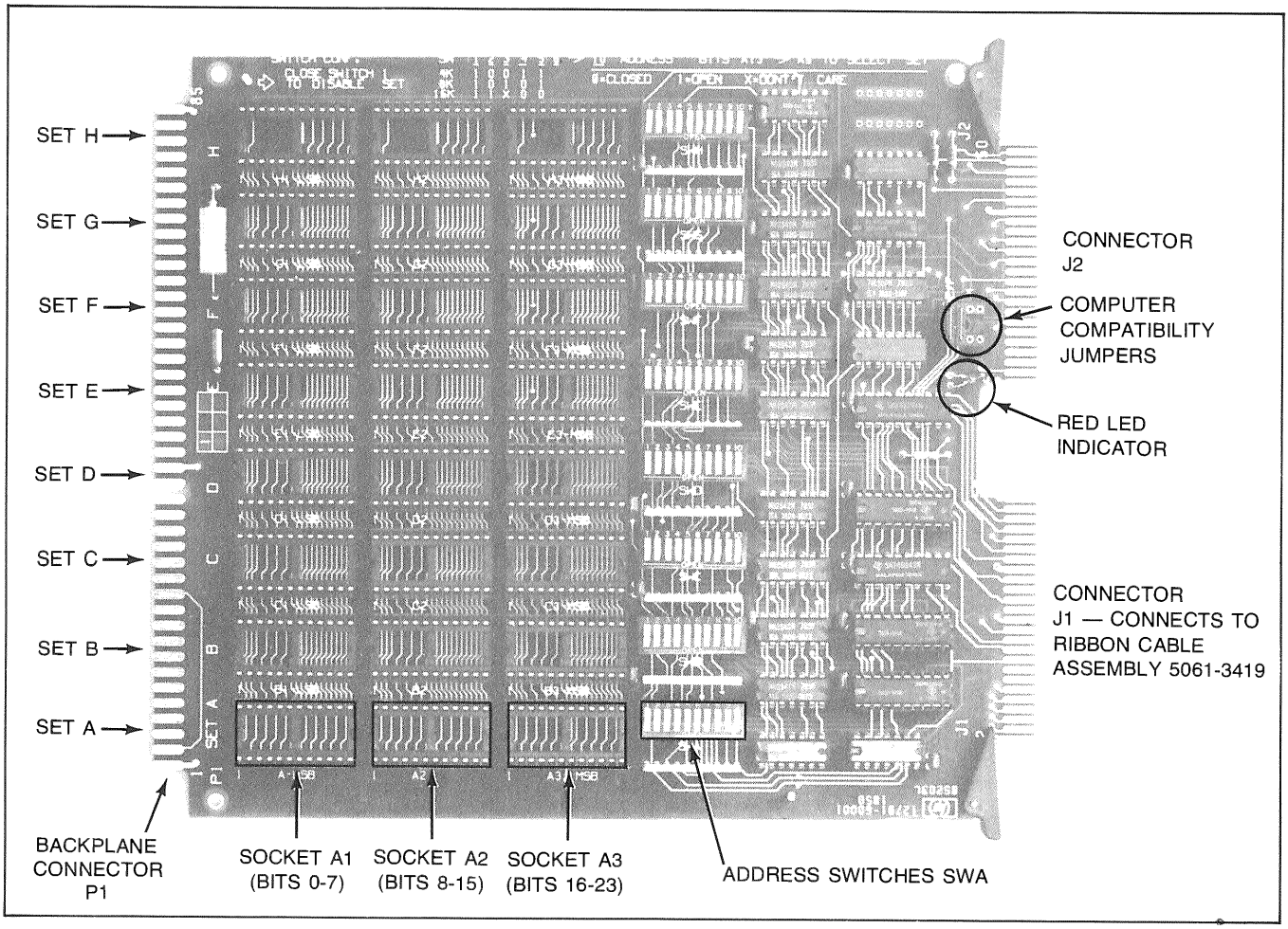
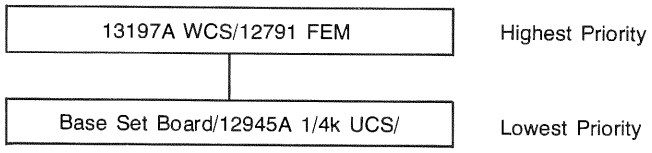


Figure 2-1. Firmware Expansion Module

In a M-Series Computer the priority is as follows:



PRODUCT CONTENTS

The HP 12791A Firmware Expansion Module Product consists of the following:

Description	HP Part No.	Quantity
Firmware Expansion Module Assembly	12791-60001	1
Ribbon Cable Assembly	5061-3419	1
HP 1000 M/E/F-Series Firmware Installation and Reference Manual	12791-90001	1

RECOMMENDED PROMs

The following are the recommended PROMs for use with the FEM.

4k PROMs		8k PROMs	
HP Part No.	1816-1163	HP Part No.	1816-1160
Signetics	N82S141F	Signetics	N82S181F
Harris	7641	Harris	7681
Monolithic Memories	6341	Monolithic Memories	6381

2-3. INSTALLATION/REMOVAL

POWER REQUIREMENTS

The +5V power required by the Firmware Expansion Module is obtained from the processor I/O backplane. An unloaded FEM (no ROMs installed) sinks 1.20 amperes of +5V I/O current. Each set of three ROMs installed on the

FEM sinks an additional .525 amperes of current, regardless if the ROMs are 4k or 8k ROMs. Therefore, a fully loaded FEM will sink 5.4 amperes. Calculate the total current required by the FEM and all other printed-circuit assemblies (PCA's) resident in the processor I/O cage. If the total current requirement is greater than the +5V I/O supply capability, then one or more interface PCA's must be removed and installed in a HP 12979A/B I/O Extender.

NOTE

The processor I/O current availability is given in the appropriate HP 1000 Operating and Reference Manual.

INSTALLATION PROCEDURE

Figure 2-1 identifies each set of sockets and the associated address switches. Control Memory allocation is contained in tables 11-1, 11-2, and 11-3 in section XI. Refer to the appropriate table to determine the starting address of the Control Memory modules which are to be installed on the FEM. Table 2-1 contains the switch settings which determine the Control Memory modules that will be addressed by the set of sockets.

To install the FEM, proceed as follows:

CAUTION

ROM IC's may be permanently damaged if oriented incorrectly when installed and power is applied.

a. If the firmware is HP supplied optional firmware, see the appropriate table in section XI to determine the module number and starting address of the firmware. If user written firmware is to be installed, the microcode should occupy Control Memory modules which are specified for user microprogramming.

b. On the FEM, load the three ROM IC's corresponding to the Control Memory modules to be installed into one of the eight sets of sockets. Ensure that the ROM IC's are oriented with the notched ends facing the same direction as the other IC's on the board (towards backplane connector P1). The ROM containing the least significant bits (bits 0-7) of the microinstruction is to be installed in socket 1, the ROM containing bits 8-15 is to be installed in socket 2, and the ROM containing the most significant bits (bits 16-23) is to be installed in socket 3.

c. Set the associated address switches for the appropriate modules of Control Memory as specified in table 2-1.

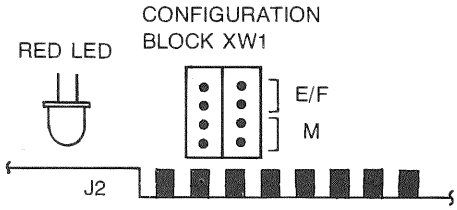
d. Repeat steps a, b, and c for each section of Control Memory which is to be installed.

e. All unused socket sets must be disabled by setting switch S1 of the unused sets to the closed position.

WARNING

Hazardous voltages are present inside the processor mainframe! Before installing the FEM, set the AC LINE AND BATTERY switches to OFF and DISCONNECT THE POWER CORD!

f. Set the computer compatibility jumpers on the FEM as shown below. The jumpers should be in the appropriate sockets to correspond to the type of computer with which the FEM is to be used.



g. Set the AC LINE and BATTERY switches to OFF and disconnect the power cord.

h. Disconnect battery cable (if present) from BAT. INPUT connector and remove I/O PCA cage cover.

i. Disconnect I/O extender cable assembly (if present) from the CPU PCA edge connector J3.

j. Loosen screw located in rear fold of bottom cover; slide cover toward rear and remove.

k. Remove existing connector assembly from CPU PCA and FAB (E/F-Series), or CPU PCA and ROM PCA (M-Series), if installed. See figure 2-2.

l. Pass the ribbon cable assembly (part no. 5061-3419) through the opening in chassis below I/O PCA cage cover.

NOTE

The ribbon cable assembly (part no. 5061-3419) supplied with the FEM must be used for reliable operation. Use of any other ribbon cable assembly may result in intermittent or unpredictable errors.

m. Connect the ribbon cable assembly (part no. 5061-3419) to FAB and CPU PCA in a E/F-Series computer, (ROM PCA and CPU PCA in a M-Series computer).

n. Replace bottom cover. Reconnect I/O extender cable assembly (if present) to CPU edge connector J3.

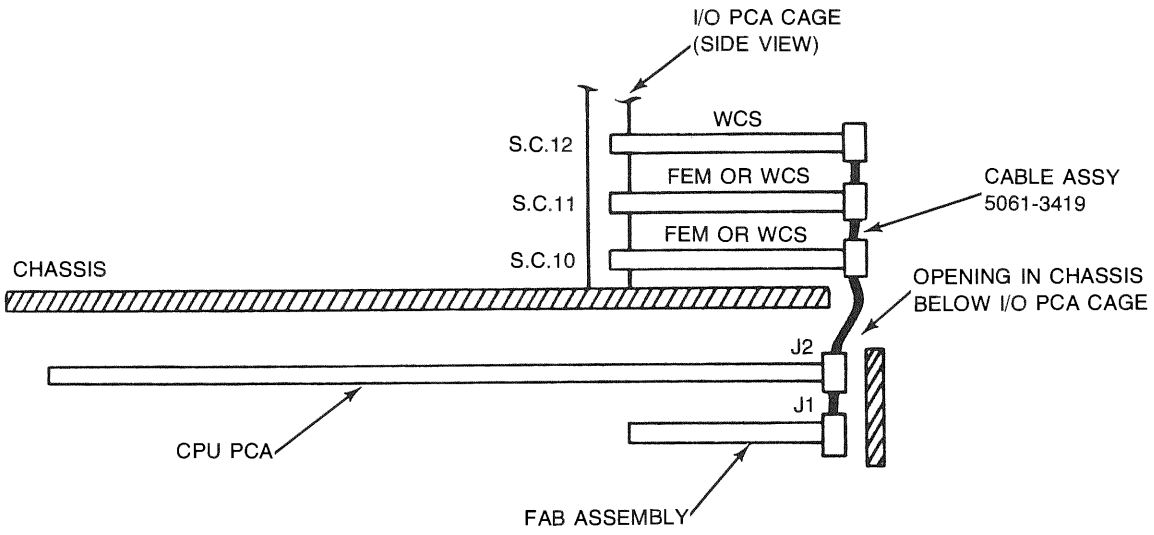
o. Install the FEM in I/O PCA cage slot 10 or 11 depending on whether or not a 13197A Writable Control Store Board (WCS) is present. If no WCS is present, install the FEM in slot 10. If one WCS is present install the FEM in slot 11.

Table 2-1. FEM Address Switch Settings

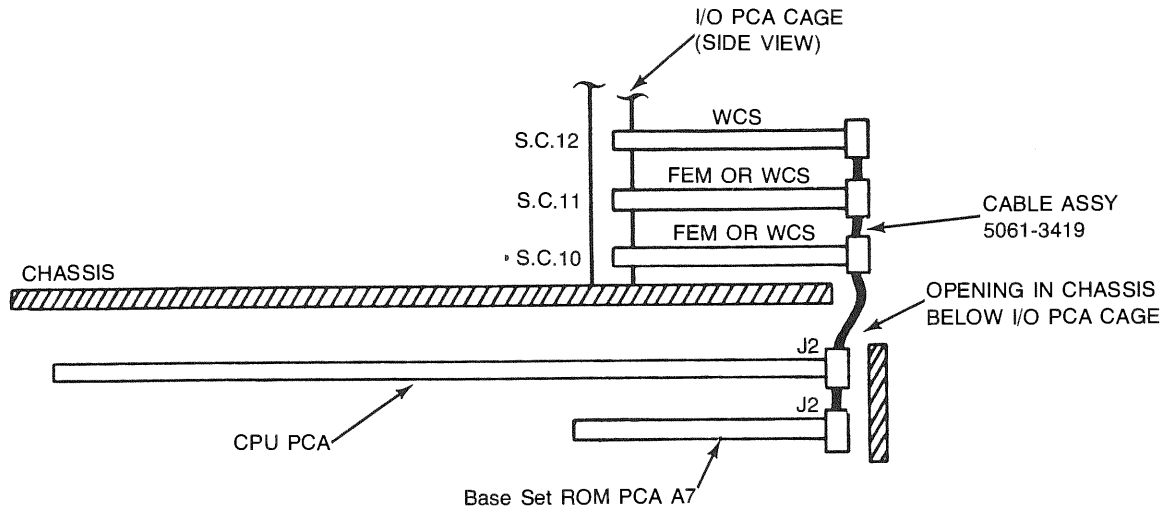
MODULE NO.	ADDRESSES		4K ROMS										8K ROMS									
			SWITCHES										SWITCHES									
	DECIMAL	OCTAL	S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S1	S2	S3	S4	S5	S6	S7	S8	S9	S10
0	0-00255	00000-00377	1	0	0	1	1	0	0	0	0	0	1	0	1	0	1	0	0	0	0	X
1	00256-00511	00400-00777																				
2	00512-00767	01000-01377	1	0	0	1	1	0	0	0	0	1										
3	00768-01023	01400-01777																				
4	01024-01279	02000-02377	1	0	0	1	1	0	0	0	1	0	1	0	1	0	1	0	0	0	1	X
5	01280-01535	02400-02777																				
6	01536-01761	03000-03377	1	0	0	1	1	0	0	0	1	1										
7	01762-02047	03400-03777																				
8	02048-02303	04000-04377	1	0	0	1	1	0	0	1	0	0	1	0	1	0	1	0	0	1	0	X
9	02304-02559	04400-04777																				
10	02560-02815	05000-05377	1	0	0	1	1	0	0	1	0	1										
11	02816-03071	05400-05777																				
12	03072-03327	06000-06377	1	0	0	1	1	0	0	1	1	0	1	0	1	0	1	0	0	1	1	X
13	03328-03583	06400-06777																				
14	03584-03849	07000-07377	1	0	0	1	1	0	0	1	1	1										
15	03850-04095	07400-07777																				
16	04096-04351	10000-10377	1	0	0	1	1	0	1	0	0	0	1	0	1	0	1	0	1	0	0	X
17	04352-04607	10400-10777																				
18	04608-04863	11000-11377	1	0	0	1	1	0	1	0	0	1										
19	04864-05119	11400-11777																				
20	05120-05375	12000-12377	1	0	0	1	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	X
21	05376-05631	12400-12777																				
22	05632-05887	13000-13377	1	0	0	1	1	0	1	0	1	1										
23	05888-06143	13400-13777																				
24	06144-06399	14000-14377	1	0	0	1	1	0	1	1	0	0	1	0	1	0	1	0	1	1	0	X
25	06400-06655	14400-14777																				
26	06656-06911	15000-15377	1	0	0	1	1	0	1	1	0	1										
27	06912-07167	15400-15777																				
28	07168-07423	16000-16377	1	0	0	1	1	0	1	1	1	0	1	0	1	0	1	0	1	1	1	X
29	07424-07679	16400-16777																				
30	07680-07935	17000-17377	1	0	0	1	1	0	1	1	1	1										
31	07936-08191	17400-17777																				
32	08192-08447	20000-20377	1	0	0	1	1	1	0	0	0	0	1	0	1	0	1	1	0	0	0	X
33	08448-08703	20400-20777																				
34	08704-08959	21000-21377	1	0	0	1	1	1	0	0	0	1										
35	08960-09215	21400-21777																				
36	09216-09571	22000-22377	1	0	0	1	1	1	0	0	1	0	1	0	1	0	1	1	0	0	1	X
37	09572-09727	22400-22777																				
38	09728-09983	23000-23377	1	0	0	1	1	1	0	0	1	1										
39	09984-10239	23400-23777																				
40	10240-10495	24000-24377	1	0	0	1	1	1	0	1	0	0	1	0	1	0	1	1	0	1	0	X
41	10496-10751	24400-24777																				
42	10752-10917	25000-25377	1	0	0	1	1	1	0	1	0	1										
43	10918-11263	25400-25777																				
44	11264-11519	26000-26377	1	0	0	1	1	1	0	1	1	0	1	0	1	0	1	1	0	1	1	X
45	11520-11775	26400-26777																				
46	11776-12031	27000-27377	1	0	0	1	1	1	0	1	1	1										
47	12032-12287	27400-27777																				
48	12288-12543	30000-30377	1	0	0	1	1	1	1	0	0	0	1	0	1	0	1	1	1	0	0	X
49	12544-12799	30400-30777																				
50	12800-13055	31000-31377	1	0	0	1	1	1	1	0	0	1										
51	13056-13311	31400-31777																				
52	13312-13557	32000-32377	1	0	0	1	1	1	1	0	1	0	1	0	1	0	1	1	1	0	1	X
53	13558-13823	32400-32777																				
54	13824-14079	33000-33377	1	0	0	1	1	1	1	0	1	1										
55	14080-14335	33400-33777																				
56	14336-14591	34000-34377	1	0	0	1	1	1	1	1	0	0	1	0	1	0	1	1	1	1	0	X
57	14592-14847	34400-34777																				
58	14848-15103	35000-35377	1	0	0	1	1	1	1	1	0	1										
59	15104-15359	35400-35777																				
60	15360-15615	36000-36377	1	0	0	1	1	1	1	1	1	0	1	0	1	0	1	1	1	1	1	X
61	15616-15871	36400-36777																				
62	15872-16127	37000-37377	1	0	0	1	1	1	1	1	1	1										
63	16128-16383	37400-37777																				

1. 0 = CLOSED 1 = OPEN X = DON'T CARE
   "CLOSED" AND "OPEN" REFER TO THE SETTINGS ON THE DIP ROCKER SWITCHES.

2. ALL UNUSED SETS MUST BE DISABLED BY SETTING S1 CLOSED.



a. Installation Details (HP 1000 E/F-Series Computer)



NOTES:

FEM → 12791A FIRMWARE EXPANSION MODULE
FAB → 13304A FIRMWARE ACCESSORY BOARD
WCS → 13197A WRITABLE CONTROL STORE

b. Installation Details (HP 1000 M-Series Computer)

Figure 2-2. Installation Details

p. Connect the cable assembly to FEM board connector J1 and to WCS PCA(s) if present. Any unused connectors should be left on if they do not interfere with the I/O PCA cage cover or I/O cable hoods directly above the FEM. If it is necessary, unused connectors can be carefully removed with a sharp knife or scissors. After removal, inspect the ribbon cable to verify that there are no shorts between any ribbon cable conductors.

q. Replace I/O PCA cage cover and reconnect battery cable (if present) to BAT. INPUT connector.

r. Plug processor power cord into power mains receptacle and set AC LINE to ON, and BATTERY switch to INT., if the power fail option is installed. If the battery is discharged upon turning on the AC LINE, it will take a few minutes for the battery to charge up to a minimum level before the processor will begin operation.

The installation is now complete and ready for use of HP optional firmware, or the user's own microprogramming application.

REMOVAL PROCEDURE

a. Set AC LINE and BATTERY switches to OFF and disconnect the power cord.

b. Disconnect battery cable (if present) from BAT. INPUT connector and remove I/O PCA cage cover.

c. Remove ribbon cable connector from FEM board connector J1, and remove FEM from I/O slot.

The removal is now complete, and additional HP optional or user written firmware can be installed as described in the installation procedure.

VERIFICATION

If HP supplied optional firmware is installed of the FEM, correct operation can be verified by running the appropriate self test and/or diagnostic on the installed firmware.

2-4. SERVICE INFORMATION

A system failure can be isolated to the FEM-ROM combination by running the appropriate self test and/or diagnostic corresponding to the firmware that is installed on the FEM.

The red LED indicator on the FEM is lit whenever a set of ROMs on the board is being addressed (i.e. the address sent to the board corresponds to the switch settings on one of the enabled sets).

If the base set is installed on the FEM, the LED will appear to be continuously lit when the computer is in the halt mode.

a. If Scientific Instruction Set (SIS), Extended Memory Area (EMA), Vector Instruction Set (VIS), or Distributed System Firmware (DS/1000) is installed on the FEM, run the associated self test and/or diagnostic. Self tests are described in the appropriate section of this manual. For diagnostic operation, the appropriate diagnostic manual must be consulted.

b. If a particular test fails, verify that the address switches on the FEM are configured correctly. All unused sets of sockets must be disabled by setting switch 1 to the closed position. Ensure that the ribbon cable and FEM are correctly seated.

c. Verify that the +5V CPU voltage is set at the recommended setting of 5.15 volts when measured at the crossover PCA test point. Refer to the appropriate installation and service manual for the power supply voltage adjustment.

d. If the test still fails, insert a known good set of ROMs in the failing locations and re-run the diagnostic and/or self test.

e. If the test now passes, defective ROMs are indicated. Change one ROM at a time to isolate the defective ROM(s).

   If the test still fails, defective FEM or ribbon cable assembly is indicated. Install a new FEM and run the tests.

   If after installing a new FEM, the test still fails, install a new ribbon cable assembly and run the tests again.

f. If a failure still exists, contact your nearest Hewlett-Packard Sales and Service Office. A list of HP Sales and Service Offices is provided in the appropriate HP 1000 Series Computer Installation and Service Manual.

HP 13197A WRITABLE CONTROL STORE

SECTION III

3-1. INTRODUCTION

This section describes the HP 13197A Writable Control Store (WCS) Kit used with the HP 1000 M-Series (2105/2108/2112), E-Series (2109/2113), and F-Series (2111/2117) computers. This section covers general information, installation, programming, and general theory of operation. It is written for the individual who already has experience as an Assembly language programmer. Additional information is provided in the following manuals.

a. Manuals listed in the Preface of this manual.

b. *RTE Driver DVR36 for HP 12978/13197A Writable Control Store Board Programming and Reference Manual,* part no. 13197-90001.

The HP 13197A Writable Control Store Kit is fully compatible with the HP 1000 M/E/F-Series computers. The Writable Control Store (WCS) holds 1024 words (four control memory modules) and is commonly called a 1K WCS. Computer commands specify which four control memory modules are contained on each HP 13197A WCS printed circuit assembly (PCA).

NOTE

Where installation or operational data for the kit is affected by differences in the HP 1000 M-Series and E/F-Series computers, these differences are noted in text. Also, terminology may differ somewhat between the M-Series and E/F-Series computers. The E/F-Series terminology will be used, but the M-Series user should note the following:

E/F-Series	M-Series
Control Memory	Control Store
Control Memory Address Register (CMAR)	ROM Address Register (RAR)
Microinstruction Register (MIR)	ROM Instruction Register (RIR)

KIT CONTENTS

The HP 13197A WCS Kit consists of the following:

a. Writable Control Store PCA, part no. 13197-60001.

b. Ribbon Cable Assembly, part no. 5061-3419.

c. *HP 1000 M/E/F-Series Firmware Installation and Reference Manual,* part no. 12791-90001.

The printed circuit assembly and ribbon cable assembly contained in the kit are shown in figure 3-1.

SPECIFICATIONS

Table 3-1 lists the characteristics and specifications of the HP 13197A Writable Control Store PCA.

3-2. INSTALLATION/REMOVAL

POWER CONSIDERATIONS

The +5V power required by the WCS is obtained from the computer I/O backplane. Each WCS PCA installed requires 2.2 amperes of current. Calculate the total current required by the WCS PCA and all other printed-circuit assemblies resident in the I/O PCA cage. If the total current requirement is greater than the +5V supply capability, then one or more interface PCA's must be removed and installed in a compatible I/O extender.

NOTE

The I/O current availability is given in the appropriate *HP 1000 Series Computer Operating and Reference Manual.*

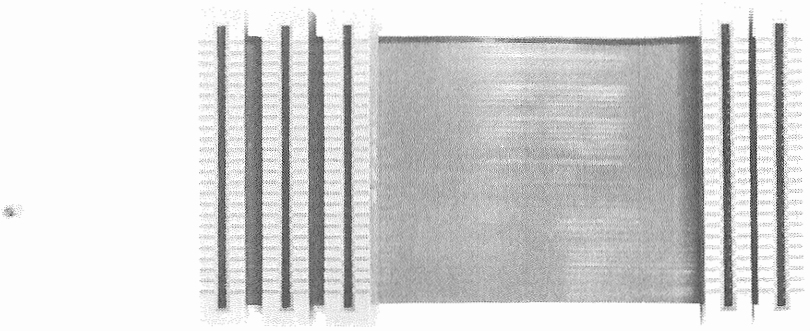
INSTALLATION PROCEDURE

The Base Set ROM PCA occupies position A7 in the HP 1000 M-Series computer as standard equipment. In the HP 1000 E/F-Series computer, position A7 is occupied by the Firmware Accessory Board (FAB). For installation of WCS in the E/F-Series, see figure 2-2a. For installation in the M-Series, see figure 2-2b.

Install the Writable Control Store kit as follows:

a. Ensure that the computer operates properly prior to installing the writable control store kit.

b. If WCS is to be installed in an M-Series computer, remove computer compatibility jumper W1 (see figure 3-2). If WCS is to be installed in an E/F-Series computer, jumper W1 remains installed.



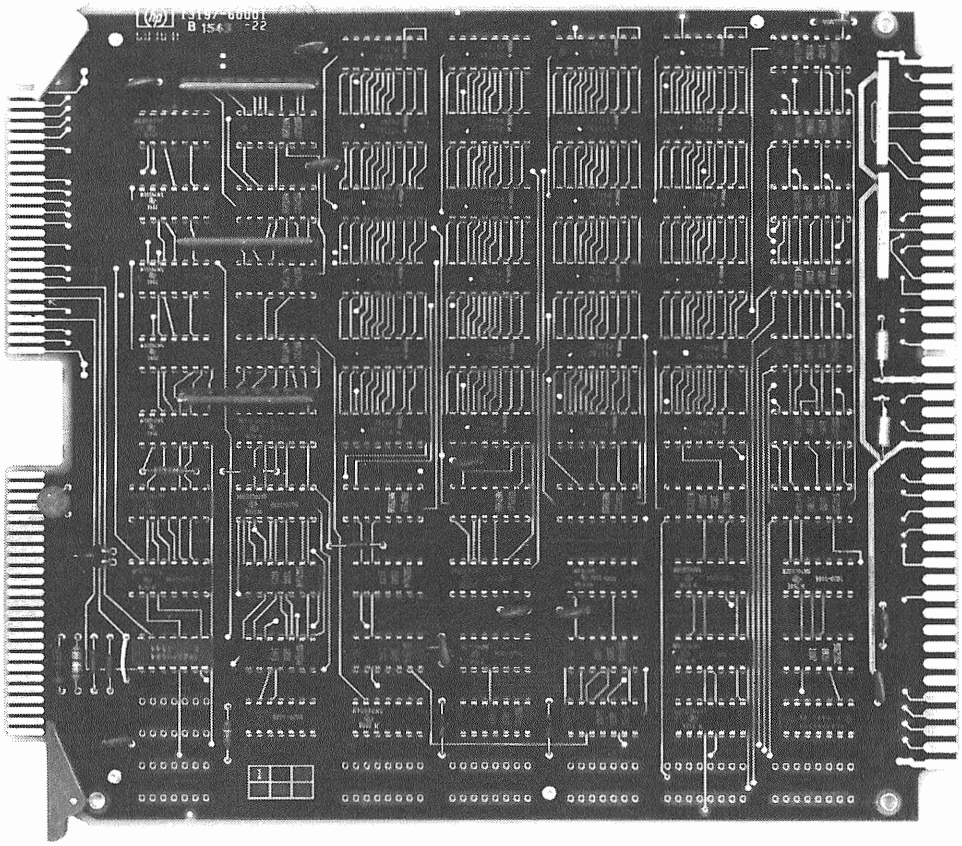


Figure 3-1. HP 13197A Writable Control Store Kit

WARNING

Hazardous voltages are present inside the processor mainframe! Before installing the writable control store board, set the ~LINE and BATTERY switches to off and DISCONNECT THE POWER CORD!!

c. Set ~LINE and BATTERY switches to OFF and disconnect the power cord.

d. Disconnect I/O extender cable assembly (if present) from CPU PCA edge connector J3.

e. Loosen screw located in rear fold of bottom cover; slide cover toward rear and remove.

f. Remove existing connector assembly from CPU PCA and FAB in an E/F-Series, (CPU PCA and ROM PCA in a M-Series Computer), if installed (See figure 2-2).

g. Disconnect battery cable (if present) from BAT. INPUT connector and remove I/O PCA cage cover.

h. Pass the flat cable assembly (part no. 5061-3419) through opening in chassis below I/O PCA cage.

i. Connect cable assembly to FAB and CPU PCA in a E/F-Series computer, (ROM PCA and CPU PCA in a M-Series Computer).

j. Replace processor bottom cover. Reconnect I/O extender cable assembly (if present) to CPU PCA edge connector J3.

k. Place the first writable control store PCA in slot number 10 (select code 10) of the I/O section of the computer. Any additional writable control store PCA's should be placed first in slot 11 then in slot 12.

l. Install the connectors of the flat cable assembly to WCS board connector J1 as shown in figure 2-2.

NOTE

If an I/O PCA that requires a cable (hood) connector on the back is installed immediately above the WCS, double the flat cable assembly back or cut it to make room for the I/O cable connector. The cable may be carefully cut with scissors or a sharp knife. If cut, inspect the cable conductors for possible shorts.

m. Replace I/O PCA cage cover and reconnect battery cable (if present) to BAT.INPUT connector.

n. Plug processor power cord into power mains receptacle and set ~LINE to ON, and BATTERY switch in INT. if the power fail option is installed.

REMOVAL PROCEDURE

a. Set ~LINE and BATTERY switches to OFF and disconnect the power cord.

b. Remove the connectors of the flat cable assembly from WCS board edge connector J1 and any other Control Memory boards installed in the I/O card cage.

Table 3-1. HP 13197A Writable Control Store PCA Specifications

CAPACITY

Words Available: 1024 per WCS PCA
Maximum WCS PCS's: two per HP 2105; three per 2108/2109/2111/2112/2113/2117
Word Size: 24 bits

MEMORY SPEED

Access: 132 nsec maximum
Full Microinstruction Cycle:
M-Series: 325 nsec.
E/F-Series: 175 or 280 nsec.

INSTALLATION

Each WCS PCA requires the use of one Input/Output slot (slot 10, 11, or 12).

DATA STORAGE OR READBACK

Input/Output Group instructions or a Dual Channel Port Controller are used to load into or read from the WCS.

WCS CURRENT REQUIREMENTS

+5 volt supply: 2.2A rms
−2 volt supply: 7 mA rms

DIMENSIONS

Width: 7-3/4 inches (196.8 mm)
Height: 8-11/16 inches (220.7 mm)

WEIGHT

Net Weight: 18 oz (511.2 gm) (card and cable only)
Shipping Weight: 4 lb (2.27 kg)

INPUT LEVELS

"1" state: 1.9 volts minimum
"0" state: 1.1 volts maximum

OUTPUT LEVELS

"1" state: 2.4 volts minimum
"0" state: 0.8 volt maximum

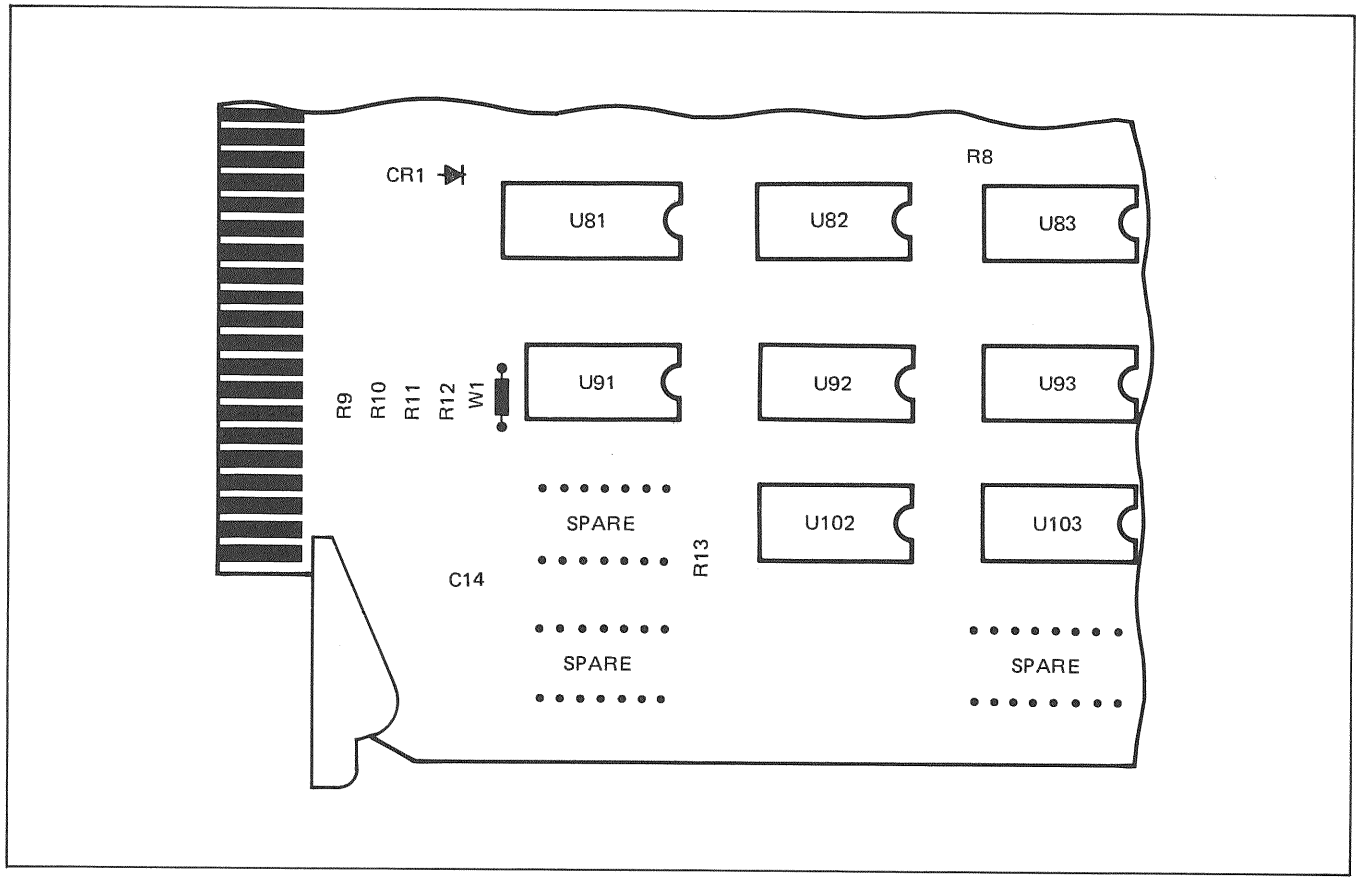


Figure 3-2. Computer Compatibility Jumper W1 Location

c. Remove the WCS board from the I/O card cage.

VERIFICATION. Perform the diagnostic test as outlined in the *WCS Diagnostic Reference Manual,* part no. 13197-90002. If the diagnostic program is completed without error, the PCA is installed and operating properly. If the diagnostic program indicates errors, halt the computer, turn off power, and recheck all of the above installation procedures. Correct where necessary, then recheck and repeat the diagnostic test.

3-3. PROGRAMMING

Standard I/O instructions control the HP 13197A WCS operation. The WCS operates in the following states:

1. Control memory operation enabled.
2. Control memory operation disabled.
3. WCS commands accepted (command state).
4. WCS data (i.e., microinstructions) can be read or written (data state).

The first two states (1 and 2) are called minor states. The second two states (3 and 4) are called major states. One minor state and one major state operate concurrently whenever power is applied to the WCS. Upon initial application of power, control memory operation is disabled (state 2), and WCS commands are accepted (state 3).

Data can be transferred via the Dual Channel Port Controller (DCPC) while in the data state.

ENABLING CONTROL MEMORY OPERATION

To allow microinstructions stored in the WCS to execute, control memory operation must be enabled. Control memory operation is enabled by the execution of a Set Flag instruction to the WCS select code (SC):

```
STF SC
```

When this instruction is executed, the WCS is enabled sometime during T5 of the I/O cycle.

DISABLING CONTROL MEMORY OPERATION

To prevent microinstructions stored in the WCS from executing, control memory operation must be disabled.

This is accomplished by execution of a Clear Flag instruction to the WCS select code (SC):

CLF SC

WCS does not become disabled until sometime during T5 of the I/O cycle.

The operation of the WCS is temporarily disabled when any I/O instruction is executed in the WCS select code. Thus, if the microprocessor is executing microcode contained in the WCS, no I/O instructions (except CLF, as above) may be executed to or from the WCS. This means that no microinstructions stored in a WCS can execute I/O instructions to itself.

NOTE

Since WCS does not return the FLG signal to the I/O backplane, the enable/disable status of the board cannot be determined by executing an SFS instruction.

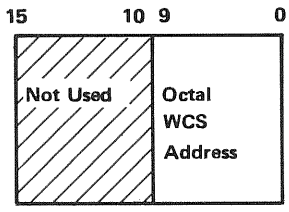
SENDING COMMANDS

When the WCS is in the command state, two commands are accepted, each of which is in the form of a 16-bit word. The first word is interpreted as a WCS address specification. The second word is interpreted as a specification for the four control memory module numbers. WCS interprets words received in the command state as alternately address or module numbers until the data state is initiated. Thus, the third word is interpreted as a WCS address, the fourth as module numbers, etc.

The command state is initiated by execution of a Clear Control Instruction to the WCS select code (SC):

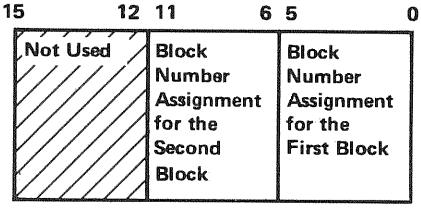
CLC SC

The WCS address word commands the WCS to set the WCS Address Register to the specified address. The WCS Address Register value determines which WCS location is read from or written into when the WCS is in the data state. The format of the WCS address word is the following:



This address is octal and is relative to the first location in the WCS. The first location is at address 0 (zero). The last location is at address 1777.

The four control memory module numbers are assigned by blocks. The 1024 words contained in the WCS are divided into two blocks of 512 words each. Each block is in turn divided into two 256-word modules. WCS addresses 0-511 (0-777 octal) are contained in the first block; addresses 512-1023 (1000-1777 octal) are contained in the second block. The modules assignment word specifies which two control memory modules are stored in each block. The module assignment word has the following format:



Bits 5-0 determine the control memory module numbers assigned to the two modules in the first block. Bits 11-6 determine the module numbers assigned to the two modules in the second block. The number of the first module is given by multiplying the block number by 2. Thus, the module number of a block is always even. For example, if bits 5-0 specify 5 for the block number assignment, the first block serves as control memory for modules 10 and 11.

The two blocks may be assigned block numbers that are not adjoining. For example, the first block can be assigned as block 5 (control memory modules 10 and 11) and the second block can be assigned as block 2 (control memory modules 4 and 5).

Control memory modules available to the user for HP 1000 M/E/F-Series computers are shown in tables 11-1, 11-2 and 11-3, respectively.

READING AND WRITING WCS DATA

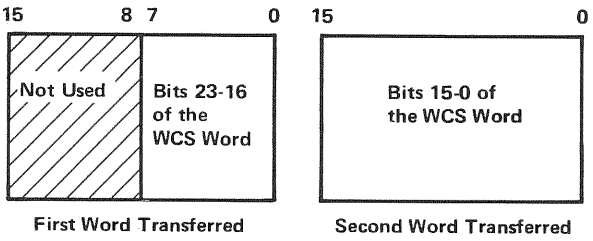
When the WCS is in the data state, data (microinstructions) can be read from and written into the WCS Random Access Memory (RAM) by standard I/O instructions. The address of the location transferred is contained in the WCS Address Register. The WCS Address Register is automatically incremented by one after each pair of input or output instructions.

The data state is initiated by execution of a Set Control instruction to the WCS select code (SC):

STC SC

Two 16-bit words are required to transfer each 24-bit WCS word. Bits 7-0 of the first word transferred hold bits 23-16

of the WCS word. Bits 15-8 of the first word are not used. The second word holds bits 15-0 of the WCS word. The format of the word pair is the following:



Thus, the WCS data requires a main memory buffer of up to 512 words per control memory module (2048 words to transfer the entire WCS contents).

PROGRAMMING EXAMPLES

The following Assembly language programs illustrate how to use the WCS facility.

LOADING WCS FROM MEMORY. The following program disables control memory operation and then loads the WCS with microinstructions stored in main memory.

Note: "SC" indicates the WCS select code.

```
        CLC SC          Puts the WCS in the command
                        state (readies the WCS to ac-
                        cept command).

        LDA ADDR        Places the address of the first
                        WCS location to be loaded in
                        the A-register.

        OTA SC          Sends the beginning WCS ad-
                        dress to the WCS.

        STC SC          Puts the WCS in the data state
                        (readies WCS to accept data).

LOOP1   DLD BUFFP,I     Places first word pair to be
                        sent to WCS in the A- and
                        B-registers.

        ISZ BUFFP       Increments main memory buf-
                        fer pointer to next word pair.

        ISZ BUFFP

        OTA SC          Outputs first word to WCS.

        OTB SC          Outputs second word to WCS.

        ISZ COUNT       Increments negative WCS
                        word count; if 0, skip because
                        load is complete.

        JMP LOOP1       Repeats loop to load two more
                        words.
```

READING WCS INTO MEMORY. The following program reads microinstructions stored in WCS and stores them in main memory.

```
        CLC SC          Puts WCS in command state.

        LDA ADDR        Places address of first WCS lo-
                        cation to be read in the
                        A-register.

        OTA SC          Sends the beginning address
                        to the WCS.

        STC SC          Puts the WCS in the data
                        state.

LOOP2   LIA SC          Reads bits 23-16 of WCS loca-
                        tion into bits 7-0 of the
                        A-register.

        LIB SC          Reads bits 15-0 of WCS loca-
                        tion into bits 15-0 of the
                        B-register.

        DST BUFFP,I     Stores two words (holding con-
                        tents of single WCS location)
                        into main memory buffer.

        ISZ BUFFP       Increments main memory buf-
                        fer pointer to next word pair.

        ISZ BUFFP

        ISZ COUNT       Increments negative WCS
                        word count; if 0, skip because
                        read is complete.

        JMP LOOP2       Repeats loop to read the next
                        WCS location.
```

SETTING BLOCK NUMBERS AND CONTROL MEMORY OPERATION. The following program assigns block numbers and, hence, control memory module numbers to the WCS. Then the program enables the WCS for operation as control memory.

```
        CLC SC          Puts WCS in the command
                        state.

        LDA BLKN        Places block numbers in the
                        A-register.
```

```
        OTB SC      Outputs to the WCS a relative
                    address; the block numbers
                    must be output in the second
                    word.

        OTA SC      Sends the block numbers from
                    the A-register to the WCS.

        STF SC      Initiates control memory op-
                    eration of WCS at T5 of this
                    I/O instruction; address 0-511
                    become modules 10 and 11 and
                    addresses 512-1023 become
                    modules 4 and 5.

        :
        :
        :

BLKN    OCT 00205   This constant specifies that
                    the first block is block number
                    5 and the second block is block
                    number 2.
```

READING WCS INTO MEMORY USING DCPC. To read the WCS using the Dual Channel Port Controller (DCPC), replace LOOP2 in the Reading WCS into Memory Section with the DCPC initialization sequence. Issue the Set Control (STC) to the WCS select code *after* starting DCPC. DCPC will use every I/O cycle until the entire block of data is read from the WCS into main memory.

The STC and CLC options of DCPC (contained in Control Word 1) should not be utilized for transfers to/from WCS, as each STC or CLC reinitializes the WORD flip-flop.

Note that DCPC issues a CLF after each word transferred, disabling operation of the board as control memory.

The following program is an example of using DCPC channel 1 to read a block of 1000_8 words from the WCS on select code 10 into main memory starting at address $10{,}000_8$.

```
        CLC 10      Puts WCS in the command
                    state.

        LDA ADDR    Places address of first location
                    to be read in the A-register.

        OTA 10      Sends the beginning address
                    to the WCS.

(LOOP2) LDA CW1     Gets the first DCPC control
                    word from main memory and
                    loads it into the A-register.

        OTA 6       Sends the first DCPC control
                    word to DCPC channel 1.

        CLC 2       Prepares DCPC channel 1 to
                    receive the second DCPC con-
                    trol word.

        LDA CW2     Gets the second DCPC control
                    word from main memory and
                    loads it into the A-register.

        OTA 2       Sends the second DCPC con-
                    trol word to DCPC channel 1.

        STC 2       Prepares the DCPC channel to
                    receive the third DCPC word.

        LDA CW3     Gets the third DCPC control
                    word.

        OTA 2       Sends the third DCPC control
                    word to DCPC channel 1.

        STC 6,C     Turns on the selected DCPC
                    channel.

        STC 10      Starts the DCPC transfer.

        SFS 6       Tests for completion of the
                    transfer.

        JMP *-1     Loops until transfer complete.

        :
        :
        :

CW1     OCT 10

CW2     OCT 110000  Specifies DCPC input and the
                    starting address (10,000₈) of
                    the block to be output.

CW3     OCT 177000  Specifies two's complement of
                    the number (1000₈) of com-
                    puter words to be transferred.
```

USING WCS AS MODULE 0

When attempting to use the WCS as module 0, special care must be taken when enabling and disabling the WCS operation because of the use of the IOG signal to select the address presented to the RAM's. When an I/O instruction is being executed referencing the WCS select code, the on-board address counter is selected to supply the RAM address; if not, then the Control Memory Address Register (CMAR) is selected to supply the RAM address. The two instructions STF and CLF, respectively, enable and disable WCS operation and cause the IOG signal to be as-

serted. Thus, when executing a STF with WCS containing module 0 code, the IOG signal disappears at the same time that WCS becomes enabled. When trying to disable operation of WCS as module 0, there is a more troublesome problem. Here, as soon as IOG comes up when executing the CLF instruction to the board, the on-board address counter is selected to specify the RAM address. To avoid problems encountered by executing the microinstruction at the address contained in the on-board counter, the counter should be set to the address of some harmless microinstruction (such as a jump to FETCH) contained in WCS. When WCS is finally disabled, the base-set ROM's will again function, starting from the address specified in the CMAR.

3-4. GENERAL THEORY OF OPERATION

Writable Control Store (WCS) consists of a bipolar semiconductor Random Access Memory (RAM) containing 24 integrated-circuit (IC) packages mounted on a printed-circuit assembly (PCA). Also included is the flat jumper cable assembly necessary for complete mechanization within the computer. The WCS PCA should be installed only in slots 10 (standard), 11, and 12 of the computer I/O slots. Each IC package is configured in 1024 bits and organized as one bit per word. Thus, one module of WCS is capable of storing 1024 words of 24 bits each. For the purpose of execution of WCS instructions, WCS can be configured to be addressed as any four of the computer's control memory modules. Two WCS PCA's can be installed on an HP 2105 Computer. Three WCS PCA's can be installed on an HP 2108, 2109, 2111, 2112, 2113, or 2117 Computer.

WCS MODULE IDENTIFICATION

For proper addressing of WCS, an integrated-circuit comparator and two block number registers are used on the WCS PCA to identify the PCA as particular modules of control memory. For example, if the WCS board is configured for block 2, the PCA will be enabled when the Control Memory Address Register (CMAR) contains the pattern "000010" in its six most-significant bits (14-9), and will be disabled otherwise. When enabled, the word in WCS addressed by CMAR bits 8-0 will be sent to the Microinstruction Register (MIR) as signals ROM0 through ROM23. The computer will then execute this word (microinstruction as though it came from standard control memory.

WCS CONNECTION

WCS is connected to the computer CPU through the I/O structure (for loading and checking), and also through a 50-conductor ribbon cable connector. It is this connector that enables WCS to be used as an extension of the computer's basic control memory. The cable connects one, two or three WCS PCA's to the CPU PCA and the FAB in the HP 1000 E/F-Series. (In an M-Series, WCS connects to CPU and ROM PCA.) The CMAR on the CPU sends a 14-bit address (12-bit address in an M-Series) to the WCS PCA(s) through this cable and the addressed WCS then sends its data (microinstruction) from that address back through this cable to the MIR.

WCS ADDRESSING

The WCS Address Register determines which address is loaded or read while the WCS is in the data state. Thus, before loading or reading the WCS Random Access Memory, the WCS Address Register must be set. This is accomplished by sending the WCS address to the WCS while it is in the command state. Refer to section 3-3 for the explanation of how to set the WCS Address Register.

WCS OPERATION AS CONTROL MEMORY

Once loaded and enabled, WCS becomes an extension of control memory. Microprograms stored in the WCS are executed exactly as those stored in ROM. Since the WCS can be loaded via standard I/O instructions, it may be used to debug and store additions to the computer instruction set while the computer is in an operating condition. This feature permits dynamic expansion of the computer instruction set.

WCS TIMING DIAGRAM

Figure 3-3 illustrates the HP 13197A WCS timing.

NOTE

Pressing the PRESET switch on the operator panel, or executing the CLC 0 instruction, issues the CRS signal to all I/O boards installed in HP 1000 Series computers. The CRS signal disables all WCS boards from operation as control memory.

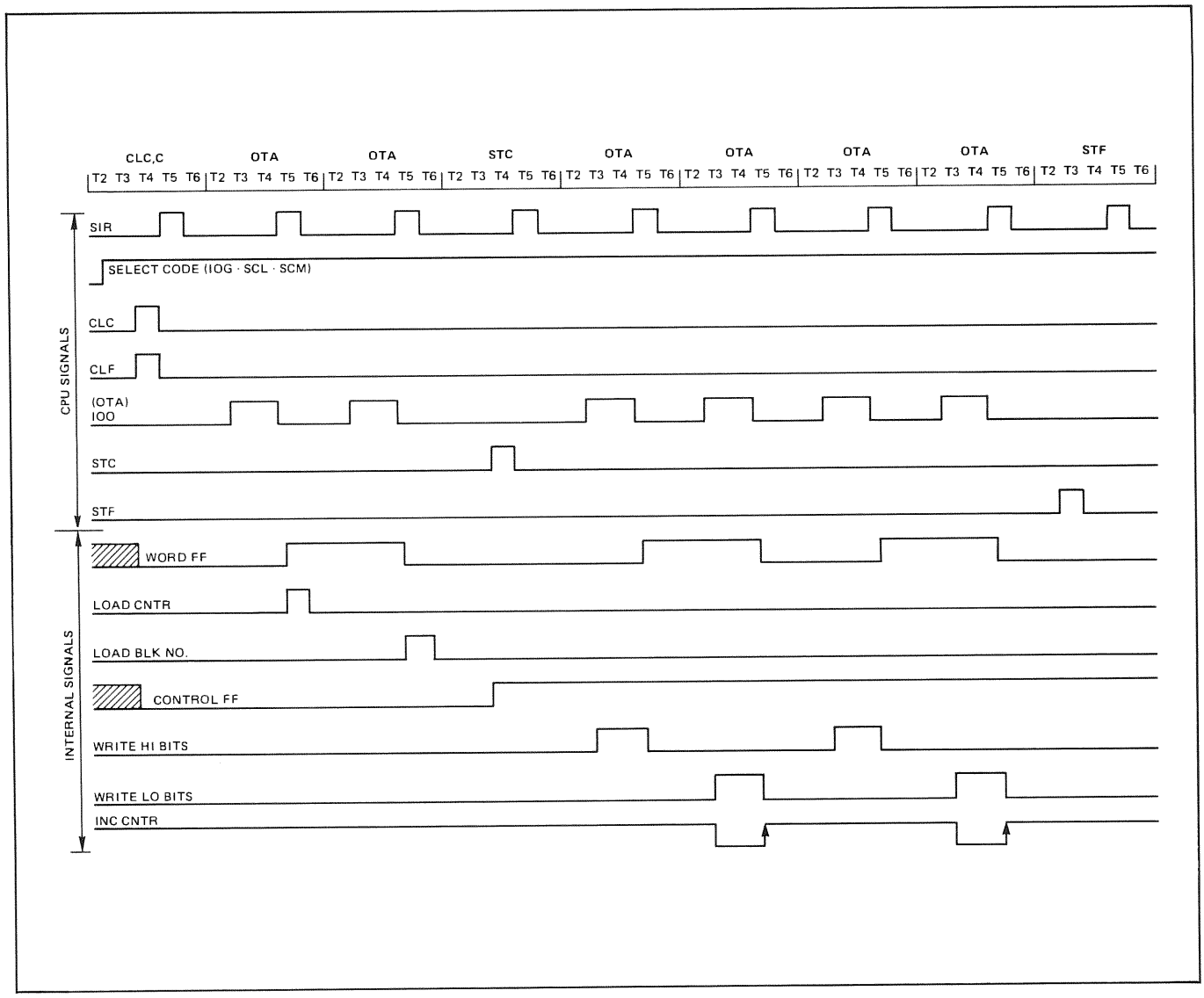


Figure 3-3. HP 13197A WCS Timing Diagram

HP 13305A DYNAMIC MAPPING SYSTEM

SECTION IV

4-1. INTRODUCTION

This section provides installation instructions for the HP 13305A Dynamic Mapping System Kit, which is an accessory for the HP 1000 E/F-Series Computers. Additional information is provided in the manuals listed in the Preface.

4-2. DESCRIPTION

The Dynamic Mapping System Kit consists of the following hardware:

DESCRIPTION	HP PART NO.	HP PRODUCT NO.
Memory Expansion Module	12731-60001	12731A
Memory Protect PCA	12892-60003	12892B
1K ROM IC (bits 3-0)	13307-80027	13307A
1K ROM IC (bits 7-4)	13307-80028	
1K ROM IC (bits 11-8)	13307-80029	
1K ROM IC (bits 15-12)	13307-80030	
1K ROM IC (bits 19-16)	13307-80031	
1K ROM IC (bits 23-20)	13307-80032	

REQUIRED HARDWARE

One of the following accessories is required for the installation of the six 1K ROM ICs in the E/F-Series Computer:

a. HP 13304A Firmware Accessory Board Kit

b. HP 13047A User Control Store Kit

The 13304A Firmware Accessory Board is standard in 2109E, 2113E, 2111F, and 2117F computers.

4-3. INSTALLATION

Install the memory expansion module (MEM) and memory protect PCA in the computer memory PCA cage as follows:

a. On MEM, ensure that jumpers W1 through W4 are configured as shown in figure 4-1. The functions of these jumpers are described in table 4-1.

b. On memory protect PCA, ensure that configuration jumper block U21 is configured as shown in figure 4-2.

c. On the rear of the computer set the battery EXT/INT OFF switch to OFF.

d. Switch the ~LINE ON/OFF switch to OFF, and disconnect the power cord.

e. Remove memory PCA retainer and install memory expansion module, part no. 12731-60001, in slot 112.

f. Install memory protect PCA, part no. 12892-60003, in slot 111; replace memory PCA retainer.

The six 1K ROM integrated circuits (ICs) are allocated to control store module 32 (decimal) and can be installed on either the HP 13304A Firmware Accessory Board (FAB) or the HP 13047A User Control Store (UCS) board. Install the ROM ICs as described in one of the following two procedures.

FIRMWARE ACCESSORY BOARD

a. Refer to section I of this manual for the FAB removal procedure.

b. Install the following ROM ICs in the specified sockets on the FAB and set the jumpers as shown below to correspond to Control Memory module 32 (decimal).

LOCATION	ROM IC	BITS	MODULE NO.
A1 (XU602)	13307-80027	3-0	32
A2 (XU603)	13307-80028	7-4	
A3 (XU604)	13307-80029	11-8	
A4 (XU606)	13307-80030	15-12	
A5 (XU607)	13307-80031	19-16	
A6 (XU608)	13307-80032	23-20	

JUMPER	SETTING
9A	0
10A	0
11A	0
12A	0
13	1

c. Install the FAB following the procedures in section I.

d. Perform verification as described in section 4-4.

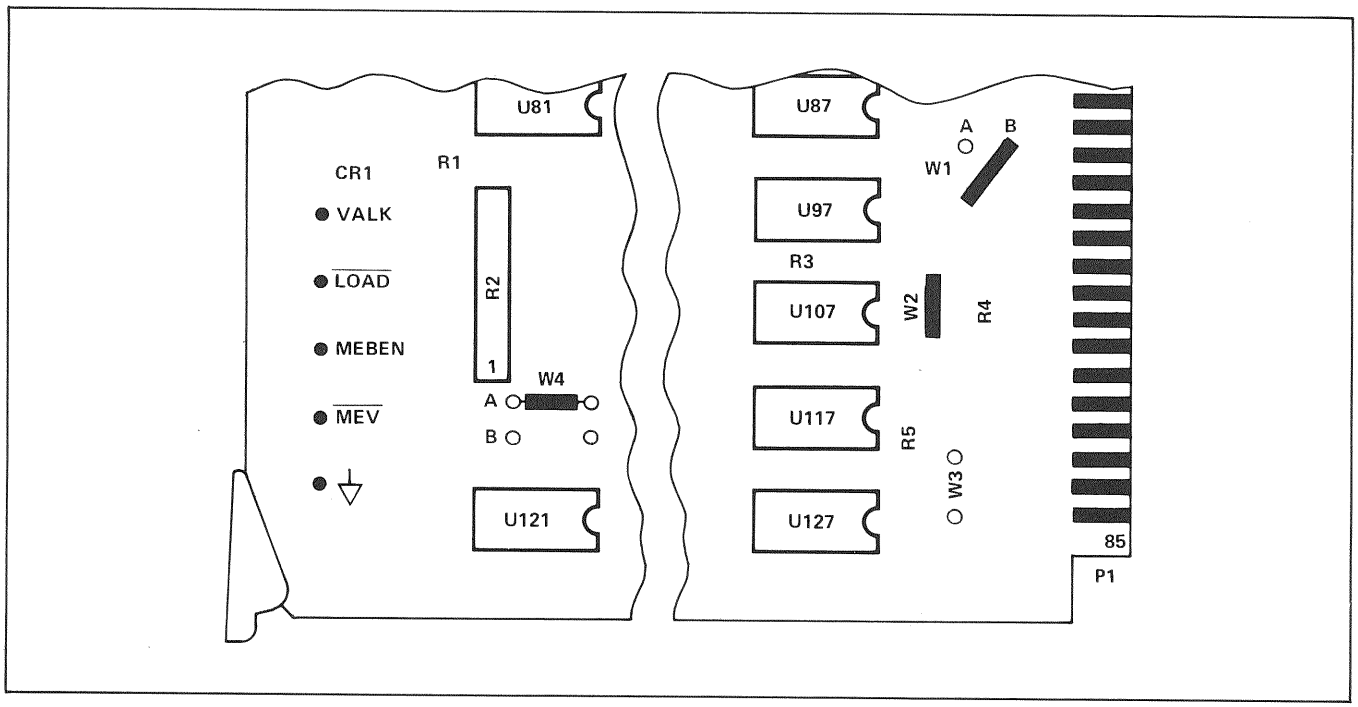


Figure 4-1. MEM Configuration Jumpers

Table 4-1. Memory Expansion Module Jumper Functions

JUMPER	DESCRIPTION
W1	Plug-in jumper; selects computer compatibility as follows: W1 = A = HP 1000 M-Series Computer (2108/2112) W1 = B = HP 1000 E/F-Series Computer (2109/2113/2111/2117)
W2	Plug-in jumper; factory test only: W2 = IN = Normal operation W2 = OUT = Factory test
W3	Hardwired jumper; factory test only: W3 = IN = Factory test W3 = OUT = Normal operation
W4	Hardwired jumper: Reset Memory Expansion Module. With the Memory Protect enabled and the computer issues IAK (Interrupt Acknowledge) in response to an IRQ (Interrupt Request), Memory Protect is turned off and the Memory Expansion Module (MEM) is switched automatically to the System Map. If an I/O instruction is in the trap cell allocated to the interrupting device, Memory Protect is turned back on and asserts the RME signal which controls the following: W4 = A = MEM remains in System Map. W4 = B = MEM returns to same map in use prior to IAK being issued. Note: MEM jumper W4 and Memory Protect RME jumper *must* be configured alike to respond to the RME signal. That is, if the Memory Protect RME jumper is OUT, MEM jumper W4 must be in position "A"; if the Memory Protect RME jumper is IN, MEM jumper W4 must be in position "B".

USER CONTROL STORE

a. Refer to the *HP 13047A User Control Store (UCS) Installation and Service Manual* part no. 13047-90001 for configuration settings of the UCS board.

b. Install the 6 ROMs into any vacant set of sockets and configure the address for module 32 (decimal).

c. Install the UCS board as described in the UCS Installation and Service manual.

d. Perform verification as described below.

4-4. VERIFICATION

Verify the Dynamic Mapping System operation by running the following diagnostics:

DIAGNOSTIC	MANUAL	PAPER TAPE
Memory Protect-Parity Error Test	12892-90005	12892-16001
Memory Expansion Module Test	12929-90003	12929-16001

If the diagnostic tests are completed without an error halt, the DMS is operating correctly. If the tests indicate an error halt, refer to the FAB section or UCS for troubleshooting information. If trouble still persists, contact your nearest HP Sales and Service Office. (A list of HP Sales and Service Offices is given in the *HP 1000 E/F-Series Computer Operating and Reference Manual,* and the *HP 1000 E/F-Series Computer Installation and Service Manual.*

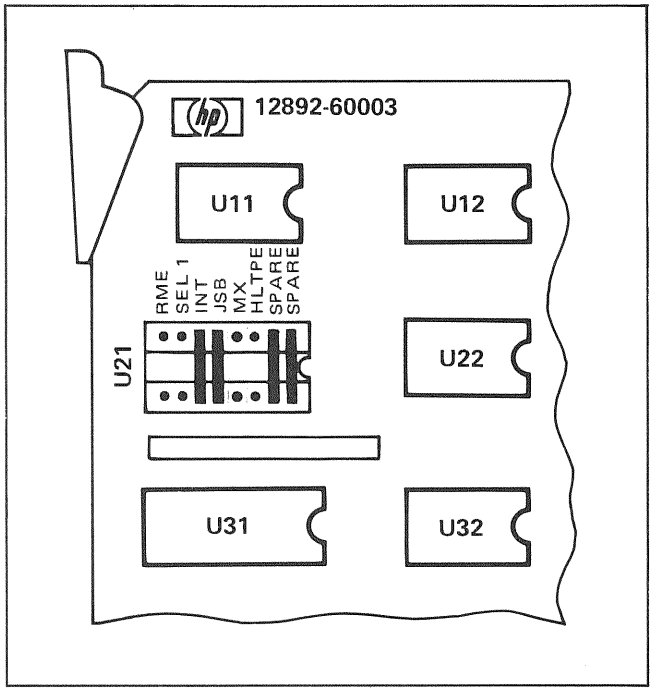


Figure 4-2. Memory Protect Configuration Jumpers

HP RTE IV A/B EXTENDED MEMORY AREA FIRMWARE

SECTION V

5-1. INTRODUCTION

This section provides installation instructions for the HP Extended Memory Area (EMA) Firmware. This firmware is to be installed in an E-Series Computer or an F-Series Computer for use with RTE IV A/B: Additional information is provided in the manuals listed in the Preface.

5-2. DESCRIPTION

The HP EMA firmware consists of three 4K ROMs that are installed on the FAB board. The firmware routines handle map switching (if required) and addressing to data words located in extended memory.

The HP EMA firmware consists of the following:

DESCRIPTION	PART NO.
4K ROM IC (Bits 23-16)	92067-80003
4K ROM IC (Bits 15-8)	92067-80002
4K ROM IC (Bits 7-0)	92067-80001

5-3. INSTALLATION

The three EMA ROMs can be installed on the HP 13304A Firmware Accessory Board (FAB) or the HP 12791A Firmware Expansion Module (FEM). If a FEM with an unused block of sockets is available, it may be desirable to install the ROMs on the FEM to facilitate future access to the ROMs.

FIRMWARE ACCESSORY BOARD

a. Refer to section I of this manual for the FAB removal procedure.

b. Install the following ROM ICs in the specified sockets on the FAB and set the jumpers to correspond to Control Memory modules 36 and 37.

NOTE

Sockets C1 through C3 are recommended for the EMA firmware location, due to location requirements of other HP firmware accessories, such as the HP 13306A Fast Fortran Processor.

If DS/1000 ROMs, part numbers 91740-80018, 91740-80019, and 91740-80020, are presently installed on the FAB board, they should be residing in the MSMP of blocks B, C, or D. For this case, the EMA ROMs should be installed in the LSMP of this block. For example, if DS/1000 ROMs are occupying C4, C5, and C6, then the EMA ROMs should be installed in sockets C1, C2, and C3 (refer to the table below and figure 1-2 to associate each EMA ROM with the appropriate socket).

LOCATION	ROM IC	BITS	MODULE NO.
B1 (XU401) C1 (XU201) D1 (XU101)	92067-80001 (EMA ROM)	7-0	36, 37
B2 (XU402) C2 (XU202) D2 (XU102)	92067-80002 (EMA ROM)	15-8	
B3 (XU404) C3 (XU202) D3 (XU104)	92067-80003 (EMA ROM)	23-16	
B4 (XU406) C4 (XU206) D4 (XU106)	91740-80049 (DS/1000 ROM)	7-0	38, 39
B5 (XU408) C5 (XU208) D5 (XU108)	91740-80050 (DS/1000 ROM)	15-8	
B6 (XU409) C6 (XU209) D6 (XU109)	91740-80051 (DS/1000 ROM)	23-16	

c. Set jumpers 10 through 13 as shown in below. Jumper notations A, B, C, and D correspond to blocks A, B, C, and D respectively.

JUMPER	SETTING
10C	1
11C	0
12C	0
13	1

d. Refer to section I of this manual for the FAB installation procedure.

e. Perform the verification as described in section 5-4.

FIRMWARE EXPANSION MODULE

a. Refer to section II of this manual for the FEM removal and installation procedure.

b. Install the three ROM ICs in any available set of sockets and configure the switches as shown in table 2-1 for Control Memory modules 36 and 37.

c. Refer to section II for the FEM installation procedure.

d. Perform verification as described below.

5-4. VERIFICATION

Installation
After installing the EMA ROMs, verify correct installation by running the EMA self-test. The EMA self-test checks for correct IC orientation and correct EMA firmware addressing.

To execute the EMA self-test proceed as follows:

a. Store 105242 (octal) in the A-Register.
b. Store 0 in the P-Register.
c. Store 0 in the S-Register.
d. Press PRESET.
e. Press INSTR STEP.

If the EMA self-test completes with the S-Register equal to 102077 then the firmware is operational. If the test completes with the S-Register NOT EQUAL to 102077, then check for the following conditions:

a. Incorrect IC orientation on the FAB or FEM.
b. Incorrect jumper positioning on the FAB board, or switch settings on the FEM.
c. IC pin(s) are bent under or broken off.

If a failure still exists, refer to the Service Information paragraph of the FAB or FEM section of this manual for troubleshooting procedures.

Operation
To verify functional operation of the EMA firmware, the EMA on-line diagnostic should be run. Refer to the EMA On-Line Diagnostic Reference Manual, part number 92067-90007, for operating instructions. Follow the troubleshooting procedures recommended in the EMA On-Line Diagnostic Reference Manual if a failure exists.

HP 13306A FAST FORTRAN PROCESSOR FIRMWARE

SECTION VI

6-1. INTRODUCTION

This section provides installation instructions for the HP 13306A Fast FORTRAN Processor Kit, which is an accessory for the HP 1000 E-Series Computer. Additional information is provided in the manuals listed in the Preface.

6-2. DESCRIPTION

The HP 13306A Fast FORTRAN Processor (FFP) Kit consists of nine read-only-memory (ROM) integrated-circuits (IC's). Six 1K ROM IC's are allocated to control memory module 33 (decimal) and three 4K ROM IC's are allocated to control memory modules 34 and 35 (decimal), as follows:

DESCRIPTION	HP PART NO.
4K ROM IC (Bits 7-0)	5090-0589
4K ROM IC (Bits 15-8)	5090-0590
4K ROM IC (Bits 23-16)	5090-0591
1K ROM IC (Bits 3-0)	13306-80013
1K ROM IC (Bits 7-4)	13306-80014
1K ROM IC (Bits 11-8)	13306-80015
1K ROM IC (Bits 15-12)	13306-80016
1K ROM IC (Bits 19-16)	13306-80017
1K ROM IC (Bits 23-20)	13306-80018

6-3. INSTALLATION

The HP 13304A Firmware Accessory Board Kit is required for the installation of the nine FFP ROM IC's. Install the FFP ROM IC's on the firmware accessory board (FAB) as follows:

a. Refer to section I of this manual for removal of the FAB.

b. On the FAB, install the nine ROM IC's in the following locations (see figure 1-2):

LOCATION	ROM IC	BITS	MODULE NO.
A7 (XU802)	13306-80013	3-0	33
A8 (XU803)	13306-80014	7-4	
A9 (XU804)	13306-80015	11-8	
A10 (XU806)	13306-80016	15-12	
A11 (XU807)	13306-80017	19-16	
A12 (XU808)	13306-80018	23-20	
B4 (XU406)	5090-0589	7-0	34,35
B5 (XU408)	5090-0590	15-8	
B6 (XU409)	5090-0591	24-16	

Ensure that the IC's are oriented correctly as shown in figure 1-2 by matching pin 1 of each IC with the white dot on each IC socket.

c. Configure the control store module address jumpers for modules 33, 34, and 35 as shown below. Figures 1-1 and 1-2 can be used for reference.

JUMPER	SETTING
9A	0
10A	0
11A	0
12A	0
10B	0
11B	0
12B	0
13	1

d. Refer to section I for the FAB installation procedure.

e. Perform verification as described below.

6-4. VERIFICATION

After installing the FFP, verify proper operation by performing the Fast FORTRAN Processor diagnostic test described in the *Diagnostic Reference Manual*. Part numbers for the diagnostic test are as follows:

DIAGNOSTIC	MANUAL	PAPER TAPE
Fast FORTRAN Processor	12977-90002	12997-16004 12977-16005

If the diagnostic test is completed without an error halt, the FFP is operating correctly. If the diagnostic test indicates an error halt, refer to the FAB section of this manual for troubleshooting information.

HP 1000 F-SERIES FAST FORTRAN PROCESSOR FIRMWARE

SECTION VII

7-1. INTRODUCTION

This section provides installation and reference information for the F-Series Fast FORTRAN Processor. Additional information is provided in the manuals listed in the Preface.

NOTE

F-Series FFP ROMs, part nos. 5950-1615 thru 5090-1623, require compatible F-Series Base Instruction Set ROMs, part nos. 12740-80019 thru 12740-80024 and visa versa for correct operation.

7-2. DESCRIPTION

The F-Series FFP consists of nine read-only-memory (ROM) integrated-circuits (IC's). Six 1K ROM IC's are allocated to control memory module 33 (decimal) and three 4K ROM IC's are allocated to control memory modules 34 and 35 (decimal), as follows:

DESCRIPTION	HP PART NO.
1K ROM IC (Bits 3-0)	5090-1615
1K ROM IC (Bits 7-4)	5090-1616
1K ROM IC (Bits 11-8)	5090-1617
1K ROM IC (Bits 15-12)	5090-1618
1K ROM IC (Bits 19-16)	5090-1619
1K ROM IC (Bits 23-20)	5090-1620
4K ROM IC (Bits 7-0)	5090-1621
4K ROM IC (Bits 15-8)	5090-1622
4K ROM IC (Bits 23-16)	5090-1623

7-3. INSTALLATION

The F-Series FFP ROMs are standard on the F-Series Computer. They are installed on the HP 13304A Firmware Accessory Board (FAB). If a Firmware Expansion Module (FEM) is available the three 4K ROMs can be installed here for ease of future access. To install or remove the FFP ROMs, proceed as follows.

a. Refer to section I of this manual for the FAB removal procedure.

b. The nine ROM IC's should be installed in the following locations.

LOCATION	ROM IC	BITS	MODULE NO.
A7 (XU802)	5090-1615	3-0	
A8 (XU803)	5090-1616	7-4	
A9 (XU804)	5090-1617	11-8	33
A10 (XU806)	5090-1618	15-12	
A11 (XU807)	5090-1619	19-16	
A12 (XU808)	5090-1620	23-20	
B4 (XU406)	5090-1621	7-0	
B5 (XU408)	5090-1622	15-8	34,35
B6 (XU409)	5090-1623	23-16	

c. Configure control memory address jumpers for modules 33, 34, and 35 as shown below. Figures 1-1 and 1-2 can be used for reference.

JUMPER	SETTING
9A	0
10A	0
11A	0
12A	0
10B	0
11B	0
12B	0
13	1

d. Refer to section I for the FAB installation procedure.

e. Perform verification as described below.

7-4. VERIFICATION

INSTALLATION

After installing the FFP ROMs, verify proper installation by running the firmware self-test. The firmware self-test checks for correct IC orientation and if the FFP firmware is correctly addressed.

NOTE

The FFP firmware self-test is present only in the enhanced F-Series FFP firmware, part nos. 5090-1615 to 5090-1623.

To execute the FFP self-test proceed as follows:

a. Store 105200 (octal) in the A-register.
b. Store 0 in the P-register.
c. Press PRESET.
d. Press INSTR STEP.

One of three results should be displayed in the S-register:

a. S = 102077 indicates successful completion.
b. S = 102001 indicates module 33 defective or missing.
c. S = 102002 indicates module 35 defective or missing.

Any other indication in the S-register indicates that FFP is defective or not installed properly. If other than a 102077B is displayed on the S-register, check for the following conditions.

a. Incorrect IC orientation on the FAB.
b. Incorrect jumper positioning on the FAB.
c. IC pin(s) are bent under or broken off.

If a failure still exists, refer to the Service Information paragraph of the FAB section of this manual (section I) for troubleshooting procedure.

OPERATION

To verify functional operation of the FFP firmware, the FFP/Floating Point Processor/Scientific Instruction Set off-line diagnostic should be run. Refer to the FFP/ Floating Point Processor/Scientific Instruction Set Diagnostic Reference Manual for execution procedure.

DIAGNOSTIC	MANUAL	ABSOLUTE BINARY NO.
Floating Point Processor/ Scientific Instruction Set/ Fast FORTRAN Processor	12740-90004	12740-16001

If the diagnostic test is completed without an error halt, the FFP is operating correctly. If the diagnostic test indicates an error halt, refer to the FAB section of this manual for troubleshooting information.

HP 1000 F-SERIES SCIENTIFIC INSTRUCTION SET FIRMWARE

SECTION VIII

8-1. INTRODUCTION

This section provides installation and reference information for the F-Series Scientific Instruction Set (SIS) firmware. Additional information is provided in the manuals listed in the Preface.

8-2. DESCRIPTION

The Scientific Instruction Set (SIS) firmware consists of six read-only-memory (ROM) integrated-circuits (IC's). The six ROMs are allocated to control memory modules 40, 41, 42, and 43 as follows:

DESCRIPTION	HP PART NO.
4K ROM IC (bits 7-0)	12823-80013
4K ROM IC (bits 15-8)	12823-80014
4K ROM IC (bits 23-16)	12823-80015
4K ROM IC (bits 7-0)	12823-80016
4K ROM IC (bits 15-8)	12823-80017
4K ROM IC (bits 23-16)	12823-80018

8-3. INSTALLATION

The F-Series SIS ROMs are standard on the F-Series Computer. They are installed on the HP 13304A Firmware Accessory Board (FAB). If a Firmware Expansion Module (FEM) is available, it is recommended that the ROMs be installed here to facilitate future service. To install or remove the SIS ROMs, proceed as follows.

a. Refer to section I of this manual for the FAB removal procedure.

b. Due to allocations of the FAB for other HP optional firmware, the SIS ROMs should be installed in the following locations. Refer to figure 1-2 in section I for socket locations.

LOCATION	ROM IC	BITS	MODULE NO.
D1 (XU101)	12823-80013	7-0	40,41
D2 (XU102)	12823-80014	15-8	
D3 (XU104)	12823-80015	23-16	
D4 (XU106)	12823-80016	7-0	42,43
D5 (XU108)	12823-80017	15-8	
D6 (XU109)	12823-80018	23-16	

c. Configure control memory address jumpers for modules 40, 41, 42, and 43 as shown below. Figures 1-1 and 1-2 can be used for reference.

JUMPER	SETTING
10D	0
11D	1
12D	0
13	1

d. Refer to section I of this manual for the FAB installation procedure.

e. Perform verification as described below.

8-4. VERIFICATION

INSTALLATION

After installing the SIS ROMs, verify proper installation by running the firmware self-test. The firmware self-test checks for correct IC orientation and correct SIS firmware addressing.

To execute the SIS self-test proceed as follows:

a. Store 105337 (octal) in the A-register.

b. Store 0 in the P-register.

c. Press RESET.

d. Press INSTR STEP.

A 102077 (octal) in the S-register indicates successful completion. Any other value displayed in the S-register indicates the SIS firmware self test failed. Refer to the Service Information paragraph of the FAB section of this manual (section I) for troubleshooting procedure.

S = 102001 Indicates floating point PCA's not cabled or not powered.

S = 102002 Indicates a numerical error in the diagnostic calculation; defective floating point PCA(s) or ROMs.

OPERATION

To verify functional operation of the SIS firmware, the FPP/SIS/FFP off-line diagnostic should be run. Refer to the FPP/SIS/FFP Diagnostic Reference Manual for execution procedure.

DIAGNOSTIC	MANUAL	ABSOLUTE BINARY NO.
Floating Point Processor/ Scientific Instruction Set/ Fast FORTRAN Processor	12740-90004	12740-16001

If the diagnostic test is completed without an error halt, the SIS is operating correctly. If the diagnostic test indicates an error halt, refer to the Service Information paragraph of the FAB section of this manual (section I) for troubleshooting procedure.

HP 12824A VECTOR INSTRUCTION SET FIRMWARE

SECTION IX

9-1. INTRODUCTION

This section provides installation and reference information for the HP 12824A Vector Instruction Set (VIS) firmware, which is an option for the F-Series Computer. Additional information is provided in the manuals listed in the Preface.

9-2. DESCRIPTION

The Vector Instruction Set (VIS) firmware consists of six read-only-memory (ROM) integrated-circuits (IC's) the six ROMs are allocated to control memory modules 12, 13, 14, and 15.

DESCRIPTION	HP PART NO.
4K ROM IC (bits 7-0)	12824-80001
4K ROM IC (bits 15-8)	12824-80002
4K ROM IC (bits 23-16)	12824-80003
4K ROM IC (bits 7-0)	12824-80004
4K ROM IC (bits 15-8)	12824-80005
4K ROM IC (bits 23-16)	12824-80006

The 12791A Firmware Expansion Module is an accessory which is required for the installation of the six 4K ROMs in a F-Series Computer.

9-3. INSTALLATION

The VIS ROMs are installed on the 12791A Firmware Expansion Module (FEM). To install or remove the six VIS ROMs, proceed as follows.

a. Refer to section II of this manual for the FEM removal procedure (if necessary).

b. The six VIS ROMs can be installed in any two available socket sets on the FEM. For example, assume we are going to install the ROMs in SETA and SETB. Refer to figure 2-1 for location of the sockets.

LOCATION	ROM IC	BITS	MODULE NO.
A1	12824-80001	7-0	12,13
A2	12824-80002	15-8	
A3	12824-80003	23-16	
B1	12824-80004	7-0	14,15
B2	12824-80005	15-8	
B3	12824-80006	23-16	

c. Configure the SETA control memory address switches, SWA, for modules 12 and 13. Configure SETB control memory address switches, SWB, for modules 14 and 15 as shown below. Refer to figure 2-1 and table 2-1 for reference.

SWA		SWB	
SWITCH	SETTING	SWITCH	SETTING
S1	1	S1	1
S2	0	S2	0
S3	0	S3	0
S4	1	S4	1
S5	1	S5	1
S6	0	S6	0
S7	0	S7	0
S8	1	S8	1
S9	1	98	1
S10	0	S10	1

d. Refer to section II of this manual for the FEM installation procedure.

e. Perform verification as described below.

9-4. VERIFICATION

Installation
After installing the VIS ROMs, verify proper installation by running the VIS firmware self-test. The firmware self-test checks for correct IC orientation and correct VIS firmware addressing.

To execute the VIS self-test proceed as follows:

a. Store 105477 (octal) in the A-register.

b. Store 0 in the P-register.

c. Press PRESET.

d. Press INSTR STEP.

A 102077 (octal) in the S-register indicates successful completion. Any other value displayed in the S-register indicates the VIS firmware self-test failed. Refer to the Service Information paragraph of the FEM section of this manual (section II) for troubleshooting procedure.

Operation
To verify functional operation of the VIS firmware, the VIS on-line diagnostic should be run. Refer to the *VIS Users Manual,* part number 12824-90001, for operating instructions. Troubleshooting procedures are recommended in the FEM section of this manual.

HP 91740B DISTRIBUTED SYSTEM FIRMWARE

SECTION X

10-1. INTRODUCTION

This section provides quick reference information for the HP 91740B E/F-Series Distributed System (DS/1000) Firmware. Complete installation information can be found in the *HP 91740B Distributed System (DS/1000) Firmware Installation Manual,* part no. 91740-90009, which is supplied with the product. Additional information is provided in the manuals listed in the Preface.

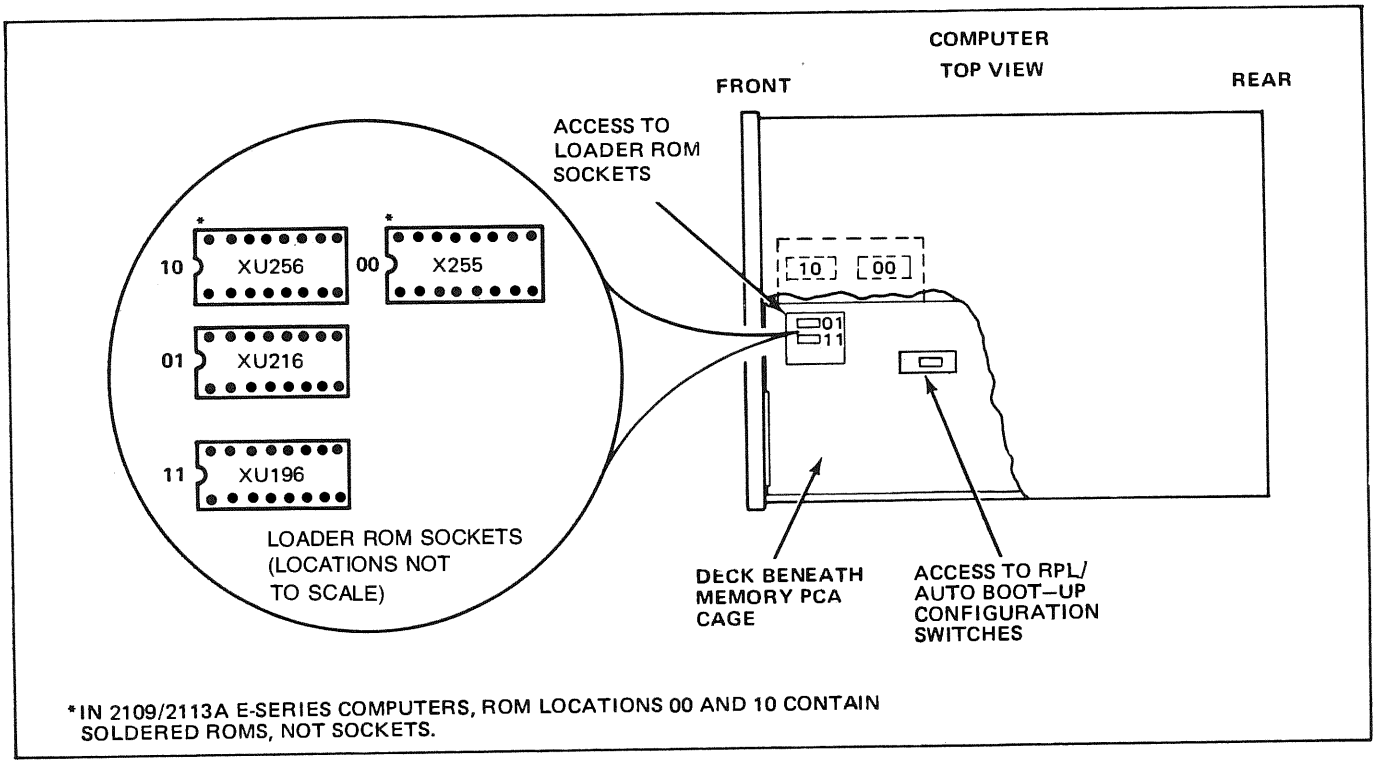
10-2. DESCRIPTION

The HP 91740B Firmware consists of one DS/1000 Communications Bootstrap Loader (CBL) ROM and three DS/1000 Driver Microcode ROM's. The CBL is an Initial Binary Loader (IBL) that is installed in one of the loader ROM sockets on the Central Processing Unit (CPU) PCA. The driver ROM's contain a microprogram that allows communication between other Hewlett-Packard Computers that are equipped with DS/1000 and the appropriate communication interfaces. These driver ROM's are installed on the HP 13304A Firmware Accessory Board (FAB). The HP part numbers for the HP 91740B Firmware are as follows:

DESCRIPTION	HP PART NO.
CBL ROM	
1k ROM IC	91740-80048
DRIVER MICROCODE ROM's	
4k ROM IC (Bits 7-0)	91740-80049
4k ROM IC (Bits 15-8)	91740-80050
4k ROM IC (Bits 23-16)	91740-80051

10-3. INSTALLATION

A loader ROM socket on the CPU board is required for installation of CBL ROM (Figure 10-1). The HP 13304A Firmware Accessory Board is required for installation of the three driver microcode ROM's. These ROM's should be installed in the MSMP (most significant module pair) of block C.



*IN 2109/2113A E-SERIES COMPUTERS, ROM LOCATIONS 00 AND 10 CONTAIN SOLDERED ROMS, NOT SOCKETS.

a. Install the CBL ROM in loader ROM socket 11 in an A-Model computer (2109A, 2113A), or in socket 10 or 11 in a 2109B/E, 2113B/E, 2111F, or 2117F model computer.

b. Refer to section I of this manual for the FAB removal procedure.

c. Due to the allocations of the FAB for other HP optional firmware, and that the DS/1000 driver microcode operates in a most significant module pair (MSMP) block, the DS/1000 ROMs should be installed in the following locations. Refer to figure 1-2 in section I for socket locations.

LOCATION	ROM IC	BITS	MODULE NO.
C4 (XU106)	91740-80049	7-0	38,39
C5 (XU108)	91740-80050	15-8	
C6 (XU109)	91740-80051	23-16	

c. Configure control memory address jumpers for modules 38 and 39 as shown below. Refer to figures 1-1 and 1-2 for location of jumper and settings.

JUMPER	SETTING
10C	1
11C	0
12C	0
13	1

d. Refer to section I of this manual for the FAB installation procedure.

e. Perform verification as described below.

10-4. VERIFICATION

After reinstalling the computer in your system, verify correct DS/1000 Firmware installation by running the DS/1000 Self-Test. The DS/1000 Self-Test checks for correct IC orientation and correct DS/1000 firmware addressing.

To execute the DS/1000 Self-Test proceed as follows:

a. Press < Register Select >, as required, to select the S-register for display in the Display Register. The light associated with the S-register will be on, once the S-register is selected.

b. Press CLEAR DISPLAY to clear the contents of the Display Register. If the CBL ROM was installed in loader socket 11_2 (XU196), press switches 14 and 15. If the CBL ROM was installed in loader socket 10_2 (XU256), press switch 15. This sets the bits in the Display Register which selects the CBL ROM.

c. Set bits 6 through 11 of the Display Register to the select code of the DS/1000 communications interface. The select code corresponds to the octal number marked on the computer chassis adjacent to the card slot containing the DS/1000 communications interface card. If a system contains multiple DS/1000 communications PCA's, choose the select code of the primary downloading PCA.

d. Press STORE.

e. Press PRESET and then IBL/TEST. Do NOT press RUN!

f. Press < Register Select >, as required, to select the P-register. Do NOT clear the display. Press switches 3, 4, and 5 to set bits 3, 4, and 5 in the Display Register. Press STORE.

g. Press RUN.

If the DS/1000 CBL ROM and Driver Microcode ROM's are installed properly, the RUN light should remain lit and the Display Register should indicate 014423_8. If the Display Register is partitioned into four equal sections (Table 10-1) with each section representing a BCD digit (bits 15-12 representing the most significant digit), the number displayed should be 1913. This number corresponds to the approximate release time of this firmware (the thirteenth week of 1979).

If the Display Register indicates 102055_8, the RUN light is off, and the T-register select light is on, then the CBL

ROM is installed properly; but, a problem concerning the DS/1000 Driver Microcode ROM's has been detected. The FAB assembly should be removed and inspected for the following:

a. Incorrect ROM IC orientation.

b. Incorrect jumper positioning.

c. Bent or broken ROM IC pin(s).

d. Incorrect 4K ROM IC part numbers.

e. Damaged parts.

If the Display Register contains any other value, the CBL ROM should be inspected for the following.

a. Incorrect orientation.

b. Bent or broken pin(s).

c. Incorrect part number. Also, other Display Register values may result from a CPU failure.

If these inspections locate a problem, correct it and run the DS/1000 Self-Test again. If the failure still exists, isolate the faulty ROM IC(s) by substituting a good ROM IC(s). If failure still exists, contact your nearest Hewlett-Packard Sales and Service Office. A list of HP Sales and Service Offices is provided in your Computer Installation and Service Manual.

This firmware requires that the software communications driver (%DVA65, HP Part Number 91740-16071) must be revision level 1805 or later.

Refer to *Network Manager's Manual,* part no. 91740-90003 for generation and operating procedures.

Table 10-1. Display Register with Self-Test Passed

BCD	1				9				1				3			
LAMPS ON BITS				☆	☆			☆				☆			☆	☆
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OCTAL	0	1			4			4			2		3			

11-1. CONTROL MEMORY MAPS

This section contains the Control Memory allocation for HP 1000 M/E/F-Series computers.

CONTROL MEMORY MODULE ALLOCATION	MODULE NO.	ADDRESS DECIMAL	ADDRESS OCTAL	SOFTWARE ENTRY POINT	
HP BASE SET	0	0-00255	00000-00377	YES	1K
	1	00256-00511	00400-00777	YES	
HP DYNAMIC MAPPING INSTRUCTIONS	2	00512-00767	01000-01377	YES	
	3	00768-01023	01400-01777	YES	
HP FAST FORTRAN PROCESSOR	4	01024-01279	02000-02377	YES	2K
	5	01280-01535	02400-02777	YES	
	6	01536-01761	03000-03377	YES	
HP RESERVED	7	01762-02047	03400-03777	YES	
	8	02048-02303	04000-04377	YES	3K
	9	02304-02559	04400-04777	YES	
DS/1000	10	02560-02815	05000-05377	YES	
	11	02816-03071	05400-05777	YES	
RECOMMENDED FOR USER MICROPROGRAMMING	12	03072-03327	06000-06377	YES	4K
	13	03328-03583	06400-06777	YES	
HP BASE SET	14	03584-03849	07000-07377	YES	
	15	03850-04095	07400-07777	YES	

Figure 11-1. M-Series Control Memory Map

CONTROL MEMORY MODULE ALLOCATION	MODULE NO.	ADDRESS		SOFTWARE ENTRY POINT	
		DECIMAL	OCTAL		
HP BASE SET	0	0-00255!	00000-00377	YES	1K
	1	00256-00511	00400-00777	YES	
	2	00512-00767	01000-01377	YES	
	3	00768-01023	01400-01777	YES	
AVAILABLE FOR USER MICROPROGRAMMING	4	01024-01279	02000-02377	NO	2K
	5	01280-01535	02400-02777	NO	
	6	01536-01761	03000-03377	NO	
	7	01762-02047	03400-03777	NO	
	8	02048-02303	04000-04377	NO	3K
	9	02304-02559	04400-04777	NO	
	10	02560-02815	05000-05377	NO	
	11	02816-03071	05400-05777	NO	
	12	03072-03327	06000-06377	NO	4K
	13	03328-03583	06400-06777	NO	
	14	03584-03849	07000-07377	NO	
	15	03850-04095	07400-07777	NO	
	16	04096-04351	10000-10377	NO	5K
	17	04352-04607	10400-10777	NO	
	18	04608-04863	11000-11377	NO	
	19	04864-05119	11400-11777	NO	
	20	05120-05375	12000-12377	NO	6K
	21	05376-05631	12400-12777	NO	
	22	05632-05887	13000-13377	NO	
	23	05888-06143	13400-13777	NO	
	24	06144-06399	14000-14377	NO	7K
	25	06400-06655	14400-14777	NO	
	26	06656-06911	15000-15377	NO	
	27	06912-07167	15400-15777	NO	
	28	07168-07423	16000-16377	NO	8K
	29	07424-07679	16400-16777	NO	
HP DYNAMIC MAPPING SYSTEM →	30	07680-07935	17000-17377	NO	
	31	07936-08191	17400-17777	NO	
HP FAST FORTRAN PROCESSOR	32	08192-08447	20000-20377	YES	9K
	33	08448-08703	20400-20777	NO	
	34	08704-08959	21000-21377	YES	
	35	08960-09215	21400-21777	YES	
EXTENDED MEMORY AREA DS/1000	36	09216-09571	22000-22377	YES	10K
	37	09572-09727	22400-22777	YES	
	38	09728-09983	23000-23377	YES	
	39	09984-10239	23400-23777	YES	
HP RESERVED	40	10240-10495	24000-24377	YES	11K
	41	10496-10751	24400-24777	NO	
	42	10752-10917	25000-25377	NO	
	43	10918-11263	25400-25777	NO	
RECOMMENDED FOR USER MICROPROGRAMMING	44	11264-11519	26000-26377	YES	12K
	45	11520-11775	26400-26777	YES	
	46	11776-12031	27000-27377	YES	
	47	12032-12287	27400-27777	YES	
	48	12288-12543	30000-30377	YES	13K
	49	12544-12799	30400-30777	YES	
	50	12800-13055	31000-31377	YES	
	51	13056-13311	31400-31777	NO	
	52	13312-13557	32000-32377	NO	14K
	53	13558-13823	32400-32777	NO	
	54	13824-14079	33000-33377	NO	
	55	14080-14335	33400-33777	NO	
	56	14336-14591	34000-34377	YES	15K
	57	14592-14847	34400-34777	YES	
	58	14848-15103	35000-35377	YES	
	59	15104-15359	35400-35777	YES	
	60	15360-15615	36000-36377	YES	16K
	61	15616-15871	36400-36777	NO	
	62	15872-16127	37000-37377	YES	
	63	16128-16383	37400-37777	NO	

Figure 11-2. E-Series Control Memory Map

CONTROL MEMORY MODULE ALLOCATION	MODULE NO.	ADDRESS		SOFTWARE ENTRY POINT	
		DECIMAL	OCTAL		
HP BASE SET	0	0-00255	00000-00377	YES	1K
	1	00256-00511	00400-00777	YES	
	2	00512-00767	01000-01377	YES	
	3	00768-01023	01400-01777	YES	
HP RESERVED	4	01024-01279	02000-02377	YES	2K
	5	01280-01535	02400-02777	NO	
	6	01536-01761	03000-03377	NO	
	7	01762-02047	03400-03777	NO	
	8	02048-02303	04000-04377	YES	3K
	9	02304-02559	04400-04777	NO	
	10	02560-02815	05000-05377	NO	
	11	02816-03071	05400-05777	NO	
VECTOR INSTRUCTION SET	12	03072-03327	06000-06377	YES	4K
	13	03328-03583	06400-06777	NO	
	14	03584-03849	07000-07377	NO	
	15	03850-04095	07400-07777	NO	
HP RESERVED	16	04096-04351	10000-10377	YES	5K
	17	04352-04607	10400-10777	NO	
	18	04608-04863	11000-11377	YES	
	19	04864-05119	11400-11777	NO	
	20	05120-05375	12000-12377	YES	6K
	21	05376-05631	12400-12777	NO	
	22	05632-05887	13000-13377	NO	
	23	05888-06143	13400-13777	NO	
	24	06144-06399	14000-14377	NO	7K
	25	06400-06655	14400-14777	NO	
	26	06656-06911	15000-15377	NO	
	27	06912-07167	15400-15777	NO	
AVAILABLE FOR USER MICROPROGRAMMING	28	07168-07423	16000-16377	NO	8K
	29	07424-07679	16400-16777	NO	
	30	07680-07935	17000-17377	NO	
	31	07936-08191	17400-17777	NO	
HP DYNAMIC MAPPING SYSTEM →	32	08192-08447	20000-20377	YES	9K
HP FAST FORTRAN PROCESSOR	33	08448-08703	20400-20777	NO	
	34	08704-08959	21000-21377	YES	
	35	08960-09215	21400-21777	YES	
EXTENDED MEMORY AREA	36	09216-09571	22000-22377	YES	10K
	37	09572-09727	22400-22777	NO	
DS/1000	38	09728-09983	23000-23377	YES	
	39	09984-10239	23400-23777	NO	
SCIENTIFIC INSTRUCTION SET	40	10240-10495	24000-24377	YES	11K
	41	10496-10751	24400-24777	NO	
	42	10752-10917	25000-25377	NO	
	43	10918-11263	25400-25777	NO	
HP RESERVED	44	11264-11519	26000-26377	NO	12K
	45	11520-11775	26400-26777	NO	
	46	11776-12031	27000-27377	YES	
	47	12032-12287	27400-27777	YES	
RECOMMENDED FOR USER MICROPROGRAMMING	48	12288-12543	30000-30377	YES	13K
	49	12544-12799	30400-30777	YES	
	50	12800-13055	31000-31377	YES	
	51	13056-13311	31400-31777	NO	
	52	13312-13557	32000-32377	NO	14K
	53	13558-13823	32400-32777	NO	
	54	13824-14079	33000-33377	NO	
	55	14080-14335	33400-33777	NO	
	56	14336-14591	34000-34377	YES	15K
	57	14592-14847	34400-34777	YES	
	58	14848-15103	35000-35377	YES	
	59	15104-15359	35400-35777	YES	
	60	15360-15615	36000-36377	YES	16K
	61	15616-15871	36400-36777	NO	
	62	15872-16127	37000-37377	YES	
	63	16128-16383	37400-37777	NO	

Figure 11-3. F-Series Control Memory Map

HP 1000 E-SERIES BASE INSTRUCTION SET AND EIG/FLOATING POINT FIRMWARE

SECTION XII

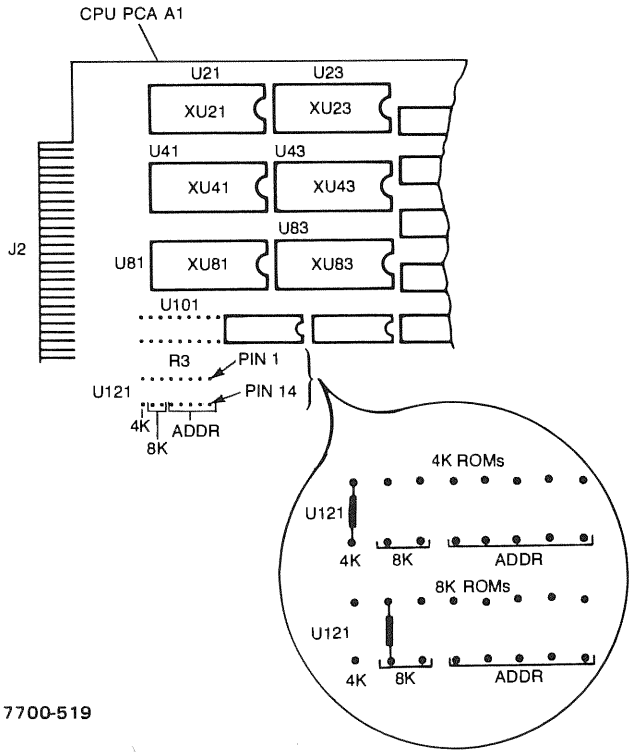
12-1. INTRODUCTION

This section provides installation and reference information for the E-Series Base Set (BS) and Extended Instruction Group/Floating Point (EIG/FP) Firmware. Additional information is provided in the manuals listed in the Preface.

12-2. DESCRIPTION

The E-Series Base Set and EIG/Floating Point ROMs (BS and EIG/FP) consist of 3 read-only-memory (ROM) integrated-circuits (IC's).

Description	HP Part No.
8K ROM IC (bits 7-0)	02113-80003
8K ROM IC (bits 15-8)	02113-80004
8K ROM IC (bits 23-16)	02113-80005



12-3. INSTALLATION

The BS and EIG/FP ROMs can be installed on the CPU board or a Firmware Expansion Module (FEM). If a FEM is available, it is recommended that the ROMs be installed here to facilitate future service.

CPU BOARD

a. Remove the CPU board as described in the appropriate Installation and Service Manual.

b. The ROMs must be installed in the following locations.

Location	ROM IC	Bits	Module No.
U21	VACANT	—	—
U41	VACANT	—	—
U81	VACANT	—	—
U23	02113-80003	7-0	0, 1, 2, 3
U43	02113-80004	8-15	
U83	02113-80005	16-23	

c. Configure the CPU board for operation with 8K ROMs.

Only the 8K jumper nearest the 4K jumper must be in (pins 7 and 10 of IC location U121). All other jumpers must be out. The silk screen indicating a second 8K jumper (pins 6 and 11) is in error, and this jumper must be out.

d. Install the CPU board as described in the appropriate Installation and Service Manual.

e. Perform the verification as described below.

FIRMWARE EXPANSION MODULE

a. Refer to section II of this manual for the FEM removal procedure (if necessary).

b. The ROMs can be installed in any available socket set on the FEM. For example, assume we are going to use SET A.

Location	ROM IC
A1	02113-80003
A2	02113-80004
A3	02113-80005

c. Configure SWA for 8K ROMs modules 0, 1, 2, 3. Refer to figure 2-1 and table 2-1.

All unused socket sets must have switch S1 closed.

SWA

Switch	Setting
S1	1
S2	0
S3	1
S4	0
S5	1
S6	0
S7	0
S8	0
S9	0
S10	X (Don't care)

d. Install the FEM board.

e. Perform the verification as described below.

12-4. VERIFICATION

INSTALLATION

After installing the ROMs, verify proper installation by running the firmware self test.

The base set includes three tests that quickly test the computer and memory. These firmware self-tests are not designed as a substitute for more complex software diagnostics and it may frequently be the case that you require a more thorough and detailed testing than provided by these standard self-test routines.

Test 1 tests most of the computer registers and functions. This test will not alter or destroy the contents of any working register or memory. An error condition will set all display register indicator bits (A, B, M, T, P, S) and the overflow register. The execution time is negligible.

Test 2 is a fast microprogrammed memory test that checks the presently enabled memory space (up to 32k words). The microprogram reads each memory location, complements the data and writes it back, reads it, compares it to expected data, then complements it and writes it back into memory. The execution time is negligible and is non-destructive to memory data. An error condition is usually accompanied by a parity error indication and will set all display register indicator bits and clear the overflow register. The A-register will contain the expected (good) data, the B-register will contain the actual (bad) data, and the M-register will contain the logical memory location of the failure.

Test 3 is a significantly more sophisticated microprogrammed memory test. All memory installed in the computer will be tested. Execution time is dependent on the amount of memory installed; approximately one second per 32k words. The display register will increment as each 32k words of memory are tested. Error reporting is the same as in Test 2 except the S-register will contain the number of the 32k words where the memory failure occurred.

On a cold power-up (as described below), Tests 1 and 3 will each be executed once. Pressing the IBL/TEST switch on the operator panel will not only perform the loader function, it will also cause the execution of Tests 1 and 2.

Executing the octal instruction 100000 via the INSTR STEP switch on the operator panel with the LOCK/OPERATE switch in the OPERATE position will execute Tests 1 and 3 once. The information contained in the S-register (when selected) will be the final background pattern used to test memory. This may also be used to easily load the entire memory with the same bit pattern. *While* the tests are executing, the LOCK/OPERATE switch may be set to the LOCK position and the microprogrammed self-tests will loop continuously until the LOCK/OPERATE switch is returned to the OPERATE position. A memory failure, of course, will terminate the test and report the error.

To check most computer registers and functions and all physical memory, perform the cold power-up procedure as follows:

a. Set ~ POWER switch to OFF. If computer is equipped with an optional power fail recovery system, set BATTERY switch to OFF.

b. Set the LOCK/OPERATE switch to OPERATE. Wait approximately six seconds and then set ~ POWER switch to ON.

c. Set BATTERY switch to INT (if installed).

d. The self-test will begin execution and the Display Register can be observed incrementing if a dynamic mapping system (DMS) is installed.

e. Upon successful completion, the T-register will automatically be selected for display.

f. If a computer failure is detected, the Display Register, all six working register indicators (A, B, M, T, P, S), and the OVERFLOW indicator are lighted. Refer to the appropriate Installation and Service manual for troubleshooting procedure.

g. If a memory failure is detected, the Display Register, and all six working register indicators (A, B, M, T, P, S) are lighted and the OVERFLOW indicator is not lighted. To isolate the memory failure, refer to the appropriate Memory Systems Installation and Service Manual.

To execute tests 1 and 3 once from the operator panel:

a. Store 100000 (octal) in the A-register.
b. Store 0 in the P-register.
c. Press PRESET.
d. Press INSTR STEP.

Upon successful completion, the T-register will automatically be selected for display. A failure will result in the conditions indicated in steps f and g above.

OPERATION

To verify operation of the CPU and all Base Set instructions, refer to the Diagnostic Configurator Reference Manual (part no. 02100-90157), Table A-1 or A-2, and run the appropriate instruction group diagnostic.

Description	Manual	Absolute Binary No.
Memory Reference Instruction Group	02100-90218	24315-16001
Alter Skip Instruction Group	02100-90211	24316-16001
Shift Rotate Instruction Group	02100-90212	24317-16001
EAU Instruction Group	02100-90214	24319-16001
Floating Point Instruction Group	24320-90001	24320-16001
I/O Instruction Group/I/O Extender	02100-90213	24318-16001
Extended Instruction Group (Index)	12943-90004	12943-16002
Extended Instruction Group (Word, Byte, Bit)	12943-90004	12943-16001

HP 1000 F-SERIES BASE INSTRUCTION SET AND EIG/FLOATING POINT FIRMWARE

SECTION XIII

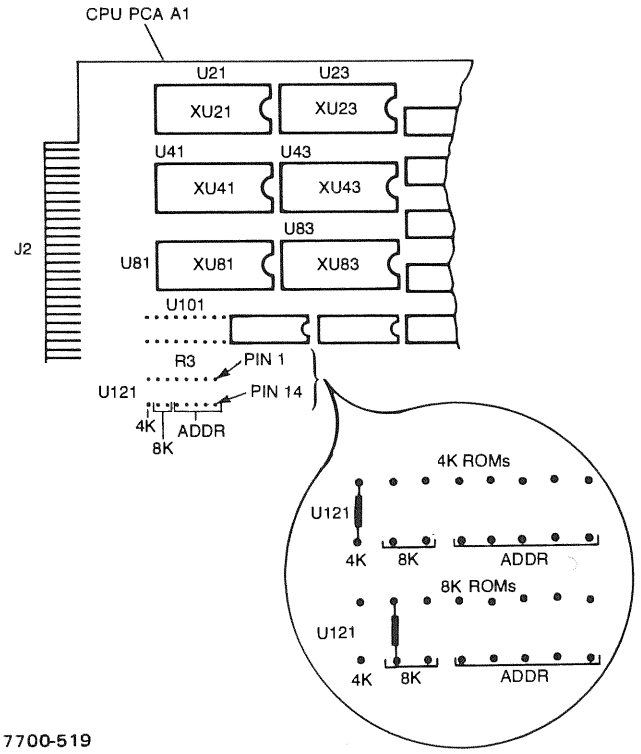
13-1. INTRODUCTION

This section provides installation and reference information for the F-Series Base Set (BS) and Extended Instruction Group/Floating Point (EIG/FP) Firmware. Additional information is provided in the manuals listed in the Preface.

13-2. DESCRIPTION

The F-Series Base Set and EIG/Floating Point ROMs (BS and EIG/FP) consist of 3 read-only-memory (ROM) integrated circuits (IC's).

Description	HP Part No.
8K ROM IC (bits 7-0)	02117-80001
8K ROM IC (bits 15-8)	02117-80002
8K ROM IC (bits 23-16)	02117-80003



7700-519

13-3. INSTALLATION

The BS and EIG/FP ROMs can be installed on the CPU board or a Firmware Expansion Module (FEM). If a FEM is available, it is recommended that the ROMs be installed here to facilitate future service.

CPU BOARD

a. Remove the CPU board as described in the appropriate Installation and Service Manual.

b. The ROMs must be installed in the following locations.

Location	ROM IC	Bits	Module No.
U21	VACANT	—	—
U41	VACANT	—	—
U81	VACANT	—	—
U23	02117-80001	7-0	0, 1, 2, 3
U43	02117-80002	15-8	
U83	02117-80003	23-16	

c. Configure the CPU board for operation with 8K ROMs.

Only the 8K jumper nearest the 4K jumper must be in (pins 6 and 9 of IC location U121). All other jumpers must be out. The silk screen indicating a second 8K jumper is in error.

d. Install the CPU board as described in the appropriate Installation and Service Manual.

e. Perform the verification as described below.

FIRMWARE EXPANSION MODULE

a. Refer to section II of this manual for the FEM removal procedure (if necessary).

b. The ROMs can be installed in any available socket set on the FEM. For example, assume we are going to use Set A.

Location	ROM IC
A1	02117-80001
A2	02117-80002
A3	02117-80003

c. For 8K ROM configuration, configure SWA for modules 0, 1, 2, 3. Refer to figure 2-1 and table 2-1 for reference.

All unused socket sets must have switch S1 closed.

SWA

Switch	Setting
S1	1
S2	0
S3	1
S4	0
S5	1
S6	0
S7	0
S8	8
S9	0
S10	X (Don't care)

d. Install the FEM board.

e. Perform the verification as described below.

13-4. VERIFICATION

INSTALLATION

After installing the ROMs, verify proper installation by running the firmware self test.

CPU AND MEMORY. The base set includes three tests that quickly test the computer and memory. These firmware self-tests are not designed as a substitute for more complex software diagnostics and it may frequently be the case that you require a more thorough and detailed testing than provided by these standard self-test routines.

Test 1 tests most of the computer registers and functions. This test will not alter or destroy the contents of any working register or memory. An error condition will set all display register indicator bits (A, B, M, T, P, S) and the overflow register. The execution time is negligible.

Test 2 is a fast microprogrammed memory test that checks the presently enabled memory space (up to 32k words). The microprogram reads each memory location, complements the data and writes it back, reads it, compares it to expected data, then complements it and writes it back into memory. The execution time is negligible and is nondestructive to memory data. An error condition is usually accompanied by a parity error indication and will set all display register indicator bits and clear the overflow register. The A-register will contain the expected (good) data, the B-register will contain the actual (bad) data, and the M-register will contain the logical memory location of the failure.

Test 3 is a significantly more sophisticated microprogrammed memory test. All memory installed in the computer will be tested. Execution time is dependent on the amount of memory installed; approximately one second per 32k words. The display register will increment as each 32k words of memory are tested. Error reporting is the same as in Test 2 except the S-register will contain the number of the 32k words where the memory failure occurred.

On a cold power-up (as described below), Tests 1 and 3 will each be executed once. Pressing the IBL/TEST switch on the operator panel will not only perform the loader function, it will also cause the execution of Tests 1 and 2.

Executing the octal instruction 100000 via the INSTR STEP switch on the operator panel with the LOCK/OPERATE switch in the OPERATE position will execute Tests 1 and 3 once. The information contained in the S-register (when selected) will be the final background pattern used to test memory. This may also be used to easily load the entire memory with the same bit pattern. *While* the tests are executing, the LOCK/OPERATE switch may be set to the LOCK position and the microprogrammed self-tests will loop continuously until the LOCK/OPERATE switch is returned to the OPERATE position. A memory failure, of course, will terminate the test and report the error.

To check most computer registers and functions and all physical memory, perform the cold power-up procedure as follows:

a. Set ~ POWER switch to OFF. If computer is equipped with an optional power fail recovery system, set BATTERY switch to OFF.

b. Set the LOCK/OPERATE switch to OPERATE. Wait approximately six seconds and then set ~ POWER switch to ON.

c. Set BATTERY switch to INT (if installed).

d. The self-test will begin execution and the Display Register can be observed incrementing if a dynamic mapping system (DMS) is installed.

e. Upon successful completion, the T-register will automatically be selected for display.

f. If a computer failure is detected, the Display Register, all six working register indicators (A, B, M, T, P, S), and the OVERFLOW indicator are lighted. Refer to the appropriate Installation and Service manual for troubleshooting procedure.

g. If a memory failure is detected, the Display Register, and all six working register indicators (A, B, M, T, P, S) are lighted and the OVERFLOW indicator is not lighted. To isolate the memory failure, refer to the appropriate Memory Systems Installation and Service Manual.

To execute tests 1 and 3 once from the operator panel:

a. Store 100000 (octal) in the A-register.

b. Store 0 in the P-register.

c. Press PRESET.

d. Press INSTR STEP.

Upon successful completion, the T-register will automatically be selected for display. A failure will result in the conditions indicated in steps f and g above.

FLOATING POINT. The F-Series computer includes a firmware self-test for testing the floating point PCA's. This self-test detects obvious trouble symptoms but is not intended as a substitute for the more comprehensive software diagnostic. (The self-test can only be executed in the single-step front panel mode; if entered in the run-mode, a NOP is performed.) To execute the firmware self-test, proceed as follows:

a. Store 105004 (octal) in the A-register.

b. Store 0 in the P-register and press PRESET. If the OVFL light remains on, check that the FPP-MPP cable is installed correctly (not twisted). Otherwise, a defective CPU, floating point PCA, or FPP is indicated. Use software diagnostics for further troubleshooting.

c. Press INSTR STEP.

d. A 102077 (octal) in the display register (S) indicates successful completion. If 10200X (octal) is returned in the display register, the firmware test failed and the halt code is interpreted as shown in table 13-1. If the firmware test returns an error halt code, use software diagnostics for further troubleshooting.

Table 13-1. Floating Point Self-Test Error Halts

HALT	PROBABLE PROBLEM
102001	a. Power not supplied to floating-point PCA's. b. FPP-MPP cable not properly connected. Refer to Installation and Reference Manual. c. Floating point CONTROL PCA not installed or not connected properly. d. If A-register not 177777 (octal) and B-register not 0, then floating point ROMs defective.
102002	a. If A- and B-registers equal 0 and OVFL lit, then FPP-MPP cable twisted. b. If A- and B-registers equal 177777 (octal), then floating point ARITH PCA not connected properly or CPU-MPP cable not connected.
102003	a. Floating point PCA, ALU PCA, or cables defective.
102004	a. Floating point PCA, ALU PCA, or cables defective.
XXXXXX	a. If display register does not indicate any of the above halts, either the floating point ROMs are not present, ROMs are defective, or computer is defective.

OPERATION

To verify operation of the CPU and all Base Set Instructions, and HFPP, refer to the Diagnostic Configurator Reference Manual (part no. 02100-90157), Table A-1 or A-2, and run the appropriate instruction group diagnostic.

Description	Manual	Absolute Binary No.
Memory Reference Instruction Group	02100-90218	24315-16001
Alter Skip Instruction Group	02100-90211	24316-16001
Shift Rotate Instruction Group	02100-90212	24317-16001
EAU Instruction Group	02100-90214	24319-16001
I/O Instruction Group/I/O Extender	02100-90213	24318-16001
Extended Instruction Group (Index)	12943-90004	12943-16002
Extended Instruction Group (Word, Byte, Bit)	12943-90004	12943-16001
F-Series FPP/SIS/FFP	12740-90004	12740-16001

HP 12823F F-SERIES ENHANCEMENT UPGRADE KIT

APPENDIX A

A-1. DESCRIPTION

The HP 12823F F-Series Enhancement Upgrade Kit allows the customer to upgrade a F-Series Computer (2111F or 2117F) which was shipped with a serial prefix less than 1920 with the enhanced Base Set, enhanced FFP, and enhanced SIS ROMs. The 12823F product consists of the eighteen read-only-memory (ROM) integrated circuits (ICs) which are listed under the designation "New Part No." below.

BASE INSTRUCTION SET

Description	Old Part No.	Location
4K ROM IC (bits 7-0)	12740-80014	A1U21
4K ROM IC (bits 15-8)	12740-80015	A1U41
4K ROM IC (bits 23-16)	12740-80016	A1U81
4K ROM IC (bits 7-0)	12740-80011	A1U23
4K ROM IC (bits 15-8)	12740-80012	A1U43
4K ROM IC (bits 23-16)	12740-80013	A1U83

Description	New Part No.	Location
8K ROM IC (bits 7-0)	02117-80001	A1U23
8K ROM IC (bits 15-8)	02117-80002	A1U43
8K ROM IC (bits 23-16)	02117-80003	A1U83
	VACANT	A1U21
	VACANT	A1U41
	VACANT	A1U81

SCIENTIFIC INSTRUCTION SET (SIS)

Description	Old Part No.	New Part No.
4K ROM IC (bits 7-0)	12823-80001	12823-80013
4K ROM IC (bits 15-8)	12823-80002	12823-80014
4K ROM IC (bits 23-16)	12823-80003	12823-80015
4K ROM IC (bits 7-0)	12823-80004	12823-80016
4K ROM IC (bits 15-8)	12823-80005	12823-80017
4K ROM IC (bits 23-16)	12823-80006	12823-80018

FAST FORTRAN PROCESSOR (FFP)

Description	Old Part No.	New Part No.
1K ROM IC (bits 3-0)	13306-80013	5090-1615
1K ROM IC (bits 7-4)	13306-80014	5090-1616
1K ROM IC (bits 11-8)	13306-80015	5090-1617
1K ROM IC (bits 15-12)	13306-80016	5090-1618
1K ROM IC (bits 19-16)	13306-80017	5090-1619
1K ROM IC (bits 23-20)	13306-80018	5090-1620
4K ROM IC (bits 7-0)	5090-0589	5090-1621
4K ROM IC (bits 15-8)	5090-0590	5090-1622
4K ROM IC (bits 23-16)	5090-0591	5090-1623

A-2. INSTALLATION

a. For installation of the Base Instruction Set, refer to section XIII of this manual.

b. For installation of the Scientific Instruction Set ROMs, refer to section VIII of this manual.

c. For installation of the Fast FORTRAN Processor ROMs, refer to section VII of this manual.

d. Perform the appropriate self-test and diagnostic to verify installation and functional operation of the firmware.

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Arranged alphabetically by country

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