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BLC-80/24,-80/28
Board Level Computer

Microcomputer Systems

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BLC-80/24,-80/28
Board Level Computer
Hardware Reference Manual

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PREFACE

This manual provides technical data and user application information for the BLC-80/24 and BLC-80/28 Board Level Computers.

The material contained in this manual is for information only and is subject to change without notice.

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Chapter 1

GENERAL INFORMATION

1.1 INTRODUCTION

The BLC-80/24 and BLC-80/28 Board Level Computers are 8-bit computer systems on a single printed circuit assembly. The BLC-80/24,-80/28 board includes an 4.84 MHz 8085A-2 microprocessor unit (MPU), 48 programmable parallel I/O lines, one serial I/O port, one programmable interval timer, and one programmable interrupt controller. Sockets are provided for a maximum of 32K bytes of read only memory (ROM). The BLC-80/24 provides 4K bytes of on-board static random access memory (RAM) and BLC-80/28 provides 8K bytes of RAM.

On-board I/O capabilities are expanded via two Board Level Expansion (BLX) bus connectors on the BLC-80/24,-80/28 board. These connectors allow any of the optional expansion modules to be used on the BLC-80/24,-80/28 board. The component side of the BLC-80/28 is shown in Figure 1-1.

This manual provides information needed to operate the BLC-80/24,-80/28 Board Level Computer. For optimum application of this versatile board, read the entire manual before attempting installation and operation.

The manual is organized as follows:

Chapter 1 provides an overview of the BLC-80/24,-80/28 board.

Chapter 2 provides the physical, environmental, and electrical specifications.

Chapter 3 describes the details of operation of the BLC-80/24,-80/28 board.

Chapter 4 discusses the user selectable options and how to implement them in a system.

Chapter 5 describes how the BLC-80/24,-80/28 board interfaces with other components in a system.

Appendices contain logic diagrams, schematics and connector pin assignments for the BLC-80/24,-80/28 and an illustration incorporating tabular type information for the BLC-80/24,-80/28 jumper configurations. Also included in the Appendices is detailed information on the 8085 instruction set.

1.2 GENERAL FUNCTIONAL DESCRIPTION

The BLC-80/24,-80/28 is divided into the nine functional sections listed below. Figure 1-2 is a simplified block diagram of the BLC-80/24,-80/28. A brief discussion of these functional sections is provided in the following paragraphs. Refer to Chapter 3 for more detailed information.

1. CPU Section
2. I/O and Memory Decode Section
3. Memory
4. Interval Timer Section
5. Serial Input/Output Section
6. Parallel Input/Output Section
7. Interrupt Section
8. System Bus Interface
9. BLX Interface

1.2.1 CPU Section

The BLC-80/24,-80/28 board is controlled by an 8085A-2 microprocessor operating at 4.84 MHz. Processor support is provided by a 8224 Clock Generator/Driver and associated circuitry. The board can be jumpered to operate at 2.42 MHz, if necessary. This section provides the following functions:

1. CPU high level clocks and clock source for serial I/O timing.
2. Address, control, and data signals for I/O ports and both on-board and off-board memory.
3. Instruction decode and execution.
4. Service of interrupt requests from both on-board and off-board sources.
5. Establishment of WAIT states in response to slower memory or I/O devices.

1.2.2 I/O and Memory Decode Section

The I/O and Memory decoders decode the 8085A issued addresses. One decoder is a PROM that generates enable signals for each I/O device being addressed. Another PROM decoder is used to select the RAM.

1.2.3 Memory

Up to 64K bytes of total system memory may be directly addressed by the BLC-80/24,-80/28. Of this amount, a maximum of 36K bytes may reside on-board the BLC-80/24 (4K RAM + 32K ROM). A maximum of 40K bytes may reside on-board the BLC-80/28 (8K RAM + 32K ROM).

The on-board static RAM is implemented with 2K x 8, static RAM devices. These high-speed devices require only a +5 volt supply, and are therefore well suited for battery backup applications.

The board will accept a wide variety of ROM, PROM, and EPROM devices. Either 24-pin or 28-pin devices may be used. Refer to Chapter 4 for complete information.

1.2.4 Interval Timer Section

The on-board 8253 Programmable Interval Timer (PIT) is most often used for controlling on-board I/O and CPU interrupts. The PIT provides three independent counter outputs which may be configured to a variety of applications, including frequency output, rate generator, interval timer and real-time interrupts. One of the counters serves as the baud rate clock for the on-board 8251 Programmable Communications Interface device.

1.2.5 Serial Input/Output Section

Serial I/O operation is handled by an 8251 Programmable Communications Interface device. It provides a bi-directional serial communications channel for the BLC-80/24,-80/28. The board is configured to the RS232C standard. However, this may be converted to a current loop teletypewriter serial interface using optional equipment. Baud rates are software programmable using the on-board interval timer.

1.2.6 Parallel Input/Output Section

The BLC-80/24,-80/28 board utilizes two 8255 Programmable Peripheral Interface devices to control the six, 8-bit, parallel I/O ports. The two 8255 devices provide 48 lines for control and interchange of data with peripheral devices.

Chapter 2

SPECIFICATIONS

2.1 INTRODUCTION

This chapter describes physical, functional, environmental, and electrical specification requirements for the BLC-80/24,-80/28 board.

2.2 PHYSICAL DIMENSIONS

The BLC-80/24,-80/28 is fabricated on a 6.75-inch by 12-inch printed circuit board. Figure 2-1 illustrates an outline of the board with its dimensions.

2.3 FUNCTIONAL SPECIFICATIONS

The functional specifications for the BLC-80/24,-80/28 board are summarized in Table 2-1.

2.4 ELECTRICAL SPECIFICATIONS

Electrical specifications, consisting of DC power requirements, AC and DC characteristics, and board timing requirements are provided in the following tables and figures:

TABLE 2-1 BLC-80/24,-80/28 BOARD SPECIFICATIONS

ITEM	SPECIFICATION
CPU	8085-2
Operating Rate	4.84 MHz (default) 2.42 MHz (optional)
Single Clock Cycle	206 ns (at 4.84 MHz)
Basic Instruction Cycle (four clock cycles)	824 ns
WORD SIZE	
Instruction	8, 16, or 24 bits
Data	8 bits
Address	16 bits
SYSTEM CLOCK	9.68 MHz
RAM ACCESS TIME	100 ns maximum (Valid data out from read command) 150 ns maximum (ALE to valid data).
MEMORY CAPACITY	64K Bytes (65,536 bytes)
Maximum On board ROM/PROM	32K Bytes (32,768 bytes)
Maximum On board RAM	
BLC-80/24	4K Bytes (4,096 bytes)
BLC-80/28	8K Bytes (8,192 bytes)
MEMORY ADDRESSING	All notations in hexadecimal
(factory configuration)	
On-board RAM	
BLC-80/24	3000-3FFF
BLC-80/28	3000-4FFF
On-board ROM/PROM	0-0FF
ON-BOARD I/O ADDRESSING	
BLX Connector J5	C0-CF
BLX Connector J6	F0-FF
Interrupt Controller	D8 or D9 ICW1, OCW2, OCW3, Status, and Poll D9 or DB ICW1, OCW2, OCW4, and Masks

TABLE 2-2 BLC 80/24,-80/28 DC POWER REQUIREMENTS

VOLTAGES	CURRENT MAXIMUM (IMAX)	CURRENT MINIMUM (IMIN)
+5 Vdc (+ or -5%) +12 Vdc (+ or -5%) -12 Vdc (+ or -5%)	IMAX = 3.95 A IMAX = 40 MA IMAX = 20 MA	IMIN = 3.17 A

IMAX -- Assumes that four 2764 PROMs are present and that eight optional termination networks have been installed in the parallel interface.

IMIN -- Assumes that the 2764 PROMs and optional termination networks are not present.

TABLE 2-3 (cont.)

SIGNALS	SYMBOL	PARAMETER DESCRIPTIONS	TEST CONDITIONS	MIN	MAX	UNITS
INTO/-INT7/	V_{IL}	Input Low Voltage			0.80	V
	V_{IH}	Input High Voltage		2.0		V
	I_{IL}	Input Current at Low V	V_{IN} = 0.4V		-0.2	mA
	I_{IH}	Input Current at High V	V_{IN} = 2.4V		30	uA
	C_L*	Capacitive Load			18	pF
BPRN/	V_{IL}	Input Low Voltage			0.80	V
	V_{IH}	Input High Voltage		2.0		V
	I_{IL}	Input Current at Low V	V_{IN} = 0.45V		-0.5	mA
	I_{IH}	Input Current at High V	V_{IN} = 2.4V		100	pF
	C_L*	Capacitive Load			15	pF
AACK/	V_{IL}	Input Low Voltage			0.8	V
	V_{IH}	Input High Voltage		2.0		V
	I_L	Input Current at Low V	V_{IN} = 0.4V		-2.0	mA
	I_{IH}	Input Current at High V	V_{IN} = 2.4V		-1.0	mA
	C_L*	Capacitive Load			18	pF
BUSY/ (OPEN COLLECTOR)	V_{OL}	Output Low Voltage	I_{OL} = 32 mA		0.5	V
	C_L*	Capacitive Load			20	pF
INIT/ (SYSTEM RESET)	V_{OL}	Output Low Voltage	I_{OL} = 56 mA		0.5	V
	V_{OH}	Output High Voltage	OPEN COLLECTOR			
	V_{IL}	Input Low Voltage			0.8	V
	V_{IH}	Input High Voltage		2.0		V
	I_{IL}	Input Current at Low V	V_{IN} = .4V		-3.0	mA
	I_{IH}	Input Current at High V	V_{IN} = 2.4V		-1.0	mA
	C_L*	Capacitive Load			18	pF
BCLK/	V_{OL}	Output Low Voltage	I_{OL} = 59.5 mA		0.5	V
	V_{OH}	Output High Voltage	I_{OH} = -3 mA	2.7		V
	V_{IL}	Input Low Voltage			0.8	V
	V_{IH}	Input High Voltage		2.0		V
	I_{IL}	Input Current at Low V	V_{IN} = 0.45V		-0.5	mA
	I_{IH}	Input Current at High V	V_{IN} = 5.25V		100	uA
	C_L*	Capacitive Load			15	pF

* Capacitive load values are approximations.

TABLE 2-5 BLC-80/24,-80/28 BOARD PARALLEL I/O DC CHARACTERISTICS (CONNECTORS J1/J2)

SIGNALS	SYMBOL	PARAMETER DESCRIPTIONS	TEST CONDITIONS	MIN	MAX	UNITS
PORTS E4 AND	V_{OL}	Output Low Voltage	I_{OL} = 32 mA		0.5	V
E8	V_{OH}	Output High Voltage	I_{OH} = -5 mA	2.4		V
BIDIREC-	V_{IL}	Input Low Voltage			.90	V
TIONAL	V_{IH}	Input High Voltage		2.0		V
DRIVERS	I_{IL}	Input Current at Low V	V_{IN} = 0.45		-0.2	mA
	C_L*	Capacitive Load			18	pF
8255A	V_{OL}	Output Low Voltage	I_{OL} = 1.7 mA		0.45	V
DRIVER/	V_{OH}	Output High Voltage	I_{OH} = -200 uA	2.4		V
RECEIVER	V_{IL}	Input Low Voltage			0.8	V
	V_{IH}	Input High Voltage		2.0		V
	I_{IL}	Input Current at Low V	V_{IN} = 0.45		10	uA
	I_{IH}	Input Current at High V	V_{IN} = 5.0		10	uA
	C_L*	Capacitive Load			10	pF

* Capacitive load values are approximations.

TABLE 2-6 (cont.)

PARAMETER	DESCRIPTION	OVERALL		READ		WRITE		REMARKS
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{DXL}	Read data setup to XACK			-97				
t_{XKH}	XACK hold time	0		0	65	0	65	
t_{CPM} (tppd)	Parallel Priority Resolution		35					
t_{BWS}	Bus clock low or high interval	35						Supplied by system
t_{BS}	BPRN to BCLK setup time	23						
t_{DBY}	BCLK to BUSY		55					
t_{NOD} (t_{PNO})	BPRN to BPRO delay		30					
t_{BCY}	Bus clock period	102	104					From BLC-80/24 when terminated
t_{BW}	Bus clock low or high interval	35	74					From BLC-80/24 when terminated
t_{INIT} (t_{INT})	Initialization width	10ms						After all voltages have stabilized
t_{CBRQ}	BCLK to CBRQ delay	50						

TABLE 2-7 (cont.)

PARAMETER	DESCRIPTION	OVERALL		READ		WRITE		REMARKS
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{CPM} (tppd)	Parallel Priority Resolution		35					
t_{BWS}	Bus clock low or high interval	35						Supplied by system
t_{BS}	BPRN to BCLK setup time	23						
t_{DBY}	BLCK to BUSY delay		55					
t_{NOD} (t_{PNO})	BPRN to BPRO delay		30					
t_{BCY}	Bus clock period	102	104					From BLC-80/24 when terminated
t_{BW}	Bus clock low or high interval	35	74					From BLC-80/24 when terminated
t_{INIT} (t_{INT})	Initialization width	10ms						After all voltages have stabilized
t_{CBRQ}	BCLK to CBRQ delay		50					

Chapter 3

DETAILED FUNCTIONAL DESCRIPTION

3.1 INTRODUCTION

This chapter provides a description of each major functional block on the BLC-80/24,-80/28 board. Emphasis is placed on providing information on how the functional blocks interact during each mode of operation. Since several programmable devices reside on the BLC-80/24,-80/28 board, applicable programming information for these devices are also given. This chapter does not provide detailed descriptions of the internal operation of each Large-Scale-Integration (LSI) device on the board. Logic diagrams may be referred to in Appendix A.

3.1.1 BLC-80/24,-80/28 Signal Notation

Throughout this manual, and particularly in this chapter, various signals are referred to by their mnemonic terms. Some of these terms end with a slash (/). Table 3-1 outlines the signal notation for mnemonic terms ending with a slash and for those without the slash.

3.2 OVERALL BLOCK DIAGRAM DESCRIPTION

Conceptually, the BLC-80/24,-80/28 board may be divided into the following nine major functional blocks:

1. CPU Section (See section 3.2.1)
2. I/O AND Memory Decode (See section 3.2.2)
3. Memory (See section 3.2.3)
4. Interval Timer (See section 3.2.4)
5. Serial I/O (See section 3.2.5)
6. Parallel I/O (See section 3.2.6)
7. Interrupts (See section 3.2.7)
8. System Bus Interface (See section 3.2.8)
9. BLX Interface (See section 3.2.9)

These functional blocks are described in subsequent paragraphs in this chapter. Other functions such as buffering and the data/address buses are mentioned when appropriate throughout this chapter.

3.2.1 CPU Section

The CPU section consist of the 8085A-2 Microprocessor Unit (MPU), the 8224 clock generator, and an eight-bit latch. The 8224 clock generator is used to supply the clock input and RESET signal to the MPU. The clock signal can be either 9.69

MHz or 4.84 MHz. The eight-bit latch output is combined with the eight bit output from the 8085A-2 MPU address line to form the 16-bit address bus.

The operation details of the 8085A-2 are well documented. For this reason, no attempt is made to describe the 8085A-2 in detail. However, since many functions of the BLC-80/24 and BLC-80/28 boards are based on the operation of the 8085A-2 MPU, a brief review of the MPU's processing operation and its response to interrupts and hold requests are provided in the following paragraphs. The instruction set for the 8085A-2 MPU is contained in Appendix D.

The 8085A-2 MPU (or CPU) performs system processing functions and generates the address and control signals required to access memory and I/O devices. The AD0-AD7 pins (refer to Appendix A, sheet 3) are used to multiplex the eight-bit input/output data and the lower eight bits of the address. During the first part of a machine cycle, for example, the lower eight bits of the address are strobed into Latch U72 by the Address Latch Enable (ALE) signal; the outputs of U72 are combined with the upper eight bits of the address to form the 16-bit address bus. During the remainder of the machine cycle, AD0-AD7 pins of the CPU are used for data input/output.

Initialization

When power is applied in a start-up sequence, the contents of the 8085A-2 CPU program counter, instruction register, and interrupt enable flip-flop are subject to random factors and cannot be predicted. For this reason, a power-up sequence is used to set the CPU, bus controller, and I/O ports to a known internal state.

The 8224 clock generator produces the RESET signal at power-up time (Appendix A, sheet 3). This signal is routed to the CPU and throughout the board. If power is already on, the RESET signal may be generated by the AUX RESET/ signal (front panel switch closure). The RESET signal is routed off-board via P1-14, as INIT/. Notice that INIT/ may also be an input from P1-14.

The RESET signal clears the CPU program counter, instruction register, and interrupt enable flip-flop; sets the parallel I/O ports to the input mode; resets the serial I/O port to the "idle" mode; resets the bus controller; and via the INIT/ signal, sets the system to a known internal state.

Clock Signals

The 8085A-2 MPU internally divides the 9.68 MHz clock input by two to develop the timing requirements for the various time-dependent functions. These functions are described in the following paragraphs.

Basic Machine Cycle

During a machine cycle (see Table 3-2), several distinct CPU activities occur. Each activity occurs within an interval of time called a "state". A state is the smallest unit of CPU operation; it is the interval between two successive clock pulses. During this interval, the CPU may move information on or off the address and data buses, or it may send or receive signals on the control lines. Each activity performed during a state forms a small part of the machine cycle, just as a machine cycle forms part of the instruction cycle.

The 8085A-2 CPU may pass through three to five active states in every machine cycle and one or more optional Wait states. The number of states in a particular machine cycle depends on the type of machine cycle and the number of activities that must be performed. Each state in a machine cycle is marked by a particular behavior; thus, each state has a unique label. Refer to Table 3-3.

The relationship between instruction cycles, and T-states is illustrated in Figure 3-1. The execution of a store Accumulator Direct (STA), involving on-board memory, is illustrated in this figure. Note that in this instruction, the opcode fetch (designated M1) requires four T-states, and the remaining three cycles each require three T-states.

Opcode fetch is the only machine cycle requiring more than three T-states, as the CPU must interpret the requirements of the opcode fetched during states T1 through T3 to decide what must be done in the remaining state(s). The timing relationship of a typical opcode fetch is illustrated in Figure 3-2.

At the beginning of T1 in every machine cycle the CPU pulls IO-/M low, signifying that the machine cycle is a memory reference operation. The high order bits of the program counter are placed on address lines A9-A15. The low order bits of the program counter are placed on AD0-AD7 (PCL) and the Address Latch Enable (ALE) is then activated to latch these low order address bits. These address bits remain true only for one clock cycle. After that, AD0-AD7 go to their high-impedance state (as indicated by a dashed line). The Address Latch Enable (ALE) is then activated.

At the beginning of T2 the RD/ line is pulled low, enabling the addressed memory device, which then drives the AD0-AD7 address lines. After a period of time determined by the access time of the addressed memory device, the valid data will be present on the AD0-AD7 lines.

During the T3 state, the CPU loads the data on AD0-AD7 into its instruction register and drives RD/ high, disabling the addressed memory device.

TABLE 3-3 BIT STATUS

MACHINE STATE	STATUS AND BUSES				CONTROL		
	S1,S0	IO/M	A_8-A_{15}	AD_0-AD_7	RD,WR	INTA	ALE
T_1	X	X	X	X	1	1	1†
T_2	X	X	X	X	X	X	0
T_{wait}	X	X	X	X	X	X	0
T_3	X	X	X	X	X	X	0
T_4	1	0	X	TS	1	1	0
T_5	1	0	X	TS	1	1	0
T_6	1	0	X	TS	1	1	0
T_{reset}	X	TS	TS	TS	TS	1	0
T_{halt}	0	TS	TS	TS	TS	1	0
T_{hold}	X	TS	TS	TS	TS	1	0

NOTE: 0 = LOGIC "0" 1 = LOGIC "1" TS = HIGH IMPEDANCE
X = UNSPECIFIED
† ALE NOT GENERATED DURING 2ND AND 3RD MACHINE CYCLES OF DAD INSTRUCTION

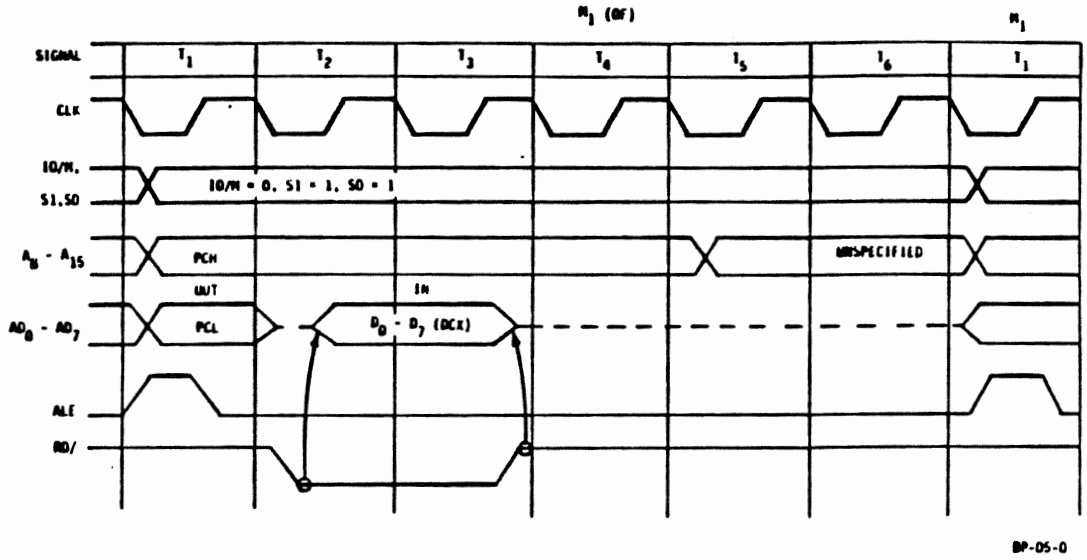


Figure 3-2 Opcode Fetch machine Cycle

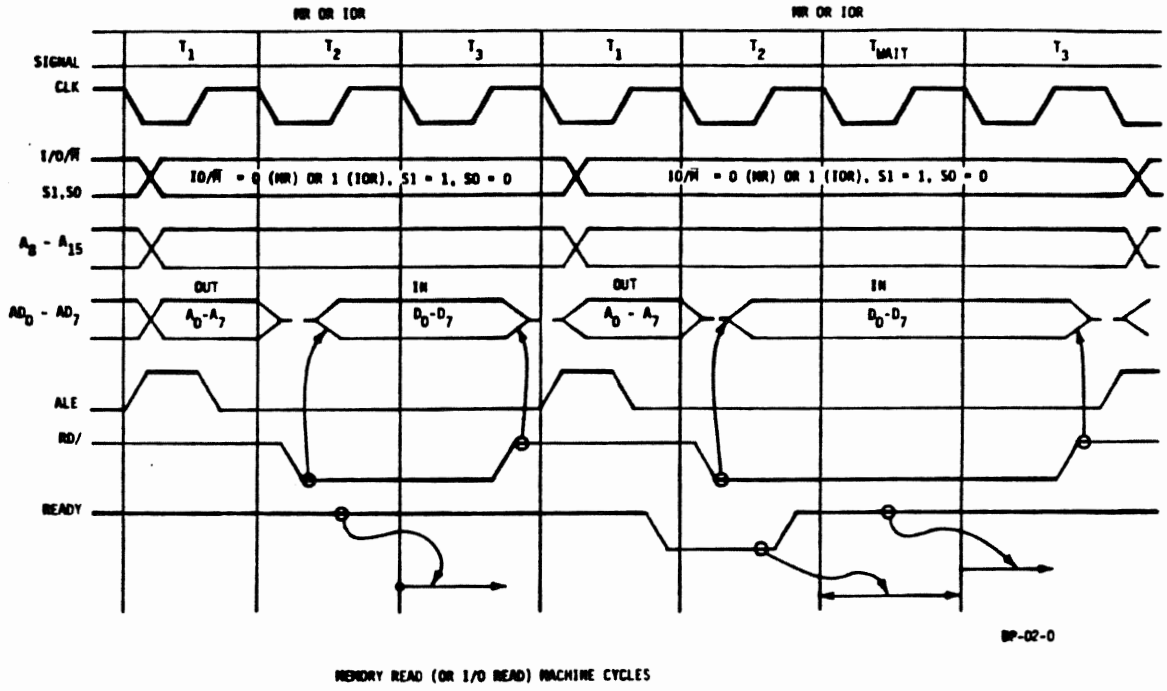


Figure 3-3 Memory or I/O Read Machine Cycle

During the first clock cycle (T1), the lower eight bits (A0-A7) of the memory or I/O address (depending on the machine cycle in progress) are output by the CPU onto AD0-AD7. During T2 and T3 cycles, the AD0-AD7 lines become the data bus. During T1, the Address Latch Enable (ALE) is issued by the CPU. The trailing edge of this signal strobes the lower eight address bits into the demultiplexer and RAM/IO/Timer. The address bytes from the demultiplexer are placed on the address bus along with the high order address bits (A8-AF). This 16-bit address bus (AD0-AD7 and A8-AF) is distributed to address ROM/EPROM and RAM.

8085A-2 Interrupt Handling

The 8085A-2 CPU contains five interrupt inputs; three maskable, and one general purpose. Each of these interrupts (except the general purpose interrupt) causes the internal execution of a RESTART command, if the interrupts are enabled and the interrupt mask is NOT set.

INTERRUPT	PRIORITY	RESTART ADDRESS*	TRIGGER
TRAP	1	24H	Rising edge and high level until sampled.
RST 7.5	2	3CH	Rising edge (latched)
RST 6.5	3	34H	High level until sampled.
RST 5.5	4	2CH	High level until sampled.
INTR	5	**	High level until sampled.

* The PC is pushed on the stack prior to branching to the RESTART address.

** The address branched to depends on the instruction provided to the CPU when the interrupt is acknowledged.

Interrupt Acknowledge Timing

Figure 3-5 illustrates the CPU timing in response to the INTR input being driven high by PIC U23 (Appendix A, sheet 9 - assuming the CPU interrupt enable flip-flop has been set by a previously executed Enable Interrupt instruction). The status of the TRAP, RST 7.5, RST 6.5, RST 5.5, and INTR inputs are sampled during CLK of the T-state immediately preceding T1 of M1. If INTR was the only valid interrupt, the CPU clears its interrupt enable flip-flop and enters the Interrupt Acknowledge (INA) machine cycle. With two exceptions, the INA machine cycle is identical with the Opcode Fetch (OF) machine cycle. The first exception

is that IO/M = 1, which signifies that the opcode fetched will be from an I/O device. The second exception is that INTA is asserted instead of RD. Although the contents of CPU program counter are sent out on the address lines, the address lines are ignored.

When INTA is asserted, the PIC provides a CALL instruction which causes the CPU to push the contents of the program counter onto the stack before jumping to a new location. After receiving the CALL opcode, the CPU performs a second INA machine cycle (M2) to access the second byte of the CALL instruction from the PIC. The timing of M2 is identical with M1 except that M2 has three T-states. M2 is followed by M3 to access the third byte of the CALL instruction. When all three bytes have been received, the CPU executes the instruction. The CPU inhibits the incrementing of the program counter during the three INA cycles so that the correct program counter value can be pushed onto the stack during M4 and M5.

During M4 and M5, the CPU performs Memory Write (MW) machine cycles to write (push) the contents of the program counter onto the top of the stack. The CPU then places the two bytes accessed during M2 and M3 into the upper and lower bytes of the program counter. This has the same effect as jumping the execution of the program to the location specified by the CALL instruction.

After the interrupt service routine is executed, the CPU pops the stack and loads it into the program counter, and resumes system operation at the point of the interrupt. (It is the programmer's responsibility to ensure that the interrupt enable flip-flop is set before returning from the service routine.)

3.2.2 I/O And Memory Decode

When the 8085A-2 CPU issues an address, the I/O and memory decode circuitry must determine which device or memory location is being addressed. This decoding is primarily done with two custom programmed PROMs (U67 and U48, located on Appendix A, sheet 4 and sheet 6), a 2-4 decoder (U56), and 3-8 decoder (U57, located on Appendix A, sheet 5), and support logic gates. The I/O and memory decoding operations are discussed in the following paragraphs.

Memory Decode

During an on-board RAM read/write cycle, address lines AA through AC are decoded by U57 (Appendix A, sheet 5) to provide one of eight possible RAM chip select signals. Since each RAM device is 2K x 8, only one device will be selected at any one time.

If no on-board RAM address is decoded by the 74S573 (U48, sheet 6) the RAMACK/ signal is false and the bus controller will assume an off-board read/write request has been made. The off-board request will be acknowledged by XACK/ (P1-23, sheet 10) which subsequently produces the MULTIBUS RDY/ signal. This in turn, provides the CPU ready signal.

IOSYNC/ (sheet 4) will furnish the READY signal, via the wait-state circuitry (sheet 3). If the CPU is operating at the slower speed (2.42 MHz), IOSYNC/ will provide a READY signal without a wait state, via jumper 156-157 (sheet 3).

If the addressed, on-board I/O device is on an Expansion Module board, the signal IOASYNC/ will supply the required READY signal (via wait-state circuitry). A minimum of one wait-state is required when accessing an Expansion Module board.

An off-board I/O operation is characterized by the signal ONBDIO being false (ONBDIO = 0), and the absence of any on-board acknowledge (ACK, sheet 3) signal. These two conditions will allow the bus controller (U60, sheet 10) to institute a bus cycle, provided the command signal (CMD, sheet 3) is true. At the same time, the MULTIBUS data receivers (U64, sheet 10) will be turned-on. If an XACK/ signal is not received within 10 ms of command time, the failsafe timer will produce the required READY signal (U28, sheet 3).

I/O Addressing

The on-board 8085A-2 CPU communicates with the programmable devices through a sequence of I/O read and I/O write commands. Each device has a specific fixed (dedicated) address, or group of addresses, through which commands and or data are issued or accepted. All of these fixed on-board I/O addresses are listed in Table 3-4. In addition to the board's programmable I/O devices, certain other functions have specific addresses assigned to them. These addresses are also included in the table.

3.2.3 Memory

The BLC-80/24,-80/28 board memory consists of RAM and ROM/PROM/EPROM devices. These can be used in various addressing schemes. Provisions are made on the basic BLC-80/24,-80/28 board for installation of up to 32K bytes of on-board Erasable Programmable Read Only Memory (EPROM). Either 2758 EPROMs, 2716 EPROMS, 2732 EPROMs, or 2764 EPROMs may be mounted. The board's default configuration is for 2758 (1K x 8) devices. Refer to Chapter 4 for jumper information used to configure the board to the EPROM size being used.

NOTE

Although 2758 EPROMs, 2716 EPROMs, 2732 EPROMs, or 2762 EPROMs may be mounted, they may not be mixed.

The EPROM section is used for permanent (non-volatile) storage of the system monitor or other programs such as tape load and/or dump or program debug routines. Four sockets are provided for ROM devices on the basic board.

Table 3-5 provides the addressing for the various EPROM configurations possible on the BLC-80/24,-80/28 board.

In the factory configuration, 4K bytes of RAM reside on-board the BLC-80/24 and 8K byte of RAM reside on the BLC-80/28. Default RAM addressing on the BLC-80/24 is assigned from 3000 - 3FFF. Default RAM addressing on the BLC-80/28 is assigned from 3000 - 4FFF.

3.2.4 Interval Timer

Refer to sheet 6 of the logic diagrams located in Appendix A. The 8253 Programmable Interval Timer (PIT) includes three independently controlled counters that are used for on-board I/O and CPU interrupts. Each counter has its own input and output. Counter 0 is used as the CPU interrupt interval, connected to IR2 on the interrupt controller (TMR00). It can also be used as an input to counter 1. Counter 1 can also be routed to the interrupt matrix or off-board via the parallel interface.

Counter 2 is used exclusively for the baud rate timer, clocking the serial interface controller (8251).

8253 PIT Programming

The on-board 8253 PIT may be programmed to operate in one of six different modes. In addition, the BLC-80/24,-80/28 board interval timer configuration provides several jumper selectable clock rates that can be used for counter inputs. Normally, the counter output 2 is used as the baud rate generator for the 8251 serial interface device.

Jumper configurations for the PIT clock inputs are summarized in Chapter 4. In the default configuration, the following frequencies are jumpered to the PIC:

a. 1.23 MHz to CLK 0 Input
b. 153.60 kHz to CLK 1 Input
c. 1.23 MHz to CLK 2 Input

The following paragraphs describe the PIT mode control, operation, and addressing as implemented on the BLC-80/24,-80/28 board.

Mode Control Word And Count

All three counters must be initialized separately prior to their use. The initialization for each counter consists of the following two steps:

a. A mode control word (refer to Figure 3-6) is written to the control register for each individual counter.

b. A down-counter number is loaded into each counter. One or two bytes must be sent to the PIT, as determined by the mode control word. Load most-significant byte of count into Counter 0 at port D0.

Operation

The following information describes a counter read, and modes of operation for the PIT.

There are two methods that can be used to read the contents of a particular counter. The first method involves a simple read of the desired counter. The only requirement with this method is that in order to ensure a stable count reading, the desired counter must be inhibited by controlling its gate input. Only Counter 0 and Counter 1 can be read using this method because the gate input to Counter 2 is not controllable.

The second method allows the counter to be read "on-the-fly". The recommended procedure is to use a mode control word to latch the contents of the count register; this ensures that the count reading is accurate and stable. The latched value of the count can then be read.

Before one or all of the counters can be used, they must be programmed for mode and count. The mode can be programmed at any time with the Mode Control Word (refer to Figure 3-6). This word specifies which counters are selected, what their mode is, and the type of count byte that will subsequently be sent.

The mode control word (refer to Figure 3-6) does the following:

a. Selects counter to be loaded.

b. Selects counter operating mode.

c. Selects one of the following four counter read/load functions:

(1) Counter latch (for stable read operation)
(2) Read or load most-significant byte only.
(3) Read or load least-significant byte only.
(4) Read or load least-significant byte first, then most-significant byte.

d. Sets counter for either binary or BCD count.

The count mode selected in the control word controls the counter output. As shown in Figure 3-6, the PIT device can operate in any of the following six modes:

a. Mode 0
b. Mode 1
c. Mode 2
d. Mode 3
e. Mode 4
f. Mode 5

Mode 3 is the primary operating mode for all three counters on the 8253. In this mode, the counter output remains high until one half of the count value in the count register has been decremented (for even numbers). The output then goes low for the other half of the count. If the value in the count register is odd, the counter output is high for (n+1)/2 counts, and low for (n-1)/2 counts.

Addressing

As listed in Table 3-6, the PIT uses the following four I/O addresses: DC, DD, DE, DF. Addresses DC, DD, and DE respectively, are used in loading and reading the count in counters 0, 1, and 2. Address DF is used in writing the mode control word to the desired counter.

3.2.5 Serial I/O

The 8251 Programmable Communications Interface (PCI) device provides RS232C compatibility, and is configured with board jumpers as a data set. The PCI converts parallel output data into virtually any series output data format for half or full-duplex operation. The PCI also converts serial input data into parallel data format.

Synchronous or asynchronous mode, character size, parity bits, stop bits, and baud rates are all programmable. Data, clocks, and control lines to and from connector J3 are buffered with drivers and receivers. A second serial I/O channel may be derived by jumper connection, in conjunction with parallel port CC. Refer to Chapter 4 for jumper information.

8251A PCI Programming

The CPU must load the 8251 with a set of control words before input/output operation can begin. These control words must immediately follow either an internal or an external RESET operation. The control words are either a Mode Instruction or Command Instruction. The following rules must be followed in writing control words:

a. The Mode instruction must immediately follow a RESET operation.

b. The Command instruction must follow the Mode instruction, however, SYNC characters or data (if Sync mode) may be interspersed.

Mode Instruction Format

The Mode instruction word defines the general characteristics of the PCI and must follow a reset operation. Once the Mode instruction word has been written into the PCI, sync characters or command instructions may be inserted. The Mode instruction word defines the following:

a. For Sync Mode:

(1) Character length
(2) Parity enable
(3) Even/odd parity generation and check
(4) External sync detect
(5) Single or double character sync

b. For Async Mode:

(1) Baud rate factor (X16 or X64)
(2) Character length
(3) Parity enable

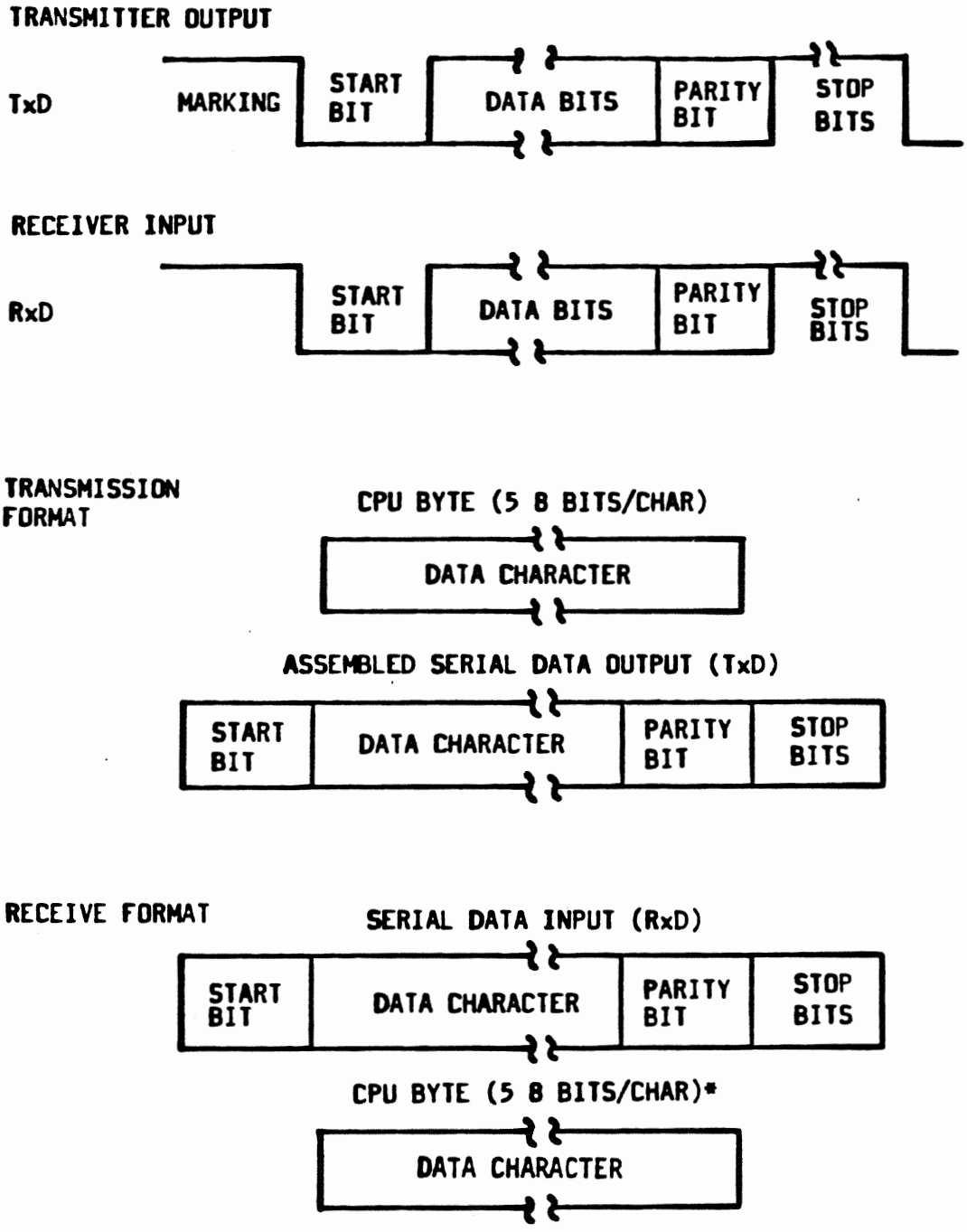
Figure 3-7 illustrates the mode instruction format for asynchronous mode of operation. Figure 3-8 illustrates the byte configurations that are selectable by the Mode instruction word. Figure 3-9 illustrates the Mode instruction word format for synchronous mode. Figure 3-10 illustrates the data byte configurations. Note that the examples indicate two SYNC characters. However, only one may be programmed by setting bit 7 of the Mode instruction word to a logic one. Table 3-7 illustrates the significance of each bit in the Mode instruction word for both asynchronous and synchronous operation.

Command Instruction Format

The command instruction controls the actual operation of the 8251A. Figure 3-11 defines the significance of each bit of the Command instruction.

8251A Status Word Definition

The status of the 8251A may be read by the programmer at any time during operation. This is accomplished by issuing a normal "Read" command and setting C/D to a logic one. Each status bit and its significance is detailed in Figure 3-12. It is assumed that the programmer has placed the data or control word in the accumulator prior to executing the output instructions. After the input instructions, the programmer must provide for storage of the input status word or data word which will reside in the accumulator after execution of the instruction.



*NOTE: IF THE CHARACTER LENGTH IS DEFINED AS 5, 6, or 7 BITS THE UNUSED BITS ARE SET TO "ZERO"

AA-14-0

Figure 3-8 Asynchronous Mode Data Byte Configuration

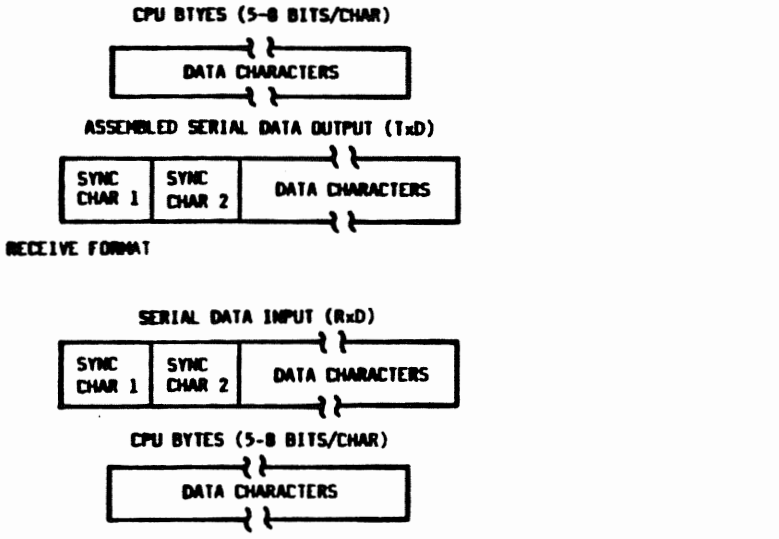
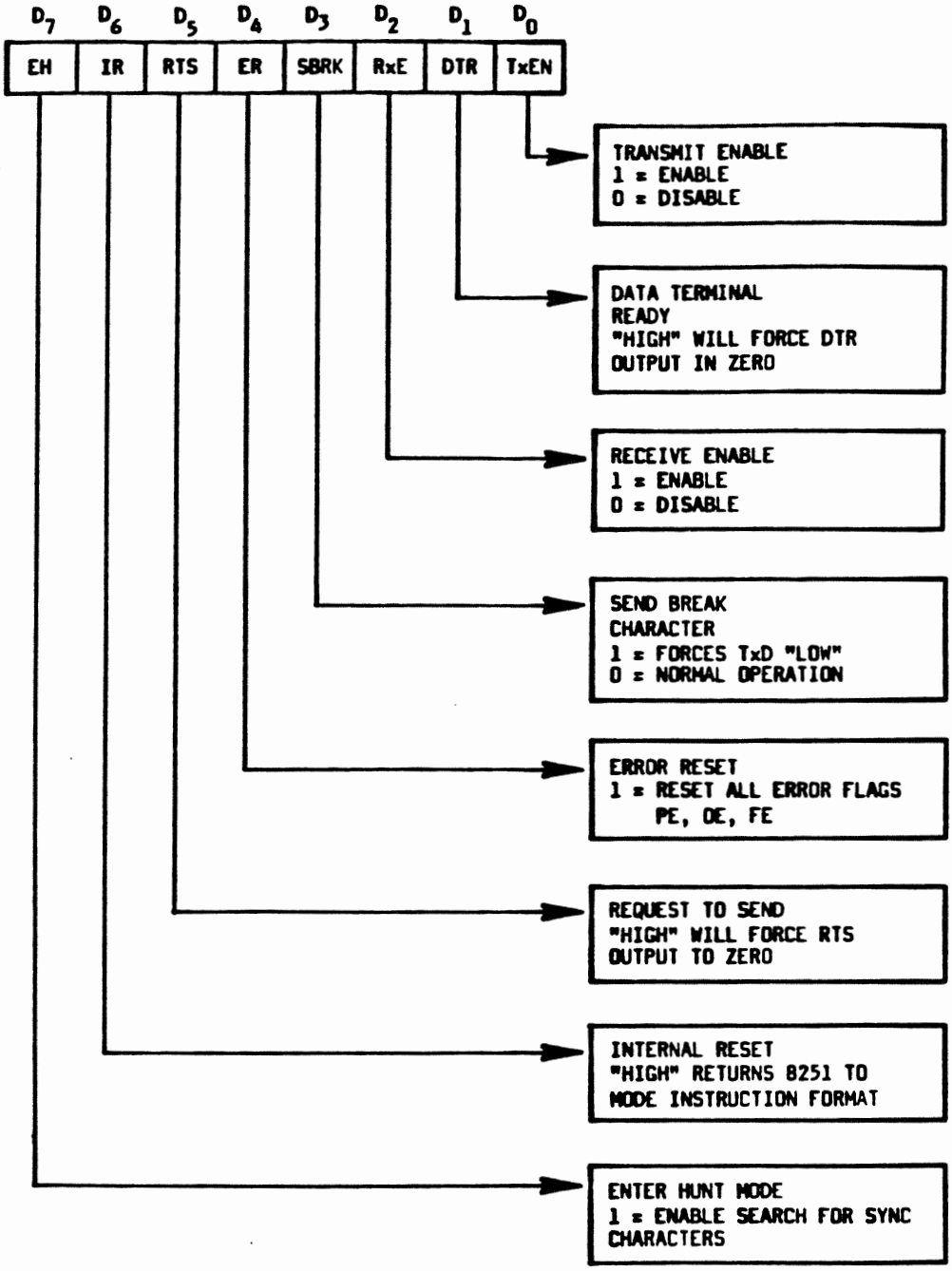


Figure 3-10 Synchronous Mode Data Byte Configurations



AA-17-0

Figure 3-11 Command Instruction Format

8251A Address/Decoding

Address bits AA through AF are decoded by the I/O decode PROM U67 and its associated circuitry (Appendix A, sheet 4). Address AO is applied directly to the C/D pin (12) of the 8251A (Appendix A, sheet 5). A logic one on Address AO indicates a control word or status is on the data bus (DO through D7). A logic zero on Address AO indicates that a data byte is on the data bus.

Transmit and Receive Clock Generation

The oscillator signal from a 8224 clock generator is input to the 8253 PIT on logic sheet 6. The oscillator's frequency is divided into eight different frequencies by the 8253 PIT which are available to the 8251 for baud rate generation. Table 3-8 lists the frequencies available to the 8251 for baud rate generation.

The effective baud rate output by the 8251 is dependent on the frequency from the 8253 PIT and by the baud rate factor selected by bits DO and D1 of the Mode instruction word (Asynchronous). Inputs to TxC and RxC are supplied by the same source, through the appropriate jumpers. The division of the frequency is performed within the 8251, and is dependent on whether a divisor of one, 16, or 64 was directed by the Mode instruction.

3.2.6 Parallel I/O

The two 8255 Programmable Peripheral Interface devices provide 48 programmable I/O lines (refer to Appendix A, sheets 7 and 8). Two bus transceivers are included to interface 16 of the I/O lines to connector J1 and J2. Four IC sockets are provided so that, depending on the application, TTL drivers or I/O terminators may be installed to complete the interface to connectors J1 and J2. The 48 lines are grouped into six ports of eight lines each. These ports can be programmed to be simple I/O ports or strobed I/O ports with handshaking. Two ports can be programmed as bidirectional ports with control lines. The BLC-80/24,-80/28 board includes various features such as RS232C interface lines, timer gates, and interrupts that can be contolled by the parallel I/O lines.

8255A PPI Programming

Each of the six parallel I/O ports (three on each 8255A device) may be programmed independently. However, as implemented on the BLC-80/24,-80/28 board, some lines have restricted use in certain modes. The modes allowed on the BLC-80/24,-80/28 board are listed in Table 3-9. Default jumpers set the port E4 and E8 bus transceivers to the output (transmit) mode. Optional jumper connections allow the bus transceivers to be set to either the input mode or a bit-programmable input/output mode. Refer to Chapter 4 for complete jumper information.

Ports E5, E6, E9 and EA do not have bus transceivers installed at the factory. Line drivers or terminators can be installed for these ports as described in Chapter 4.

In order to use any of the parallel port lines, the 8255A PPI devices must first be programmed for the desired mode and direction of data flow. The following paragraphs provide this information.

Control Word Format

The control word format illustrated in Figure 3-13 is used to initialize each PPI port. Group A (control word bits 3 through 6) defines the operating mode for port A and the upper four bits of port C. Group B (control word bits 0 through 2) defines the operating mode for port B and the lower four bits of port C. Bit 7 of the control word controls the mode set flag. The Control words are sent to port E7 for the J1 PPI device, and port EB for the J2 PPI device. There are restrictions associated with the use of certain ports in modes 1 and 2. Refer to Chapter 4 for these restrictions.

Mode Combinations

Table 3-10 summarizes the various mode combinations possible with ports A and B of the PPI, and indicates how each port C bit can be used. This table may serve as a usefull starting point for selecting a particular configuration. Once the selection of the desired mode combinations and the port C assignments are made, refer to the jumper configurations in Chapter 4 for implementation details.

3.2.7 Interrupts

The 8259 Programmable Interrupt Controller (PIC) functions as an overall manager in an interrupt-driven system environment. It accepts requests from the peripheral equipment, determines which of the incoming requests is of the highest importance (priority), ascertains whether the incoming request has a higher priority value than the level currently being serviced, and may issue an interrupt to the 8085A-2 CPU based on this determination.

The interrupt section provides twelve priority interrupts. Eight interrupts connect to the inputs of the 8259 Programmable Interrupt Controller (PIC); the remaining four interrupts connect directly to the 8085A-2 CPU. All interrupts, except TRAP, are maskable; the TRAP interrupt may be used to handle a power-fail (PFIN/) signal input via auxiliary connector P2. In the factory configuration, all four of these interrupts are grounded by jumper connections, and are therefore disabled.

There are 23 jumper-selectable interrupt sources: PPI (4), PCI (3), PIT (2), external via J1 and J2 (2), MULTIBUS lines (8), and Expansion Module boards (4).

TABLE 3-10 PARALLEL I/O INTERFACE CONFIGURATIONS

CONFIGURATION NUMBER	PPI PORT A (E4 or E8)	PPI PORT B (E5 or E9)	PPI PORT C (CC) LOWER				PPI PORT C (CC) UPPER			
			C_0	C_1	C_2	C_3	C_4	C_5	C_6	C_7
1	MODE 0-IN	MODE 0-I/O	--I/O--				--I/O--			
2	MODE 0-OUT	MODE 0-I/O	--I/O--				--I/O--			
3	MODE 0-IN	MODE 1-I/O	R	R	R	I	O	O	O	U
4	MODE 0-IN	MODE 1-I/O	R	R	R	O	I	I	I	U
5	MODE 0-OUT	MODE 1-I/O	R	R	R	I	O	O	O	U
6	MODE 0-OUT	MODE 1-I/O	R	R	R	O	I	I	I	U
7	MODE 1-IN	MODE 0-I/O	I	I	I	R	R	R	O	O
8	MODE 1-IN	MODE 0-I/O	O	O	O	R	R	R	I	I
9	MODE 1-OUT	MODE 0-I/O	I	I	I	R	O	O	R	R
10	MODE 1-OUT	MODE 0-I/O	O	O	O	R	I	I	R	R
11	MODE 1-IN	MODE 1-I/O	R	R	R	R	R	R	I	I
12	MODE 1-IN	MODE 1-I/O	R	R	R	R	R	R	O	O
13	MODE 1-OUT	MODE 1-I/O	R	R	R	R	I	I	R	R
14	MODE 1-OUT	MODE 1-I/O	R	R	R	R	O	O	R	R
15	MODE 2-B	MODE 0-I/O	U	I	I	R	R	R	R	R
16	MODE 2-B	MODE 0-I/O	U	O	O	R	R	R	R	R
17	MODE 2-B	MODE 1-I/O	R	R	R	R	R	R	R	R

NOTES:

I - INPUT

O - OUTPUT

I/O - INPUT OR OUTPUT

B - BIDIRECTIONAL

R - RESERVED

U - No unused drivers/terminators available. These bits may be used, however, to connect to the serial I/O interface or the Interval Timer.

Fully Nested Mode

In this mode, the PIC input signals are assigned a priority from 0 through 7. The PIC operates in this mode unless specifically programmed otherwise. Interrupt IRO has the highest priority and IR7 has the lowest priority. When an interrupt is acknowledged, the highest priority request is available to the 8085A-2 CPU.

Automatic Rotating Mode

In this mode, the interrupt priority rotates. Once an interrupt on a given input is serviced, that interrupt assumes the lowest priority. Thus, if there are a number of simultaneous interrupts, the priority will rotate among the interrupts in numerical order.

Specific Rotating Mode

In this mode, the software can change interrupt priority by specifying the bottom priority, which automatically sets the highest priority.

Poll Mode

In this mode, the 8085A-2 hardware and a software routine are used to initiate a Poll command. In the Poll Mode, the addressed PIC treats an I/O Read Command as an interrupt acknowledge and reads the priority level. This mode is useful if there is a common service routine for several devices.

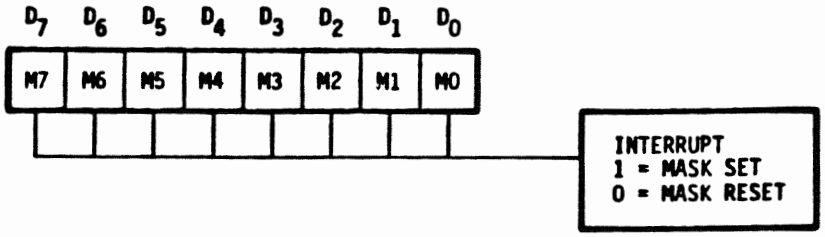
Initialization Command Words

The on-board PIC requires a separate initialization sequence to work in a particular mode. The initialization sequence requires three initialization Command Words (ICWs). The ICW formats are illustrated in Figures 3-14 through 3-16.

Operation Command Words

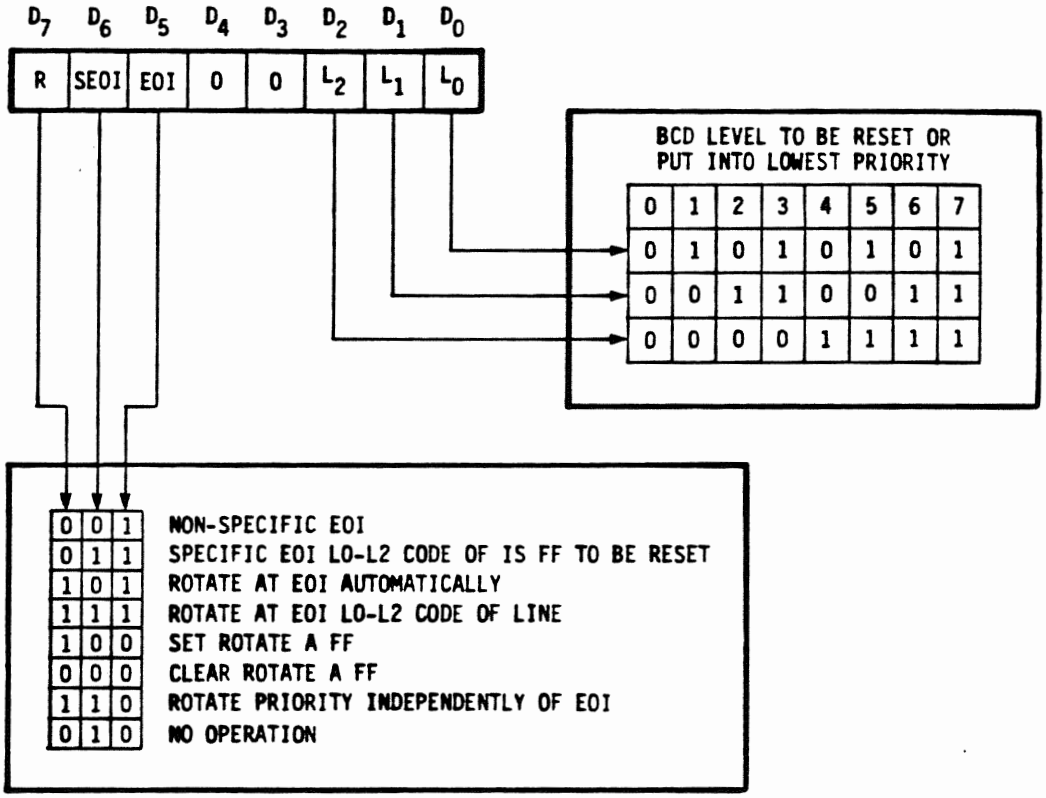
After initialization, the PIC can be programmed at any time by an Operation Command Word (OCW) for the operations listed below. The OCW formats are illustrated in Figures 3-17 through 3-19.

a. Auto-rotating priority
b. Specific rotating priority
c. Status read of Interrupt Request Register (IRR)
d. Status read of In-Service Register (ISR)
e. Interrupt mask bits are set, reset or read
f. Special mask mode set or reset



DS-24-0

Figure 3-17 Operation Command Word One Format (OCW1)



DS-25-0

Figure 3-18 Operation Command Word Two Format (OCW2)

3.2.8 System Bus Interface

The System Bus (MULTIBUS) Interface includes a Bus Controller, bidirectional address and data bus drivers, and the bus interrupt driver/receivers. The bus controller allows the BLC-80/24,-80/28 board to operate as a bus master in a serial or parallel priority arrangement with other bus masters in the system in which the 8085A-2 CPU can request the MULTIBUS lines when needed. The System Bus Interface (Appendix A, sheet 10) consists of a 8218 bus controller (U60), a data latch/driver (U64), and address drivers (U62, U63).

The bus controller arbitrates all BLC-80/24,-80/28 board requests for use of the System Bus lines, synchronously with respect to the Bus Clock (BCLK/). When the BLC-80/24,-80/28 acquires control of the bus, the bus controller generates the appropriate memory or I/O command signal, gates the address onto the address lines, and gates data on/off the bus, at the appropriate times. An external RC network connected to the bus controller's Delay-Adjust (DLADJ/) input guarantees the required set up and hold time relationship between the address/data lines and the control signals.

The negative-going edge of the Bus Clock (BCLK/) signal provides a timing reference for the controller's bus arbitration logic.

Bus arbitration activity begins when an off-board memory or an I/O request is generated and applied to the Command Request (CMDRQ) input. The request is strobed in by RSTB/ (which is always enabled). Following the next rising and falling edge of BCLK/ the bus controller generates Bus Request, BREQ/ (connector pin P1-18) and forces Bus Priority Out, SPRO/ (connector pin P1-16) inactive (high). BREQ/ is used to request the system bus when priority is decided by a parallel priority resolution circuit. BPRO/ is used to allow lower priority masters to gain control of the bus when a serial priority resolution structure is used. BPRO/ would go to the Bus Priority In (BPRN/) input of the next lower priority master.

When an off-board request activates the Command Request input (CMDRQ) and ADEN/ is activated, the bus controller's timing logic starts the internal sequence which ultimately (depending on the RC network at DLYADJ/) generates the appropriate memory/IO read/write control output (MRDC/, MWTC/, IORC/, or IOWC/) based on the active command request input (MRD/, MWT/, IORD/, or IOWRT/) from the CPU.

When control of the bus is granted to the BLC-80/24 or BLC-80/28 board, a low level appears on its Bus Priority In (BPRN/) input. The bus controller activates its BUSY/ (connector pin P1-17) and Address and Data Enable (ADEN/) outputs. Busy/ "locks" the BLC-80/24,-80/28 board onto the bus prohibiting any other master from acquiring control of the bus. ADEN/ enables the system address drivers (U62, U63) and data latch/drivers (U64). When the external acknowledge signal (XACK/ or AACK/) is received it will be gated (as MULTIBUS RDY/) to the CPU RDY input via the wait circuitry (Appendix A, sheet 3).

Chapter 4

SELECTABLE OPTIONS

4.1 INTRODUCTION

The BLC-80/24 and BLC-80/28 jumper connections are used to configure the board to meet a user's particular system requirements. Much of the versatility of the BLC-80/24,-80/28 board is due to the use of these jumper connections. Table 4-1 lists the factory default jumper connections on the board. Physical location of jumper pins on the board are illustrated in Appendix C. Jumper connections are illustrated schematically in Appendix A. Detailed information on the programming and operations of programmable devices are contained in Chapter 3.

Information on the various jumper configurations and other selectable options for the BLC-80/24,-80/28 board is organized in this chapter as follows:

Section 4.2 ROM/PROM/EPROM Options

Section 4.3 RAM Capacity and Addressing Options

Section 4.4 Serial Input/Output Interface Options

Section 4.5 Parallel Input/Output Interface Options

Section 4.6 Interrupt Matrix Jumper Configurations

Section 4.7 Internal Timer Jumper Configurations

Section 4.8 System Clock Jumper Selection

Section 4.9 MULTIBUS Interface Jumper Options

Section 4.10 Failsafe Timer Selection

Section 4.11 Power Failure Battery Backup

4.2 ROM/PROM/EPROM OPTIONS

Sockets XU40 through XU43 are reserved for optional ROM/PROM/EPROM devices. A maximum of 32K bytes may be installed. A summary of compatible device types, capability, and addressing is provided in Table 4-2. Device types may not be mixed; however, empty sockets are allowed (provided they are not addressed).

After selecting the ROM type which best suits the particular application, carefully insert each device into its socket.

TABLE 4-1 (cont.)

BLC-80/24,-80/28 JUMPER PAIR	APPENDIX A SCHEMATIC SHEET	FUNCTION
74 - 75	8	Connects port EA, bit 3 to PIA1/
87 to 86,85,84 and 83	9	Connects ground to 8259 IR7 input gates
100 - 118	9	Connects OITO to IR2 on PIC
101 - 106	3	Connects INT1 to IR1 on PIC
123 to 122,121, 120 and 119	9	Connects ground to all 8085A interrupt inputs (disabled)
125 - 126	3	Connects 9.68 MHz clock input to 8085A CPU
129 - 133	6	Connects 1.075 MHz to CLK0 on PIT
130 - 134	6	Connects 1.075 MHz to CLK1 on PIT
131 - 136	6	Connects 2.15 MHz to input of U53 counter
138 - 139	3	Connects 8224 OSC output to divider network
140 - 143	3	Enables failsafe timer
142 - 145	3	Connects RAMACK/ to READY gate
148-149 (BLC-80/24 only	6	RAM size jumper (for maximum of 4K bytes)
158 - 159	10	Connects 9.68 MHz BCLK/to P1-13 (output)
160 - 161	10	Connects BPRO/ to P1-16
164 - 165	10	Connects 9.68 MHz CCLK/ to P1-31 (output)
176 - 177	2	Used for +5 volt battery backup
187 - 188	9	Disables PROMOFF, PROMWT
189 - 190	3	CPU hold to ground
191 - 192	3	Connects RESET output from 8224 to 8085A reset gate
193 - 194	10	Connects ADEN output from 8218 to 8303 output enable gate
196 - 197	4	MCS0, MCS1 enable
198 - 199	6	RAMACK output from RAM Address Decoder
200 - 17	5	Connects internal receive clock to 8253 PIT
201 - 202	6	Connects 1.075 MHz to 8253 Clock 2
205 - 152	6	Sets on-board RAM address range
206 - 153	6	Sets on-board RAM address range

CAUTION: Never install any device into a board when power is applied. Damage to the board, device, and power supply could result.

CAUTION: ROM/EPROM sockets XU40 through XU43 are 28-pin sockets. If the user is inserting 24-pin devices, ensure they are positioned correctly.

Once the optional ROM devices are installed, the ROM-type header (shorting plug) must be inserted into the appropriate sockets. Socket J7 is used for this purpose. The factory configuration is for 2758-type devices (1K x 8). This configuration requires the header to be inserted as shown in Appendix A, sheet 4. Positions for other device types are marked on the board, and are listed in Table 4-3.

When using EPROMs having access times less than 300 ns, no EPROM wait states are necessary at either operating speed. For the EPROM acknowledge to bypass the wait state generating circuit, a jumper between pins 141 and 144 must be inserted. Closing pins 156 and 157 causes both EPROM and on-board I/O to by-pass the wait state generator. This should only be done when operating the BLC-80/24,-80/28 board in the slower (2.42 MHz) mode.

EPROMs with access times greater than 500 ns cannot be used with the BLC-80/24, -80/28 board in the 4.84 MHz operating mode.

4.3 RAM CAPACITY AND ADDRESSING OPTIONS

The RAM capacity jumper for the BLC-80/24 board is configured at the factory to indicate 4K bytes on-board. The RAM capacity jumper for the BLC-80/28 board is configured at the factory to indicate 8K bytes on-board. To alter these configurations, refer to Table 4-4.

4.4 SERIAL INPUT/OUTPUT INTERFACE OPTIONS

The BLC-80/24,-80/28 board serial port is configured at the factory to the RS232C standard interface. The J4 header (shorting plug) straps the board as data set (modem). Table 4-5 lists the signals strapped by the shorting plug, and provides pin identification. The J4 header can be modified to configure the serial port to a data terminal, rather than a data set. If the user's application requires external clocks or other serial interface modifications, refer to Table 4-6. For serial port cabling information, refer to Chapter 5.

4.5 PARALLEL INPUT/OUTPUT INTERFACE OPTIONS

Parallel ports E6 and EA each have a jumper matrix betwen the 8255 PPI device and the driver/terminator sockets. All other parallel ports do not have jumper

TABLE 4-4 RAM JUMPER CONNECTIONS

FUNCTION	JUMPER PAIR	DESCRIPTION		
RAM AMOUNT ON-BOARD	148 - 149	Indicates 4K RAM on-board (BLC-80/24 default configuration)		
	148 - 149 146 - 147	Both jumpers in indicates 2K RAM; or both jumpers out indicates 8K RAM (BLC-80/28 default configuration)		
RAM ADDRESSING Selects maximum (Four jumper pairs set an on-board RAM starting address. They represent the most significant four bits of the starting address. Jumper pair closed means that the corresponding address bit is a "1". Jumper pair open means that the corresponding address bit is a "0".)		2K	4K	8K
	152 - 205	--	--	2000-3FFF
	*152 - 205 and *153 - 206	3800-3FFF	3000-3FFF	3000-4FFF
	151 - 204	4800-5FFF	4000-4FFF	4000-5FFF
	151 - 204 and 153 - 206	5800-5FFF	5000-5FFF	5000-6FFF
	151 - 204 and 152 - 205	6800-7FFF	6000-7FFF	6000-7FFF
	151 - 204 and 152 - 205 and 153 - 206	7800-7FFF	7000-7FFF	7000-8FFF
	150 - 203	8800-8FFF	8000-8FFF	8000-9FFF
	150 - 203 and 153 - 206	9800-9FFF	9000-9FFF	9000-AFFF
	150 - 203 and 152 - 205	A800-AFFF	A000-AFFF	A000-BFFF

TABLE 4-5 SERIAL PORT HEADER LOCATIONS

8251 FUNCTION	J4 STRAP	SERIAL PORT CONNECTOR	SIGNAL DIRECTION
TxD	2-13	J3-6 Rec Data	Output
RxD	1-14	J3-4 Trans Data	Input
DTR/	5-9	J3-12 DSR	Output
DSR/	6-9	J3-13 DTR	Input
RTS/	4-11	J3-10 CTS	Output
CTS/	3-12	J3-8 RTS	Input

matrices, and their operation is determined by software programming. Refer to Table 3-9 (located in Chapter 3) for a list of operating modes allowed for each parallel port. Table 4-7 lists the types of terminators and line drivers that are recommended for the driver/terminator sockets.

Before a user configures a parallel port for a particular application, refer to section 3.2.6 (in Chapter 3) for 8255 PPI programming information. Jumper information for all parallel ports, including bit restrictions, is provided in Table 4-8.

4.6 INTERRUPT MATRIX JUMPER CONFIGURATIONS

The BLC-80/24,-80/28 board can resolve 12 levels of interrupt priority. Eight of these levels are controlled by the 8259 PIC and the remaining four are direct inputs to the 8085A CPU. All interrupts are routed through the interrupt matrix (shown in Appendix A, sheet 9). Table 4-9 lists all the matrix jumper pins and their functions. The board is shipped from the factory with the following jumpers installed:

1. 101 - 106 --- INT2/ from MULTIBUS Interface
2. 200 - 108 --- Counter 0 output
3. 83 through 87 --- Grounded
4. 119 through 123 --- Grounded

Refer to section 3.2.7 (in Chapter 3) for 8259 PIC programming information.

4.7 INTERNAL TIMER JUMPER CONFIGURATIONS

The 8253 Programmable Interval Timer (PIT) is configured at the factory with five jumpers installed, as listed in Table 4-10. Two jumpers select the gate operation for the 8253 PIT device itself and three jumpers select the input frequencies to each of the three independent counters within the PIT. Outputs 0 and 1 from the timer are routed directly to the interrupt matrix. These outputs may then be jumpered to the desired on-board interrupt level (jumper pins 118 and 103 shown in Appendix A, sheet 3).

Output 2 is used for the 8251 Programmable Communications Interface (PCI) transmit and receive clocks.

4.8 SYSTEM CLOCK JUMPER SELECTION

The BLC-80/24,-80/28 board is configured at the factory to operate at 4.82 MHz. Alternately, the board may be operated at 2.42 MHz, by jumper selection. Refer to Table 4-11 for information pertaining to this option.

TABLE 4-8 PARALLEL PORTS E4-EA JUMPER CONNECTIONS

JUMPER CONFIGURATION

PORT	MODE	DRIVER (D)/ TERMINATOR (T)	DELETE	ADD	EFFECT	PORT	RESTRICTIONS
E4	0 Input	8303: U3	26-27*	27-41	8303 = input enabled	E5	None; can be in mode 0 or 1, input or output.
						E6	None; can be in Mode 0, input or output, unless Port E5 is in Mode 1.
E4	0 Output (latched)	8303:U3	None	26-27*	8303 = output enabled	E5	None; can be in Mode 0 or 1, input or output.
						E6	None; can be in Mode 0, input or output, unless Port E5 is in Mode 1.
E4	1 Input (strobed)	8303: U3	26-27*	27-41*	8303 = output enabled	E5	None; can be in Mode 0 or 1, input or output.
		T: XU4 D: XU5	--	32-47*	Connects J1-26 to STB_A/ input.	E6	Port E6 bits perform the following:
			33-48* and 31-45*	31-48 --	Connects IBF_A output to J1-18 Disconnect Port E6, bit 3 (INTR) from driver at U4.		• Bits 0, 1, 2 -- Control for Port E5 if in Mode 1. • Bit 3 -- Port E4 Interrupt to interrupt jumper matrix. • Bit 4 -- Port E4 Strobe (STB/) input.

*Default jumper connected at factory.

TABLE 4-8 (cont.)

JUMPER CONFIGURATION

PORT	MODE	DRIVER (D)/ TERMINATOR (T)	DELETE	ADD	EFFECT	PORT	RESTRICTIONS
E4	2 (bidirectional)	8303: U3 T: XU5	26-27*	27-49	Allows ACK_A/ output to control 8287 in/out direction.	E5	None.
						E6	Port E6 bits perform the following:
			--	32-47*	Connects J1-26 to STB_A input.		• Bit 0 -- Cannot be used.
			33-48* and 28-42*	28-48	Connects IBF_A output to J1-24.		• Bits 1, 2 -- Can be used for input or output if Port E5 is in Mode 0.
			--	34-49	Connects J1-30 to ACD_A/ input.		• Bit 3 -- Port E4 Interrupt to interrupt jumper matrix.
			35-50*	31-50	Connects OBF_A/ output to J1-18.		• Bit 4 -- Port E4 Strobe (STB/) input.
			31-45	--	Disconnects Port E6, bit 3 (INTR) from driver at U4.		• Bit 5 -- Port E4 Input Buffer Full (IBF) output.
							• Bit 6 -- Port E4 Acknowledge (ACK/) input.
							• Bit 7 -- Port E4 Output Buffer Full (OBF/) output.

*Default jumper connected at factory.

TABLE 4-8 (cont.)

JUMPER CONFIGURATION

PORT	MODE	DRIVER (D)/ TERMINATOR (T)	DELETE	ADD	EFFECT	PORT	RESTRICTIONS
							• Bit 3 -- If Port E4 is in Mode 0, bit 3 can be input or output. Otherwise, bit 3 is reserved. • Bits 4-7 -- Depends on Port E4 mode; see table 3-10.
E5	1 Output (latched)	T: XU4 D: XU5, XU6, XU7	--	29-43*	Connects OBF_B/ output to J1-22.	E4	None.
			35-50* and 30-44*	35-44	Connects J1-32 to ACK_B/ input.	E6	Port E6 bits perform the following: • Bit 0 -- Port E5 Interrupt to interrupt jumper matrix. • Bit 1 -- Port E5 Output Buffer Full (OBF/) output. • Bit 2 -- Port E5 Acknowledge (ACK/) input.
			28-42*	--	Disconnects Port E6, bit 0 (INTR) from driver at U4.		

*Default jumper connected at factory.

TABLE 4-8 (cont.)

JUMPER CONFIGURATION

PORT	MODE	DRIVER (D)/ TERMINATOR (T)	DELETE	ADD	EFFECT	PORT	RESTRICTIONS
				30-44*	Connects bit 2 to J1-20.		
				31-45*	Connects bit 3 to J1-18.		
E6 (upper)	0 Output (latched)	D: XU4	None		Same as for Port E6 (upper) Mode 0 Input.	E4 & E5	Same as for Port E6 (upper) Mode 0 Input.
E6 (lower)	0 Output (latched)	D: XU5	None		Same as for Port E6 (lower) Mode 0 Input.	E4 & E5	Same as for Port E6 (lower) Mode 0 Input.
E8	0 Input	8303: U8	55-56*	56-70	8303 = input enabled	E9	None; can be Mode 0 or 1, input or output.
						EA	None; can be in Mode 0, input or output, unless Port E9 is in Mode 1.
E8	0 Output (latched)	8303: U8	None	55-56*	8303 = output enabled	E9	None; can be in Mode 0 or 1, input or output.
						EA	None; can be in Mode 0, input or output, unless Port E9 is in Mode 1.
E8	1 Input (strobed)	8303: U8 T: XU9 D: XU10	55-56* --	56-70* 62-76*	8303 = output enabled Connects J2-26 to STB_A/ input.	E9	None; can be in Mode 0 or 1, input or output.

*Default jumper connected at factory.

TABLE 4-8 (cont.)

JUMPER CONFIGURATION

PORT	MODE	DRIVER (D)/ TERMINATOR (T)	DELETE	ADD	EFFECT	PORT	RESTRICTIONS
							• Bit 3 -- Port E8 Interrupt to interrupt jumper matrix. • Bits 4, 5 -- Input or output (both must be in same direction). • Bit 6 -- Port E8 Acknowledge (ACK/) input. • Bit 7 -- Port E8 Output Buffer Full (OBF/) output.
E8	2 (bidirectional)	8303: U8 T: XU9 D: XU10	55-56*	56-78	Allows ACK_A/ output to control 8287 in/out direction.	E9 EA	None. Port EA bits perform the following:
			--	62-76*	Connects J2-26 to STB_A input.		• Bit 0 -- Can only be used for serial interface.
			63-77* and	57-77	Connects IBF_A output to J2-24.		• Bits 1, 2 -- Can be used for input or output if Port E9 is in Mode 0.
			--	64-78*	Connects J2-30 to ACK_A/ input.		• Bit 3 -- Port E8 Interrupt to interrupt jumper matrix.

*Default jumper connected at the factory.

TABLE 4-8 (cont.)

JUMPER CONFIGURATION

PORT	MODE	DRIVER (D)/ TERMINATOR (T)	DELETE	ADD	EFFECT	PORT	RESTRICTIONS
			57-71*	--	Disconnects Port EA bit 0 (INTR) from driver at XU10.		• Bit 1 -- Port E9 Input Buffer Full (IBF) output. • Bit 2 - Port E9 Strobe (STB/) input. • Bit 3 -- If Port E8 is in Mode 0, bit 3 can be input or output. Otherwise, bit 3 is reserved. • Bits 4, 5 -- Depends on Port E8 mode; see table 3-10. • Bits 6, 7 -- Input or output (both must be in same direction). See table 3-10.
E9	1 Output (latched)	T: XU9 D: XU10, XU11, XU12	--	58-72	Connects IBF_B/ output to J2-22.	E8	None.
			59-73* and 65-79*	65-73	Connects J2-32 to ACK_B/ input.	EA	Port EA bits perform the following: • Bit 0 -- Port E9 interrupt to interrupt jumper matrix.

*Default jumper connected at the factory.

TABLE 4-8 (cont.)

JUMPER CONFIGURATION

PORT	MODE	DRIVER (D)/ TERMINATOR (T)	DELETE	ADD	EFFECT	PORT	RESTRICTIONS
EA (upper)	0 Output (latched)	D: XU9	None		Same as for Port EA (upper) Mode 0 Input.	E8 & E9	Same as for Port EA (upper) Mode 0 Input.
EA (lower)	0 Output (latched)	D: XU10	None		Same as for Port EA (lower) Mode 0 Input.	E8 & E9	Same as for Port EA (lower) Mode 0 Input.

*Default jumper connected at the factory.

TABLE 4-10 RAM JUMPER CONNECTIONS

FUNCTION	JUMPER PAIR	DESCRIPTION
Inputs/Outputs	*129 - 133	Provides 1.075 MHz to CLK0.
	*130 - 134	Provides 1.075 MHz to CLK1.
	*201 - 202	Provides 1.075 MHz to CLK2.
	128 - 133	Provides 134.4 kHz to CLK0.
	128 - 134	Provides 134.4 kHz to CLK1.
	128 - 202	Provides 134.4 kHz to CLK2.
	134 - 135	Connects Timer 0 output to Timer 1 input.
	132 - 135	Connects Timer 0 output to parallel port E6 jumper matrix.
	132 - 133	Connects parallel port E6 jumper matrix to CLK0 timer input.
	132 - 134	Connects parallel port E6 jumper matrix to CLK1 timer input.
	132 - 202	Connects parallel port E6 jumper matrix to CLK2 timer input.
	132 - 128	Connects 134.4 kHz to parallel port E6 jumper matrix.
	132 - 129	Connects 1.075 MHz to parallel port E6 jumper matrix.
Gate inputs	* 36 - 51	Provides +5 volts to gate 0 input of 8253 PIT.
	* 37 - 51	Provides +5 volts to gate 1 input of 8253 PIT.

*Indicates default connection at factory.

TABLE 4-11 BLC-80/24,-80/28 TIMING JUMPER CONFIGURATIONS

FUNCTION	JUMPER PAIR	DESCRIPTION
9.68 MHz Clock	*125 - 126	Use for 4.84 MHz operation.
4.84 MHz Clock	124 - 125	Use for 2.42 MHz operation.
4.84 MHz Clock	156 - 157	Use for 2.42 MHz operation.
8224 OSC Output	*138 - 139	Connects 8224 OSC output to U53 counter.

* Indicates default connection at factory.

TABLE 4-12 MULTIBUS INTERFACE JUMPER CONNECTIONS

FUNCTION	JUMPER PAIR	DESCRIPTION
MULTIBUS SIGNALS		
AACK/	162 - 163	Connects AACK/ signal from P1-25
BPRO/	*160 - 161	Connects BPRO/ to P1-16
BCLK/	*158 - 159	Connects BCLK/ to P1-13
CCLK/	*164 - 165	Connects CCLK/ to P1-31
PFSR/	53 - XX	Connects PFSR/ to selected Port E6 bit.

* Indicates default connection at factory.

Chapter 5

SYSTEM INTERFACING

5.1 INTRODUCTION

The BLC-80/24,-80/28 connectors are used to interface the board with other system components. Off-board system access is provided by the System Bus (MULTIBUS) connector (P1) and the auxiliary connector (P2). Off-board peripheral operations are handled through 48 parallel I/O lines (connectors J1/J2), a serial communications channel (connector J3), and two special purpose Board Level Expansion (BLX) connectors (J5 and J6).

This chapter defines the connectors and compatible connector hardware and lists the signals and their functions.

5.2 CONNECTORS

The BLC-80/24,-80/28 board connector locations are illustrated in Figure 5-1. Table 5-1 lists recommended suppliers for such connectors. Detailed information for the BLC-80/24,-80/28 connectors are listed in tabular form as follows:

- P1 - System bus interface. Table 5-2 lists the P1 connector pin assignments. Table 5-3 lists the P1 signal functions.
- P2 - Auxiliary interface. Table 5-4 lists the P2 connector pin assignments. Table 5-5 lists the P2 signal definitions.
- J1/J2 - Parallel I/O interface. Table 5-6 lists the J1 connector pin assignments and signal functions. Table 5-7 lists the J2 connector pin assignments and signal functions.
- J3 - Serial I/O interface. Tables 5-8 and 5-9 lists the J3 connector pin assignments and signal functions.
- J5/J6 - BLX Expansion module interface. Table 5-10 lists the J5 and J6 connector pin assignments. Table 5-11 lists the J5/J6 signal functions.

5.2.1 System Bus Connectors P1 and P2

System Bus (MULTIBUS) connector P1 and auxiliary connector P2 interface the BLC-80/24,-80/28 board signals and power lines to the other boards in the user's system. Pin assignments for P1 and P2 are listed in Tables 5-2 and 5-4, respectively. Signal definitions are provided in Table 5-3 and 5-5.

TABLE 5-1 COMPATIBLE CONNECTORS FOR BLC-80/24,-80/28

FUNCTION	CONNECTOR TYPE	VENDOR	VENDOR PART NO.
MULTIBUS Connector P1	Solder PCB	ELFAB VIKING	BS1562043PBB 2KH43/9AMK12
	Wire Wrap (no ears)	EDAC ELFAB	337-086-0540-201 BW1562D-43PBB
	Wire Wrap (with 0.128 mounting holes)	EDAC ELFAB	337-086-540-201 BW1562A-43PBB
Auxiliary Connector P2	Wire Wrap	EDAC ELFAB	345-060-524-802 BS1020A-30PBB
	With 0.128 mounting holes	T1 VIKING	H421121-30 3KH30/9JNK
	No EARs	EDAC ELFAB	345-060-540-201 BW1020D-30PBB
Parallel I/O Connector J1/J2	Flat Crimp	3M 3M AMP ANSLEY SAE	3415-0001 (w/o ears) 3415-0000 (w/ears) 88083-1 609-5015 S06750 Series
	Soldered	GTE MASTERITE MICROPLASTICS VIKING	6AD01-25-1A1-DD NDD8GR25-DR-H-X MP-0100-25-DP-1 3KH25/9JN5
	Wire Wrap	VIKING TI ITT CANNON	3KH25/JND5 H421011-25 EC4A050A1A
Serial I/O Connector J3	PCB Soldered Mounting holes	AMP EDAC	1-583715-1 345-026-520-202
	Flat Crimp	3M AMP	3462-0001 88373-5
	Soldered pierced tail	EDAC	345-026-500-201
	Wire Wrap	EDAC	345-026-540-201
BLX Connector J5/J6	Soldered PCB Soldered PCB	VIKING VIKING	293-001 292-001

NOTES: 1. Connector heights are not warranted to conform to the user's packaging equipment.

2. The National Semiconductor mother boards are mechanically compatible with these connectors and wirewrap pins.

TABLE 5-2 (cont.)

	(COMPONENT SIDE)			(SOLDER SIDE)		
	PIN	MNEMONIC	DESCRIPTION	PIN	MNEMONIC	DESCRIPTION
POWER SUPPLIES	75	GND	Signal GND	76	GND	Signal GND
	77		Reserved	78		Reserved
	79	-12V	-12Vdc	80	-12V	-12Vdc
	81	+5V	+5Vdc	82	+5V	+5Vdc
	83	+5V	-5Vdc	84	+5V	+5Vdc
	85	GND	Signal GND	86	GND	Signal GND

NOTE: All odd-numbered pins (1, 3, 5 ... 85) are on component side of the board. Pin 1 is the left most pin when viewed from the component side of the board with the extractors at the top. All unassigned pins are reserved.

TABLE 5-3 (cont.)

CCLK/	Constant clock; provides a clock signal of constant frequency (9.677 MHz) for use by optional memory and I/O expansion boards. CCLK/ has period of 103.3 nanoseconds, 50% duty cycle.
INT0/ - INT7/	Eternally generated interrupt requests.
ADR0/ - ADRF/	16 Address lines; used to transmit the address of the memory location or I/O port to be accessed. ADRF/ is the most significant bit.
DAT0/ - DAT7/	Bi-directional data lines; used to transmit/receive information to/from a memory location or I/O port. DAT7/ is the most significant bit.
CBRQ/	Common Bus Request; indicates that a bus master wishes control of the bus but does not presently have control. As soon as control of the bus is obtained, their requesting bus controller raises the CBRQ/ signal.

TABLE 5-4 CONNECTOR P2 PIN ASSIGNMENTS

PIN ASSIGNMENT	SIGNAL MNEMONIC	DESCRIPTION
P2-1, 2 P2-21, 22	Signal GND	Battery Ground
P2-3 P2-4	+5V AUX	Battery +5V Power Input
P2-13	PFSR/	Power Fail Sense Reset
P2-17	PFSN/	Power Fail Sense
P2-19	PFIN/	Power Fail Interrupt
P2-20	MPRO/	Memory Protect
P2-28	HALT/	Halt Indicator
P2-32	ALE	Bus Master ALE
P2-38	AUX RESET/	System Reset Switch Input

5.2.2 Parallel I/O Connectors J1/J2

Parallel I/O ports E4, E5, E6, E8, E9 and EA are controlled by two 8255 Parallel Peripheral Interface (PPI) devices on the BLC-80/24,-80/28 board. The I/O ports are connected to the user's external equipment via edge connectors J1 and J2 (J1 connector handles ports E4, E5, E6 and connector J2 handles ports E8, E9, and EA). Pin assignments and signal functions for edge connectors J1 and J2 are provided in Tables 5-6 and 5-7, respectively.

5.2.3 Serial I/O Connector J3

Pin assignments and signal names for the serial I/O port interface connector (J3) are listed in Table 5-8. Two cables are required for interfacing to this connector. One cable assembly consists of a 25 conductor flat cable with a 26-pin board edge connector at one end and an RS232C interface connector at the other end. A second cable assembly consists of an RS232 connector on one end and spade lugs on the other end. The spade lugs are used to connect the cable to a teletypewriter.

For user applications where cables will be made for the BLC-80/24,-80/28 board it is important to note that the mating connector for J3 has 26 pins, whereas the RS232C connector has 25 pins. Consequently, when connecting the 26-pin mating connector to a 25-pin conductor flat cable, the user must be sure that the cable makes contact with pins 1 and 2 of the mating connector and not pin 26. Table 5-9 provides pin correspondence between connector J3 and the RS232C connector. When attaching the connector to J3, the user must be sure that the board edge connector is oriented properly with respect to pin 1 on the board.

5.2.4 BLX Connectors J5 and J6

The BLC-80/24,-80/28 board is equipped with two Board Level Expansion (BLX) bus connectors (J5 and J6). This allows on-board I/O expansion, using optional BLX Expansion Module boards (i.e., BLX-350 Parallel Port board, BLX-351 Serial port board, etc.). Table 5-10 provides the BLX bus connector pin assignments, and Table 5-11 provides signal descriptions. Each of the two connectors has identical pin assignments and physical layout.

TABLE 5-7 CONNECTOR J2 PIN ASSIGNMENTS

PIN	SIGNAL	PIN	SIGNAL
1	GND	2	PORT E9 - BIT 7
3	GND	4	PORT E9 - BIT 6
5	GND	6	PORT E9 - BIT 5
7	GND	8	PORT E9 - BIT 4
9	GND	10	PORT E9 - BIT 3
11	GND	12	PORT E9 - BIT 2
13	GND	14	PORT E9 - BIT 1
15	GND	16	PORT E9 - BIT 0
17	GND	18	PORT EA - BIT 3
19	GND	20	PORT EA - BIT 2
21	GND	22	PORT EA - BIT 1
23	GND	24	PORT EA - BIT 0
25	GND	26	PORT EA - BIT 4
27	GND	28	PORT EA - BIT 5
29	GND	30	PORT EA - BIT 6
31	GND	32	PORT EA - BIT 7
33	GND	34	PORT E8 - BIT 7
35	GND	36	PORT E8 - BIT 6
37	GND	38	PORT E8 - BIT 5
39	GND	40	PORT E8 - BIT 4
41	GND	42	PORT E8 - BIT 3
43	GND	44	PORT E8 - BIT 2
45	GND	46	PORT E8 - BIT 1
47	GND	48	PORT E8 - BIT 0
49	GND	50	EXTERNAL INTERRUPT OR + 5V OR OPEN

NOTES:

1. All odd-numbered pins are on the component side of the board. Pin 1 is rightmost when board is viewed with I/O connectors on top.

2. Cable connector numbering convention may not agree with board edge connector numbering.

TABLE 5-9 RS232C SIGNALS PIN CORRESPONDENCE

(25-Pin to 26-Pin)

SIGNAL NAME PIN	J3	25-PIN CONNECTOR
Protective Ground	2	1
Secondary Transmitted Data	1	14
Transmitted Data	4	2
Transmitter Signal Element Timing	3	15
Received Data	6	3
Secondary Received Data	5	16
Request to Send	8	4
Receiver Signal Element Timing	7	17
Clear to Send	10	5
(No connection)	9	18
Data Set Ready	12	6
Secondary Request to Send	11	19
Signal Ground	14	7
Data Terminal Ready	13	20
Received Line Signal Detect	16	8
(No connection)	15	21
(No connection)	18	9
Ring Indicator	17	22
(No connection)	20	10
TTY Adapter Power (-12V)	19	23
TTY Adapter Power (+12V)	22	11
Transmitter Signal Element Timing	21	24
(No connection)	24	12
(+5V)	23	25
Secondary Clear to Send	26	13
Signal Ground	25	No Connection

TABLE 5-11 BLX BUS SIGNAL DESCRIPTIONS FOR CONNECTOR J5/J6

IORD/	Commands the BLX board to perform the read operation.
IOWRT/	Commands the BLX board to perform the write operation.
MRESET/	Initializes the BLX board to a known internal state.
MCS0/	Chip select. Selects I/O addresses C0-C7 on the J5 BLX board and addresses F0-F7 on the J6 BLX board.
MCS1/	Chip select. Selects I/O addresses C8-CF on the J5 BLX board and addresses F8-FF on the J6 BLX board.
MA0-2	Least three bits of the I/O address. Used in conjuction with the chip select and command lines.
MPST/	BLX present indicator. Informs BLC-80/24,-80/28 board that a BLX board(s) is installed.
MINTRO-1	Interrupt request lines from the BLX board to the BLC-80/24,-80/28 board interrupt matrix.
MWAIT/	Causes BLC-80/24,-80/28 board to execute wait states until BLX board is ready to respond.
MCLK/	9.68 MHz BLX board timing reference from BLC-80/24,-80/28 board.
OPTO-1	Optional use lines. May be used for additional interrupt request lines.
MDO-7	Bidirectional data lines.

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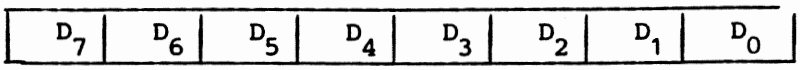
Appendix D

8085 INSTRUCTION SET DESCRIPTION

D.1 8085 INSTRUCTIONS

Data in the 8085 are manipulated in words of 8 binary digits:

DATA WORD

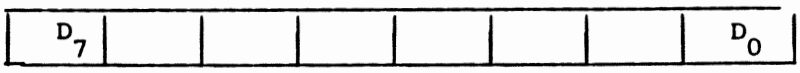


MSB LSB

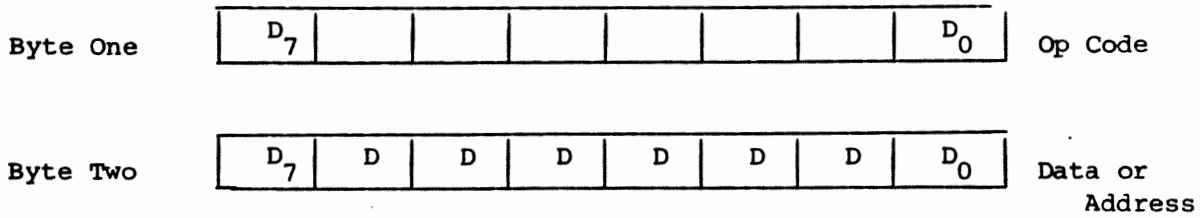
When a register or data word contains a binary number, it is necessary to establish the order in which the bits of the number are written. In the 8085, BIT 0 is referred to as the Least Significant Bit (LSB), and BIT 7 (of an 8-bit number) is referred to as the Most Significant Bit (MSB).

The 8085 program instructions may be one, two or three bytes in length. Multiple byte instructions must be stored in successive memory locations; the address of the first byte is always used as the address of the instruction. The exact instruction format depends on the particular operation to be executed.

Single-Byte Instructions



Two-Byte Instructions



Register Indirect - The branch instruction indicates that the HL register contains the address of the next instruction to be executed. The high-order bits of the address are in the H register, the low-order bits in the L register.

The RST instruction is a special one-byte call instruction (usually used during interrupt sequences). RST includes a three-bit field; program control is transferred to the instruction whose address is eight times the contents of this three-bit field.

D.1.2 Condition Flags

There are five condition flags associated with the execution of the 8085 instructions. They are Zero, Sign, Parity, Carry, and Auxiliary Carry. Each is represented by a 1-bit register in the CPU. A flag is reset by forcing the bit to 0. Unless otherwise indicated, when an instruction affects a flag, it does so in the following manner:

Zero - if the result of an instruction has the value 0, this flag is set; otherwise it is reset.

Sign - if the most significant bit of the result of the operation has the value of 1, this flag is set; otherwise it is reset.

Parity - if the modulo 2 sum of the bits of the result of the operation is Ø, (i.e., if the result has even parity), this flag is set; otherwise it is reset (i.e., if the result has odd parity).

Carry - if the instruction resulted in a carry (from addition), or a borrow (from subtraction or a comparison) out of the high-order bit, this flag is set; otherwise it is reset.

Auxiliary Carry - if the instruction caused a carry out of bit 3 and into bit 4 of the resulting value, the auxiliary carry is set; otherwise it is reset. This flag is affected by single precision additions, subtractions, increments, decrements, comparisons, and logical operations, but is principally used with additions and increments preceding a decimal adjust accumulator (DAA) instruction.

D.1.3 Coding of Conditions

A condition is coded in bits 3-5 of the op code of branch and call instructions, as follows:

000 No zero (NZ); Condition Flag Z=Ø
001 Zero (Z); Condition Flag Z=1

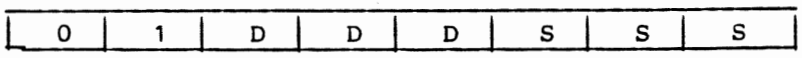
Data transfer	These instructions move data between registers or between memory and registers.
Arithmetic	These instructions add, subtract, increment or decrement data in registers or memory.
Logical	These instructions perform logical transformations of data in registers or memory; they rotate a number, complement a number, AND, OR, XOR and COMPARE two numbers.
Branch	These instructions perform conditional and unconditional jumps to different places in the series of instructions.
Stack	These instructions access the stack.
I/O and Machine Control	These instructions access the I/O ports, set or reset condition flags and directly control some aspects of processor operation.

D.1.7 Data Transfer Instruction [MOV rl,r2 MOV r,M MOV M,r MVI r,data MVI M,data LXI rp, data16 LDA addr STA addr LHLD addr LDAX rp STAX rp XCHG]

Function - transfers data between registers or between a register and memory. Data may be transferred one byte at a time or two bytes at a time, depending on whether a single register or a register pair is specified by the instruction. Condition flags are not affected by any instruction in this group.

Move (MOV)

Function - transfers a single byte of data between registers or between a register and memory. Instruction formats:



(See D.1.4)

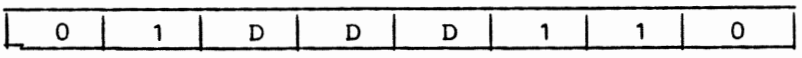
MOV rl, r2 (Move Register) (rl)<-(r2)

Register r2 content is moved to register rl.

Cycles:	1
States:	5
Addressing:	register
Flags:	none

MOV r,M (Move from Memory) (r)<-((H)(L))

The content of the memory location whose address is in registers H and L is moved to register r.



Cycles:	2
States:	7
Addressing:	register indirect
Flags:	none

Load Register Pair Immediate (LXI)

Function - loads a 16-bit operand into a specific 16-bit register. Instruction format:

LXI r_H,data 16 (Load Register Pair Immediate) (r_L)<-byte 2
(r_H)<-byte 3

Byte 3 of the instruction is moved into the high-order register (R_H) of the register pair rp. Byte 2 of the instruction is moved into the low-order register (R_L) of the register pair rp.

Byte 1

0	0	R	R	0	0	0	1

(See D.1.5)

Byte 2

low-order data

Byte 3

high-order data

MVI M,data (Move to Memory Immediate) ((H) (L))<-data

Byte 2 of the instruction is moved to the memory location whose address is in registers H and L.

Byte 1

0	0	1	1	0	1	1	0

Byte 2

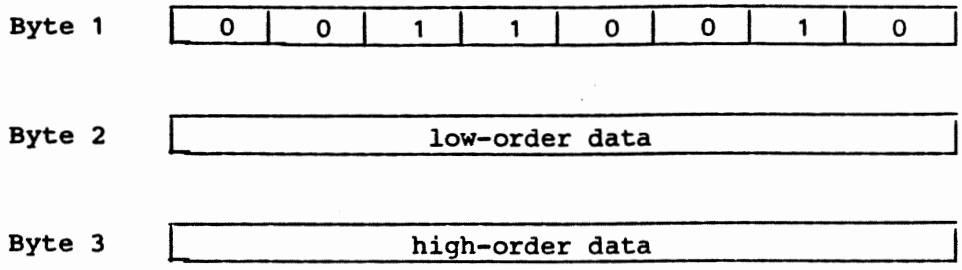
data

Cycles: 3
States: 10
Addressing: immediate/register indirect
Flags: none

Store Accumulator Direct (STA)

Function - stores accumulator content in a memory location specified by the two bytes immediately following the op code. Instruction format:

STA addr (Store Accumulator Direct) (addr)<-(A)



Cycles: 4
States: 13
Addressing: direct
Flags: none

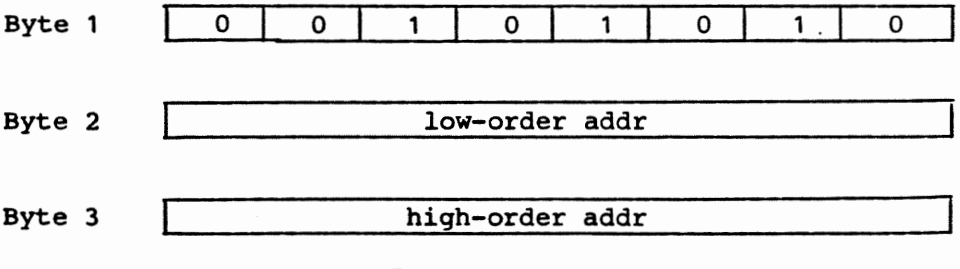
Load H and L Registers Direct (LHLD)

Function - loads two consecutive bytes from memory into H and L registers (H-Pair). The address of the first byte is specified by the two bytes immediately following the op code. The address of the second byte is the next higher address. Instruction format:

LHLD (Load H and L Direct) $(L) \leftarrow (addr_H\ addr_L)$

$(H) \leftarrow (addr_H\ addr_{L+1})$

The content of the memory location whose address is specified in byte 2 and byte 3 of the instruction is moved to register L. The content of the memory location at the succeeding address is moved to register H.



Cycles: 5
States: 16
Addressing: direct
Flags: none

Store Accumulator Indirect (STAX)

Function - stores accumulator content in memory location specified by register pair (rp) content. Only register pair B or D may be used as register pair. Instruction format:

STAX r_H (Store Accumulator Indirect) ((rp))<-(A)

Register A content is moved to the memory location whose address is in the register pair (rp). Note: r_H is restricted to B (registers B and C) or D (registers D and E).

0	0	R	R	0	0	1	0

(RR is 00 or 01)

Cycles: 2
States: 7
Addressing: register indirect
Flags: none

Exchanged H and L with D and E (XCHG)

Function - interchanges data between register pairs H and D. Instruction format:

XCHG (Exchange H and L with D and E) (H) <-> (D)

(L) <-> (E)

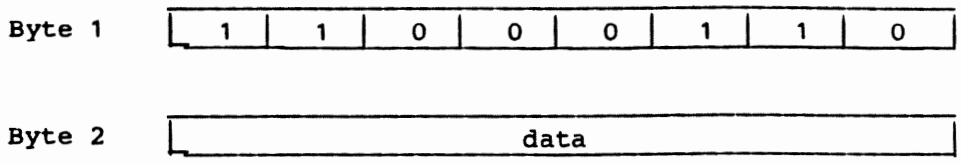
Registers H and L content is exchanged with that of registers D and E respectively.

1	1	1	0	1	0	1	1

Cycles: 1
States: 4
Addressing: register
Flags: none

ADI data (Add Immediate) (A)<-(A) + data

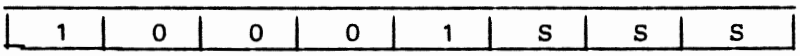
The second byte of the instruction added to the accumulator content. The result is placed in the accumulator.



Cycles: 2
States: 7
Addressing: immediate
Flags: Z,S,P,CY,AC

ADC r (Add Register with Carry) (A) = (A) + (r) + (CY)

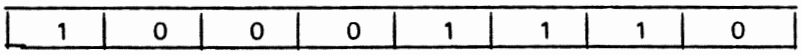
Register r content and the carry bit are added to the accumulator content. The result is placed in the accumulator.



Cycles: 1
States: 4
Addressing: register
Flags: Z,S,P,CY,AC

ADC M (Add Memory with Carry) (A)<-(A) + ((H) (L)) + (CY)

The content of the memory location whose address is in the H and L registers and the CY flag are added to the accumulator. The result is placed in the accumulator.



Cycles: 2
States: 7
Addressing: register indirect
Flags: Z,S,P,CY,AC

SUB M (Subtract Memory) (A)<-(A) - ((H) (L))

The content of the memory location whose address is in the H and L registers is subtracted from the accumulator content. The result is placed in the accumulator.

1	0	0	1	0	1	1	0

Cycles: 2
States: 7
Addressing: register indirect
Flags: Z,S,P,CY,AC

SUI data (Subtract Immediate) (A)<-(A) - data

The second byte of the instruction is subtracted from the content of the accumulator content. The result is placed in the accumulator.

1	1	0	1	0	1	1	0

Cycles: 2
States: 7
Addressing: immediate
Flags: Z,S,P,CY,AC

SBB r (Subtract Register with Borrow) (A) = (A) - (r) - (CY)

Register r content and the CY flag are subtracted from the accumulator. The result is placed in the accumulator.

1	0	0	1	1	S	S	S

(See D.1.4)

Cycles: 2
States: 7
Addressing: register indirect
Flags: Z,S,P,CY,AC

INR M (Increment Memory) ((H)(L))<-((H)(L)) + 1

The content of the memory location whose address in the H and L registers is incremented. Note: All condition flags except CY are affected.

0	0	1	1	0	1	0	0

Cycles: 3
States: 10
Addressing: register indirect
Flags: Z,S,P,AC

INX r_H (Increment Register Pair) (rp)<-(rp) + 1

Register pair (r_H r_L) content is incremented. Note: No condition flags are affected.

0	0	R	R	0	0	1	1

(See D.1.5)

Cycles: 1
States: 5
Addressing: register
Flags: none

Decrement Instructions (DCR, DCX)

Function - decrements a register, memory byte or register pair. Instruction formats:

DCR r (Decrement Register) (r)<-(r) - 1

Register r content is decremented. Note: All condition flags except CY are affected.

0	0	D	D	D	1	0	1

(See D.1.4)

Cycles: 1
States: 5
Addressing: register
Flags: Z,S,P,AC

0	0	R	R	1	0	0	1

(See D.1.5)

Cycles: 3
States: 10
Addressing: register
Flags: CY

Decimal Adjust Accumulator (DAA)

Function - adjusts the eight-bit number in the accumulator to form two four-bit binary coded-decimal digits by the following process:

1. If the value of the least significant 4 bits of the accumulator is greater than 9 or if the AC flag is set, 6 is added to the accumulator.

2. If the value of the most significant 4 bits of the accumulator is now greater than 9, or if the CY flag is set, 6 is added to the most significant 4 bits of the accumulator.

DAA (Decimal Adjust Accumulator)

NOTE: All flags are affected according to the standard rules.

0	0	1	0	0	1	1	1

Cycles: 3
States: 10
Flags: Z,S,P,CY,AC

D.1.9 Logical Instructions

[ANA r ANA M ANI data
XRA r XRA M XRI data
ORA r ORA M ORI data
CMP r CMP M CPI data
RLC RRC RAL RAR
CMA CMC STC]

Function - performs logical (Boolean) operations on data in registers or memory and on condition flags; unless otherwise indicated, the Zero (Z), Sign (S), Parity (P), Auxiliary Carry (AC) and Carry (CY) flags will be affected according to the standard rules. The instructions are: AND, OR, XOR, compare, rotate, and complement.

Cycles:	2
States:	7
Addressing:	immediate
Flags:	Z,S,P,CY,AC

Exclusive OR (XRA, XRI)

Function - exclusive-ORs a byte or memory or register content with the accumulator content, and places the result in the accumulator. Instruction format:

XRA r (Exclusive OR Register) (A)<-(A)⊻(r)

Register r content is exclusive-ORd with the accumulator content. The result is placed in the accumulator. The CY and AC flags are cleared.

1	0	1	0	1	S	S	S

(See D.1.4)
SSS - Source Register

Cycles:	1
States:	4
Addressing:	register
Flags:	Z,S,P,CY,AC

XRA M (Exclusive OR Memory) (A)<-(A)⊻((H)(L))

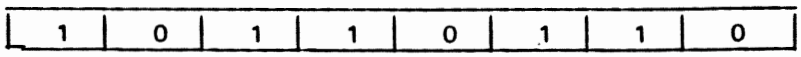
The content of the memory location whose address is contained in the H and L registers is exclusive-ORd with the accumulator content. The result is placed in the accumulator. The CY and AC flags are cleared.

1	0	1	0	1	1	1	0

Cycles:	2
States:	7
Addressing:	register indirect
Flags:	Z,S,P,CY,AC

ORA M (OR Memory) (A)<-(A) V ((H) (L))

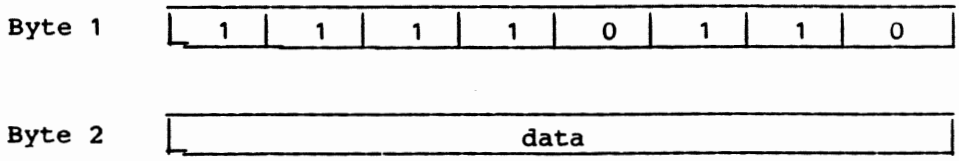
The content of the memory location whose address is contained in the H and L registers is ORd with the content of the accumulator. The result is placed in the accumulator. The CY and AC flags are cleared.



Cycles: 2
States: 7
Addressing: register indirect
Flags: Z,S,P,CY,AC

ORI data (OR Immediate) (A)<-(A) V data

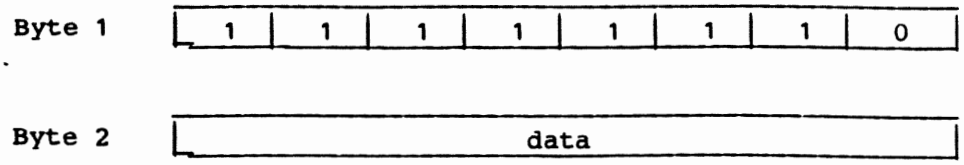
The content of the second byte of the instruction is ORd with the accumulator content. The result is placed in the accumulator. The CY and AC flags are cleared.



Cycles: 2
States: 7
Addressing: immediate
Flags: Z,S,P,CY,AC

Compare (CMP,CPI)

Function - compares the contents of the accumulator with a memory byte or the contents of a register or memory location. The condition flags are affected by the result, but the content of the accumulator is left unchanged.



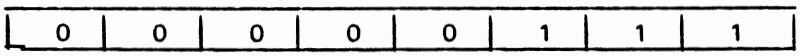
Cycles: 2
States: 7
Addressing: immediate
Flags: Z,S,P,CY,AC

Rotate (RLC, RRC, RAL, RAR)

Function - recirculate accumulator contents one position to the right or left; affect only the Carry flag (CY). Instruction formats:

RLC (Rotate Left)

Accumulator content is rotated left one position. That is, all bits are shifted one position, with the highest-ordered bit going to the lowest-order position. The CY flag is also set to the value shifted out of the highest-order bit position. Only the CY flag is affected.

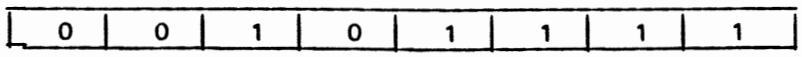


Cycles: 1
States: 4
Flags: CY

RRC (Rotate Right)

Accumulator content is rotated right one position. That is, all bits are shifted right one position, with the lowest-ordered bit going to the highest-order position. The CY flag is also set to the value shifted out of the low order bit position. Only the CY flag is affected.

CMA (Complement Accumulator) (A)<-(A)



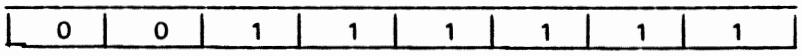
Cycles: 1
States: 4
Flags: none

Complement Carry and Set Carry (CMC, STC)

Function - directly control the setting of the Carry flag; affects no other flags. Instruction formats:

CMC (Complement Carry) (CY)<-($\overline{CY}$)

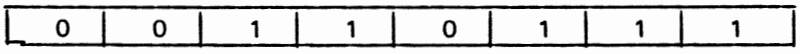
The CY flag is complemented. No other flags are affected.



Cycles: 1
States: 4
Flags: CY

STC (Set Carry) (CY)<-1

The CY flag is set to 1. No other flags are affected.

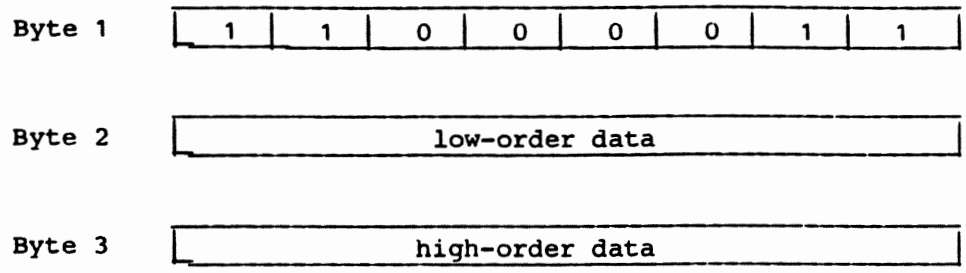


Cycles: 1
States: 4
Flags: CY

Conditional jump instructions occur for any condition flag except Auxiliary Carry (AC). Instruction formats:

JMP addr (Unconditional Jump) (PC)<-$addr_H$ addr

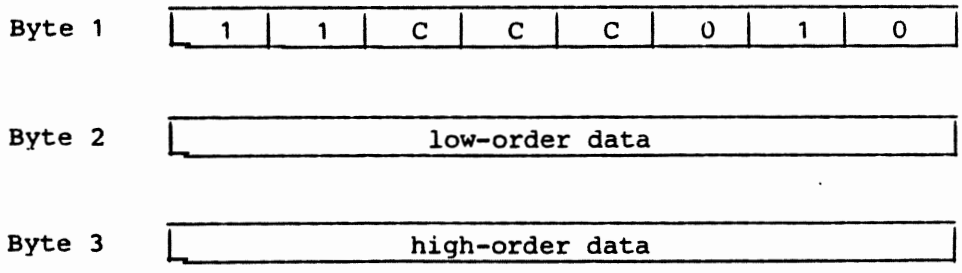
Control is transferred to the instruction whose address is specified in byte 3 and byte 2 of the current instruction.



Cycles: 3
States: 10
Addressing: immediate
Flags: none

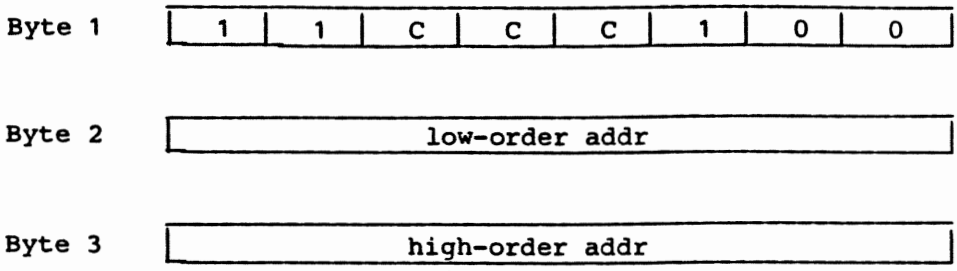
JZ addr (Jump if Z = 1 If (CCC), (PC)<- $addr_H$ $addr_L$
JNZ addr Jump if Z = 0
JC addr Jump if CY = 1
JNC addr Jump if CY = 0
JPE addr Jump if P = 1
JPO addr Jump if P = 0
JM addr Jump if S = 1
JP addr Jump if S = 0)

If the specified condition is true, control is transfered to the instruction whose address is specified in byte 2 and byte 3 of the current instruction; otherwise, control continues sequentially.



Cycles: 3
States: 10
Addressing: immediate
Flags: none

If the specified condition is true, the transfers specified in the Call instruction (see above) are performed; otherwise control continues sequentially.



Cycles: 3/5
States: 11/17
Addressing: immediate/register indirect
Flags: none

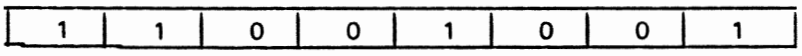
Return (RET,RZ,RNZ,RC,RNC,RPO,RPE,RP,RM)

Function - transfer program control back to a location from which an exit had occurred during a Call instruction. This is accomplished by transferring, or "popping" the top two bytes from the stack into the program counter. Return instructions may be unconditional or conditional. Instruction formats:

RET (Unconditional Return)

(PC_L)<-((SP))
(PC_H)<-((SP) + 1)
(SP)<-(SP) + 2

The content of the memory location whose address is specified in register SP is moved to the low-order bytes of register PC. The content of the memory location whose address is one more than the content of register SP is moved to the high-order bytes of register PC. The content of register SP is incremented by 2.



Cycles: 3
States: 10
Addressing: register indirect
Flags: none

1	1	N	N	N	1	1	1

Cycles: 3
States: 11
Addressing: register indirect
Flags: none

NNN	LOCATION
000	0000_{16}
001	0000_{16}
010	0010_{16}
011	0018_{16}
100	0020_{16}
101	0028_{16}
110	0030_{16}
111	0038_{16}

15	14	13	12	11	10	9	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	N	N	N	0	0	0

Program Counter After Restart

Load PC From H and L Register (PCHL)

Function - changes the PC by loading the contents of the H register into the upper byte of the PC and the contents of the L register into the lower byte of the PC. Program control is transferred to the new address.

PCHL (Jump H and L indirect; move H and L to PC) (PC_H)<-(H)
(PC_L)<-(L)

1	1	1	0	1	0	0	1

Cycles: 1
States: 5
Addressing: register
Flags: none

Register A content is moved to the memory location whose address is one less than register SP. The contents of the condition flags are assembled into a processor status word and the word is moved to the memory location whose address is two less than the register SP content. Register SP content is decreased by two.

1	1	1	1	0	1	0	1

Cycles: 3
States: 11
Addressing: register indirect
Flags: none

Pop (POP B, POP D, POP H)

Functions - load register pairs with data contained in the stack. Instruction formats:

POP r_H (pop) (r_L)<-((SP))
(r_H)<-((SP) + 1)
(SP)<-(SP) + 2

The content of the memory location whose address is specified by the content of register Stack Pointer (SP) is moved to the low-order register of register pair (r_H r_L). The content of the memory location whose address is one more than the content of register SP is moved to the high-order register of r_H r_L. The content of register SP is increased by two. Note: Register pair r_H r_L = SP may not be specified.

1	1	R	R	1	0	0	1

(See D.1.5)

Cycles: 3
States: 10
Addressing: register indirect
Flags: none

SPHL (Move H and L to SP) (SP)<-(H)(L)

Registers H and L (16-bits) contents are moved to register SP.

1	1	1	1	1	0	0	1

Cycles: 1
States: 5
Addressing: register
Flags: none

D.1.12 I/O and Machine Control Instructions

I/O and Machine Control Instruction Group [EI DI IN port OUT port HLT NOP RIM SIM] Function - transfers I/O data; controls interrupt and machine. Each instruction is a single byte which, when executed, does not affect any condition flags.

Interrupt Control (EI, DI)

Function - control interrupts. (See also RIM, SIM). Two instructions are provided for the control of interrupts. An enable interrupt (EI) must be executed before the microprocessor will recognize any interrupt requests from the system's devices. Once the microprocessor recognizes an interrupt, it will ignore all further requests until another EI is executed. If the programmer wishes to ignore interrupts, then a disable interrupt (DI) instruction is used. Instruction formats:

EI (Enable Interrupts)

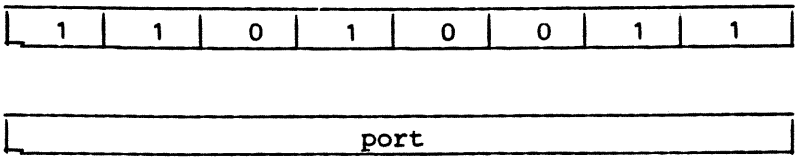
The interrupt system is enabled following the execution of the next instruction.

1	1	1	1	1	0	1	1

Cycles: 1
States: 4
Flags: none

OUT port (Output) (port data)<-(A)

Register A content is placed on the eight bit bi-directional data bus for transmission to the specified port.



Cycles: 3
States: 10
Addressing: direct
Flags: none

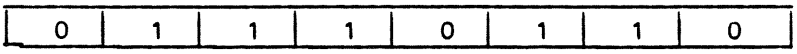
Machine Control (HLT, NOP)

Function - deactivate the microprocessor; stop processing of microprocessor's instructions; execute an operation that has no effect.

Instruction formats:

HLT (Halt)

The processor is stopped. The registers and flags are unaffected.



Cycles: 3
States: 10
Addressing: immediate
Flags: none

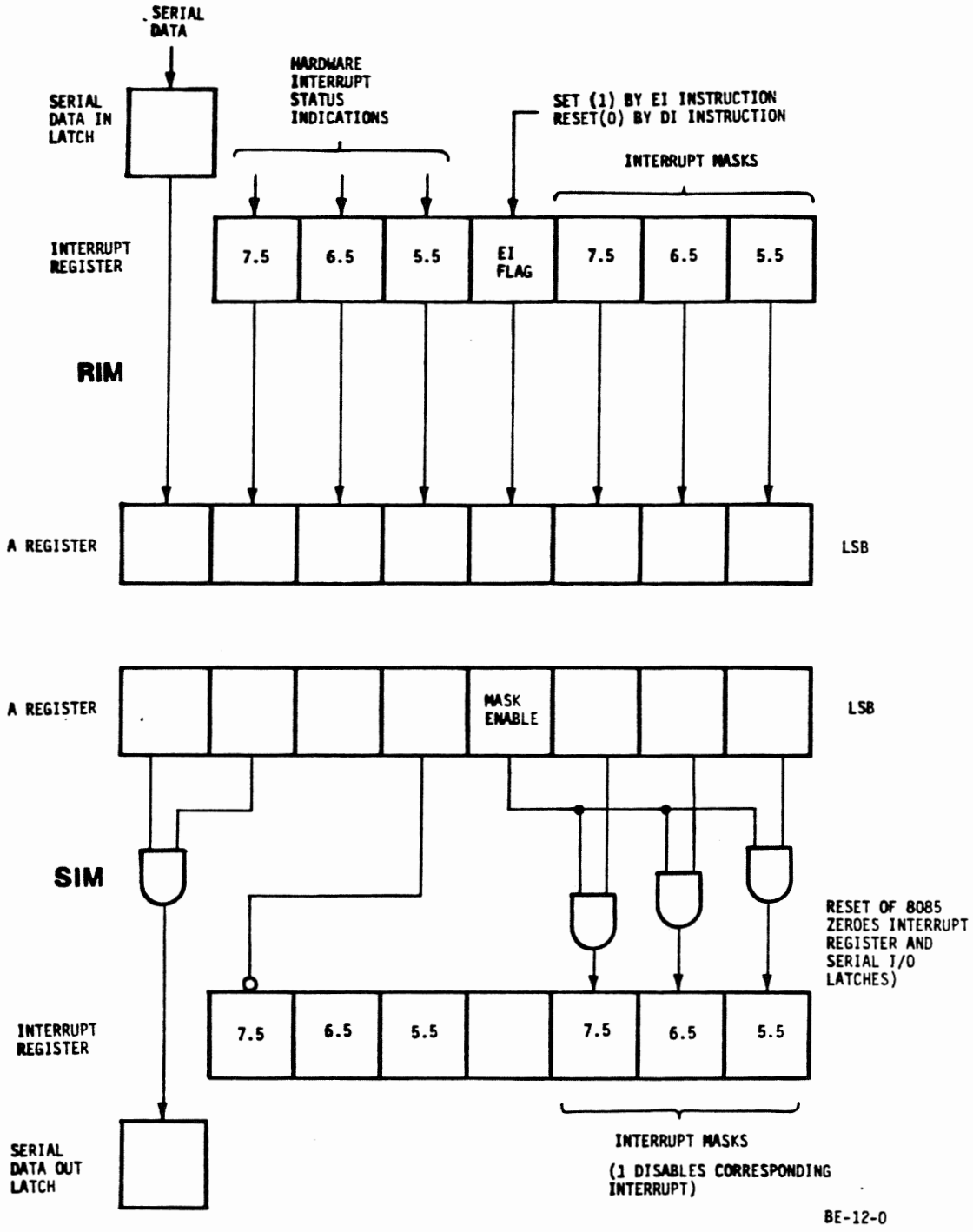


Figure D-1 Effect of Executing RIM and SIM Instructions

TABLE D-1 8085 INSTRUCTION SET SUMMARY

Mnemonic	Description	Operation	Op Code D7	D6	D5	D4	D3	D2	D1	D0	Bytes	Machine Cycles M	Micro Cycles T	Status Flags S	Z	AC	P	CY
DATA TRANSFER GROUP																		
LDA	Load Accumulator Direct	(A)<-((byte 3)(byte 2))	0	0	1	1	1	0	1	0	3	4	13					
LDAX B	Load Accumulator Indirect	(A)<-((BC))	0	0	0	0	1	0	1	0	1	2	7					
LDAX D	Load Accumulator Indirect	(A)<-((DE))	0	0	0	1	1	0	1	0	1	2	7					
LHLD	Load H and L Direct	(L)<-((byte 3)(byte 2)) (H)<-((byte 3)(byte 2)+1)	0	0	1	0	1	0	1	0	3	5	16					
LXI B	Load Immediate Registers B and C	(B)<-byte 3 (C)<-byte 2	0	0	0	0	0	0	0	1	3	3	10					
LXI D	Load Immediate Registers D and E	(D)<-byte 3 (E)<-byte 2	0	0	0	1	0	0	0	1	3	3	10					
LXI H	Load Immediate Registers H and L	(H)<-byte 3 (L)<-byte 2	0	0	1	0	0	0	0	1	3	3	10					
LXI SP	Load Immediate Stack Pointer	(SPL)<-byte 2 (SPH)<-byte 3	0	0	1	1	0	0	0	1	3	3	10					
MOV M,r	Move to Memory	((HL))<-(r)	0	1	1	1	0	S	S	S	1	2	7					
MOV r,M	Move from Memory	(r)<-((HL))	0	1	D	D	D	1	1	0	1	2	7					
MOV r1,r2	Move Registers	(r1)<-(r2)	0	1	D	D	D	S	S	S	1	1	4					
MVI M	Move to Memory Immediate	((HL))<-byte 2	0	0	1	1	0	1	1	0	2	3	10					
MVI r	Move Immediate	(r)<-byte 2	0	0	D	D	D	1	1	0	2	2	7					
SHLD	Store H and L Direct	((byte 3)(byte 2))<-(L) ((byte 3)(byte 2)+1)<-(H)	0	0	1	0	0	0	1	0	3	5	16					
STA	Store Accumulator Direct	((byte 3)(byte 2))<-(A)	0	0	1	1	0	0	1	0	3	4	13					
STAX B	Store Accumulator Indirect	((BC))<-(A)	0	0	0	0	0	0	1	0	1	2	7					
STAX D	Store Accumulator Indirect	((DE))<-(A)	0	0	0	1	0	0	1	0	1	2	7					
XCHG	Exchange H and L with D and E	(H)<->(D) (L)<->(E)	1	1	1	0	1	0	1	1	1	1	4					
ARITHMETIC GROUP																		
ACI	Add Immediate with Carry	(A)<-(A) + byte 2 + (CY)	1	1	0	0	1	1	1	0	2	2	7	*	*	*	*	*
ADC M	Add Memory with Carry	(A)<-(A) + ((HL)) + (CY)	1	0	0	0	1	1	1	0	1	2	7	*	*	*	*	*
ADC r	Add Register with Carry	(A)<-(A) + (r) + (CY)	1	0	0	0	1	S	S	S	1	1	4	*	*	*	*	*
ADD M	Add Memory	(A)<-(A) + ((HL))	1	0	0	0	0	1	1	0	1	2	7	*	*	*	*	*
ADD r	Add Register	(A)<-(A) + (r)	1	0	0	0	0	S	S	S	1	1	4	*	*	*	*	*
ADI	Add Immediate	(A)<-(A) + byte 2	1	1	0	0	0	1	1	0	2	2	7	*	*	*	*	*
DAA	Decimal Adjust Accumulator	8 bit number in Accumulator is converted to two 4-bit BCD numbers.	0	0	1	0	0	1	1	1	1	1	4	*	*	*	*	*
DAD B	Add B and C to H and L	(HL)<-(HL) + (BC)	0	0	0	0	1	0	0	1	1	3	10					*
DAD D	Add D and E to H and L	(HL)<-(HL) + (DE)	0	0	0	1	1	0	0	1	1	3	10					*
DAD H	Add H and L to H and L	(HL)<-(HL) + (HL)	0	0	1	0	1	0	0	1	1	3	10					*
DAD SP	Add Stack Pointer to H and L	(HL)<-(HL) + (SP)	0	0	1	1	1	0	0	1	1	3	10					*
DCR M	Decrement Memory	((HL))<-((HL)) - 1	0	0	1	1	0	1	0	1	1	3	10	*	*	*	*	
DCR r	Decrement Register	(r)<-(r) - 1	0	0	D	D	D	1	0	1	1	1	4	*	*	*	*	
DCX B	Decrement Registers B and C	(BC)<-(BC) - 1	0	0	0	0	1	0	1	1	1	1	6					
DCX D	Decrement Registers D and E	(DE)<-(DE) - 1	0	0	0	1	1	0	1	1	1	1	6					
DCX H	Decrement Registers H and L	(HL)<-(HL) - 1	0	0	1	0	1	0	1	1	1	1	6					
DCX SP	Decrement Stack Pointer	(SP)<-(SP) - 1	0	0	1	1	1	0	1	1	1	1	6					
INR M	Increment Memory	((HL))<-((HL)) + 1	0	0	1	1	0	1	0	0	1	3	10	*	*	*	*	
INR r	Increment Register	(r)<-(r) + 1	0	0	D	D	D	1	0	0	1	1	4	*	*	*	*	
INX B	Increment Registers B and C	(BC)<-(BC) + 1	0	0	0	0	0	0	1	1	1	1	6					
INX D	Increment Registers D and E	(DE)<-(DE) + 1	0	0	0	1	0	0	1	1	1	1	6					
INX H	Increment Registers H and L	(HL)<-(HL) + 1	0	0	1	0	0	0	1	1	1	1	6					
INX SP	Increment Stack Pointer	(SP)<-(SP) + 1	0	0	1	1	0	0	1	1	1	1	6					
SBB M	Subtract Memory with Borrow	(A)<-(A)-((HL))-(CY)	1	0	0	1	1	1	1	0	1	2	7	*	*	*	*	*
SBB r	Subtract Register with Borrow	(A)<-(A)-(r)-(CY)	1	0	0	1	1	S	S	S	1	1	4	*	*	*	*	*
SBI	Subtract Immediate with Borrow	(A)<-(A)-byte 2-(CY)	1	1	0	1	1	1	1	0	2	2	7	*	*	*	*	*
SUB M	Subtract Memory	(A)<-(A)-((HYL))	1	0	0	1	0	1	1	0	1	2	7	*	*	*	*	*
SUB r	Subtract Register	(A)<-(A)-(r)	1	0	0	1	0	S	S	S	1	1	4	*	*	*	*	*
SUI	Subtract Immediate	(A)<-(A)-byte 2	1	1	0	1	0	1	1	0	2	2	7	*	*	*	*	*
LOGICAL GROUP																		
ANA M	AND Memory	(A)<-(A)∧((HL))	1	0	1	0	0	1	1	0	1	2	7	*	*		*	0
ANA r	AND Register	(A)<-(A)∧(r)	1	0	1	0	0	S	S	S	1	1	4	*	*		*	0
ANI	AND Immediate	(A)<-(A)∧byte 2	1	1	1	0	0	1	1	0	2	2	7	*	*		*	0
CMA	Complement Accumulator	(A)<-$\overline{(A)}$	0	0	1	0	1	1	1	1	1	1	4					
CMC	Complement Carry	(CY)<-$\overline{(CY)}$	0	0	1	1	1	1	1	1	1	1	4					*
CMP M	Compare Memory	(A)vs.((HL)) } A unchanged;	1	0	1	1	1	1	1	0	1	2	7	*	a	*	*	a
CMP r	Compare Register	(A)vs.(r) } status flags	1	0	1	1	1	S	S	S	1	1	4	*	b	*	*	b
CPI	Compare Immediate	(A)vs.byte 2 } affected.	1	1	1	1	1	1	1	0	2	2	7	*	c	*	*	c
ORA M	OR Memory	(A)<-(A) V ((HL))	1	0	1	1	0	1	1	0	1	2	7	*	*	0	*	0
ORA r	OR Register	(A)<-(A) V (r)	1	0	1	1	0	S	S	S	1	1	4	*	*	0	*	0
ORI	OR Immediate	(A)<-(A) V byte 2	1	1	1	1	0	1	1	0	2	2	7	*	*	0	*	0
RAL	Rotate Left through Carry	(A_{n+1})<-(A_n); (CY)<-(A_7) (A_0)<-(CY)	0	0	0	1	0	1	1	1	1	1	4					*
RAR	Rotate Right through Carry	(A_n)<-(A_{n+1}); (CY)<-(A_0) (A_7)<-(CY)	0	0	0	1	1	1	1	1	1	1	4					*
RLC	Rotate Left	(A_{n+1})<-(A_n); (A_0)<-(A_7) (CY)<-(A_7)	0	0	0	0	0	1	1	1	1	1	4					*
RRC	Rotate Right	(A_n)<-(A_{n+1}); (A_7)<-(A_0) (CY)<-(A_0)	0	0	0	0	1	1	1	1	1	1	4					*
STC	Set Carry	(CY)<-1	0	0	1	1	0	1	1	1	1	1	4					1
XRA M	Exclusive OR Memory	(A)<-(A) ⊻ ((HL))	1	0	1	0	1	1	1	0	1	2	7	*	*	0	*	0
XRA r	Exclusive OR Register	(A)<-(A) ⊻ (r)	1	0	1	0	1	S	S	S	1	1	4	*	*	0	*	0
XRI	Exclusive OR Immediate	(A)<-(A) ⊻ byte 2	1	1	1	0	1	1	1	0	2	2	7	*	*	0	*	0

TABLE D-1 (cont.)

Mnemonic	Description	Operation	Op Code D7	D6	D5	D4	D3	D2	D1	D0	Bytes	Machine Cycles M	Micro Cycles T	Status Flags S	Z	AC	P	CY
STACK, I/O, AND MACHINE CONTROL GROUP																		
IN	Input	(A)<-(port data)	1	1	0	1	1	0	1	1	2	3	10					
OUT	Output	(port data)<-(A)	1	1	0	1	0	0	1	1	2	3	10					
HLT	Halt	Processor is stopped, registers and flags are unaffected.	0	1	1	1	0	1	1	0	1	2	7					
NOP	No Operation	No operation is performed, registers and flags are unaffected	0	0	0	0	0	0	0	0	1	1	4					
DI	Disable Interrupts	The Interrupt system id disabled following the execution of the DI instruction.	1	1	1	1	0	0	1	1	1	1	4					
EI	Enable Interrupts	The interrupt system is enabled following the execution of the DI instruction.	1	1	1	1	1	0	1	1	1	1	4					
RIM	Read Interrupts, Masks and Serial Input Data	$(A_6\text{-}A_0)$<-(I) (A_7)<-(SID)	0	0	1	0	0	0	0	0	1	1	4					
SIM	Set Interrupts, Masks and Serial Output Data	Set Interrupt Register and SOD latch.	0	0	1	1	0	0	0	0	1	1	4					
POP B	Pop Registers B and C on Stack	(C)<-((SP)) (B)<-((SP) + 1) (SP)<-(SP) + 2	1	1	0	0	0	0	0	1	1	3	10					
POP D	Pop Registers D and E off Stack	(D)<-((SP)) (E)<-((SP) + 1) (SP)<-(SP) + 2	1	1	0	1	0	0	0	1	1	3	10					
POP H	Pop Registers H and L off Stack	(H)<-((SP)) (L)<-((SP) + 1) (SP)<-(SP) + 2	1	1	1	0	0	0	0	1	1	3	10					
POP PSW	Pop Accumulator and Flags off Stack	(CY)<-$((SP))_0$ (P)<-$((SP))_2$ (AC)<-$((SP))_4$ (Z)<-$((SP))_6$ (S)<-$((SP))_7$ (A)<-((SP) + 1) (SP)<-(SP) + 2	1	1	1	1	0	0	0	1	1	3	10	*	*	*	*	*
PUSH B	Push Registers B and C on Stack	((SP) - 1)<-(B) ((SP) - 2)<-(C) (SP)<-(SP) - 2	1	1	0	0	0	1	0	1	1	3	12					
PUSH D	Push Registers D and E on Stack	((SP) - 1)<-(D) ((SP) - 2)<-(E) (SP)<-(SP) - 2	1	1	0	1	0	1	0	1	1	3	12					
PUSH H	Push Registers H and L on Stack	((SP) - 1)<-(H) ((SP) - 2)<-(L) (SP)<-(SP) - 2	1	1	1	0	0	1	0	1	1	3	12					
PUSH PSW	Push Accumulator and Flags on Stack	((SP) - 1)<-(A) $((SP) - 2)_0$<-(CY) $((SP) - 2)_1$<-1 $((SP) - 2)_2$<-(P) $((SP) - 2)_3$<-0 $((SP) - 2)_4$<-(AC) $((SP) - 2)_5$<-0 $((SP) - 2)_6$<-(Z) $((SP) - 2)_7$<-(S) (SP)<-(SP) - 2	1	1	1	1	0	1	0	1	1	3	12					
SPHL	Move H and L to Stack Pointer	(SP)<-(H)(L)	1	1	1	1	1	0	0	1	1	1	6					
XTHL	Exchange Top of Stack with H and L	(L)<—>((SP)) (H)<—>((SP) + 1)	1	1	1	0	0	0	1	1	1	5	16					

CONDITION FLAGS AND STANDARD RULES

There are five condition flags associated with the execution of instructions on the INS8080A. They are Zero, Sign, Parity, Carry, and Auxiliary Carry, and each flag is represented by a 1-bit register in the CPU. A flag is "set" by forcing the bit to 1, "reset" by forcing the bit to 0. The bit positions of the flags are indicated in the PUSH and POP PSW instructions.

Unless indicated otherwise, when an instruction affects a flag, it affects it in the following manner:

ZERO (Z): If the result of an instruction has the value 0, this flag is set; otherwise, it is reset.

SIGN (S): If the most significant bit of the result of the operation has the value 1, this flag is set; otherwise, it is reset.

PARITY (P): If the module 2 sum of the bits of the result of the operation is 0 (that is, if the result has even parity), this flag is set; otherwise, it is reset (that is, if the result has odd parity).

CARRY (CY): If the instruction resulted in a carry (from addition) or a borrow (from subtraction or a comparison) out of the high-order bit, this flag is set; otherwise, it is reset.

AUXILIARY CARRY (AC): If the instruction caused a carry out of bit 3 and into bit 4 of the resulting value, the auxiliary carry is set; otherwise, it is reset. This flag is affected by single-precision additions, subtractions, increments, decrements, comparisons, and logical operations; however, AC is used principally with additions and increments preceding a DAA (Decimal Adjust Accumulator) instruction.

The flags affected by these instructions are indicated by a "*" or (where the flag is set or reset) by "1" or "0" in the flag column in the summary table. Flags are not affected by Branch instructions. The notations a, b, c in the flag columns are explained below:

a. Z = 1 if (A) = ((HL)); CY = 1 if (A) < ((HL))

b. Z = 1 if (A) = (r); CY = 1 if (A) < (r)

c. Z = 1 if (A) = byte 2; CY = 1 if (A) < byte 2

In the Machine Cycles and Microcycles columns, the first number of a pair (e.g., the "3" of "3/5") signifies the number of Machine Cycles or Microcycles that the execution of the instruction takes when the condition is not satisfied; the second number of the pair signifies the number of Machine Cycles or Microcycles that the execution of the instruction takes when the condition is satisfied.