DG24 User's Manual

Real Time Devices

DG24 User's Manual

A User's Guide to the DG24
Digital I/O Interface

Real Time Devices Inc.
1930 Park Forest Avenue
P.O. Box 906
State College, PA 16804

First Printing - April 1987

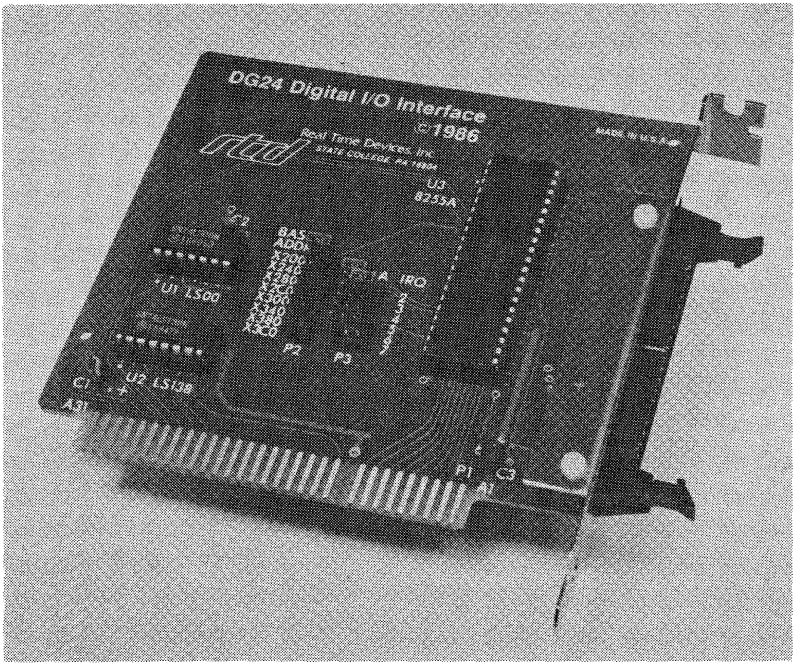
Printed in U.S.A.

Contents

Page

Illustrations

Tables


DG24 Digital I/O Interface
©1986
Real Time Devices, Inc.
U3
8255A
U1 LS00
U2 LS08
IRQ
P1
P2
P3

Chapter 1

Introduction

The DG24 is a highly versatile digital I/O port for the IBM PC/XT/AT, or compatible, computer. The board uses the popular 8255 Programmable Peripheral Interface (PPI) chip and provides for the control or monitoring of 24 digital I/O signals. The 8255 used is capable of 10 MHz transfer rates and therefore does not require WAIT states when using a PC/AT. The DG24's base address is jumper selectable and interrupts are supported.

The PPI may be configured in combinations of three basic modes of operation: Basic I/O, Strobed I/O, and Bi-directional Strobed I/O. Applications of the DG24 include instrument interfacing, event sensing, process control, and automated testing.

All 24 digital lines, as well as +/-12 and +5 volts, the PC's reset signal, and digital ground, are accessible through a 40-pin header connector at the end of the board. This connector is compatible with Real Time Devices' XB40 I/O extender board and XC40 expansion cable. The XB40 consists of two 20-pin screw terminals and a prototype area. The screw terminals allow wires to easily connect to the DG24 and the prototype area allows development of custom application circuits. The XC40 is a cable assembly which terminates in a 40-pin wire wrap header connector. This connector is suitable for installation in standard perf-board material.

The software included with the DG24 provides sample programs for controlling each of the PPI operating modes. Example CALL statements are also included for applications requiring high-speed data transfers.

This manual has been organized into three chapters, with a group of appendices containing reference material.

CHAPTER 1 briefly describes the DG24 operating features, I/O capability, and software.

CHAPTER 2 explains how to install the DG24 in your computer. This incudes selecting the base address and interrupt capability, and connecting signals to the I/O connector.

CHAPTER 3 describes how to control the DG24's PPI. Detailed specifications of the PPI are provided which explain its various operating modes and communication with the Control Word and I/O ports. Some considerations are also given if you require the use of interrupts.

APPENDICES contain technical information related to your DG24. This includes the DG24 and 8255 PPI specifications, I/O connector pin-out, and connector types. References and warranty information are also provided.

Every effort has been made to design a quality, easy to use, yet low cost digital I/O interface board. We are convinced that you will find the DG24 to be a valuable interfacing tool for your PC.

Chapter 2

Installation

The DG24 plugs into any expansion slot, including a short slot, of an IBM PC/XT/AT or compatible computer. It may be advantageous, therefore, to choose an available short slot inside your computer.

The board's I/O address and interrupt channel are jumper selectable. Preventing possible contention with other devices simply involves changing three jumpers. If the board address is unjumpered or incorrect, the DG24 will not operate. Before installing the board into your computer the jumper selections must be made.

All connections to external signals are made through one 40 pin I/O connector, which can be accessed through the rear of the computer after the board is installed.

JUMPER SETTINGS

Base Address Selection - Connector P2

To select the board's base I/O address, the jumper on the connecter labeled P2 must be positioned to correspond to the address desired. The jumper should be placed horizontally across the pair of header pins beside the base address you select (see Figure 2-1). The base addresses labeled beside connector P2 are hexadecimal values.

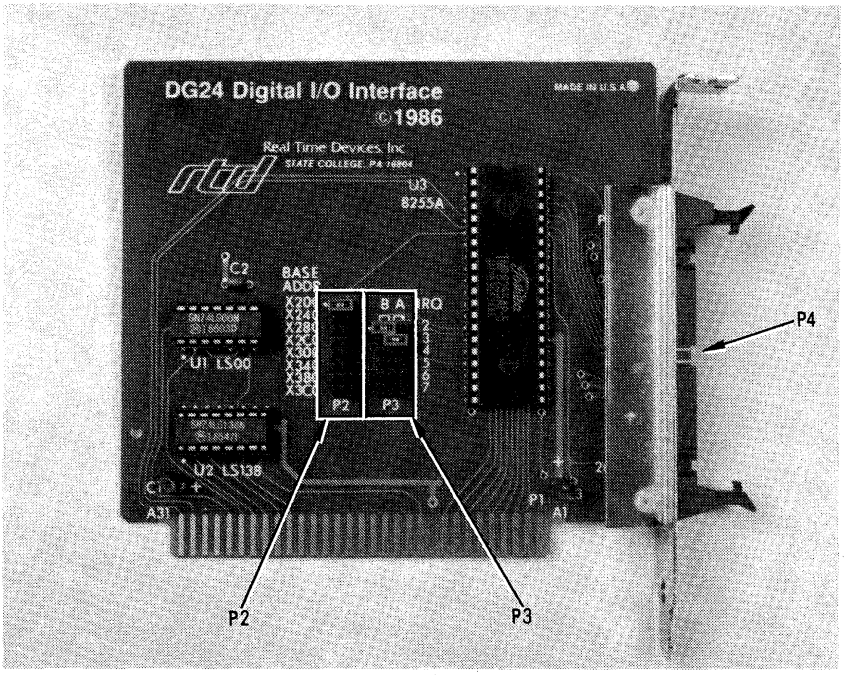
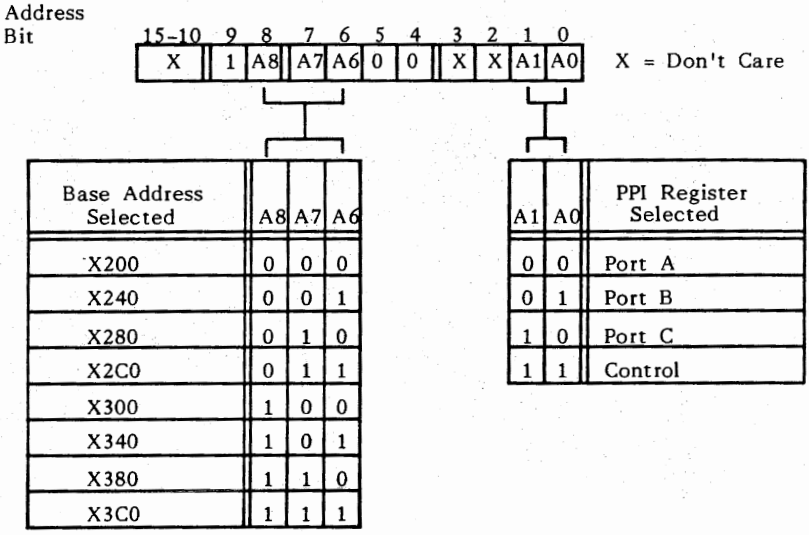


Fig. 2-1 DG24 Component Locations

When choosing a base address, be careful not to use one that will cause contention with another peripheral. The DG24 occupies 16 I/O addresses beginning with the base address selected, however only four addresses are actually used. Chapter 3 "Controlling the 8255 PPI" explains the function of these four addresses. Figure 2-2 shows how the PC's I/O port address bits are decoded by the DG24.



Base Address Selected	A8	A7	A6
X200	0	0	0
X240	0	0	1
X280	0	1	0
X2C0	0	1	1
X300	1	0	0
X340	1	0	1
X380	1	1	0
X3C0	1	1	1

A1	A0	PPI Register Selected
0	0	Port A
0	1	Port B
1	0	Port C
1	1	Control

Fig. 2-2 DG24 I/O Port Address Decode

The DG24 base address has been preset to X'200'. For future reference, you may wish to record the base address you selected in Table 2-1. If the base address is changed from the preset value of X'200', the example software provided with the DG24 will need to be modified to reflect the new value. The procedure to do this is explained in the comments which accompany each of the sample programs.

Interrupt Channel Selection - Connector P3

The DG24 may be configured to generate interrupts during PPI Mode 1 or Mode 2 operation. The two PPI interrupts, INTRA and INTRB, are available at the DG24 P3 connector and are labeled "A" and "B" across the top of the connector. To select the PC interrupt channels used to service these interrupts, position the jumpers on the connecter labled P3 to correspond to the desired interrupt channel numbers. The jumpers should be placed horizontally across the pair of header pins corresponding to INTRA or INTRB and beside the interrupt channel number (see Figure 2-1). Note that INTRA and INTRB must each use a separate PC interrupt channel. If interrupts are not used, the jumpers must be positioned as shown in Figure 2-3.

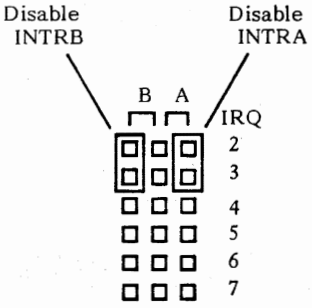


Fig. 2-3 Interrupt Disable Jumper Positions

The DG24 interrupts are preset to the disabled position. For future reference you may wish to record the interrupt channel assignments in Table 2-1.

Table 2-1 DG24 User-Selected Options
I/O Base Address _____ (hex) _____ (decimal)
INTR/IRQ Channel Selection INTRA IRQ _____ INTRB IRQ _____

Chapter 3, "Controlling the 8255 PPI", describes considerations for using the DG24 interrupts.

BOARD INSTALLATION

After selecting the base address and interrupt capability, the DG24 may be installed inside the computer.

1. TURN OFF THE POWER TO YOUR COMPUTER FIRST. Refer to the owner's manual for your computer, and remove the top cover.

2. Select the expansion slot you wish to use and remove the corresponding blank bracket from the rear panel of the computer.

3. Close both ejector latches on the DG24 I/O connecter, and orient the board inside the computer so that the connector protrudes through the rear of the computer, and the card edge connector lines up with the selected expansion slot connector.

4. After you are certain the board lines up correctly, push down on the metal bracket tab and the top of the board until the board is seated firmly in the expansion slot connector.

5. Reinstall the screw that was remove with the blank bracket and replace the cover to your computer.

EXTERNAL CONNECTIONS - Connector P4

All external connections to the DG24 are made to the I/O connector, labeled P4 (see Figure 2-1), which is accessible through the rear panel of the computer after the board is installed. The P4 mating connector type required is listed in Appendix B as well as the pin assignment of all signals associated with the DG24.

To attach the mating connector, first open the ejector tabs on the DG24 I/O connector. Then, observing the keying of both connectors, install the mating connector and push firmly until the ejector tabs snap closed, securing the connector in place.

This completes the installation; your DG24 is now properly configured. Next, you must decide how to control the PPI for your specific application.

Chapter 3

Controlling the 8255 PPI

As shown in the block diagram, Figure 3-1, the DG24 provides all the necessary interfacing signals to control the 8255 PPI.

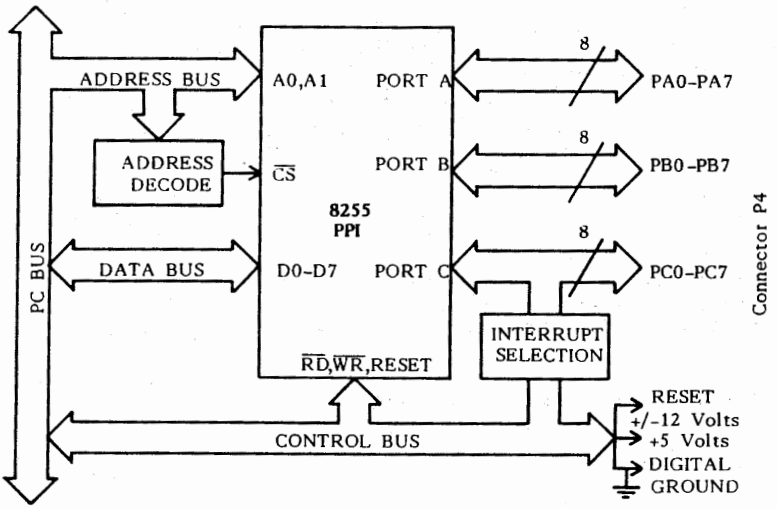


Fig. 3-1 DG24 Block Diagram

These signals are used to communicate with the internal registers of the PPI. Table 3-1 shows how the DG24 maps the PPI registers to four contiguous I/O addresses, beginning with the base address you selected in Chapter 2.

Table 3-1 PPI Register/DG24 I/O Address Assignments

PPI Register	Base Address +
Port A	0
Port B	1
Port C	2
Control Word	3

The 8255 PPI is a versatile digital I/O interface chip; your application will determine how the I/O ports should be configured and the different operating modes selected. The accompaning data sheet, reprinted by permission of Intel Corporation, Copyright 1981, presents a very good discussion of controlling this chip.

8255 DESCRIPTION

The first section of the data sheet entitled "8255A Functional Description" gives a general explanation of the I/O ports. This and the information contained in the section entitled "8255A Operational Description" will allow you to determine how to most efficiently utilize the I/O ports for your application.

The first part of the Operational Description explains how the Control Word is used to select the operating modes of the PPI and is also used to individually set or reset the Port C bits. This bit set/reset feature is useful for controlling separate bits without effecting the other bits of Port C. The bit set/reset feature can be used with Port C bits only.

If your application requires the use of interrupts, you will also want to read the information under the heading "Interrupt Control Functions". This section describes how the Interrupt Enable (INTE) mask is used to enable the INTRA and INTRB interrupt signals generated when using Modes 1 and 2.

The remainder of the Operational Description discusses the three operating modes in detail. This information includes timing diagrams, examples of how the operating modes may be combined, and describes the Port C Status Word used in Modes 1 and 2. Port A and Port B source current capabilities are also defined. Values referenced on the timing diagrams are defined in Appendix A, "Specifications".

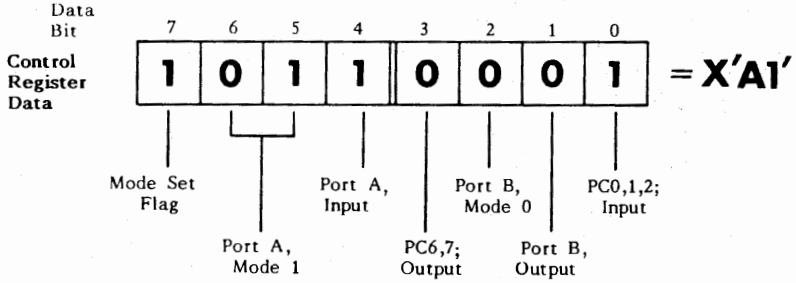
The section entitled "Applications of the 8255A" gives some practical examples of how the PPI can be used for specific applications.

MODE SELECTION

Once you have decided how to define the operating modes of Ports A, B, and C, determine the data that you will need to write to the Control Word (refer to the "8255A Operational Description", Figure 6, of the reprint). For example, to select:

Port A	Mode 1, Input
Port B	Mode 0, Output
PC 0,1,2	Mode 0, Input
PC 6,7	Mode 0, Output

you would write the following data:



Note that PC 3,4, and 5 are used for the Port A handshaking and interrupt signals and are therefore not available for I/O ("8255A Operational Description", Figure 8); however PC 0,1,2,6, and 7 can be used for digital I/O. The interrupt signal generated on PC 3 may be jumpered to one of the the PC's interrupt channels. The interrupt channel selection was described in Chapter 2.

Finally, you will need to write the data to the Control Word to select the operating modes of the I/O ports. Refer to Table 3-1 to determine the address of the Control Word. To select the operating modes used in the above example, the data X'A1' would be written to I/O location X'203' (DG24 Base Address = X'200'). The following BASICA statement will write this data to the Control Word:

```
OUT &H203,&HA1
```

If your application will require changing the operating modes of the I/O ports, be aware that all output registers and status flags are reset whenever the mode is changed. Also, the Control Word can only be written into; no Read operation of the Control Word Register is allowed.

PROGRAMMING THE DG24

Due to the versatility of the 8255 PPI, it would not be possible to provide utility software flexible enough for every application. However, the software included with your DG24 shows some example programs for controlling each operating mode. These programs are written in BASICA and are extensively commented.

Also included are examples of CALL statements which are used from BASICA. These CALL statements envoke assembly language subroutines which provide for a more efficient and faster execution of a routine. CALL statements would be used for high-speed data transfers. Because the 8255 used on the DG24 is capable of 10 MHz transfer rates, WAIT states are not required when using a PC/AT machine.

A directory of the software included with your DG24, as well as a brief description of each program, is listed in the file README.DOC on the Program Disk.

INTERRUPT CONSIDERATIONS

The interrupts generated in PPI Mode 1 and Mode 2 operation may be jumpered to any of the PC interrupt channels 2-7. The channel selection is made by jumpering pins on the DG24 P3 connector as explained in the Interrupt Channel Selection description in Chapter 2.

The PPI interrupts must be enabled by writing a "1" to the INTE mask bit as described in the data sheet reprint section entitled "8255A Operational Description" Interrupt Control Functions. The INTE mask bits are disabled during power up reset and whenever the PPI mode is changed.

Before you attempt to use interrupts, be certain you are familiar with the procedure for intializing the interrupt vectors and the PC's interrupt controller, and setting up the interrupt handling routines. Reference 1 in Appendix C contains a very good description of the PC's system interrupts.

intel

8255A FUNCTIONAL DESCRIPTION

Group A and Group B Controls

The functional configuration of each port is programmed by the systems software. In essence, the CPU "outputs" a control word to the 8255A. The control word contains information such as "mode", "bit set", "bit reset", etc., that initializes the functional configuration of the 8255A.

Each of the Control blocks (Group A and Group B) accepts "commands" from the Read/Write Control Logic, receives "control words" from the internal data bus and issues the proper commands to its associated ports.

Control Group A – Port A and Port C upper (C7-C4)
Control Group B – Port B and Port C lower (C3-C0)

The Control Word Register can Only be written into. No Read operation of the Control Word Register is allowed.

Ports A, B, and C

The 8255A contains three 8-bit ports (A, B, and C). All can be configured in a wide variety of functional characteristics by the system software but each has its own special features or "personality" to further enhance the power and flexibility of the 8255A.

Port A. One 8-bit data output latch/buffer and one 8-bit data input latch.

Port B. One 8-bit data input/output latch/buffer and one 8-bit data input buffer.

Port C. One 8-bit data output latch/buffer and one 8-bit data input buffer (no latch for input). This port can be divided into two 4-bit ports under the mode control. Each 4-bit port contains a 4-bit latch and it can be used for the control signal outputs and status signal inputs in conjunction with ports A and B.

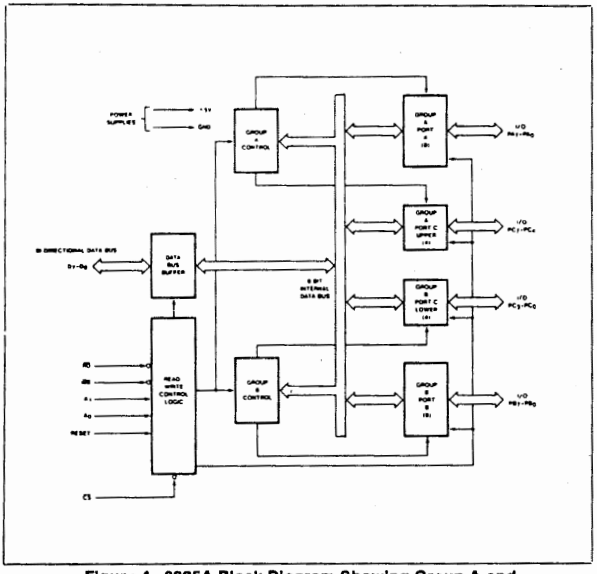


Figure 4. 8225A Block Diagram Showing Group A and Group B Control Functions

PIN CONFIGURATION

PIN NAMES

D_7 - D_0	DATA BUS (BI DIRECTIONAL)
RESET	RESET INPUT
$\overline{CS}$	CHIP SELECT
$\overline{RD}$	READ INPUT
$\overline{WR}$	WRITE INPUT
A0, A1	PORT ADDRESS
PA7-PA0	PORT A (BIT)
PB7-PB0	PORT B (BIT)
PC7-PC0	PORT C (BIT)
V_{CC}	+5 VOLTS
GND	0 VOLTS

8255A OPERATIONAL DESCRIPTION

Mode Selection

There are three basic modes of operation that can be selected by the system software:

Mode 0 — Basic Input/Output
Mode 1 — Strobed Input/Output
Mode 2 — Bi-Directional Bus

When the reset input goes "high" all ports will be set to the input mode (i.e., all 24 lines will be in the high impedance state). After the reset is removed the 8255A can remain in the input mode with no additional initialization required. During the execution of the system program any of the other modes may be selected using a single output instruction. This allows a single 8255A to service a variety of peripheral devices with a simple software maintenance routine.

The modes for Port A and Port B can be separately defined, while Port C is divided into two portions as required by the Port A and Port B definitions. All of the output registers, including the status flip-flops, will be reset whenever the mode is changed. Modes may be combined so that their functional definition can be "tailored" to almost any I/O structure. For instance; Group B can be programmed in Mode 0 to monitor simple switch closings or display computational results, Group A could be programmed in Mode 1 to monitor a keyboard or tape reader on an interrupt-driven basis.

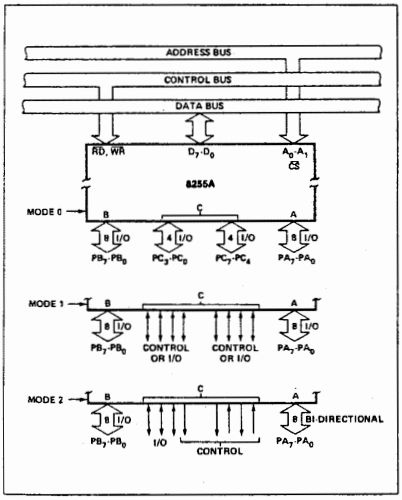


Figure 5. Basic Mode Definitions and Bus Interface

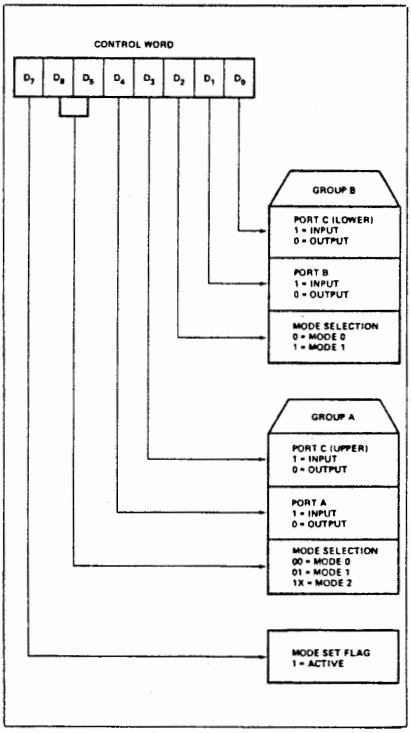


Figure 6. Mode Definition Format

The mode definitions and possible mode combinations may seem confusing at first but after a cursory review of the complete device operation a simple, logical I/O approach will surface. The design of the 8255A has taken into account things such as efficient PC board layout, control signal definition vs PC layout and complete functional flexibility to support almost any peripheral device with no external logic. Such design represents the maximum use of the available pins.

Single Bit Set/Reset Feature

Any of the eight bits of Port C can be Set or Reset using a single OUTput instruction. This feature reduces software requirements in Control-based applications.

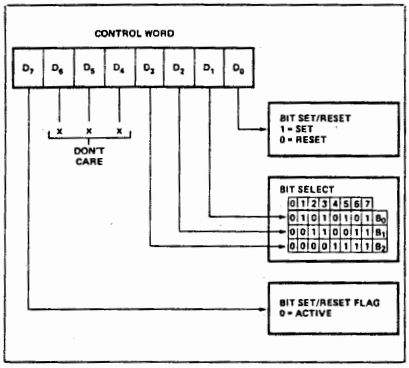


Figure 7. Bit Set/Reset Format

When Port C is being used as status/control for Port A or B, these bits can be set or reset by using the Bit Set/Reset operation just as if they were data output ports.

Interrupt Control Functions

When the 8255A is programmed to operate in mode 1 or mode 2, control signals are provided that can be used as interrupt request inputs to the CPU. The interrupt request signals, generated from port C, can be inhibited or enabled by setting or resetting the associated INTE flip-flop, using the bit set/reset function of port C.

This function allows the Programmer to disallow or allow a specific I/O device to interrupt the CPU without affecting any other device in the interrupt structure.

INTE flip-flop definition:

(BIT-SET) — INTE is SET — Interrupt enable
(BIT-RESET) — INTE is RESET — Interrupt disable

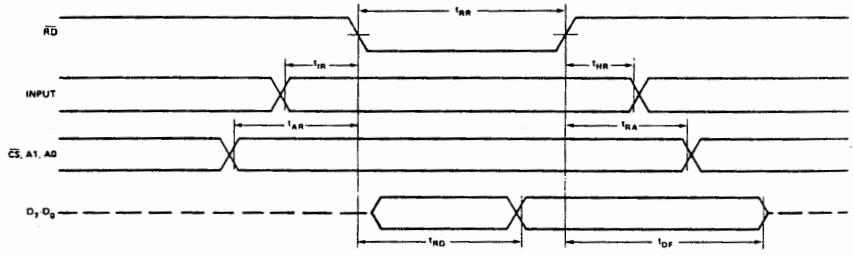
Note: All Mask flip-flops are automatically reset during mode selection and device Reset.

Operating Modes

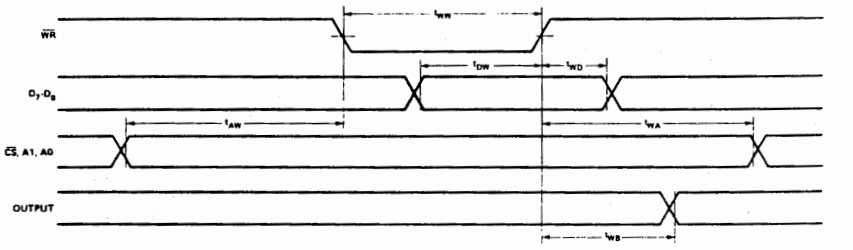
MODE 0 (Basic Input/Output). This functional configuration provides simple input and output operations for each of the three ports. No "handshaking" is required, data is simply written to or read from a specified port.

Mode 0 Basic Functional Definitions:

- Two 8-bit ports and two 4-bit ports.
- Any port can be input or output.
- Outputs are latched.
- Inputs are not latched.
- 16 different Input/Output configurations are possible in this Mode.



MODE 0 (Basic Input)

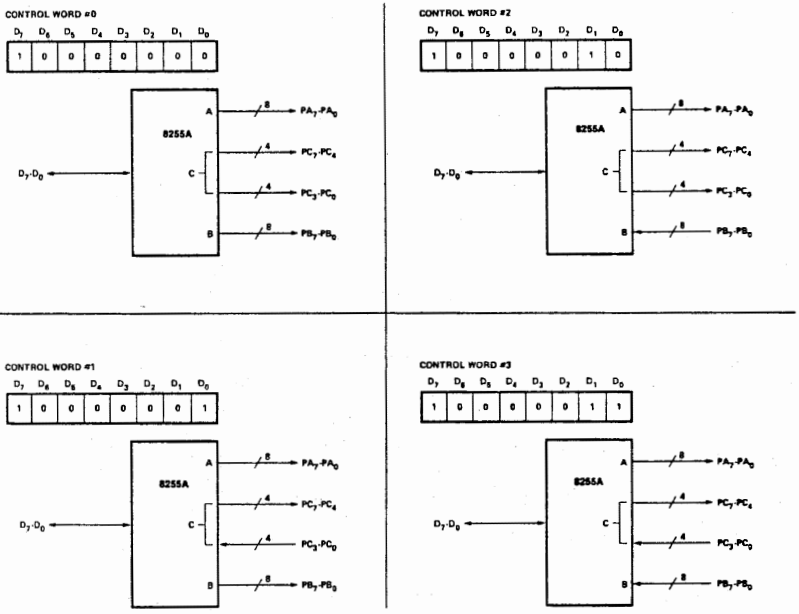


MODE 0 (Basic Output)

MODE 0 Port Definition

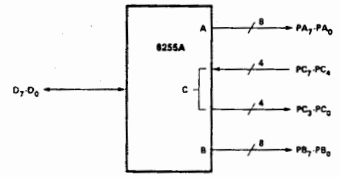
A		B		GROUP A			GROUP B	
D_4	D_3	D_1	D_0	PORT A	PORT C (UPPER)	#	PORT B	PORT C (LOWER)
0	0	0	0	OUTPUT	OUTPUT	0	OUTPUT	OUTPUT
0	0	0	1	OUTPUT	OUTPUT	1	OUTPUT	INPUT
0	0	1	0	OUTPUT	OUTPUT	2	INPUT	OUTPUT
0	0	1	1	OUTPUT	OUTPUT	3	INPUT	INPUT
0	1	0	0	OUTPUT	INPUT	4	OUTPUT	OUTPUT
0	1	0	1	OUTPUT	INPUT	5	OUTPUT	INPUT
0	1	1	0	OUTPUT	INPUT	6	INPUT	OUTPUT
0	1	1	1	OUTPUT	INPUT	7	INPUT	INPUT
1	0	0	0	INPUT	OUTPUT	8	OUTPUT	OUTPUT
1	0	0	1	INPUT	OUTPUT	9	OUTPUT	INPUT
1	0	1	0	INPUT	OUTPUT	10	INPUT	OUTPUT
1	0	1	1	INPUT	OUTPUT	11	INPUT	INPUT
1	1	0	0	INPUT	INPUT	12	OUTPUT	OUTPUT
1	1	0	1	INPUT	INPUT	13	OUTPUT	INPUT
1	1	1	0	INPUT	INPUT	14	INPUT	OUTPUT
1	1	1	1	INPUT	INPUT	15	INPUT	INPUT

MODE 0 Configurations



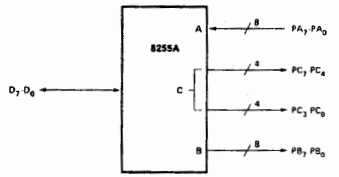
CONTROL WORD #4

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	0	1	0	0	0



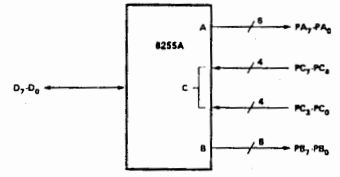
CONTROL WORD #8

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	1	0	0	0	0



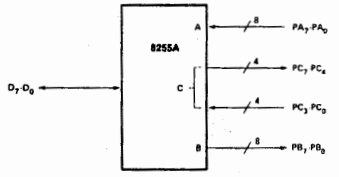
CONTROL WORD #5

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	0	1	0	0	1



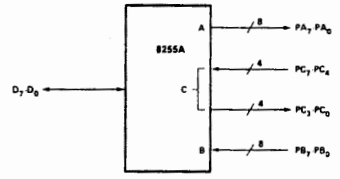
CONTROL WORD #9

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	1	0	0	0	1



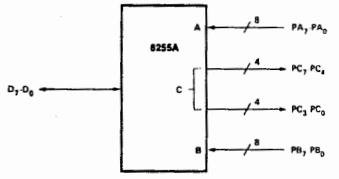
CONTROL WORD #6

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	0	1	0	1	0



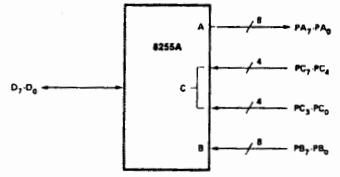
CONTROL WORD #10

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	1	0	0	1	0



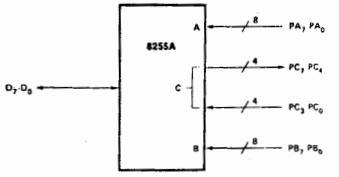
CONTROL WORD #7

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	0	1	0	1	1



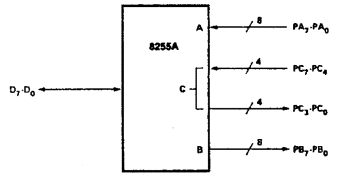
CONTROL WORD #11

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	1	0	0	1	1



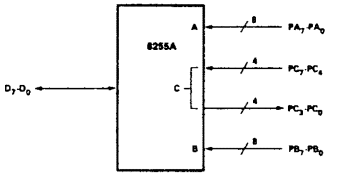
CONTROL WORD #12

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	1	1	0	0	0



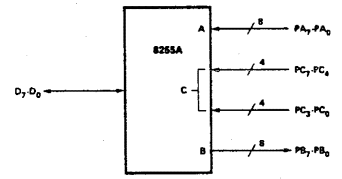
CONTROL WORD #14

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	1	1	0	1	0



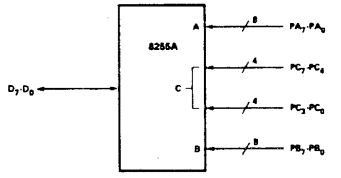
CONTROL WORD #13

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	1	1	0	0	1



CONTROL WORD #15

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	1	1	0	1	1



Operating Modes

MODE 1 (Strobed Input/Output). This functional configuration provides a means for transferring I/O data to or from a specified port in conjunction with strobes or "handshaking" signals. In mode 1, port A and Port B use the lines on port C to generate or accept these "handshaking" signals.

Mode 1 Basic Functional Definitions:

- Two Groups (Group A and Group B)
- Each group contains one 8-bit data port and one 4-bit control/data port.
- The 8-bit data port can be either input or output. Both inputs and outputs are latched.
- The 4-bit port is used for control and status of the 8-bit data port.

Input Control Signal Definition

STB (Strobe Input). A "low" on this input loads data into the input latch.

IBF (Input Buffer Full F/F)

A "high" on this output indicates that the data has been loaded into the input latch; in essence, an acknowledgement. IBF is set by STB input being low and is reset by the rising edge of the RD input.

INTR (Interrupt Request)

A "high" on this output can be used to interrupt the CPU when an input device is requesting service. INTR is set by the $\overline{STB}$ is a "one", IBF is a "one" and INTE is a "one". It is reset by the falling edge of $\overline{RD}$. This procedure allows an input device to request service from the CPU by simply strobing its data into the port.

INTE A

Controlled by bit set/reset of PC_4.

INTE B

Controlled by bit set/reset of PC_2.

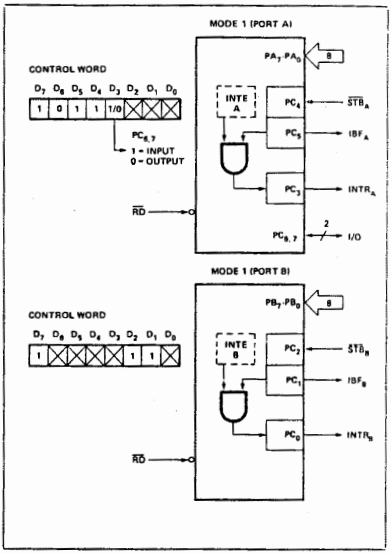


Figure 8. MODE 1 Input

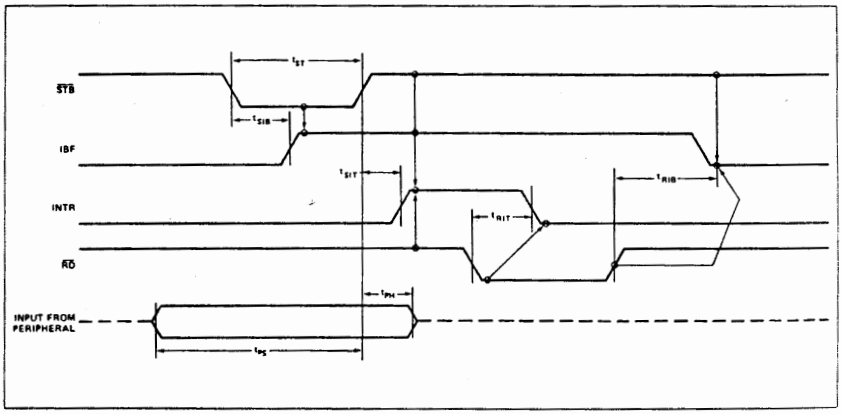


Figure 9. MODE 1 (Strobed Input)

Output Control Signal Definition

$\overline{OBF}$ (Output Buffer Full F/F). The OBF output will go "low" to indicate that the CPU has written data out to the specified port. The OBF F/F will be set by the rising edge of the WR input and reset by ACK input being low.

$\overline{ACK}$ (Acknowledge Input). A "low" on this input informs the 8255A that the data from port A or port B has been accepted. In essence, a response from the peripheral device indicating that it has received the data output by the CPU.

INTR (Interrupt Request). A "high" on this output can be used to interrupt the CPU when an output device has accepted data transmitted by the CPU. INTR is set when ACK is a "one", OBF is a "one" and INTE is a "one". It is reset by the falling edge of WR.

INTE A

Controlled by bit set/reset of PC_6.

INTE B

Controlled by bit set/reset of PC_2.

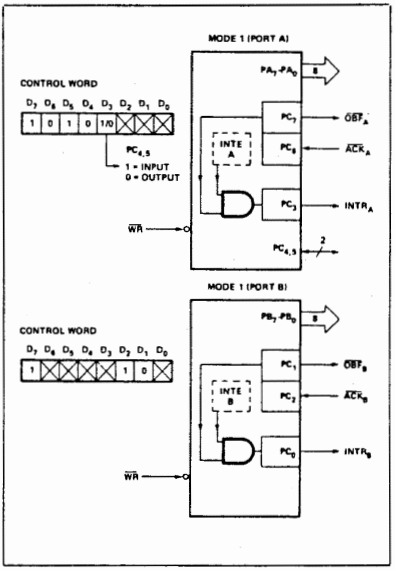


Figure 10. MODE 1 Output

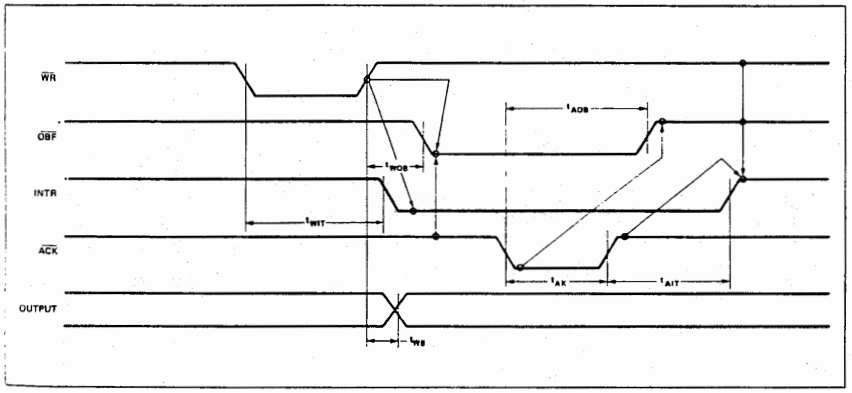


Figure 11. Mode 1 (Strobed Output)

Combinations of MODE 1

Port A and Port B can be individually defined as input or output in Mode 1 to support a wide variety of strobed I/O applications.

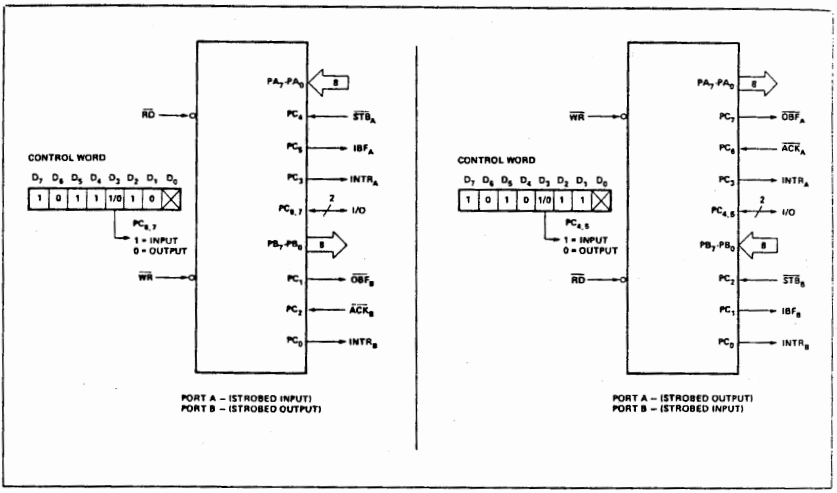


Figure 12. Combinations of MODE 1

Operating Modes

MODE 2 (Strobed Bidirectional Bus I/O). This functional configuration provides a means for communicating with a peripheral device or structure on a single 8-bit bus for both transmitting and receiving data (bidirectional bus I/O). "Handshaking" signals are provided to maintain proper bus flow discipline in a similar manner to MODE 1. Interrupt generation and enable/disable functions are also available.

MODE 2 Basic Functional Definitions:

- Used in Group A only.
- One 8-bit, bi-directional bus Port (Port A) and a 5-bit control Port (Port C).
- Both inputs and outputs are latched.
- The 5-bit control port (Port C) is used for control and status for the 8-bit, bi-directional bus port (Port A).

Bidirectional Bus I/O Control Signal Definition

INTR (Interrupt Request). A high on this output can be used to interrupt the CPU for both input or output operations.

Output Operations

$\overline{OBF}$ (Output Buffer Ful). The OBF output will go "low" to indicate that the CPU has written data out to port A.

$\overline{ACK}$ (Acknowledge). A "low" on this input enables the tri-state output buffer of port A to send out the data. Otherwise, the output buffer will be in the high impedance state.

INTE 1 (The INTE Flip-Flop Associated with OBF). Controlled by bit set/reset of PC_6.

Input Operations

$\overline{STB}$ (Strobe Input)

STB (Strobe Input). A "low" on this input loads data into the input latch.

IBF (Input Buffer Full F/F). A "high" on this output indicates that data has been loaded into the input latch.

INTE 2 (The INTE Flip-Flop Associated with IBF). Controlled by bit set/reset of PC_4.

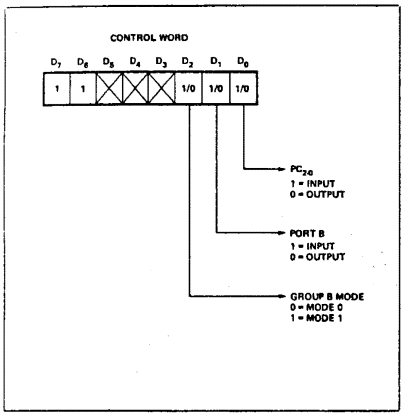


Figure 13. MODE Control Word

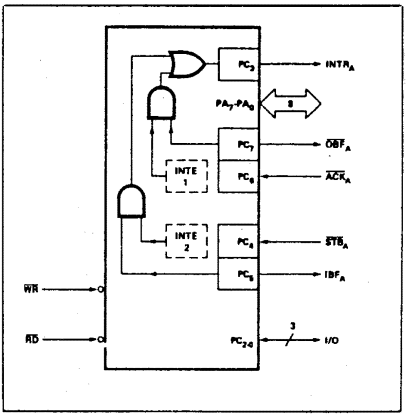


Figure 14. MODE 2

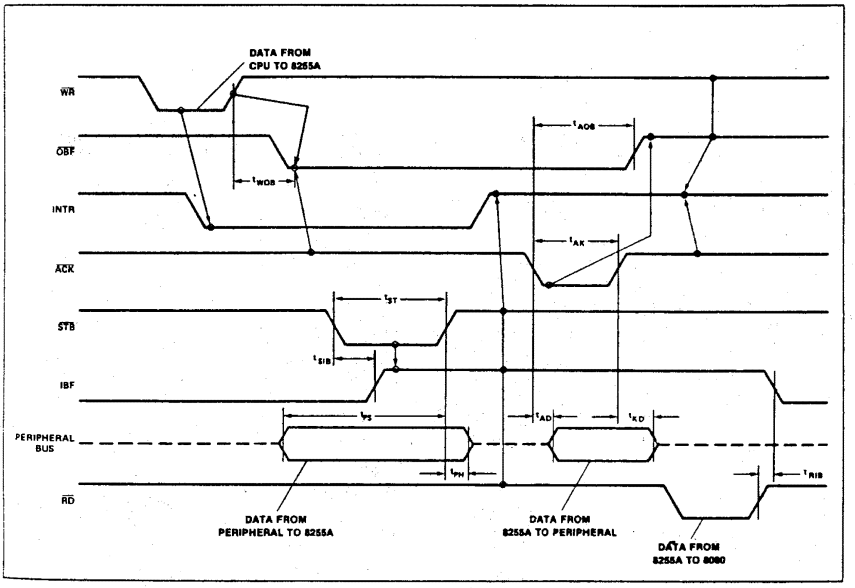


Figure 15. MODE 2 (Bidirectional)

NOTE: Any sequence where $\overline{WR}$ occurs before $\overline{ACK}$ and $\overline{STB}$ occurs before $\overline{RD}$ is permissible.
(INTR = IBF • $\overline{MASK}$ • $\overline{STB}$ • $\overline{RD}$ + $\overline{OBF}$ • $\overline{MASK}$ • $\overline{ACK}$ • $\overline{WR}$)

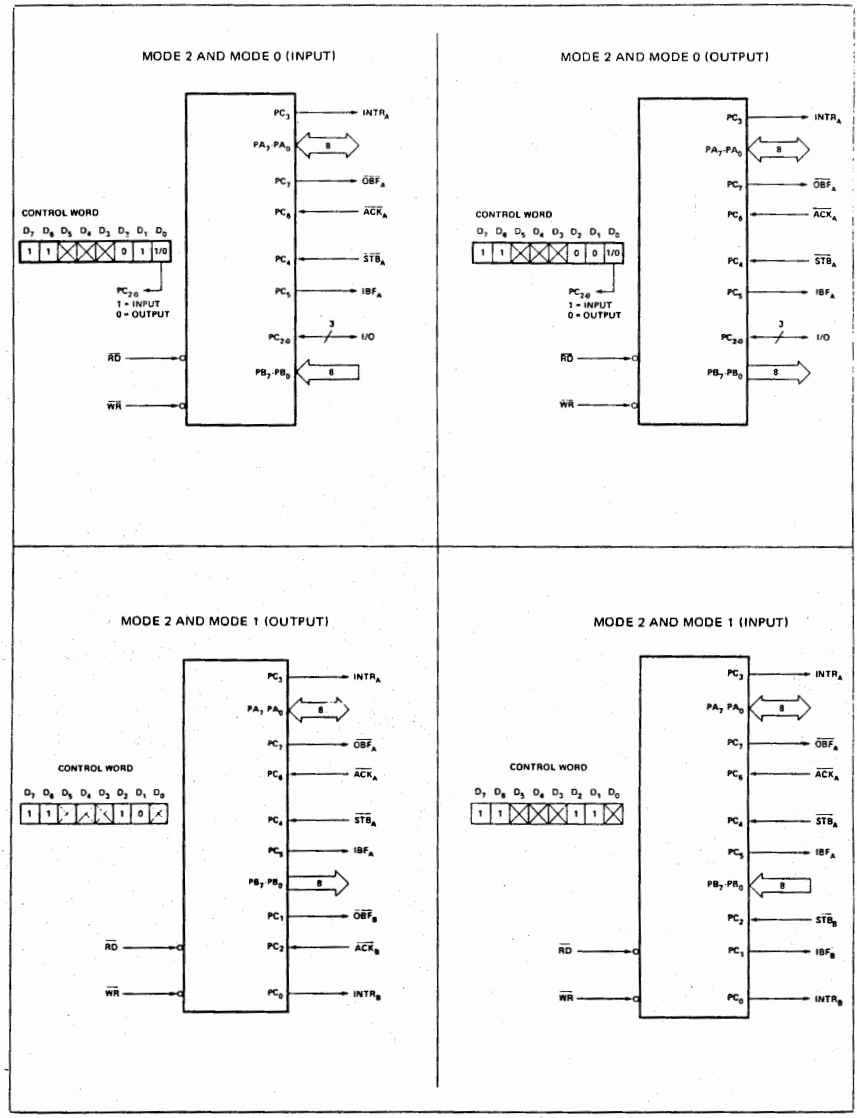


Figure 16. MODE ¼ Combinations

Mode Definition Summary

	MODE 0		MODE 1		MODE 2	
	IN	OUT	IN	OUT	GROUP A ONLY	
PA_0	IN	OUT	IN	OUT	⟷	
PA_1	IN	OUT	IN	OUT	⟷	
PA_2	IN	OUT	IN	OUT	⟷	
PA_3	IN	OUT	IN	OUT	⟷	
PA_4	IN	OUT	IN	OUT	⟷	
PA_5	IN	OUT	IN	OUT	⟷	
PA_6	IN	OUT	IN	OUT	⟷	
PA_7	IN	OUT	IN	OUT	⟷	
PB_0	IN	OUT	IN	OUT	—	MODE 0 OR MODE 1 ONLY
PB_1	IN	OUT	IN	OUT	—	
PB_2	IN	OUT	IN	OUT	—	
PB_3	IN	OUT	IN	OUT	—	
PB_4	IN	OUT	IN	OUT	—	
PB_5	IN	OUT	IN	OUT	—	
PB_6	IN	OUT	IN	OUT	—	
PB_7	IN	OUT	IN	OUT	—	
PC_0	IN	OUT	$INTR_B$	$INTR_B$	I/O	
PC_1	IN	OUT	IBF_B	$\overline{OBF}_B$	I/O	
PC_2	IN	OUT	$\overline{STB}_B$	$\overline{ACK}_B$	I/O	
PC_3	IN	OUT	$INTR_A$	$INTR_A$	$INTR_A$	
PC_4	IN	OUT	$\overline{STB}_A$	I/O	$\overline{STB}_A$	
PC_5	IN	OUT	IBF_A	I/O	IBF_A	
PC_6	IN	OUT	I/O	$\overline{ACK}_A$	$\overline{ACK}_A$	
PC_7	IN	OUT	I/O	$\overline{OBF}_A$	$\overline{OBF}_A$	

Special Mode Combination Considerations

There are several combinations of modes when not all of the bits in Port C are used for control or status. The remaining bits can be used as follows:

If Programmed as Inputs –
All input lines can be accessed during a normal Port C read.

If Programmed as Outputs –
Bits in C upper (PC_7-PC_4) must be individually accessed using the bit set/reset function.

Bits in C lower (PC_3-PC_0) can be accessed using the bit set/reset function or accessed as a threesome by writing into Port C.

Source Current Capability on Port B and Port C

Any set of **eight** output buffers, selected randomly from Ports B and C can source 1mA at 1.5 volts. This feature allows the 8255 to directly drive Darlington type drivers and high-voltage displays that require such source current.

Reading Port C Status

In Mode 0, Port C transfers data to or from the peripheral device. When the 8255 is programmed to function in Modes 1 or 2, Port C generates or accepts "hand-shaking" signals with the peripheral device. Reading the contents of Port C allows the programmer to test or verify the "status" of each peripheral device and change the program flow accordingly.

There is no special instruction to read the status information from Port C. A normal read operation of Port C is executed to perform this function.

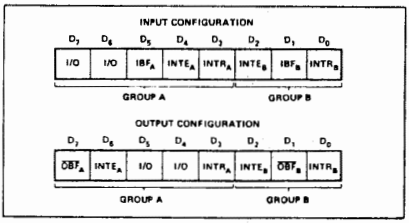


Figure 17. MODE 1 Status Word Format

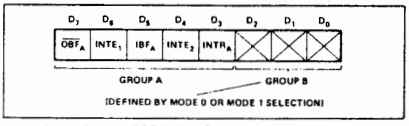


Figure 18. MODE 2 Status Word Format

APPLICATIONS OF THE 8255A

The 8255A is a very powerful tool for interfacing peripheral equipment to the microcomputer system. It represents the optimum use of available pins and is flexible enough to interface almost any I/O device without the need for additional external logic.

Each peripheral device in a microcomputer system usually has a "service routine" associated with it. The routine manages the software interface between the device and the CPU. The functional definition of the 8255A is programmed by the I/O service routine and becomes an extension of the system software. By examining the I/O devices interface characteristics for both data transfer and timing, and matching this information to the examples and tables in the detailed operational description, a control word can easily be developed to initialize the 8255A to exactly "fit" the application. Figures 19 through 25 present a few examples of typical applications of the 8255A.

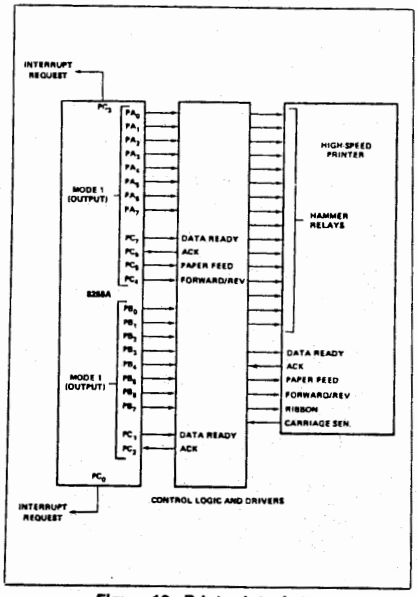


Figure 19. Printer Interface

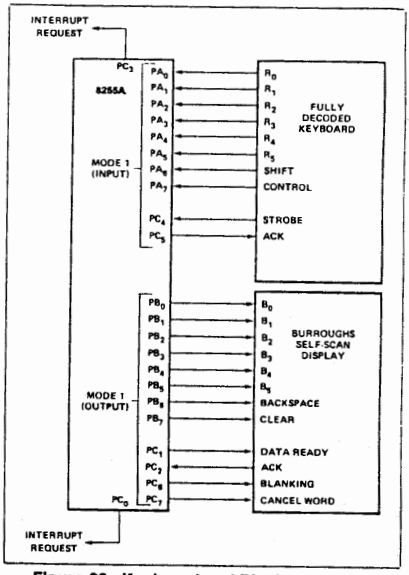


Figure 20. Keyboard and Display Interface

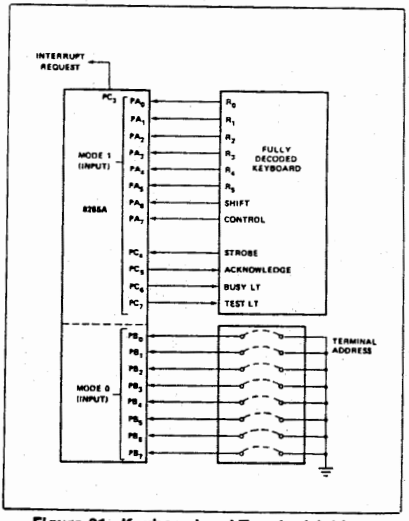


Figure 21. Keyboard and Terminal Address Interface

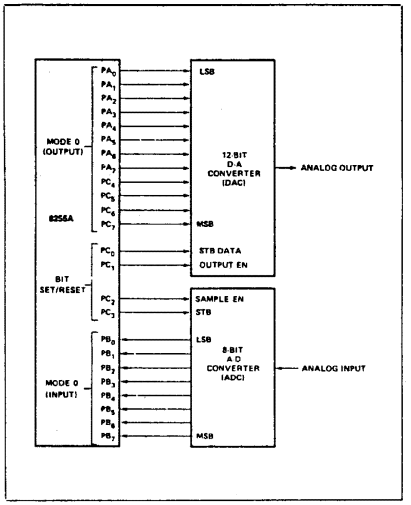


Figure 22. Digital to Analog, Analog to Digital

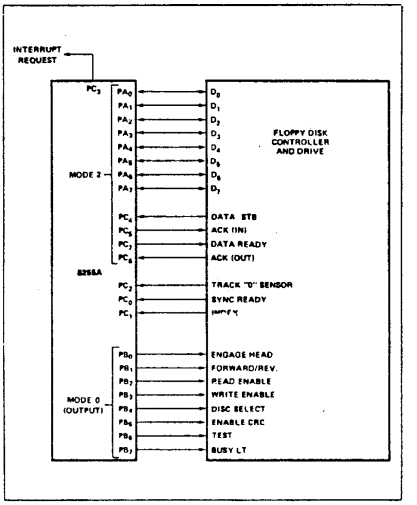


Figure 23. Basic CRT Controller Interface

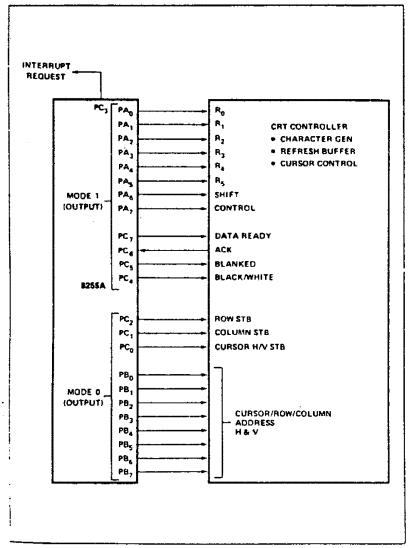


Figure 24. Basic Floppy Disc Interface

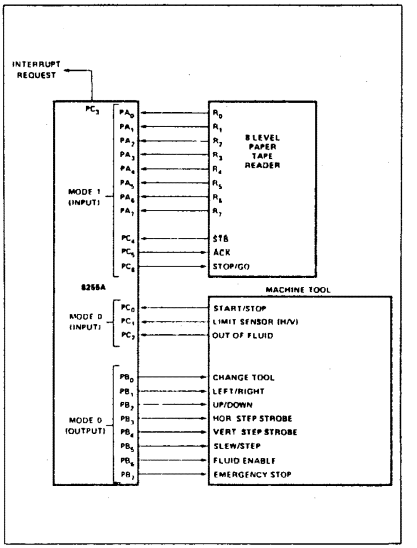


Figure 25. Machine Tool Controller Interface

Appendix A

Specifications

DG24 SPECIFICATIONS

Interface

IBM PC/XT/AT compatible
No PC/AT WAIT states required
Jumper-selectable base address,
I/O mapped: (hex) 200 300
240 340
280 380
2C0 3C0
Jumper-selectable interrupts
Both 8255 interrupts (INTRA,INTRB) are provided.
PC IRQ channels
supported: 2 - 7

Digital I/O

The DG24 utilizes an 8255 programmable peripheral interface (PPI) chip. It provides 24 digital I/O lines which are divided into three 8-bit ports: A, B, and C. Port A, Port B, and each half of Port C may be individually programmed as input or output. In addition, strobed I/O operations may be performed using some of the Port C lines to control data transfers.

The three modes of operation are summarized below:

Mode 0 -- Basic I/O; provides simple input and output operations for each port. Data is written to or read from a specified port.

Mode 1 -- Strobed I/O; uses handshaking signals to transfer data through Port A or Port B. Interrupts may be utilized.

Mode 2 -- Strobed Bidirectional I/O; Port A is used as a bidirectional data bus. Data transfers occur in conjunction with handshaking signals similar to Mode 1 operation. Interrupts may be utilized.

Miscellaneous Outputs (PC-bus sourced)

Reset Driver
+5 Vdc
+/-12 Vdc
Digital ground

Software Features

Sample BASICA programs are provided which demonstrate the control of each of the PPI operating modes. Example CALL statements are also included to show how the 8255 may be used for high-speed applications.

A complete directory of all software included with the DG24 is listed on the accompanying disk.

Electrical

Current requirements:
+5V 20 mA

Mechanical

Connectors:
40-pin, right angle, shrouded male header with ejector tabs
Edge-connector -- IBM PC/XT/AT compatible

Environmental:

Operating temperature:	0 to +50 deg. Centigrade
Storage temperature:	-20 to +70 deg. Centigrade
Humidity:	0 to 90%, non-condensing

Size: 3.875" X 4.500" (Short slot)

Options: XB40 Expansion Board
XC40 Expansion Cable

Warranty: 1 year

intel

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias . . . . . 0°C to 70°C
Storage Temperature . . . . . −65°C to +150°C
Voltage on Any Pin
With Respect to Ground . . . . . −0.5V to +7V
Power Dissipation . . . . . 250 mW

NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. CHARACTERISTICS (T_A = 0°C to 70°C, V_{CC} = +5V ± 5%, GND = 0V)

Symbol	Parameter	Min.	Max.	Unit	Test Conditions
V_{IL}	Input Low Voltage	-0.3	0.8	V	
V_{IH}	Input High Voltage	2.2	5.5	V	
V_{OL} (DB)	Output Low Voltage (Data Bus)		0.45	V	I_{OL} = 2.5mA
V_{OL}(PER)	Output Low Voltage (Peripheral Port)		0.45	V	I_{OL} = 1.7mA
V_{OH}(DB)	Output High Voltage (Data Bus)	2.4		V	I_{OH} = -400μA
V_{OH}(PER)	Output High Voltage (Peripheral Port)	4.2		V	I_{OH} = -100μA
I_{DAR}[1]	Darlington Drive Current	-1.0	-5.0	mA	R_{EXT} =1.1KΩ; V_{EXT}= 1.5V
I_{CC}	Power Supply Current		5.0	mA	
I_{IL}	Input Load Current		±10	μA	V_{IN} = V_{CC} to 0V
I_{OFL}	Output Float Leakage		±10	μA	V_{OUT} = V_{CC} to 0V

NOTE:
1. Available on any 8 pins from Port B and C.

CAPACITANCE (T_A = 25°C, V_{CC} = GND = 0V)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
C_{IN}	Input Capacitance			10	pF	fc = 1MHz
$C_{I/O}$	I/O Capacitance			20	pF	Unmeasured pins returned to GND

A.C. CHARACTERISTICS (T_A = 0°C to 70°C, V_{CC} = +5V ± 5%, GND = 0V)

Bus Parameters

READ

Symbol	Parameter	Min.	Max.	Unit
t_{AR}	Address Stable Before READ	0		ns
t_{RA}	Address Stable After READ	0		ns
t_{RR}	READ Pulse Width	150		ns
t_{RD}	Data Valid From READ[1]		100	ns
t_{DF}	Data Float After READ	0	40	ns
t_{RV}	Time Between READs and/or WRITEs	150		ns

A.C. CHARACTERISTICS (Continued)

WRITE

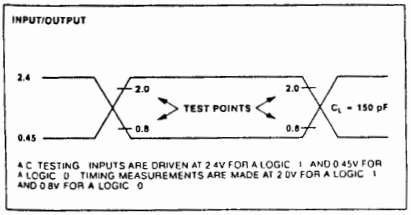
Symbol	Parameter	Min.	Max.	Unit
t_{AW}	Address Stable Before WRITE	0		ns
t_{WA}	Address Stable After WRITE	20		ns
t_{WW}	WRITE Pulse Width	120		ns
t_{DW}	Data Valid to WRITE (T.E.)	100		ns
t_{WD}	Data Valid After WRITE	30		ns

OTHER TIMINGS

Symbol	Parameter	Min.	Max.	Unit
t_{WB}	WR = 1 to Output[1]		350	ns
t_{IR}	Peripheral Data Before RD	0		ns
t_{HR}	Peripheral Data After RD	0		ns
t_{AK}	ACK Pulse Width	300		ns
t_{ST}	STB Pulse Width	350		ns
t_{PS}	Per. Data Before T.E. of STB	0		ns
t_{PH}	Per. Data After T.E. of STB	150		ns
t_{AD}	ACK = 0 to Output[1]		300	ns
t_{KD}	ACK = 1 to Output Float	20	250	ns
t_{WOB}	WR = 1 to OBF = 0[1]		300	ns
t_{AOB}	ACK = 0 to OBF = 1[1]		350	ns
t_{SIB}	STB = 0 to IBF = 1[1]		350	ns
t_{RIB}	RD = 1 to IBF = 0[1]		300	ns
t_{RIT}	RD = 0 to INTR = 0[1]		400	ns
t_{SIT}	STB = 1 to INTR = 1[1]		300	ns
t_{AIT}	ACK = 1 to INTR = 1[1]		350	ns
t_{WIT}	WR = 0 to INTR = 0[1,3]		450	ns

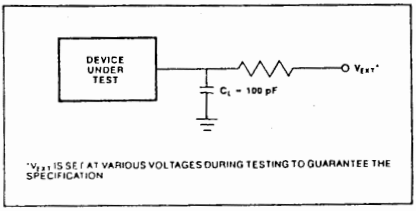
NOTES:
1. Test Conditions: C_L = 150pF.
2. Period of Reset pulse must be at least 50μs during or after power on. Subsequent Reset pulse can be 500 ns min.
3. INTR↑ may occur as early as $\overline{WR}$↓.

A.C. TESTING INPUT, OUTPUT WAVEFORM



A.C. TESTING INPUTS ARE DRIVEN AT 2.4V FOR A LOGIC "1" AND 0.45V FOR A LOGIC "0". TIMING MEASUREMENTS ARE MADE AT 2.0V FOR A LOGIC "1" AND 0.8V FOR A LOGIC "0".

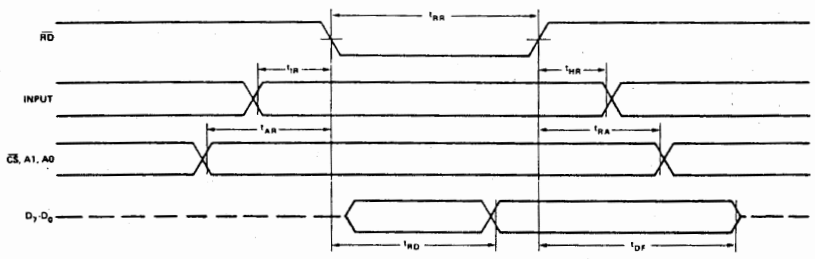
A.C. TESTING LOAD CIRCUIT



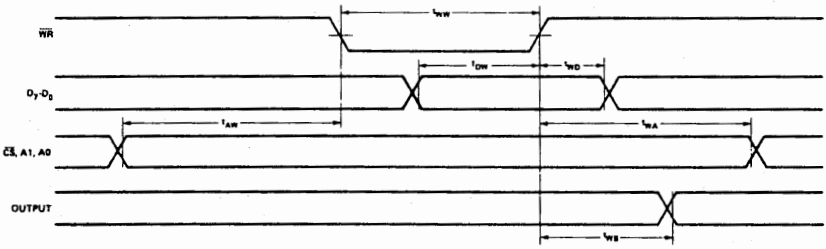
*V_{EXT} IS SET AT VARIOUS VOLTAGES DURING TESTING TO GUARANTEE THE SPECIFICATION

WAVEFORMS

MODE 0 (BASIC INPUT)

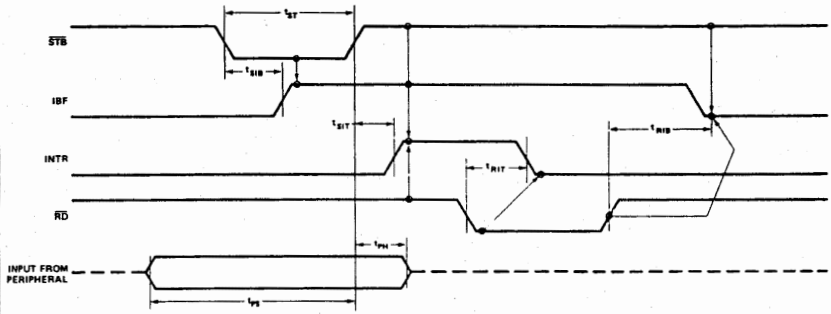


MODE 0 (BASIC OUTPUT)

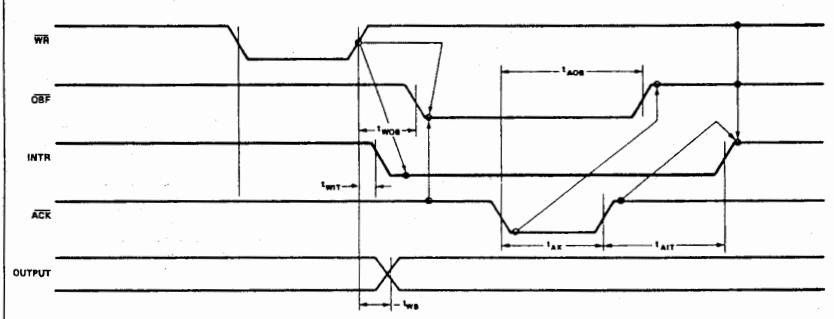


WAVEFORMS (Continued)

MODE 1 (STROBED INPUT)

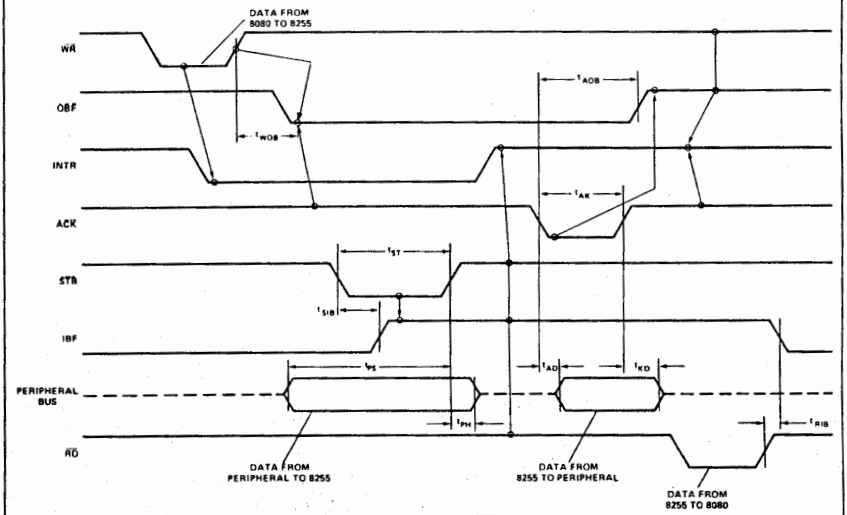


MODE 1 (STROBED OUTPUT)



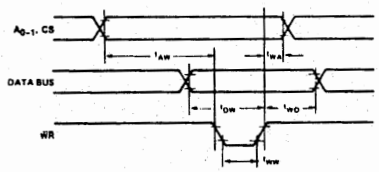
WAVEFORMS (Continued)

MODE 2 (BIDIRECTIONAL)

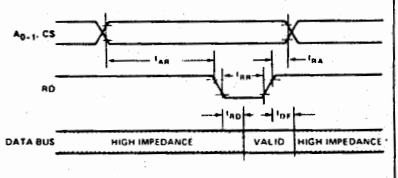


NOTE: Any sequence where $\overline{WR}$ occurs before $\overline{ACK}$ and $\overline{STB}$ occurs before $\overline{RD}$ is permissible.
(INTR = IBF • $\overline{MASK}$ • $\overline{STB}$ • $\overline{RD}$ + $\overline{OBF}$ • $\overline{MASK}$ • $\overline{ACK}$ • $\overline{WR}$)

WRITE TIMING



READ TIMING



Appendix B

I/O Connector

1	Digital Gnd	21	+5 Volts
2		22	
3		23	
4	Digital Gnd	24	
5		25	
6		26	Digital Gnd
7	PA7	27	PA6
8	PA5	28	PA4
9	PA3	29	PA2
10	PA1	30	PA0
11	PC7	31	PC6
12	PC5	32	PC4
13	PC3	33	PC2
14	PC1	34	PC0
15	PB7	35	PB6
16	PB5	36	PB4
17	PB3	37	PB2
18	PB1	38	PB0
19	+12 Volts	39	RESET DRV
20	-12 Volts	40	Digital Gnd

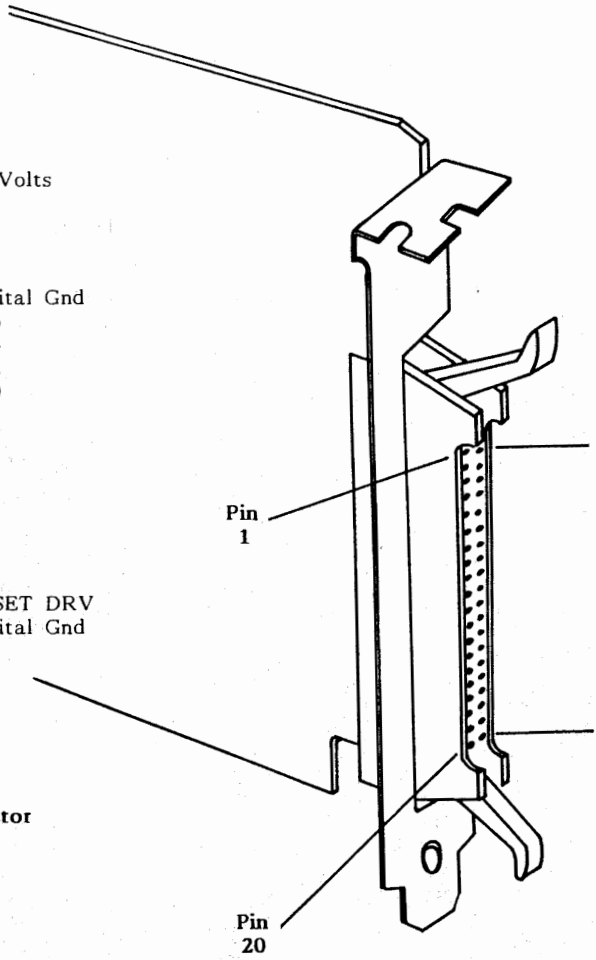


Fig. B-1 DG24 P4 Connector Pin Assignment

Table B-1 DG24 P4 Connector/Mating Connector

Manufacturer	DG24 P4 Connector	P4 Mating Connector
KEL-AM Inc. 3M Robinson Nugent MIL C-83503	6201-040-258	6230-040-601 3417-7040 IDS-C40PK-C-SR-TG M83503/7-09

Appendix C

References

(1) Eggebrecht, Lewis C. Interfacing To The IBM Personal Computer. Howard W. Sams & Co., Inc., Indianapolis, IN. 1983
ISBN: 0-672-22027-X

(2) Jourdain, Robert Programmer's Problem Solver for the IBM PC, XT, & AT. Prentice Hall Press, New York, NY. 1986
ISBN: 0-89303-787-7

(3) Morgan, Christopher L., and Waite, Mitchell 8086/8088 16-Bit Microprocessor Primer. BYTE/McGraw-Hill, Peterborough NH. 1982
ISBN: 0-07-043109-4

(4) Lafore, Robert Assembly Language Primer for the IBM PC & XT. New American Library, New York, NY. 1984
ISBN: 0-452-25711-5

(5) Norton, Peter, and Socha, John Peter Norton's Assembly Language Book for the IBM PC. Prentice Hall Press, New York, NY. 1986
ISBN: 0-13-661901-0

(6) Abel, Peter Assembler for the IBM PC and PC-XT. Reston Publishing Company, Inc., Reston, VA. 1984
ISBN: 0-8359-0153-X

(7) Scanlon, Leo J. IBM PC Assembly Language. Robert J. Brady Co., Bowie, MD. 1983
ISBN: 0-89303-241-7

(8) Angermeyer, John, and Jaeger, Kevin MS-DOS Developer's Guide. Howard W. Sams & Co., Indianapolis, IN. 1986
ISBN: 0-672-22409-7

(9) Duncan, Ray Advanced MSDOS. Microsoft Press, Redmond, WA. 1986
ISBN: 0-914845-77-2

(10) Rugg, Tom and Feldman, Phil Turbo Pascal Program Library. Que Corporation, Indianapolis, IN. 1986
ISBN: 0-88022-244-1

(11) Robinson, Phillip R. Using Turbo Prolog. Osborne McGraw-Hill, Berkeley, CA. 1987
ISBN: 0-07-881253-4

(12) Koffman, Elliot B. Turbo Pascal A Problem-Solving Approach. Addison-Wesley Publishing Company, Inc., Reading, MA. 1986
ISBN: 0-201-11743-6

(13) Dooley, George and Szybist, Daniel Interface Projects For the IBM PC. Real Time Devices, Inc., State College, PA.

(14) Dooley, George Forth For Robot Control. Robotics Age Sep (Vol.7, No. 9:7-8) 1985

(15) Dooley, George and Szybist, Daniel Accessing the Analog World. Chemical Engineering Aug 22, 1983

Appendix D

Warranty

LIMITED WARRANTY

Real Time Devices, Inc. warrants the hardware and software products it manufactures and produces to be free from defects in materials and workmanship for one year following the date of shipment from REAL TIME DEVICES. This warranty is limited to the original purchaser of product and is not transferable.

During the one year warranty period, REAL TIME DEVICES will repair or replace, at its option, any defective products or parts at no additional charge, provided that the product is returned. shipping prepaid, to REAL TIME DEVICES. All replaced parts and products become the property of REAL TIME DEVICES.

THIS LIMITED WARRANTY DOES NOT EXTEND TO ANY PRODUCTS WHICH HAVE BEEN DAMAGED AS A RESULT OF ACCIDENT, MISUSE, ABUSE (such as: use of incorrect input voltages, improper or insufficient ventilation, failure to follow the operating instructions that are provided by REAL TIME DEVICES, "acts of God" or other contingencies beyond the control of REAL TIME DEVICES), OR AS A RESULT OF SERVICE OR MODIFICATION BY ANYONE OTHER THAN REAL TIME DEVICES. EXCEPT AS EXPRESSLY SET FORTH ABOVE, NO OTHER WARRANTIES ARE EXPRESSED OR IMPLIED, INCLUDING, BUT NOT LIMITED TO, ANY IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE, AND REAL TIME DEVICES EXPRESSLY DISCLAIMS ALL WARRANTIES NOT STATED HEREIN. ALL IMPLIED WARRANTIES, INCLUDING IMPLIED WARRANTIES FOR MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, ARE LIMITED TO THE DURATION OF THIS WARRANTY. IN THE EVENT THE PRODUCT IS NOT FREE FROM DEFECTS AS WARRANTED ABOVE, THE PURCHASER'S SOLE REMEDY SHALL BE REPAIR OR REPLACEMENT AS PROVIDED ABOVE. UNDER NO CIRCUMSTANCES WILL REAL TIME DEVICES BE LIABLE TO THE PURCHASER OR ANY USER FOR ANY DAMAGES, INCLUDING ANY INCIDENTAL OR CONSEQUENTIAL DAMAGES, EXPENSES, LOST PROFITS, LOST SAVINGS, OR OTHER DAMAGES ARISING OUT OF THE USE OF OR INABLILITY TO USE THE PRODUCT.

SOME STATES DO NOT ALLOW THE EXCLUSION OR LIMITATION OF INCIDENTAL OR CONSEQUENTIAL DAMAGES FOR CONSUMER PRODUCTS, AND SOME STATES DO NOT ALLOW LIMITATIONS ON HOW LONG AN IMPLIED WARRANTY LASTS, SO THE ABOVE LIMITATIONS OR EXCLUSIONS MAY NOT APPLY TO YOU.

THIS WARRANTY GIVES YOU SPECIFIC LEGAL RIGHTS, AND YOU MAY ALSO HAVE OTHER RIGHTS WHICH VARY FROM STATE TO STATE.

Real Time Devices, Inc.

1930 PARK FOREST AVENUE
P.O. BOX 906
STATE COLLEGE, PENNSYLVANIA 16804
(814) 234-8087 TELEX 4948141 SEDACOG