Margin Considerations for an Esaki Diode-Resistor OR Gate*

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An Esaki diode-resistor logic, powered from a three-phase supply and involving OR *gates, is analyzed. Practical switching times are of the order of 10 $|R^-|$ C. The voltages at which the current maximum and the current minimum occur set an upper limit on the achievable logical gain. For a sum of fan-in plus fan-out of 3, the margins on key diode and circuit parameters must be better than ±2 per cent, with all margins assumed equal. The margins can be ±3.5 per cent for a fan-in plus fan-out of 2, which, however, restricts the applications to shift registers, flip-flops, and the like.*

I. INTRODUCTION

Esaki diodes are being considered for high-speed logic due to their potentially high switching speeds. Several papers have already appeared on the use of Esaki diodes in logic systems.[1,2,3,4,5] In such systems the bistable *V-I* characteristic of the diodes is utilized to define two logical states ("zero" and "one"). The bias current of the diode, together with a trigger current derived from a previous stage, determines which of the two states will be attained. If the trigger current can be kept small with respect to the output current, logical gain can be achieved. This generally requires that the characteristics of the diodes be well controlled, since the logical gain will primarily depend on the margins of the diodes and of the circuit parameters. Consequently, the considerations of margins become of prime importance in the design of logical systems.

In this paper, worst-case margin considerations are given for one of the simplest types of Esaki diode logic, a diode-resistor logic powered from a three-phase supply.[6] In particular, the discussion is restricted to the least complicated logical element — an OR gate.

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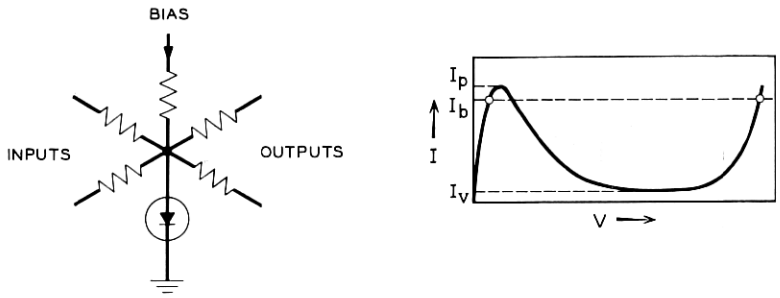

Fig. 1 — Esaki diode-resistor logic.

First, a general description of the system will be given (Section II), followed by a qualitative margin analysis (Section III).* In Section IV it is shown that the present system permits only a finite logical gain, even for zero margins and infinite switching time. The switching speed is analyzed in Section V, followed by the quantitative margin analysis (Section VI). The final result of the quantitative margin analysis is brought into a form corresponding to the qualitative analysis, which permits the reader to follow the discussion (Section VII) and the conclusion (Section VIII) without studying in detail the reasoning in Sections V and VI.

II. ESAKI DIODE-RESISTOR LOGIC

The basic stage in an Esaki diode-resistor logic consists of a series arrangement of a diode and a resistor, R_b, with input and output coupling resistors as shown in Fig. 1. The bias voltage is chosen such that, without any voltage at the far ends of the coupling resistors, it gives rise to a current through the diode which is below the peak current. Consequently, the diode will remain in its low-voltage state. With additional current supplied to the center node through one or more input (or output) resistors, the diode can be made to switch into the high-voltage state. With the bias current only slightly smaller than the peak current, very small "trigger" currents are necessary.

Once the diode is in its high-voltage state it will remain there even if current is now withdrawn at the node. It is only necessary that the current through the diode remain above the valley current I_v. The maximum current that can be withdrawn is, therefore, the difference between the bias current and the valley current. The ratio of this output current to the trigger current constitutes the logical gain.

* The authors are indebted to J. H. Vogelsong, whose unpublished margin studies are incorporated in this section.

By proper choice of the bias current, the current of at least one input or the combined current of several inputs is necessary to trigger the diode. The diode accordingly can act as an OR gate, as an AND gate or as a THRESHOLD gate. The output resistors can be connected to the node of a subsequent stage. Similarly, the input resistors are powered from nodes at previous stages. The extension of this principle leads to a logical network.

In such a network it is, however, necessary to determine the direction in which information will be propagated. One elegant method utilizes a three-phase bias supply[6] as depicted in Fig. 2. Adjacent diode stages are powered from different phases. Thus a diode on phase A, for example, is triggered from a diode on phase C, and it will trigger a diode on phase B.

Even in such a multiphase system "backswitching" can occur.[7] To illustrate this, consider the arrangement of Fig. 3. If the stages represent OR gates, one stage in a high-voltage ("one") condition will trigger a following stage. Stages 1 and 2 are powered from phase A, while stages 3 and 4 are powered from phase B. Assume that stage 1 is in the "one" condition and stage 2 is in the "zero" condition. As soon as phase B is applied, stage 3 will assume the "one" condition. Since stage 3 is coupled to stage 2, it will trigger stage 2 into the "one" condition, resulting in an erroneous "one" in stage 4.

To avoid such backswitching, a system of OR gates must be arranged in such a way that no multiple input is fed from any stage having a multiple output. Logical design then forces the use of "booster" stages, e.g., stages with one output driving stages with one input.

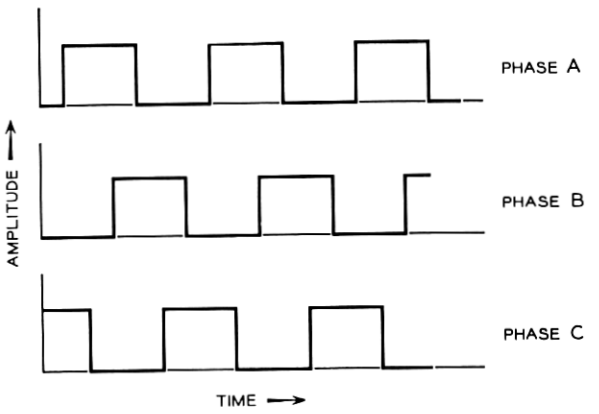

Fig. 2 — Three-phase bias supply.

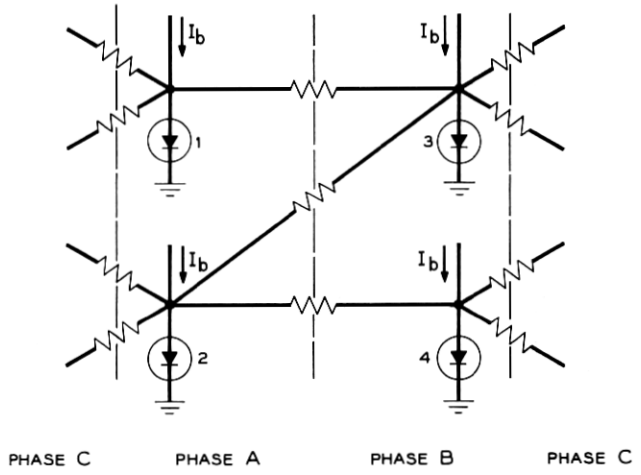

Fig. 3 — Logic network of OR gates leading to backswitching.

III. QUALITATIVE MARGIN ANALYSIS

As pointed out before, the magnitude of the trigger current depends on the difference between peak current and bias current. This difference can be made small (and therewith the logical gain large) if both parameters are tightly controlled. For an OR gate the qualitative effect of a spread in the parameters on the logical gain can be readily demonstrated.

Assume that the peak currents I_p of the devices fall in a range between I_L and I_u, and that the bias currents fall in a range between $I_{b\,\min}$ and $I_{b\,\max}$. One can then introduce such relative variations as:

$$\pi = \frac{I_u - I_L}{I_L} \tag{1}$$

and

$$\beta = \frac{I_{b\,\max} - I_{b\,\min}}{I_L}. \tag{2}$$

With a maximum valley current $I_{v\,\max}$ for all devices one can define a "valley-to-peak" ratio

$$\nu = \frac{I_{v\,\max}}{I_L}. \tag{3}$$

As pointed out before, for triggering a device, the total current through the device must exceed the peak current. It is plausible (and will be

discussed in detail in the next section) that an overdrive ΔI is necessary to ensure switching with the required speed. We thus introduce a relative overdrive

$$\delta = \frac{\Delta I}{I_L}. \tag{4}$$

In a worst-case analysis, it must be ascertained that a stage giving a minimum total output current is capable of delivering into each output stage a trigger current which is at least as big as the trigger current required in the worst-case. The logical gain, e.g., the number of stages (n) that can be connected to one output can be found by equating the minimum current that can be delivered into an output stage ($I_{\text{out min}}$) to the worst-case trigger current (I_{tr}). Due to the bilateral nature of the Esaki diode (output and input are identical), this number is the sum of inputs plus outputs ("fan-in" plus "fan-out").

For these currents the following normalizations are introduced:

$$\tau = \frac{I_{\text{tr}}}{I_L} \tag{5}$$

and

$$\eta = \frac{I_{\text{out min}}}{I_L}. \tag{6}$$

For a qualitative analysis the magnitude of these currents is found readily by graphical considerations.

Fig. 4 shows a voltage-current characteristic of an Esaki diode including variations. Since the maximum bias current must equal the

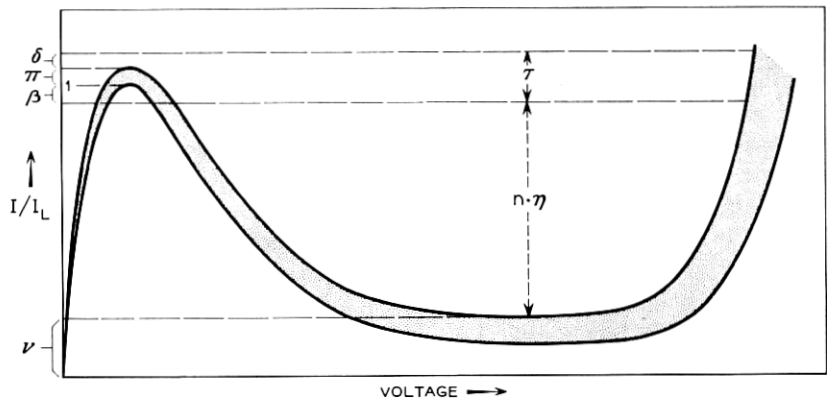

Fig. 4 — Qualitative margin analysis.

minimum peak current, the entire spread in bias currents (β) must lie below the spread in peak currents (π). Since for a unit with the highest peak current a minimum overdrive must be assured, δ must be added to the maximum peak current. From Fig. 4 one obtains for the normalized trigger current

$$\tau = \pi + \beta + \delta, \tag{7}$$

and for the total minimum output current

$$n \cdot \eta = 1 - \nu - \beta. \tag{8}$$

Equating τ and η gives the logical gain as

$$\frac{1 - \nu - \beta}{\pi + \beta + \delta} = n. \tag{9}$$

An evaluation of this equation will give a first-order estimate of the required margins. This analysis, however, neglects the effects of the peak and valley voltages, which even for zero margins will limit the logical gain under certain conditions as will be shown in the next section. For a full evaluation of the margin equations, the relation between relative overdrive δ and the switching speed must be known. This analysis will be given in Section V. The detailed margin analysis in Section VI will not only include the variables considered in (9) and the effect of the peak and valley voltages, but it also will include the variations of these voltages and the variations in the coupling resistors.

IV. LIMITATIONS DUE TO FINITE VOLTAGE LEVELS

The diode-resistor logic discussed here has an upper limit in the logical gain if stages that are to be driven have a fan-out larger than their fan-in. This limitation is determined by the magnitude of the voltages for the current peak and for the current minimum, and exists even if all error margins and the valley current are zero.

To demonstrate this effect, consider the extreme case of a stage having one input and $(n - 1)$ outputs. Assume a device characteristic as shown in Fig. 5. The magnitude of the bias current is determined by the condition that the stage under consideration is not permitted to be triggered into the high-voltage condition if none of the stages connected to either the input or the output resistor is in the high-voltage condition. Due to the bias pulse overlap with the previous and the following stages respectively, the far ends of the coupling resistors can vary in voltage between zero and V_p, the voltage at which the current maximum is reached. The coupling resistors whose far ends are at V_p will

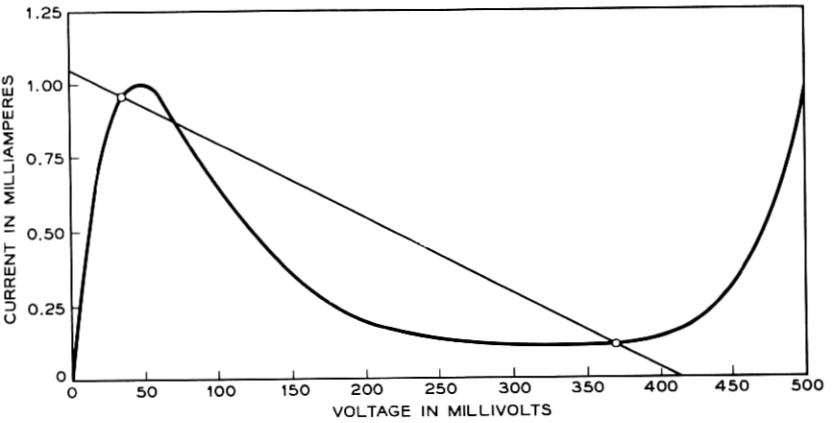

Fig. 5 — Germanium Esaki diode characteristic with load line.

not shunt any current, and it has to be ascertained that the bias current under no condition will supply a current greater than I_p to the diode. With only one coupling resistor acting as a shunt, the maximum bias current becomes

$$I_b = I_p + V_p G, \tag{10}$$

where G is the conductance of each coupling resistor.

A stage is to be triggered into the high-voltage condition at a time when the output resistors are at ground potential, and the trigger current must increase the current through the diode above the peak current. Since, for the case of one input resistor, $(n - 1)$ resistors act as shunts, one obtains for the trigger current

$$I_{tr} = I_p + (n - 1)GV_p - I_b = (n - 2)GV_p . \tag{11}$$

It must be possible to supply this trigger current from the output of one previous stage which is in the high-voltage condition. The far end of this particular coupling resistor thus is at the "valley" voltage V_v, with the near end at v_p. One thus obtains for the output current

$$I_{out} = (V_v - V_p)G. \tag{12}$$

Equating I_{out} and I_{tr} yields

$$n = \frac{V_v}{V_p} + 1. \tag{13}$$

This demonstrates that the sum of fan-in and fan-out for such an asymmetrical stage remains finite, even in the case of zero tolerances.

V. SWITCHING SPEED

The speed considerations are based on a diode characteristic as shown in Fig. 5, which shows a good but still practical characteristic for a germanium diode. The combined conductances of the input and output resistors are shown as the load line. It is chosen in such a way that while touching the peak point it intercepts the valley. This choice of the load line will allow obtaining a maximum current output.

Assume now that a current of magnitude I_0 ($> I_p$) is applied to the parallel combination of diode and load resistance as shown in Fig. 6. The capacity represents the diode capacity (plus any shunt capacitors in parallel with the diode). Any series inductances have been neglected.

During a transition from a low-voltage state into a high-voltage state, the capacity shunting the diode must be charged. The charging current at a given voltage is the difference between the supplied current I_0 and the sum of the load current and the conductive current through the diode at any given voltage. In Fig. 6 this charging current I_c can be read off as a function of voltage, since it is just the difference between the load line and the static characteristic. The time required to go from voltage V_a to voltage V_b is given by

$$t = \int_{V_a}^{V_b} \frac{C(V)\, dV}{I_c(V)} . \tag{14}$$

A numerical integration of this equation thus can give the switching time between two arbitrary points. For the problem on hand, the

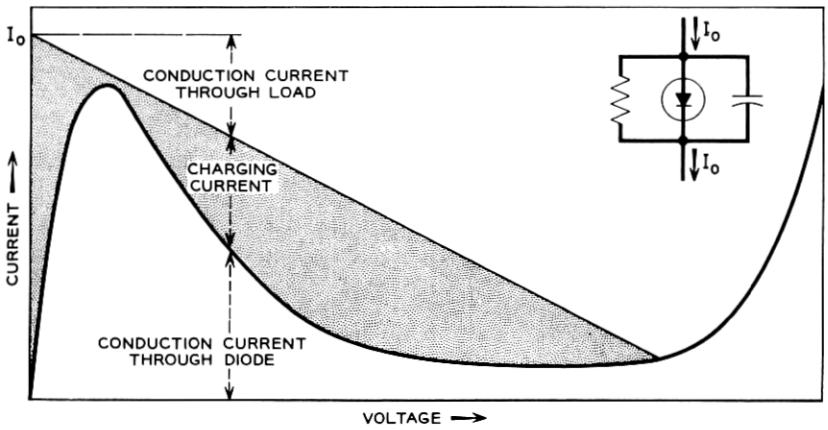

Fig. 6 — Capacitance charging current.

switching time from a low-voltage state to a high-voltage state is of interest.

Prior to switching, the diode voltage corresponds to the stable point (Fig. 5) at low voltage. After switching, the diode voltage corresponds to the stable point at high voltage. Switching is accomplished by the application of a trigger current which lifts the load line above the diode characteristic as depicted in Fig. 6. This lifting of the load line moves the high-voltage intercept to the right, and the diode voltage will approach the voltage corresponding to this intercept. After removal of the overdrive, the voltage would then decrease again. Thus, switching can be considered as completed when, with applied overdrive, the voltage of the stable point prior to the application of the trigger current is reached.

For the analysis to be independent of the particular bias current, it is convenient to consider, as final voltage, the intercept of a load line which just touches the peak. For an analytical treatment the following two simplifying assumptions will be made:

i. The voltage dependent capacity $C(V)$ will be replaced by a constant average capacity C.

ii. The diode characteristic will be approximated by two parabolic sections and a straight section.

Let A and B (Fig. 7) be the points on the diode characteristic at which the slope is equal to that of the load line, and let I_A and I_B be the charging currents at these points. Let C be the point at which one parabolic

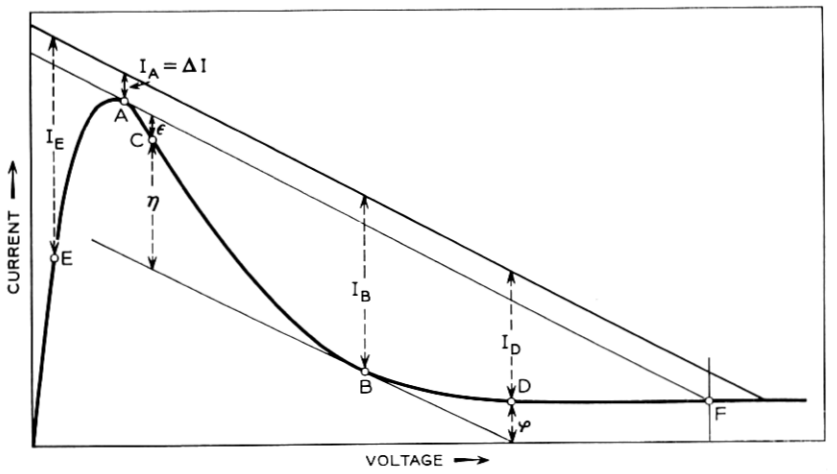

Fig. 7 — Analysis of the switching time.

approximation joins the second approximation and let D be the point where the straight section commences. Then the time needed to switch from an arbitrary point E in the low-voltage part to the final point F is given by

$$t = C\left[\int_{V_E}^{V_C} \frac{dV}{I_A + I_p\left(\frac{V - V_A}{V_2}\right)^2} + \int_{V_C}^{V_D} \frac{dV}{I_B - I_p\left(\frac{V - V_B}{V_2}\right)^2} + \int_{V_D}^{V_F} \frac{dV}{I_A + (I_D - I_A)\frac{V_F - V}{V_F - V_D}}\right]. \tag{15}$$

Here the constants describing the curvature of the parabolas are expressed in terms of the peak current, and in terms of constants V_1 and V_2 having the dimension of voltages. Such a presentation is convenient since the constant V_1 is equal to the peak voltage and the constant V_2 is of the order of magnitude of the difference between valley voltage and peak voltage. Note that V_1 and V_2 depend on the diode characteristic only and are independent of the load line. Performing the integration of (15) yields

$$\tau_s = \frac{CV_1}{I_p}\sqrt{\frac{I_p}{I_A}}\left(\tan^{-1}\frac{\epsilon}{I_A} + \tan^{-1}\frac{I_E}{I_A}\right) + \frac{CV_2}{I_p}\sqrt{\frac{I_p}{I_B}}\left(\tanh^{-1}\frac{\eta}{I_B} + \tanh^{-1}\frac{\varphi}{I_B}\right) + C\frac{V_F - V_D}{I_D - I_A}\ln\left(\frac{I_D}{I_A}\right). \tag{16}$$

The constants in this equation are defined in Fig. 7. It should be noted that I_A corresponds to the overdrive ($I_A = \Delta I$) and that $I_A/I_p = \delta$ as defined in (4). For an evaluation of this equation, the value of the capacity C must be known. This capacity, however, can be expressed through the characteristic time $\tau_0 = |R^-|C$, which time is usually considered as the figure of merit for an Esaki diode. It is therefore possible to express the switching time in terms of the time τ_0. With such a normalization, the results of the analysis will be fairly general.

Fig. 8 shows an evaluation of (16) giving the switching times in terms of the characteristic time τ_0 for switching from zero to the final voltage. The assumed value of the load line permits a maximum output current while conforming with the margin considerations. Using zero instead of a finite voltage as the starting point lengthens τ_s only insignificantly.

As can be seen in Fig. 8, the switching behavior can be fairly well approximated by

$$\tau_s/\tau_0 = 2.25\sqrt{I_p/I_A} = 2.25/\sqrt{\delta}. \tag{17}$$

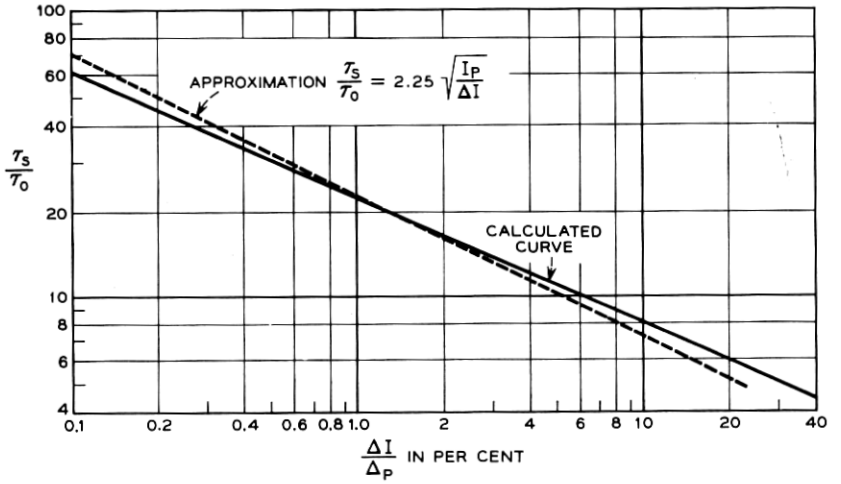

Fig. 8 — Switching speed.

VI. QUANTITATIVE MARGIN ANALYSIS

The qualitative margin analysis of Section III neglected variations of the coupling resistors, the effect of the peak and valley voltage, and the variations of these voltages. As a simplification in the complete analysis it will be assumed that the bias is supplied from a constant current source. Under this assumption the total load line of the diode is given by the sum of the conductances of the input and output resistors. These resistors will terminate at the nodes of adjacent units, and it is necessary to include the voltage of these nodes in the analysis.

As in the qualitative analysis one has to find the current which in the worst case will trigger a stage within a desired time. This current must equal the minimum current that under worst conditions will be delivered into an output resistor.

6.1 *Trigger Current Needed*

The lower the bias current, the larger will be the necessary trigger current. The maximum bias current, however, must be low enough that the stage under consideration will not assume the high-voltage condition unless one driving stage is in such a high-voltage condition. The margin of the bias current then determines the difference between the maximum and the minimum bias current.

The characteristics of all diodes in a system will show a spread, and will fall between two extreme characteristics, which represent the ac-

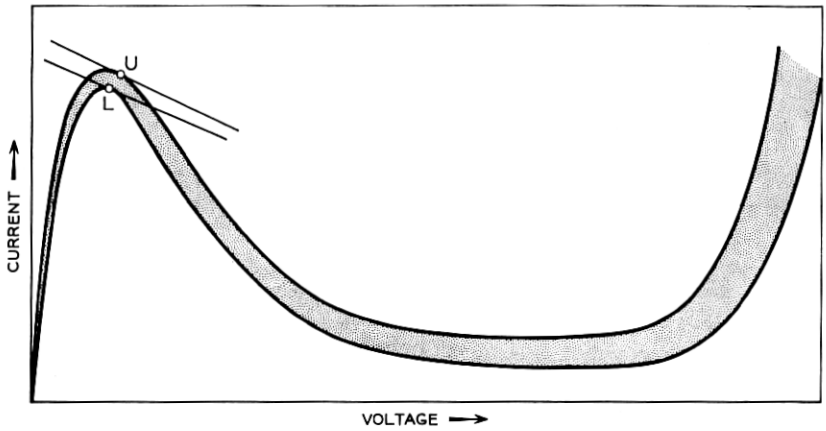

Fig. 9 — Spread in characteristics.

ceptance limits. Such extremes are indicated in Fig. 9. The conductance of the n_i input resistors and the n_0 output resistors will fall between an upper bound of value G_u and a lower bound of value G_L.

For the following analysis one determines the point L (Fig. 9) where a load line of the lowest total conductance $(n_i + n_0)\, G_L$ is tangent to the lower characteristic, and the point U where the load line of largest conductance $(n_i + n_0)\, G_U$ is tangent to the upper curve. The voltages and currents corresponding to these points are V_U, V_L, I_U and I_L respectively.

In a three-phase system as considered here, only two adjacent units will be powered at the same time. Thus one has two extreme conditions under which the unit under consideration should not be triggered:

i. The unit under consideration and the previous unit are powered, in which case the far ends of the input resistors may be as high in voltage as V_L while the output resistors are at ground potential and

ii. The unit under consideration and the following unit are powered, in which case the far ends of the output resistors may be as high as V_L in voltage while the input resistors are at ground.

The maximum permissible bias current should not switch a unit if it has the lowest peak current and if the smallest current is shunted by the coupling resistors. This current is given by

$$I_{b\ \max} = I_L + n_{\min} G_L V_L, \tag{18}$$

where $n_{\min}$ represents the minimum of n_i or n_0. The minimum bias current is below the maximum bias current by the spread in bias currents ΔI_b

$$I_{b\,\min} = I_{b\,\max} - \Delta I_b . \tag{19}$$

In order to trigger a diode it is necessary that a current of at least I_U plus necessary overdrive for speed is delivered to the diode. This current will be the sum of the minimum bias current plus the trigger current minus the current drained through the input and output resistors. However, since at least one stage has to supply the trigger current, only $n_i - 1$ input stages can act as a load. Thus one obtains under worst-case conditions

$$I_U + \Delta I = I_{tr} + I_{b\,\min} - G_U V_U n_0 - (n_i - 1)\, G_U\, (V_U - V_{\text{off min}})_L . \tag{20}$$

In this equation $V_{\text{off min}}$ is the minimum off-voltage a unit can assume. (It should be realized that the voltage V_L discussed previously can be considered as $V_{\text{off max}}$.)

To bring (20) into normalized form the following quantities are introduced

$$\rho = \frac{G_U - G_L}{G_L} , \tag{21}$$

$$\sigma = \frac{V_U - V_L}{V_L} , \tag{22}$$

$$\varphi = \frac{V_U - V_{\text{off min}}}{V_L} , \tag{23}$$

$$\gamma = \frac{G_L V_L}{I_L} . \tag{24}$$

With these definitions and with the definitions (1), (2), (3), (4) and (5), equation (20) combined with (18) and (19) gives for the normalized trigger current

$$\tau = \pi + \beta + \delta + \gamma[(1+\rho)(1+\sigma)n_0 - n_{\min} + (1+\rho)\varphi(n_i - 1)]. \tag{25}$$

The term multiplied by γ involves the additional terms not present in the equivalent equation (7) of the qualitative analysis.

6.2 *Output Current Available*

In a three-phase diode system as discussed here, the output current must be available while the stage under consideration and the output stages are powered. The nodes of the input stages accordingly are at zero potential while the output stages are at the peak voltage. Certainly the driving stage is in the high-voltage condition and its voltage corresponds to a voltage V_v in the "valley" of the characteristic.

One thus can represent the situation by a circuit as shown in Fig. 10.

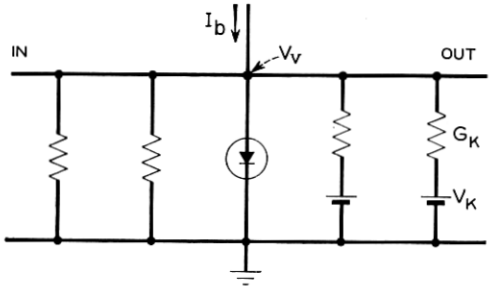

Fig. 10 — Derivation of output current.

The conductances G_k represent the coupling resistors and the voltages V_k fall in the range of the peak voltages. For the analysis it is more convenient to represent the voltages V_k and their associated conductances as current sources feeding the node. This leads to the representation as shown in Fig. 11. Here it must be remembered that $V_k = 0$ for the input conductances. From this representation the valley voltage V_v is readily obtained as

$$V_v = \frac{I_b + \Sigma V_k G_k - I_v}{\Sigma G_k} . \tag{26}$$

If G_j represents one particular coupling resistor to an output stage the current into this stage is readily obtained:

$$I_{\text{out}} = I_j = (V_v - V_j)G_j . \tag{27}$$

Substituting V_v from (26) gives

$$I_{\text{out}} = \frac{I_b + \Sigma V_k G_k - I_v - V_j \Sigma G_k}{\Sigma G_k} G_j . \tag{28}$$

This current has a minimum if

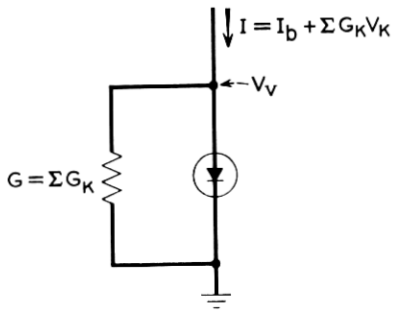

Fig. 11 — Circuit equivalent to Fig. 10.

$$\begin{aligned} I_b &= I_{b\,\min}\,, \\ G_j &= G_L \quad \text{and all other } G_k = G_U\,, \end{aligned} \tag{29}$$

and if for the output stages

$$V_j = V_u \quad \text{and all other } V_k = V_L\,.$$

Introducing these conditions into (28) and substituting, one obtains in normalized form:

$$\begin{aligned} \eta[n + (n-1)\rho] = 1 - \nu - \beta - \gamma[&(1+\rho)\,(1+\sigma)n_i - n_{\min} \\ &+ (1+\rho)\sigma(n_0 - 1)]\,. \end{aligned} \tag{30}$$

Again, this expression has additional terms which are absent in the equivalent equation (8) of the qualitative analysis.

6.3 *Logical Gain*

To determine the sum of fan-in plus fan-out, the normalized trigger current, (25), must be set equal to the normalized output current, (30). For this it is necessary to consider the particular configuration in which stages are interconnected.

For a given n, the trigger current, (25), will have a maximum if $n_i = 1$ and $n_0 = n - 1$. Similarly, the output current, (30), will have a minimum if $n_i = n - 1$ and $n_0 = 1$. Thus the worst combination of two stages is the case in which a stage with a multiple input and a single output drives a stage with a single input and a multiple output. Such a combination represents a "booster" stage, which is an important configuration to avoid backswitching. In the following, the analysis will therefore be given for such a combination. At this point it is convenient to introduce

$$n^* = n + (n-1)\rho. \tag{31}$$

For the worst-case combination of stages, (25) and (30) take then the form

$$\tau = \pi + \beta + \delta + \gamma[(n^* - 1)(1+\sigma) - 1], \tag{25a}$$

$$n^*\eta = 1 - \nu - \beta - \gamma[(n^* - 1)(1+\sigma) - 1]. \tag{30a}$$

Besides the variations of all parameters, these equations involve the value of the coupling resistors in the term γ. Since the load impedance determines the operating point in the high-voltage condition, one can express γ by this point, i.e., by the valley voltage and the valley current. Due to the variations in the load conductances and the bias current, this operating point must be defined for a particular combination of

these parameters. The combination to be chosen is the one leading to the minimum output current. One thus can use (26) to express γ in terms of the valley voltage V_v and the valley current I_v. Introducing the condition (29) into (26) (and assuming the particular configuration under discussion) gives:

$$V_v = \frac{I_{b\,\min} + V_U G_L - I_v}{(n-1)G_U + G_L}. \tag{32}$$

It is plausible (and can be proven readily) that a device characteristic leading to an operating point with a higher voltage V_v or a lower current I_v results in a higher output current. Thus the operating point as defined by (28) is a worst-case condition; such an operating point is schematically indicated in Fig. 12. It specifies an area (shaded) which must be cleared by the high-voltage branch of all diode characteristics.

Introducing a normalized valley voltage

$$y = \frac{V_v}{V_L} \tag{33}$$

and using all previous normalizations permits one to use (32) for the elimination of γ:

$$\gamma = \frac{1 - \nu - \beta}{n^* y - (\sigma + 2)}. \tag{34}$$

Equating τ and η as given in (25a) and (30a) and using the above expression for γ leads to the final result:

$$\frac{1 - \nu - \beta}{\pi + \beta + \delta} = \frac{[n + (n-1)\rho]y - (\sigma + 2)}{y - [n + (n-1)\rho](\sigma + 1) + 1}. \tag{35}$$

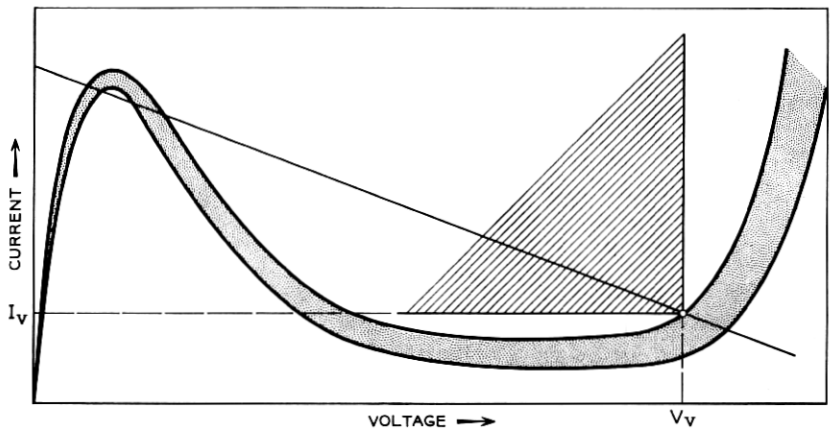

Fig. 12 — Significance of valley voltage and valley current.

VII. DISCUSSION

The final expression of the quantitative margin analysis, (35), differs from the qualitative result obtained in Section III, (9), in the right-hand side only. While in the qualitative expression the right-hand side is the sum of fan-in plus fan-out (n); in the quantitative expression the right-hand side is a function of n and these additional variables: the relative variation in the conductances of the coupling resistors ρ, (21); the relative variation in the voltage for the current peak σ, (22); and the minimum ratio of valley voltage to peak voltage ν, (33).

On account of the similarity in the results it is convenient to introduce a generalized $\tilde{n}$ defined as

$$\tilde{n} = \frac{[n + (n-1)\rho]y - (\sigma + 2)}{y - [n + (n-1)\rho](\sigma + 1) + 1}. \tag{36}$$

Even for σ and ρ equal to zero the generalized $\tilde{n}$ becomes infinite for

$$n = y + 1. \tag{37}$$

An infinite $\tilde{n}$ implies zero margins for all variables and zero overdrive. Thus the result of Section IV is recovered.

In considering the effects of finite margins, specific assumptions as to the relative magnitude of the margins on the various variables must be made. For the primary variables in the left-hand side of (9) or (35), the maximum ratio ν of valley current to peak current is assumed as 0.1, since this corresponds to a good ratio achievable in germanium units. The relative overdrive δ will be expressed in terms of the switching speed using the calculated relation obtained in Section V. The result is shown in Fig. 8, which gives the switching time τ_s in terms of the characteristic time $\tau_0 = | R^- | C$ as a function of the relative overdrive δ.

The other quantities of the left-hand side will be treated as independent variables. To keep the discussion fairly general, we assume that all significant parameters are kept within the same relative variation.

In general, the bias current will be determined by a voltage and a resistor. Thus the spread in bias current β is the result of an uncertainty in a voltage and in a resistor. In worst-case analysis the two margins have to be added. Assuming the two margins to be equal and introducing a relative maximum variation, x, from the center value, one can express β as:

$$\beta = 4x. \tag{38}$$

In the analysis, no mention has been made of noise; in particular, the

possibility of undesirable crosscoupling between stages. Such "noise" most conveniently can be expressed in an equivalent relative variation of the peak currents. The parameter π accordingly contains noise as a second variable besides the actual variation in peak currents. Equating these variations to the variations in the bias current results in:

$$\pi = 4x. \tag{39}$$

Fig. 13 shows a plot of (9) with β and π expressed by (38) and (39) respectively and with $\nu = 0.1$. It can be seen from the figure that even for small logical gain fairly tight margins are required. It also becomes apparent that switching speeds below 10 τ_0 are impractical.

To evaluate the importance of the margins of the additional variables, which enter in $\tilde{n}$, the relation (36) between actual n and generalized $\tilde{n}$ has to be evaluated. Fig. 14, as an example, shows this relation for an actual $n = 3$, which corresponds to the minimum sum of fan-in plus fan-out required in a logical network. It can be seen that with an increasing ratio of valley voltage to peak voltage (y) the limiting value of $\tilde{n} = n + (n - 1)\rho$ is rapidly approached. It also becomes apparent that, for sufficiently large values of the valley voltage, the spread in peak voltage and in the values of the coupling resistors are only of minor importance.

Since for good germanium Esaki diodes $y \geqq 8$ for $\nu \leqq 0.1$, these

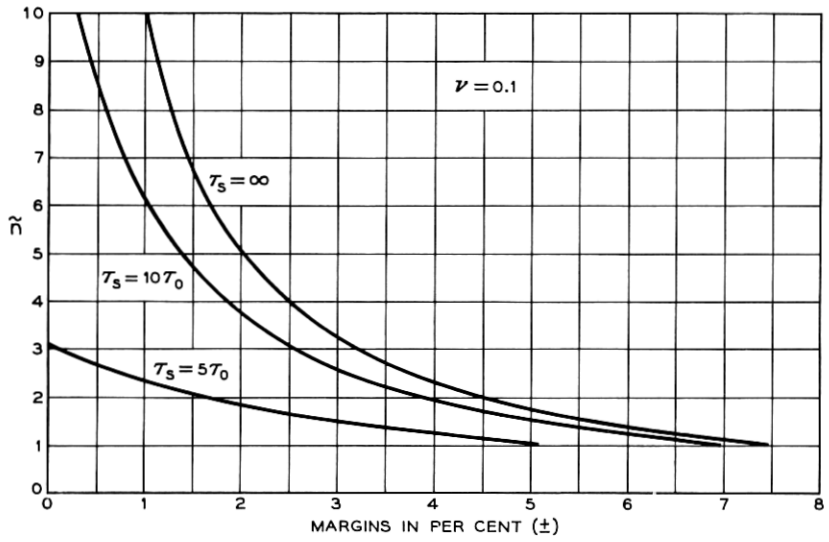

Fig. 13 — Permissible variations from nominal value of the important parameter as a function of generalized $\tilde{n}$.

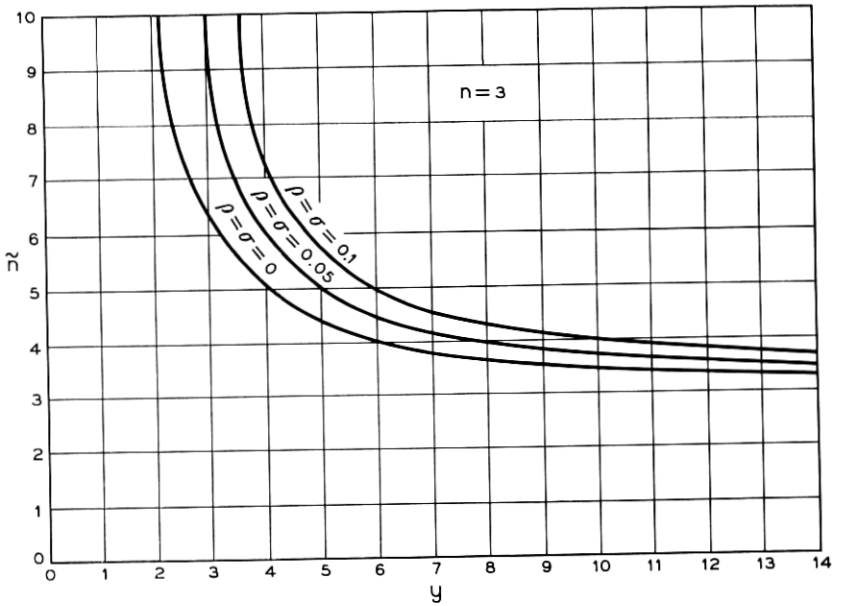

Fig. 14 — Generalized $\tilde{n}$ as a function of $y = V_v/V_L$.

values have been assumed in the construction of Fig. 15, which shows the dependence of the sum of fan-in plus fan-out (n) on the percentage variations x from the correct value of the bias voltage, the bias resistor and the peak current, and a noise equivalent current expressed as a percentage of peak current. Because the effects of the coupling resistors and the peak voltage are relatively small, a fixed relative variation of ± 2.5 per cent has been assumed for these quantities.

VIII. CONCLUSIONS

An Esaki diode resistor logic with three-phase power supply shows several basic limitations even if it only involves OR gates.

The possibility of backswitching limits the design of logical networks, requiring the incorporation of "booster" stages in which a device with one output drives a device with one input.

Switching times shorter than $10 \mid R^- \mid$ C are not practical; however, this is not a very severe limitation.

The finite ratio of the voltage for the current minimum to the voltage for the current maximum limits the logical gain even for the case of zero margins.

From Fig. 15 it is apparent that, even for a sum of fan-in plus fan-out

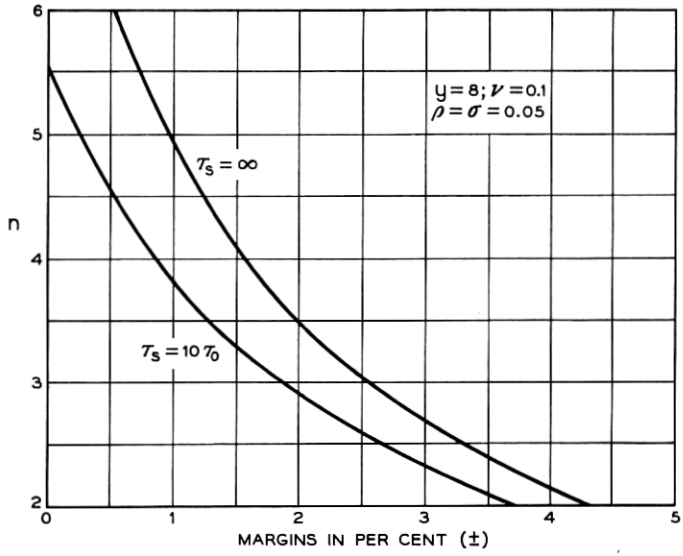

Fig. 15 — Permissible variations from nominal value of the important parameter as a function of fan-in plus fan-out for a specific example.

(n) equal to 3, worst-case margins of less than ±2.5 per cent are required. For an AND gate, a two-sided limit on the trigger current is required, making the margins even tighter. It thus appears questionable that an Esaki diode resistor logic with $n \geqq 3$ is practical, if operation under worst-case conditions is to be guaranteed.

Only for $n = 2$ do the margins appear tolerable under worst-case conditions. However, such a value of n does not permit the construction of a complete logic network, and implies a restriction to applications such as memories, flip-flops, shift register and the like.

REFERENCES

1. Lewin, M. H., Samusenko, A. G. and Lo, A. W., The Tunnel Diode as a Logic Element, Solid State Circuits Conf., Philadelphia, 1960.
2. Neff, G. W., Butler, S. A. and Critchlow, D. L., Esaki (Tunnel) Diode Logic Circuits, Solid State Circuits Conf., Philadelphia, 1960.
3. Miller, J. C., Li, K. and Lo, A. W., The Tunnel Diode as a Storage Element, Solid State Circuits Conf., Philadelphia, 1960.
4. Chow, W. F., Tunnel Diode Digital Circuitry, Solid State Circuits Conf., Philadelphia, 1960.
5. U. S. Navy Department, Bureau of Ships, Electronic Division, *The Dener Diode as a Digital Computer Element* — Phase 1, Project Lightning, Vol. 4, Ch. 8, p. 83.
6. Goto, E., On the Application of Parametrically Excited Nonlinear Resonators, J. Inst. Elect. Comm. Eng. Japan, **38**, 1955, p. 770.
7. Taylor, R. G., unpublished work.