A Block Diagram Compiler

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A computer program known as BLODI, which accepts for an input a source program written in the BLODI language, is described. The BLODI source language corresponds closely to an engineer's block diagram of a circuit and is easily learned, even by persons not familiar with computing machines. The input code consists essentially of designating the connectivity of a number of boxes drawn from an alphabet of about 30 types. These types include amplifiers, delay lines, counters, etc., which are familiar to designers of electronic circuits. The principles of the compiler are explained and applications are discussed.

I. INTRODUCTION

This paper describes a computer program known as BLODI (BLOck DIagram compiler). BLODI accepts for an input a source program written in the BLODI language, which corresponds closely to an engineer's block diagram of a circuit, and produces a machine program to simulate the circuit. BLODI has been written for both the IBM 704 and 7090 machines, and has been in use at Bell Telephone Laboratories for several months. Generally speaking, there are two situations in which it can be used profitably. One arises when a person with no knowledge of machine coding wishes to program his own problem. In this case, the BLODI language is much easier to learn than Fortran or SAP. There are, in addition, certain problems involving a rather smooth flow of data which can be most easily coded in BLODI, even by an experienced programmer.

It is rather easy to estimate the efficiency of an object program produced by BLODI. Thus a person with no knowledge of computing machines can often tell if he should code his problem in BLODI or seek the aid of an experienced programmer. This will be discussed in Section V.

BLODI was written to lighten the programming burden in problems concerning the simulation of signal-processing devices. It has the added advantage of keeping the engineer who invents such a device in close communication with the computing machine by eliminating the middleman (expert programmer).

II. BLOCK DIAGRAM OF SAMPLED (OR PULSE) SYSTEMS

The circuits* which we wish to consider here are limited to combinations of devices which accept pulses as inputs and yield pulses as outputs. While the pulses may have arbitrary sizes within certain limits, they must all occur at multiples of a fixed clock time. In general, the output of one of the devices (or boxes) can depend on the present and all past input pulses. A box whose output is independent of the current input pulse or pulses is called a *delaying-type box*. In the current form of the compiler the only delaying-type box is a simple delay line. In addition to these boxes, the circuit may have one or more ultimate outputs and original inputs. A *circuit* then means a number of boxes, ultimate outputs, and original inputs connected in such a way that the output of any box is connected to one or more inputs to boxes and ultimate outputs, and each input to a box is connected to an output from a box or an original input. (We limit ourselves to boxes with a single output.)

A closed loop is a path that starts from any point, goes only through connected boxes in the direction of the pulses (i.e., input to output), and returns to its starting point. A circuit which does not contain a closed loop with no delaying-type boxes will be called an admissible circuit. The compiler will reject any block diagram which does not describe an admissible circuit. It is easy to see that if the pulse heights were limited to a finite number of values (as they are, of course, in the machine simulation) then an admissible circuit would be a finite-state machine. On the other hand, there is no way to interpret a block diagram corresponding to a nonadmissible circuit. To be sure, one could connect physical boxes in such a manner and something would happen. The analysis, however, would involve the precise transient behavior of the devices within the pulse width — information which is not available to the compiler.

In addition to simulating pulse circuits, the compiler may be used to simulate continuous circuits whose inputs and outputs are bandlimited time functions. One must first design a pulse circuit whose output pulses would correspond to the sample values of the desired output. Extreme

^{*} For clarity the machine being simulated will be called the *circuit*. Its description in a certain canonical form will be called the *block diagram*. The word machine will always mean the IBM 704 EDPS (or 7090 EDPS).

care must be exercised here; for example, an accumulator (a device whose output is the sum of all previous input pulses) is not equivalent to an integrator. Certain continuous circuits (especially nonlinear ones) are extremely difficult to translate into pulse form. A simple circuit which is difficult to simulate on a machine (with or without the use of this compiler) is the following: Let a bandlimited input signal be connected to a full-wave rectifier, and this to a low-pass filter to return the signal to the original bandwidth.

We will see later that (with a trivial exception) the compiler can be used to simulate any admissible circuit composed of boxes drawn from a fixed list or stockpile. The boxes may have only one output (which may go to several places, however) and at most four inputs. The first constraint is no real restriction, but the second one is.* We know of no example in signal processing where a general function of more than four variables that cannot be expressed as combinations of functions of four or less variables is needed. In fact, two inputs to each box would probably be adequate but slightly awkward.

III. THE BLODI LANGUAGE

A BLODI source program is punched on standard SHARE symbolic cards in either the FAP (7090) or SAP (704) format. In general, each card corresponds to one box in the circuit; there is, however, a provision made for continuing a description of a box to the next card. The location field (columns 1 through 6) is either blank or contains the name assigned the box by the programmer. (If a box is to have any inputs, it must have a name.) The operation code field (columns 8 through 10) contains the type of box. Parameters (such as gain of an amplifier) and output connections are separated by commas and listed consecutively starting in column 12 (or column 16 for the 7090 format). The various inputs to the same box are designated by a fraction bar and numeral following the name of the box. Example:

UV AMP 5.28, XY, Z/2

Box UV is an amplifier with a gain of 5.28 which feeds box XY (first input) and the second input of box Z.

A list of all the available box types appears in Table I. Note that INP may be thought of as a box which generates signals spontaneously; actually it obtains its input from a tape designated as a parameter. Simi-

^{*} Technically speaking, this is not true. A circuit could be designed corresponding to any finite state machine. However, we consider that it is not in the proper spirit to take advantage of the fact that the pulse heights are limited to 2³⁶ values.

Table I — All the Types of Boxes Which are Recognized by the Compiler

Туре	Function	Inputs	Parameters
DEL	Delay	Signal	Number of units delay
AMP	Amplifier	Signal	Gain
ADR	Adder	1-4 Signals	None
SUB	Subtractor	+ Input	None
SOD	Bubliaciói	- Input	110116
MAX	Maximum circuit	1-4 Signals	None
MIN	Minimum circuit	1-4 Signals	None
CLP	Positive clipper		
CLN	Negative clipper	Signal	Clipping level
		Signal	Clipping level
SCL	Symmetric clipper	Signal	Clipping level
FWR	Full-wave rectifier	Signal	None
BAT	Battery or bias	(Signal)	Bias
MRP	Multiplier	2 Signals	None
DIV	Divider	Dividend	None
		Divisor	
sqt	Square rooter	Signal	None
ACC	Accumulator	Signal	Gain
FLT	Transversal filter	Signal	Number of taps
			Delay per tap
			Gains
SLF	Symmetric filter	Signal	Number of taps
	Symmetric zerot	io gran	Delay per tap
		1	Gains
AFL	Antisymmetric filter	Signal	Number of taps
m L	Antisymmetric meet	Digital	Delay per tap
			Gains
QNT	Quantizer	Signal	Number of levels
CLAI	Quantizer	Signai	Levels
LOT	Linear quantizer	Signal	Step size
$_{ m SMP}$			Period
SML	Sampler	Signal	
			Quiescent level
$_{\mathrm{HLD}}$	Cample and hold	C:1t1	Initial phase Threshold
	Sample and hold	Signal; control	
CNT	Counter	Signal	Countdown factor
	1		Threshold
			Active level
			Passive level
-			Initial phase
DTS	Double-throw switch	Control;	Threshold
		2 signals	
FLF	Flip-flop	Signal	Low threshold
			High threshold
			Low state output
			High state output
PLS	Pulser	Control	Threshold
	1		Pulse length
			Pulse level
		Α.	Quiescent level
CØS	Cosine generator	None	Period
2,000	8-30-31		Phase
			Amplitude
GEN	Function generator	None	Period
CLEAT	Tunction generator	210110	Sample values
WNG	Noise generator	None	Standard deviation
PRT			
LILI	Printer	Control;	Threshold
		3 signals	Record Limit

Type	Function	Inputs	Parameters
INP	Input	None	Tape number File maximum Samples per record Record maximum Start printing Stop printing
ØUT	Output	Signal	Tape number File maximum Samples per record Record maximum Start printing Stop printing
END	Last card of source	program	-

Table I — (Continued)

larly, OUT causes the signal appearing on its input lead to be written on the designated tape. A circuit may have several inputs and outputs. END is not a box at all but signifies the end of the source program. In addition to the types listed, it is possible for a programmer to create types of his own invention by supplying subroutines written in basic machine language. It is also quite easy to change the basic input-output programs used by BLODI to handle arbitrary tape formats.

IV. PRINCIPLE OF OPERATION

An object program produced by the compiler consists of three parts:

- (a) the prefix, which sets up the logic for the main loop;
- (b) the main loop, which is executed once for each sample processed;
- (c) the suffix, which causes the main loop to be repeated the proper number of times, empties output buffers, fills input buffers, etc.

We will concern ourselves here only with the main loop. Except for some strictly local inner loops in certain boxes, this part of the object program is compiled in the same order in which it is to be executed. Simply stated, the procedure is as follows: One storage cell in the object program is assigned for each box. Each time the main loop is entered, these cells will contain values corresponding to the last *outputs* of the respective boxes. It is then the function of the main loop to compute these output values for the next (current) time slot and to fill the cells with these values.

In order to simplify the description of the algorithm used by the compiler we will at first limit ourselves to the case where all delays are unit delays. By "compiling a box" we mean writing the necessary coding to

cause the object program to fill the output cell of the box with the current pulse value. A nondelaying-type box cannot be compiled until all the boxes feeding it have been compiled. The reason is that the output of this type of box is a function of its current inputs, and this part of the object program must not be executed until the cells corresponding to input to this box have been filled with current pulse values. On the other hand, a unit delay must be compiled before the box which feeds it. Its output is a function of (equal to, in fact) its last or old input. At object time this value must be "moved along" before it is overwritten. To reword this second rule, no box which feeds a delay line can be compiled until that delay line has been. This second rule could be dropped if we provided an additional storage cell for each unit delay and had the object program first go through and fill each of these cells with the old input to the corresponding delay line. We will see below, however, that the only price we pay for the more efficient procedure is that the compiler will reject any block diagram containing a closed loop with nothing but delays. Such a diagram would represent an admissible circuit but would be of little value, since we could never get anything but zeros out of this loop at any point. (All delay lines are initialized at zero.)

The above two rules are effected in a fairly simple manner. A binary storage cell is assigned in the compiler program for each of the output cells in the object program. The two states of each of these cells are called "full" and "empty." Initially all cells which represent inputs to delay lines are marked "full" and all others marked "empty." A box can be compiled whenever its inputs are all marked "full" and its output "empty." When a box is compiled, its output is marked "full" and its inputs "empty." Compilation proceeds until all boxes have been compiled (successful compilation) or until no uncompiled box meets the two requirements. In the latter event the compiler prints the remark CLOSED LOOP WITH NO DELAYS OR ALL DELAYS and halts. To see that one of these conditions must prevail, note that a delay line can always be compiled unless it feeds another uncompiled delay line. Therefore, if any of the uncompiled boxes are delay lines there exists a closed loop with all delays. If, on the other hand, all uncompiled boxes are nondelaying, then each must have an empty input which must be the output of an uncompiled nondelaying box. Thus, working backwards, we find a closed loop with no delay.

The order of searching for uncompiled boxes which meet the tests is immaterial from a logical point of view, but this freedom can be used to optimize the use of the accumulator. By first trying to compile a box which is fed by the last compiled box, the compiler is sometimes able to save a "storage" or "fetch" order, or both. Delays are not, of course, limited to unit delays as in the above discussion. A delay of length n sets n-1 storage cells in addition to its normal output cell. For short delays the data are "stepped along" a notch each time the main loop is executed. For longer delays the same effect is produced by address modification.

The above description is merely a sketch of the general procedure used by BLODI. Actually, it has a lot more structure of purely technical character. For example, some boxes are broken down into simpler boxes by the compiler so that parts of the object program concerning a given box may not appear in consecutive locations.

v. conclusions

BLODI has been in use at Bell Telephone Laboratories for about a year, mostly in the Department of Visual and Acoustics Research. It has been used chiefly for signal processing types of problems, and one of the authors has used the compiler to simulate a speech synthesizer of the resonant-vocoder type. It has also been used to study television coding schemes, artificial reverberation in acoustic research, and for part of the coding in a handwriting recognition problem. In appraising its value one must consider two separate questions:

- 1. What type of problem is easily coded in the BLODI language?
- 2. What type of problem causes BLODI to write efficient object programs?

The first question will be answered relative to a programmer well versed in basic and Fortran language. Whenever the problem involves a rather smooth flow of data in and out of the machine, with the output being a nearly stationary function of the input, then it can be more easily coded in BLODI than in any other existing language. When, however, the program must process input samples in a complicated order, dependent on previous results, the BLODI language becomes unbearably awkward. (This is precisely the type of circuit which is hard to design with delay lines, switches, etc.)

The second question is easily answered. Any diagram which contains many idle boxes will be inefficient, because the object program goes through the motion of calculating the state of all boxes at each clock time. For example, a program with five memory-free (delay-free) paths, only one of which is connected to the output at any one time, would result in an inefficient object program. For diagrams containing few idle boxes, however, BLODI produces object programs which are usually as efficient as those written by a competent programmer.

The version of BLODI in use at Bell Telephone Laboratories is coupled to the monitor and I-O system, BE SYS 3. Thus an installation not us-

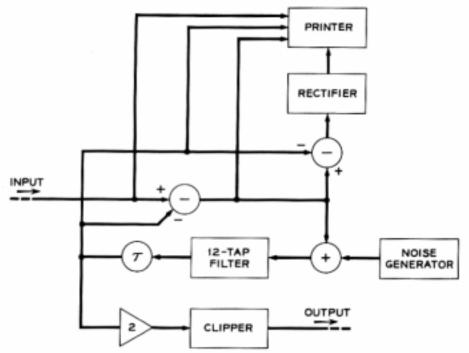


Fig. 1 — Typical BLODI program: block diagram.

	WHG	SUM/1,100	
SUM	ADR	BUFF	
BUFF	FLT	.063,1/8,.230,1/4	004,.008,.016,.032 4,1/5,.057,DELAV
DELAY	DEL	1,SCALE,SUB/2	
		PRINT/3,SUB1/2	XXX
SCALE	AMP	2+CL P	
CLIP	CLN	T2	
T2	OUT	-5	
		,,,1,1	XXX
SUB	SUB	SUM/2	
		SUB1/1,PRINT/4	XXX
T1	INP		
		PRINT/2,1,1	XXX
SUB1	SUB	R	THESE CARDS AND THE CARDS MARKED
R	FWR	PRINT/1	XXX WOULD BE OMITTED IF
PRINT	PRT	150	PRINTING WERE NOT DESIRED
	END		

Fig. 2 — Typical BLODI program: source program.

ing BE SYS 3 would have to modify the BLODI program. The changes, however, would only involve I-O and interaction with the FAP (or SAP) assembly program.

Figs. 1, 2, and 3 represent a sample BLODI program. Fig. 1 is a block diagram suitable for simulation using BLODI; Fig. 2 is the corresponding source program; and Fig. 3 shows the printed output that results from compiling the source program and running the simulation.

REFERENCE

 Frishkopf, L. S., and Harmon, L. D., Machine Recognition of Cursive Script, Fourth Annual Symposium on Information Theory, 1960.

PAGE	1		A1774		***			
			00101	REED	500		1500	
			-00216-	-WHITE			147	
			00401	MNG	Eeu		257	
			00427	567	604		979	
			00515	085	Eeu		333	
	00734	0-00000 0		-01	-076			
	02735	0140 00 0		D		**1		
	92776	0760 00 0	03012		-001			
	02737	0761 00 0			NOP			
	02740	3-00000-0			THE			
	02741	0502 60 0				+-1		
	02742	-0601-01-0				+-2		
	02743	0534 00 1				L+!		
	02744	D600-00-F				*-1.		
	02745	2 00001 1				-9925		
	02747	0500 00 1					000.1	TI
	02780	-0601-00-0				T+16		
	02751	0500 00 0				T+2		DELAY
	99750	0501 00 0				Tes		
	02753	0767 00 0			81.5			8000,6
	02754	9569-91-0			-100			0.16
	02755	0940 00 0				4+2		
	42756	0500-00-0				0		
	02757	0601 00 1			STO	0+57	777.1	12
	02340	0500-00-0	03322		-64-6	T+14		DWFF
	02761	0765 00 0	00047		LRS	43		
	02762	0200 00 0	03267		- HOW	0+1-		
	02763	0.163 00 0			LLS		00	
	92764	6769 99 9			-990			
	02765	0401 00 0				1+11		
	42746	0500-00-0				T+14		
	02767	9765 00 0				T+14	•	
	62770	0200 00 0				0+2		
	62772	0767-00-0				24	0.0	
	02772	9760 00 0			RHD			
	92774	G601 03 0				-0440		
	02775	9500 00 0				T+20		
	02776	-0601-00-0				F+16		
	02777	0765 00 0			LRS			
	93900	0200-01-0				0+8		
	0.8001	0763 00 0			LLS		0.0	
	02000	9769 90 6			PHP			
	03003	0601 00 0				T+21		
	02004	Q500-00-0				T+20		
	03005	0601 00 0				T+26		
	02006	0765 00-0				+3		
	63007	0200 00 0				C+4		
	-03010	0767 00 0				-24	-00	
	0.3011	0760 GO G			RMD	T+27		
						T+24		
	03013	0500 00 0 9601 00 0				1424		
	03014	9765 00 0			LRS			
	03015	0705 00 0				-0+5		
	03017	0763 00 0			LLS		00	
	WART /	wrest out to	2000 a. 1		100	-	16.75	

PROFE	2							
	63020	-6760	00-0	-04010-	910			
	03021	0601	00 0	0.3334	STO	7+25		
	0.0052	0500	05-0	03335	CLA	7+20		
	03053			01333		T+24		
	03024			00047				
	93025			0.3274		C+6		
	43626			-00021		21	0.0	
	03027			00010	8110			
	93939			03000		T+27		
	0.3031			03327		7+30		
	03033			03735		T+06		
	02034			00047 -03075	LRS	6+7-		
	93035			00021	LLS		00	
	03036			-00010	5110		00	
	03937			03340		T+31		
	02010			-03341-		T+20		
	03041			03337		T=30		
	03042	-0765	00-0	00003		-		
	03043	0760	00 O	03010	8110			
	-03044-	-0601-	00-0	03840		7+99		
	03045	0500	09 0	03348	CLA	T+34		
	93046			03241		T+32		
	03047			00043	LRS			
	0.0050			03276		0+10		
	0.3051			00021	LLS		0.0	
	0.5082			02010	9110			
	03053			03344		T+35		
	03015			03343		T+34		
	93056			-00000		1-04	06	
	93057			00010	R110		0.0	
	0.7060			0.1344		7+52		
	03061			03347		Teed		
	04042			01345		T+26		
	03063	0765	00 0	00043	LES	4.7		
	03064	6260	09-0-	03277	mPy.	6+41		
	03045			00021	LLS	21	0.0	
	02000			-00010	9110			
	03007			0.1746		T+37		
	63930			03344		T+35		
	03071			03342		T+33		
	03072			037-0		T+24		
	03073			03234		7+27 7+25		
	03075		***	61332		T+21		
	03075			01130		T+01		
	03077			03324		T+17		
	93190			03324		1+15		
	03101			01350		T+41		
	03102			07317		T+10		5/8-
	03103			0.1312		T+3		
	03104			03716	678	7+7		
	03105			03312	81/8	T+2		7101
	03106			00003	559			5
	03101			03300		0+12		PRINT
_	93110			43112				
	0.3111	00.70	oo o	03150	780	****		

PROE	3					
	03112	-0500-cc-c	03306		C+13	
	03113	0100 00 0			****0	
	03114	0402-00-0				
	03115	0601 00 0			C+12	
	03116	0754 00 1	00000		011	
	03117	0771 00 0		ARS.		
	03120-	0402 00 0	03147		**27	
	03121	0602 00 0	03302	SLM	C+14	
	03155	6800 00 0			6+15	
	03123	0400 00 0		900		
	03124	0601 00 0			4+15	_
	03125	0076 00 6		T500	CSPIO - 4	
	03127	0 777777 6			++060+5++-1	
		1 60000 0		576	C+15	
	03131	0360 00 0			C+16	
		-1 00000 6		GIR	C+14	
	03133	05é0 00 0			T+10	
	03134	-1-00000 p		51B		
	03135	0560 00 D			T+3	
	03136	-1 40000 B		570	170	
	03137	0560 00 0			T+7	
		-1-60060-0		SIR		
	03141	0074 00 4			OF1L2+4	
	03142	0020 00 0			*****	
	03143	740630604			BOOK PRINTSNISS	
	03144	3145630545				
	03145	0534606060				
	03146	-3 77777 7	37737		-1+7+-1	
	03147	0 00000 p	00766		5+1	
	03150	9590-00-0		05-0	0+15	
	03151	0400 00 0		ADD		
	02152	-0601-00-0			G+45	
	03153	0074 00 4			19154	
	03154	0765 60 B		Les		
	03155	0200 00 0			C+16	
	03156				21 - 00	
	03157	076D DO D		RMD		
	03160	3400 00 0			1+1	- 541
	03161	0601 00 0			T+40	BUFF
	03162	4765 00 b			43	DAFF
	03163	0200 00 D			0+17	
	03165	8767 00 0			21-00	
	93165	9190 CO 0		RND	7+41	- curr
	03167	0601 00 0			T+2	Post
	03170				Attrici	
		-0140 00 0			*+10	
	03172	6074 60 4			1051H7-1	
	03173	0 00004 0		121	**24	
	02174	4020 40 4		780	**5	
	03175	002331512			40CIRCUIT EVERLERGE	0
	03176	2167604641				
	03177	5143462124				
	03200	246060606				
	03201	0074 00 4		T 510	MRITE.4	
				120	05372700765	
	03202	0 00345 b				

MIGE 4				
	-0534 00 4 02506-			**
	-J 00000 4 03223		0+000	
03205			**16,	
			**151	
03207		130	CSPHO	
0.151.0			***	
03211	0534 00 2 03265		SIZE.	
09515			-0+577	77.2
	-1 80000 o pocco	STR		
03214	- 2 COCO1 2 03212-		***	
03215	0074 00 4 77024	T5%	OF TILD	.4
03216	0020 00 0 03023	794	**5-	
03217	741130606060	0.00	3 (50)	T218H63
03000				
03221	D11045363460			
03922		544		+
03223	-0534 00 4 03306	L 100	C+000	20+4
03934	1-00001-4-01025		*****	*
03225	-0634 00 4 03306	5100	0.000	20-4
-03006	-2-00001-4-03263	7101	-6497v	4++1
03227	0600 00 0 03352	8 572	T+003	4.3
03030	-0074-00-4-00101-	759	-PEAD+	•
03231	0 00765 0 60000		06000	000765
03232	0 00000 0 00005		0+6	
03233	-0534 00 4 03306	L100	0+000	20-4
03934	-3-00000 + 01252 -	T10	meddy	•-
03235	3 00001 4 07252		++15.	
03236	0074 00 6 77014		-05010	
03237	0 77777 0 03245		**7**	
03240		1.100	-9125-	
03241	0560 00 2 60000		0+600	
-03242		STR		
03243	2 00001 2 03241		0-2-2	-1
93944	0074 00 4 77021		47.11	
03245	0020 00 0 03252		**5	
03246			2450	T110000
03247	606060606301	010	24.544	1119900
	D14945063460			
	-3 77777 7 777777	218	-1.7 -	-1
0.1252	0900 00 0 00101		PERO-	
03253	0100 00 0 02735	175		
03254	P600 00 0 00100		PE 00-	L
0.3295	0770 00 0 02205	WEF		5
03256			-01	-
03257	0534 00 4 03352		T+000	47.4
03257	0601 00 0 01352			
			T+000	
0.3261	-3 00000 4 03220		8+1.4	
03262			ENTT:	
03263	0770 00 0 02205	EXIT MEF		5
0.7264	0020-00-0-77001	E2111 TEG		
03265	0 00000 0 00765	512E	0+765	
	00746		-0+745	
	*0000000000000			00000000
	*900000000000			03000+36
	*0000000001014			00001014
	*0000000000000			00002031
	+0000000004061			00004061
	#000000010140		+9999	60010142
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71	1040	1040	1048	-1010-	1049	1949	1090	1050	1050	1051	1051	1051	1052	1052	1058	1059	1059	105
TI	1034	1054	1054	1055	1655	1055	1056	1056	1056	1057	1967	1057	1050	1058	1044	1965	1065	100
T1	1066	1066	1066	1067	1057	1067	1068	1065	1969	1069	1069	1069	1070	1070	1070	1071	1071	101
Ti	1078	1070	1078	1073	1079	1079	1090	1090	1089	1081	1081	1081	1092	1002	1082	1083	1083	108
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Fig. 3 — Typical BLODI program: printed output,