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An Experimental Pulse Code Modulation System for Short-Haul Trunks

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An experimental 24-channel pulse code modulation system employing solid-state devices is described. Economy of design and ability to operate over existing exchange cable were dominant factors in selection of system organization and circuit alternatives. System requirements are unique to this type of system. Design considerations in meeting these requirements are presented in brief here and in detail in companion articles.

I. INTRODUCTION

The Bell System has a wealth of experience in frequency division systems. Through the years, as new systems have been developed, our knowledge of the factors affecting the performance of these systems has steadily increased. There has been no comparable experience with time division systems. Therefore, when the decision was made to develop a pulse code modulation system for commercial use, it was felt advisable to build an early experimental model to prove the feasibility of the general system arrangement and the circuit approaches adopted. The experimental system also established the over-all level of transmission performance that could be expected.

This and companion articles in this issue describe the experimental system, analyze the results of measurements on the actual system, and compare performance with objectives.

II. SYSTEM APPLICATION AND FEATURES

Development of a pulse code modulation (PCM) system was undertaken to answer the need in the Bell System for a carrier system economical for short distances of less than ten to more than 25 miles, working on exchange cable pairs. A carrier system for short distances must, of necessity, have inexpensive terminals. As will be shown, the PCM system achieves economy in the terminals by dint of a high percentage of common equipment, the cost of this common equipment being spread among all the channels. The close spacing of repeaters, resulting from the wide band of frequencies occupied by the PCM signal, sets an upper limit to the distance for which the system will be attractive.

A summary of the features of this system is given below:

Terminal:

Number of speech channels = 24.

Seven-digit binary code expresses amplitude of speech samples.

Instantaneous compandor reduces noise and crosstalk by 26 db.

Built-in signaling system uses eighth digit assigned to each channel and seventh digit during on-hook period for revertive pulsing.

Only solid-state devices are used.

Three terminals may be mounted in a 23-inch by 11-foot, 6-inch bay.

Repeatered Line:

Designed for use with 19- or 22-gauge cable pairs.

Nominal repeater spacing = 6000 feet.

Regenerative repeaters receive timing information from the pulse pattern.

Pulse repetition rate = 1.544 megabits per second.

Power supplied over phantom circuit.

Bipolar pulse pattern used to reduce base line wander and to reduce timing frequency crosstalk between systems.

This article will give a general description of the system and the design choices. Accompanying articles go into greater detail about the design and performance of critical areas of the system, viz, the coding complex and regenerative repeaters.

III. SYSTEM ORGANIZATION

3.1 *Speech Processing*

A block diagram of the speech portion of the system is shown in Fig. 1. Incoming speech to a channel unit, after passing through the hybrid,

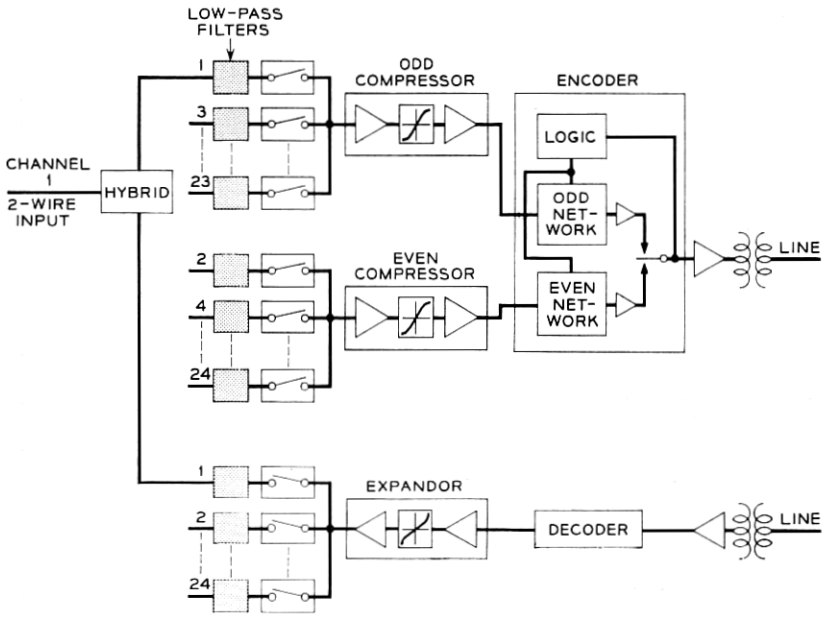

Fig. 1 — Experimental PCM system — speech portion of terminal.

is band-limited to reject all frequencies above 4 kc. This band-limited signal is sampled 8000 times per second by the sampling gate associated with this channel. The resultant sample, whose amplitude is proportional to the signal level at the instant of sampling, is passed through the compressor, which gives preferential gain to low-level signals, and presented to the coder. The coder expresses the sample amplitude as a seven-digit binary number or one of 128 different possible levels. The first digit has weight of 64; the last digit has weight of 1. The signal arrives at the coder on a pedestal 64 units high so that code 64 corresponds to zero signal amplitude. The seven-digit code goes onto the transmission line, followed by an eighth time slot which carries the supervisory signaling for that channel.

The channels are sampled in a recurring sequence, one sample from each channel or 24 samples being encoded and transmitted every 125 μsec. Since each sample requires eight time slots including the signaling, these 24 samples require a total of 192 time slots on the line. An additional or 193rd time slot is added to permit synchronizing or framing the two ends of the system. These 193 time slots comprise a framing period. This is illustrated in Fig. 2. There being 8000 such periods each second, the repetition rate of pulses on the line is 1.544 million pulses per second.

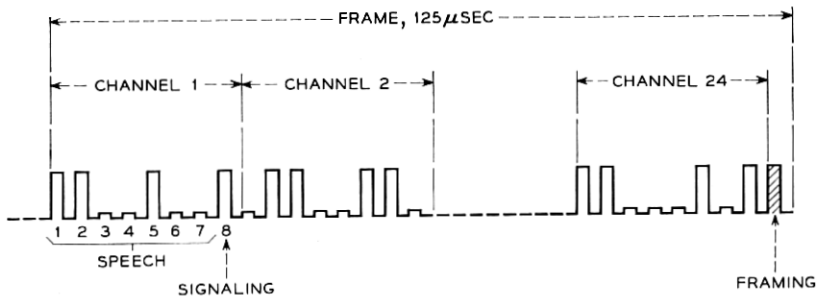

Fig. 2 — System time assignment.

The time assigned to one bit is about 0.65 μsec. The pulses have 50 per cent duty cycle and are therefore 0.325 μsec wide.

These pulses, containing speech, signaling and framing information, arrive at the receiving terminal after being reconstituted several times by the regenerative repeaters spaced at 6000-foot intervals on the line. At the receiver, the pulses are sorted out, the signaling pulses being directed to the individual channel signaling units and the speech-coded signals going into the decoder. The decoder output is a pulse amplitude modulated (PAM) signal whose amplitude is equal to the amplitude of the input to the coder, within one-half coder step. The decoder PAM pulse passes through the expandor, which has the inverse characteristic of the compressor, providing more gain for higher-level signals. The expandor is followed by a wide-band power amplifier which raises the signals to a level sufficient to require no further amplification after being switched to the channel units. A low-pass filter in the receiving section of the channel unit integrates the samples to yield the original signal.

With this general description in mind, let us proceed to a more detailed consideration of the circuits used to process the signal.

3.1.1 *Multiplex Gates*

Each of the 24 multiplex gates is operated 8000 times a second by a "channel pulse" from a control circuit named the "channel counter." The operation of the gate results in a pulse, whose amplitude is proportional to the signal level in that channel, being presented at the input of the compressor. This pulse must be held until coding is completed.

It is important that the signal stand still while it is being encoded, for if even small ripples synchronous with the digit rate are superimposed on the signal, the coder will spuriously encode one of the levels the sig-

nal reaches momentarily during the coding process. This can have the effect of enlarging the size of some coder steps by attenuating or actually eliminating others. The problem of crosstalk from control signals is a real one because of the very high level of the control pulses in the terminal. Since the effects of crosstalk and noise on the common bus are also a function of the signal level, it is advisable to keep the signal level as high as possible before encoding so that interference will have the smallest effect. For this reason voltage sampling was not considered satisfactory, and an energy-sampling approach was used. As is well known, voltage sampling results in signal attenuation equal to the percentage of time the gate is closed, whereas energy sampling[1] theoretically results in no attenuation. The energy sampling gate is shown in Fig. 3. Between sampling periods, the capacitor C1 is charged to the signal level. When the gate is closed, the complete charge of C1 is transferred through the inductor L to the common capacitor C_c. The gate is held closed for exactly one-half the resonant period of L with C1 and C_c, or 1.95 μsec (the width of the "channel pulse" driving the gate). After a signal has been encoded, the clamp is closed for 1.95 μsec to remove this signal from the common bus before the arrival of the next signal. The input impedance of the compressor is high to keep the voltage on C_c essentially constant through the coding period.

Use of the resonant transfer process results in an economy by making it unnecessary to use an input amplifier per channel. The choice of diode sampling gates is largely one of economics. The gates must, in all cases, be driven on hard enough that they can carry the maximum required signal current. If transistor gates are used, the control pulse does not need to be so powerful. If diode gates are used, the full gain requirement is placed on the drive pulse. Since it was possible to derive the required

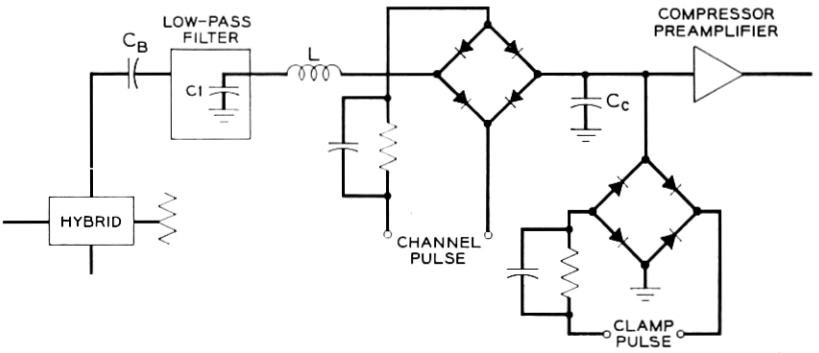

Fig. 3 — Multiplex gate and clamp.

amount of drive from the channel counter, and since this arrangement proved the most economical, diode gates were employed.

There is a balance requirement on the diode gates to minimize the pedestal associated with the operation of the gate. This is necessary to keep the signal centered on the coder characteristic. As R. H. Shennum and J. R. Gray[2] point out, any quiescent displacement from the center of the compressor curve results in increased idle circuit noise and cross-talk. The balance requirement is eased considerably by the capacitor C_B which builds up a dc potential equal, but opposite in polarity, to the average gate unbalance voltage.

3.1.2 *Compandor-Coding Circuits*

A companion article[3] describes the operation of the companding and coding portions of the system and the reasons for choosing the approach used. Suffice to say at this point that the purpose of the instantaneous compandor is to provide better definition (less quantizing* noise) for low-level signals at the expense of poorer definition for high-level signals, where quantizing noise is not so noticeable. The circuit is designed to provide 26 db of companding, which means that the coder steps near zero signal level, as reflected at the compressor input, are 20 times smaller than they would be without companding. This is important both from a quantizing noise standpoint and because the noise floor in such a system is equal to one coder step. The effect of the compandor is to make the seven-digit coder equivalent to an eleven-digit coder for small signals. The compandor achieves its nonlinear characteristic by the use of diodes whose forward voltage-current characteristic is logarithmic. The diodes shunt the signal path in the compressor and are in series with it in the expandor.

A network coder, shown schematically in Fig. 4, is used. This coder successively compares the input PAM signal to binary weighted currents and generates the PCM signal as the comparison is taking place. The switches 1 through 8 are swung from ground to battery in sequence under the control of leads from the digit generator (see Section 3.2). Each switch closure subtracts an amount of current from the current-summing point proportional to the conductance in series with the switch. Thus, closing switch No. 1 subtracts 64 units of current; switch No. 2 subtracts 32 units; etc. Whether a switch remains operated through the remainder of the coding operation or is released depends on whether current flows into or away from the summing amplifier as a result of the switch closure.

* Quantizing noise is the noise introduced by coding error which results from the finite size of coder steps.

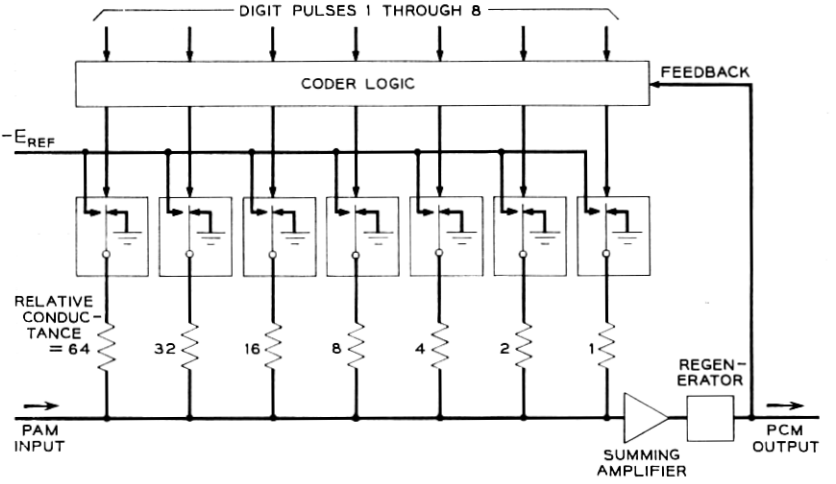

Fig. 4 — Simplified block diagram of network coder.

Operating the first switch, then, determines whether the signal is greater or less than 64. If it is greater, that switch is left closed, a space is put on the line, and the next comparison determines whether the signal exceeds 96. If the signal is less than 64, a pulse is generated, the first switch is released, and the signal is then compared to 32. This process is continued through the seven digits, a pulse being generated each time the PAM signal is less than the sum of the reference currents. As mentioned previously, code 64 corresponds to zero signal level.

The logic portion of the coder uses flip-flops to keep selected switches operated. All the flip-flops are reset by the eighth digit from the digit generator.

This type of coder demands that the input signal be present throughout the coding interval, which leads to the reason for having two compressors. A given PAM signal must be present throughout the coding interval of about 4.5 μsec, and then within 0.65 μsec that signal must be replaced by another. Rather than place this speed requirement on sampling gates and compressor, it was decided to switch the coder between two inputs and to sample on an odd-even channel basis, as shown in Fig. 1. To accomplish this switching at a digital rather than an analog position, the analog portions of the coder are duplicated and the logic section alternately put under the control of the two sections. This arrangement allows adequate time for removal of the previous signal from each compressor input and settling of the desired signal before encoding.

An alternative way to provide more guard space between channels is to use a coder which encodes at a 3-mc bit rate but reads out at a 1.5-mc rate. Such a coder, which would require a 50 per cent duty cycle of incoming PAM samples, is functionally quite simple and compares favorably in cost to the dual coder. The speed requirements for coder and compressor, however, would be doubled by such an approach.

The decoder is similar to the coder in its operation. In fact, the coder actually contains a decoder in its feedback path, as shown in Fig. 5. In response to a pulse in a given time slot on the PCM line, a reference voltage is applied to a binary-weighted resistor. This supplies into a summing point a current proportional to the weight of the pulse. Pulses from the PCM line are steered to the correct switches by logic gates using pulses from the receiving digit pulse generator (see Section 3.2).

Since all the weighted currents must be present at the time of demultiplexing, the decoder must contain storage or delay circuits to convert the serial PCM code to parallel. Capacitor storage is used for this purpose in the decoder, this approach yielding the most economical circuit. Other choices considered were blocking oscillators and flip-flops.

3.1.3 *Demultiplexing*

The pedestal applied to the PAM signal at the transmitter is removed following the decoder. This results in bipolar PAM at the receiver which has advantages in minimizing interference, as pointed out in Section IV.

Since it was not possible with available devices to derive all the re-

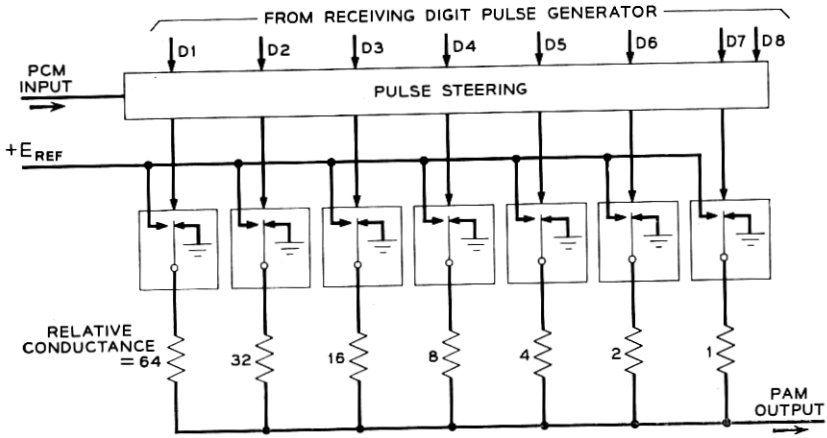

Fig. 5 — Simplified block diagram of decoder.

quired power at the receiver from the decoder and pass this power through the expandor, some signal gain must be supplied following the expandor. For economic reasons it was decided to provide this gain at a common point rather than furnish an amplifier per channel. This decision to amplify the decoded signals before distribution to the receiving channel filters results in a need for a broadband power amplifier and high-level demultiplex gates. These circuits are described in the following sections.

3.1.3.1 *Common Amplifier.* Only one expandor and common amplifier are required because the PAM pulses in the receiver do not have to occupy a full channel time slot as in the transmitter. In the receiver, the PAM pulses are 3.25 μsec wide with 1.95 μsec guard space between them.

The common amplifier is designed to provide a peak current of 300 ma at 13 volts. To obtain this high power output from a broadband amplifier, a diffused silicon transistor was used in class B operation in the manner shown in Fig. 6. Transistor Q2 with equal resistors R in emitter and collector circuits serves as a unity-gain phase shifter to drive the

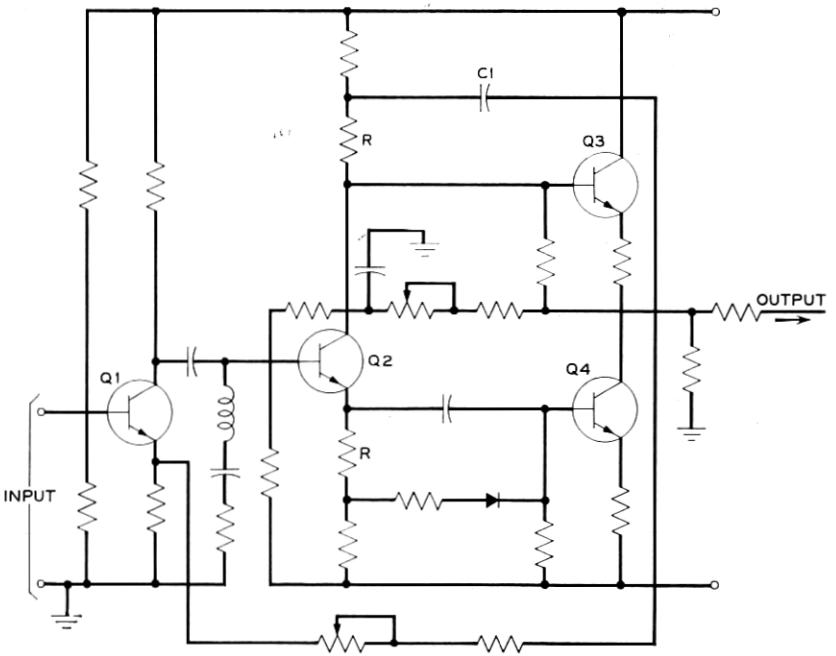

Fig. 6 — Common amplifier.

class B output stages. The capacitor C1 assures that the drive to Q3 is the same as that to Q4. Feedback is provided from the output to the emitter of the preamplifier transistor Q1.

The stabilization of this amplifier is complicated by the time variance of the load. During turn-on of the gate, the load is essentially resistive. Later in the cycle, the load becomes an RC combination. Between pulses, the load is an open circuit. To circumvent this problem, the amplifier was designed to have adequate gain and phase margin under all load conditions.

3.1.3.2 *Demultiplex Gate.* The demultiplex gate configuration is shown in Fig. 7. For large signal difference between common amplifier and filter input, two of the gate diodes are turned off, and the filter is charged by a constant current determined by the transistor drive and its current gain. As the signal levels become nearly equal, all diodes are forward biased by the drive pulse, and the circuit functions as a normal balanced gate. Constant current charging to near the signal level results in essentially full transfer of the signal voltage in the time available. This renders any amplitude modulation due to variations in width of the gate drive unnoticeable, and also provides good control of the net loss of the demultiplex gate.

Further advantages of the balanced demultiplex gate are mentioned in Section IV.

3.1.3.3 *Receiving Filter.* The decision to use a common amplifier resulted

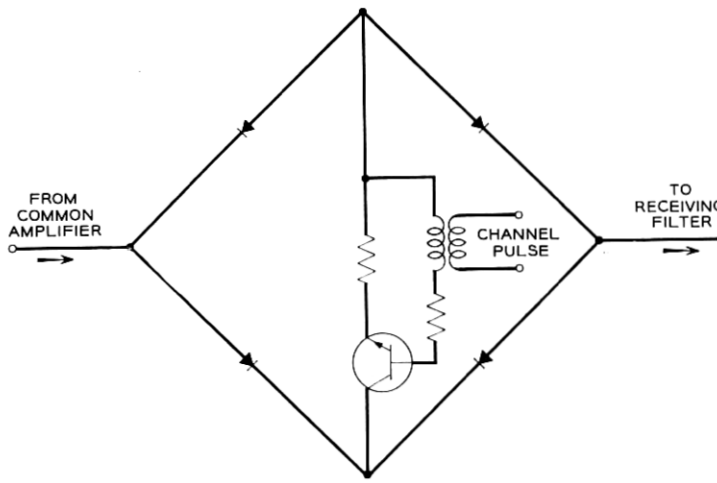

Fig. 7 — Demultiplex gate.

in loss of buffering between the demultiplex gates and hybrids. This results in the hybrid looking into a filter terminated by a time-varying impedance, as shown in Fig. 8. Balancing the hybrid to meet return loss requirements at all frequencies of interest requires that the impedance seen by the hybrid be one obtainable with passive elements.

M. R. Aaron found that the time-varying impedance could be represented by a simple series RL combination whose values were only slightly frequency dependent. Using average values of R and L, it was possible to match a constant K filter to this impedance so that a reasonable impedance was presented to the hybrid.

3.2 *Control Circuits*

The basic pulse repetition rate of the system is controlled by 1.544-mc clocks. These clocks take the form of a crystal oscillator in the transmitting terminal and slaved oscillator in the receiving terminal. The slaved oscillator is synchronized with the incoming pulse train from the repeatered line.

In addition to these clocks, control circuits are needed to define the eight time slots in a channel and the 24 channel slots in a frame. These control circuits, referred to in previous sections, are called digit pulse generators and channel counters. The digit pulse generators control the coder and decoder. The channel counters control multiplexing and demultiplexing of PAM signals. The two circuits together control the signaling circuits.

The following sections describe these two control circuits.

3.2.1 *Digit Pulse Generator*

Each terminal contains a transmitting and receiving digit pulse generator, synchronized by the transmitting or receiving clock. The digit pulse generator provides a pulse sequentially on each of eight outputs. It is of a self-starting ring counter design shown in Fig. 9.

The basic building block of this circuit is a blocking oscillator whose

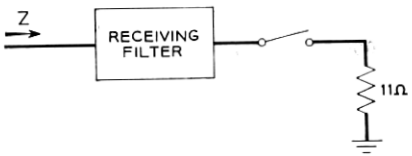

Fig. 8 — Time-varying impedance seen by hybrid.

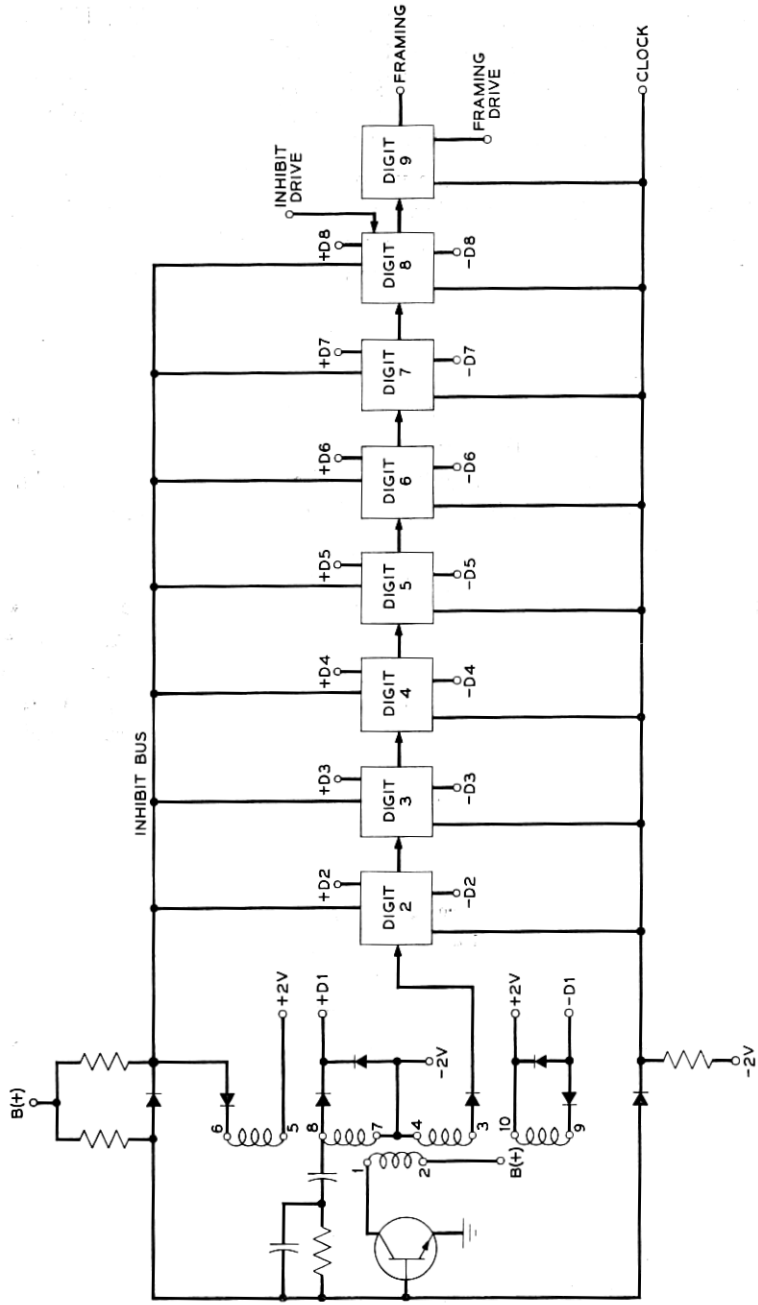

Fig. 9 — Transmitting digit pulse generator.

input is combined with the 1.544-mc clock in an AND circuit. In the presence of positive input signal, the blocking oscillator fires when the clock goes positive. The natural period of the blocking oscillator is greater than a half cycle of the clock, so that the turnoff of the blocking oscillator is initiated by the negative-going transition of the clock. The output pulse length is about 0.325 μsec. Both polarities of this pulse are available from the blocking oscillator.

Nine such blocks are used in the building of a digit pulse generator. As can be seen from Fig. 9, the output of each stage triggers the next stage by utilizing the positive overshoot of a negative-going pulse. This is one way of obtaining the required delay between stages.

A pulse is started through the ring counter by the firing of the first stage. Since we desire to have only one output active at a time, the first stage must be inhibited from firing again until the last stage has become active. This inhibiting action is accomplished by using the negative overshoot of the positive pulse from all but the eighth stage. The inhibit output from the eighth stage is used in channel 24 to make the digit pulse generator count to nine in that channel (see the inhibit drive lead), providing a time slot for framing. Under control of the framing drive lead, pulses are generated in this ninth time slot in alternate frames.

3.2.2 *Channel Counters*

Each terminal contains also a transmitting and receiving channel counter. The channel counters are similar to the digit pulse generators in that they use blocking oscillators as building blocks and pulse overshoots for delay. A channel counter, however, counts to 24, generating a pulse on each of 24 output leads in sequence. The pulse width is controlled not directly by the clock, but from a secondary "clock" derived from the digit pulse generator outputs. The pulse widths from the two channel counters are different, as pointed out in the multiplex and demultiplex gate sections. The transmitting channel counter generates 1.95-μsec pulses; the receiving channel counter generates 3.25-μsec pulses.

3.2.3 *General Design Considerations*

At the time this experimental system was built, the principal alternatives available for accomplishing these control functions were multivibrators, magnetic cores and blocking oscillators. Since the power and speed requirements were rather severe for both types of counter, and

since transformer coupling was desired, blocking oscillators were employed.

3.3 *Synchronization*

The pulse repetition rate in the receiving terminal must, of course, be exactly the same as that in the transmitting terminal. This synchronization is obtained by deriving the receiving terminal clock frequency from the incoming pulse train, just as is done at each regenerative repeater. Further synchronization between the two terminals is required to permit decoding of the speech and signal information. This synchronization must permit identification of each time slot in each channel. Since these time slots recur on a 125-μsec frame basis, this synchronization will be called "framing."

Basically, there are two types of framing systems — forward-acting and backward-acting. A forward-acting system transmits at the beginning of each frame a unique signal which cannot be encountered elsewhere in the pulse train. Due to the restrictions of the regenerative line, there can be no information in the pulse width or amplitude; therefore, this would have to be a unique code for the system herein described. The receiver control circuitry would start counting from this signal to steer the pulses to their correct destinations. A forward-acting framing circuit has the advantage of very fast action, since the system reframes each frame. Disadvantages are (1) expense, because the unique code must consist of many characters and therefore complex circuitry would be required at both ends, and (2) frequency of framing loss. Each time a pulse error is made during transmission of the framing pattern, the system is out of frame and each customer hears a transient noise.

A backward-acting system also requires a framing code to be transmitted each frame. Instead of reframing each new frame, however, the backward-acting system gets into frame and simply checks with each frame to ascertain whether it is still in frame. In this manner, the backward-acting framing system does not require an absolutely unique code and, furthermore, can be designed to ignore one or more transmission errors by insisting on a given number of errors in a specified time before deciding that the system is out of frame. Once having ascertained that framing is lost, the backward-acting system moves through the various pulse positions looking for the framing code. When it finds the framing code, it locks to it and normal operation is resumed.

The amount of time required for the backward-acting system to reframe depends on the probability of its being fooled by encountering the framing code by chance in the wrong portion of the pulse train. This probability decreases as the length of the framing code is increased. Thus,

even with the backward-acting system, reframing is accomplished more quickly with a more nearly unique framing code.

The objectives for the framing system for the PCM system were (1) the system should not go out of frame on single errors in transmission, and (2) the reframing should be rapid, consistent with low cost. The first objective leads to a backward-acting framing system. The ultimate choice of code for simplicity and therefore economy is a single digit. Since a pulse or space could exist for very long times in any position in the frame, however, neither of these can be used exclusively. Consideration of the coding procedure, though, reveals that an alternating pulse-space pattern cannot exist for long in any pulse position. This is true because the alternating pattern implies a 4-kc component in a signal and the input filters do not pass 4 kc. This alternating single pulse pattern was thus chosen. The 193rd time slot in each frame contains alternately a pulse and a space which the receiving framing circuit locks onto. The generation of this pattern is explained in Section 3.2.1. A time rate of errors in excess of a predetermined level is interpreted as loss of framing. In this event, the receiving framing circuit moves to the preceding time slot and looks for an alternating pattern. One violation of the alternating pattern is sufficient to drive it to the following time slot, etc., until a time slot is found which contains an alternating pattern for more than eight frames. To speed up the reframing process, the adjacent pulse position is looked at immediately upon violation of the alternating pattern, which means that it may be necesary to remain on a given position only 125 μsec to ascertain that it is not the 193rd position. The circuitry for accomplishing this motion from one pulse position to the next is not shown.

The framing circuit requires 0.4 to 6 milliseconds to detect an out-of-frame condition. The time required to reframe depends, of course, on how far away from the framing position the circuit is when it starts hunting. A simple calculation shows that even if it has to go through all 192 positions, only about 50 milliseconds will be required for the system to reframe.

The detection of the framing signal is illustrated in Fig. 10. A pulse on the SP lead once per frame changes the state of the binary cell when the system is in frame. The compare circuit looks for the alternating pulse pattern in the 193rd pulse position.

3.4 *Signaling*

Any transmission system must make provision for the signals necessary to establish a connection and to end the connection at the termina-

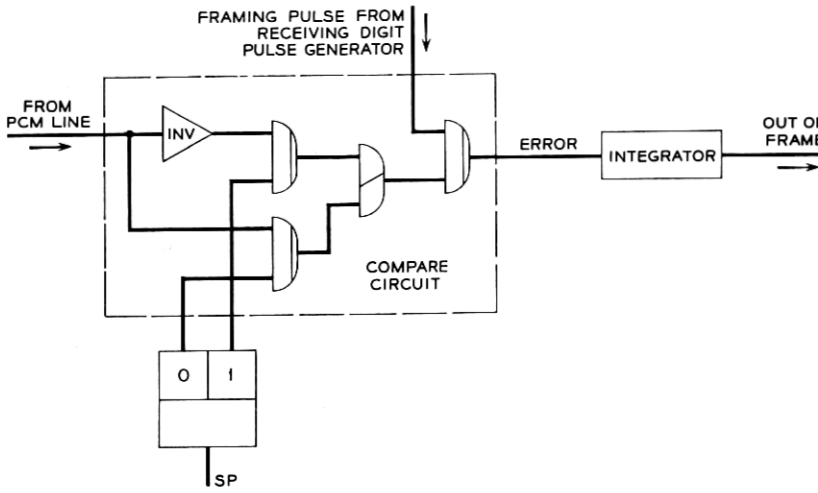

Fig. 10 — Framing detector.

tion of the call. The nature of the PCM signal makes it most economical to convert the dc signals containing this signaling information into digital form for transmission over the line and to convert the digital signals back into the desired dc conditions at the distant end.

As mentioned previously, the eighth time slot in each channel is assigned to signaling. To multiplex the signaling information from the various channels into their respective signaling time slots requires the use of simple scanning gates as shown in Fig. 11. The dc signaling information contained in the eighth time slot of each channel is demultiplexed at the receiving terminal, and the resulting pulse train is integrated to recapture the original dc signal.

If revertive pulse signaling is used between offices, two signal paths are required in one direction, one for supervision and one for revertive pulsing. In this case, both the seventh and eighth pulses of the channel are used — the eighth for supervision and the seventh, or least significant speech digit, for revertive pulsing. Except for special-purpose calls to operators, this has no effect on speech because revertive pulses are sent only before the called party answers. The seventh coder pulse is, of course, suppressed when the seventh pulse is being used for signaling.

3.5 *Power Supply*

The dc power for the terminal is furnished from a central regulated power supply. The required voltages are derived from a dc to dc con-

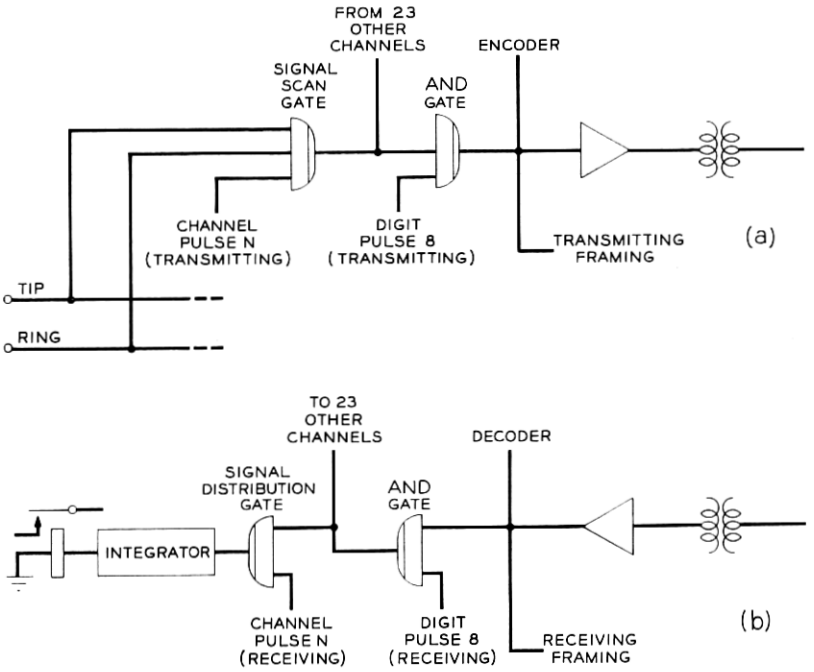

Fig. 11 — Experimental PCM system — signaling.

verter driven from the office 48-volt battery. Transistor regulators restrict absolute voltage level variations and ripple to permissible values.

3.6 *Repeatered Line*

The repeatered line is described in detail in a companion article.[4] It will therefore be treated very briefly here.

Repeaters were designed for 6000-foot spacing because this is a standard load-coil spacing. Build-out sections are provided for shorter spacing. The repeaters are fully regenerative and receive their timing information for the regenerative process from a resonant circuit driven by the incoming pulse train. Power for the repeaters is supplied over the phantom circuit.

While a pulse transmission system is relatively immune to noise, it is quite vulnerable to interference at the timing frequency. With unipolar pulses, crosstalk between timing waves was a problem if several systems were to be put into the same cable. Increased margin against this crosstalk was obtained by inverting alternate pulses on the line, thereby con-

centrating the bulk of the signal energy in the vicinity of half the pulse repetition rate. The timing frequency is derived by full-wave rectification of the bipolar pulse train. The advantage lies in the fact that the forward loss at the lower frequency is less, and the coupling loss greater, than for the 1.544-mc component. The bipolar signal also has minimum dc content, thereby restricting base line wander, which would otherwise reduce the signal-to-noise ratio.

Remote fault location and marginal checking of repeaters are accomplished by using a single fault-location pair for as many as 25 systems in a cable. Each repeater location is identified by the frequency to which a filter between its output and the fault-location line is tuned. The details and use of this system of remote testing are covered in Ref. 4.

The high bit rate of the PCM line provides obvious capability for data transmission. The entire line could be used for one broadband data channel, or time division methods could be used to subdivide the pulse train to accommodate several data channels or a mixture of data and voice channels.

IV. SYSTEM PERFORMANCE

The ultimate gauge of success of a speech communication system is determined by its subjective acceptability. Experience with frequency division systems has made it possible to spell out performance objectives which assure subjective acceptability. The signal impairments introduced by a PCM system are quite different from those introduced by a frequency division system. It is not realistic therefore, to set the objectives in the same way. A primary goal of the experimental system was to determine economically attainable system performance and to judge whether the speech quality of the system would be acceptable. Results of tests on our experimental system indicated satisfactory performance with the following design parameters.

i. Channel overload — The system presents an undistorted voltage range equal to the peak-to-peak excursion of a +3-dbm sinusoid at the zero-db system level.

ii. Idle circuit noise — Did not exceed 22 dba at the zero-db system level as measured with a 2B noise-measuring set with F1A weighting.* Performance was generally appreciably better.

iii. Idle channel crosstalk — Did not exceed −65 dbm on any channel when 15 dba of thermal noise power was applied at the input to that channel and a zero-dbm, 1-kc tone applied to any other channel.

* 28 dbrn (C message) in terms of the new 3A Noise Measuring Set.

iv. Transmission quality of quantized signals — The plot of measured signal-to-noise ratio for any channel did not fall more than 3 db below the theoretical value (shown in the article noted in Ref. 3) at any volume within 50 db of full sinusoidal excitation.

Unlike a frequency division system, essentially all the noise, distortion, and gain variation in a PCM system occurs in the terminals. The principal source of noise is quantizing error. The relation of quantizing noise to signal level depends on the number of coder steps used to describe the signal and the distribution of amplitudes of these coder steps. As described by H. Mann, et al,[3] the signal-to-quantizing noise ratio for the effective coder characteristic used can be calculated both for the ideal case and with random variation of step size.

The quantization of the signal has the further effect of placing a floor under crosstalk and idle circuit noise. This is true because, without the addition of complex circuitry, the zero-level signal voltage may be such that an infinitesimally small signal can trigger a coder step. The minimum guaranteed noise or crosstalk is thus that corresponding to one coder step. Since the coder range must accommodate up to the overload signal, this relates the crosstalk and idle circuit noise to overload level through the number of coding steps available. Such crosstalk would have the quality of infinitely clipped speech, which has been found to be remarkably intelligible. Interestingly, this same feature can eliminate all low-level crosstalk and noise from the transmitter if the zero-level signal sits at the middle of a coder step.

The principal source of crosstalk in a time division system is generally due to the carryover of the PAM sample on a common bus into the following time slot. To meet the crosstalk requirements, it is necessary that the time constant of all common points between samples be sufficiently small. This condition is met on the transmitting common bus by use of a low-impedance clamp between pulses, and on the receiving common bus by the low output impedance of the common amplifier.

Another crosstalk path is through the capacitance and reverse impedance of the back-biased diodes of the multiplex or demultiplex gates. This path can permit crosstalk from any one channel to all channels or from all channels to one channel.

The 15 dba of thermal noise specified in the discussion of the crosstalk objective is intended to scramble the zero crossings of the tone, thereby reducing the enhancement of weak crosstalk. Such noise may be expected to be present on any channel in service.

Subjective tests have shown characteristic PCM idle circuit noise to be more objectionable than equivalent thermal noise. The 22-dba quan-

tizing noise objective is the subjective equivalent of about 26-dba thermal noise.

Net loss variations can be attributed to any circuit in the signal path. The usual compandor enhancement of gain variations must be considered in assigning margins to compressor post-amplifier, expandor preamplifier, coder and decoder.

The noise, crosstalk, net loss, and distortion requirements are considered in the accompanying article by R. H. Shennum and J. R. Gray,[2] and the allocation of impairments among the various circuits of the terminal is described.

The repeatered line can introduce noise through digit errors and receiving terminal clock phase variations. The clock phase variations are attributable to dependence of the slave clock phase at repeaters and terminal on the received pulse pattern. This can result in audible noise or, strangely enough, intelligible crosstalk through amplitude, width, or position modulation of the PAM pulse.

Clock phase variation can modulate the signal amplitude only if the PAM signal amplitude is dependent on the width of the channel pulse driving the demultiplex gate. This can be true if the receiving filter is not completely charged in the time the demultiplex gate is closed. As mentioned previously, the demultiplex gate was designed to provide essentially complete charging of the receiving filter. Additionally, the demultiplex gate is a balanced configuration with no output in the absence of signal. This means that any interference due to amplitude, width, or position modulation of the received PAM will be proportional to the received signal and therefore unnoticeable.

Digit errors on the repeatered line may result in audible transients or clicks in the receiver. The magnitude of the transient depends on the weight of the digit in error. For reasonable error rates, only errors in the two most significant digits produce objectionable clicks. A given talker uses 16,000 of these digits per second or about 10^6 per minute. Thus, an error rate of one in 10^6 would result in one click per minute. An error rate of one in 10^7 would result in one click in 10 minutes. A permissible error rate, assuming strictly random error distribution, is between 10^{-6} and 10^{-7}, and the experimental system performed this well or generally appreciably better.

V. DEVICES

A PCM system makes prolific use of devices. The economy in such a design is predicated, therefore, on the availability of inexpensive devices

capable of realizing the speed, power, and other requirements. Previous unavailability of such devices has been the chief deterrent to the adoption of the PCM approach. To realize the advantages of the present device cost picture, one must take cognizance of the fact that devices are inexpensive only when produced in quantity. The experimental system design restricted itself to general-purpose transistors and diodes except where departure from this avenue could be economically justified.

Most transistor applications were filled with a diffused-base silicon NPN unit. There were two types available — one switch design and one amplifier design. A diffused-base germanium PNP was used in the compandor amplifiers and in a few logic applications where the complementtary aspect was of value. The common amplifier employs a large area diffused silicon design, chosen for its higher power capability.

Relatively low-performance alloyed germanium logic diodes, already in large-scale production, and therefore very low in cost, were used where possible. Small, high-speed diffused silicon units were used in critical positions where switching speed was important. Clamping diodes for the coder and decoder were selected from this design, the selection process being necessary to match forward voltage drops. Larger area diffused silicon diodes were used for the multiplex and demultiplex gates. Once more, a selection process was necessary for balance of forward voltage drops.

The compressor and expandor networks use small area diffused silicon diodes.

VI. EQUIPMENT DESIGN

A model of the two-way regenerative repeater is shown in Fig. 12. The design stressed efficiency of space usage to permit the maximum possible number to be mounted in a manhole. Watertight containers were designed to house the repeaters and fault-location circuits for the field experiment.

The experimental terminal, fully equipped, would contain about 300 transistors and 900 diodes. These and their accompanying components were mounted on printed wiring boards of a type shown in Fig. 13. The boards used two-sided wiring to achieve a high component density. Transistors were mounted in sockets for the experimental terminal, although in a production model they would be soldered to the board. Test points were brought out to the front panel made of formed aluminum.

The printed boards can be assembled to form a terminal, shown by the artist's conception in Fig. 14. Circuit functions are assigned to printed

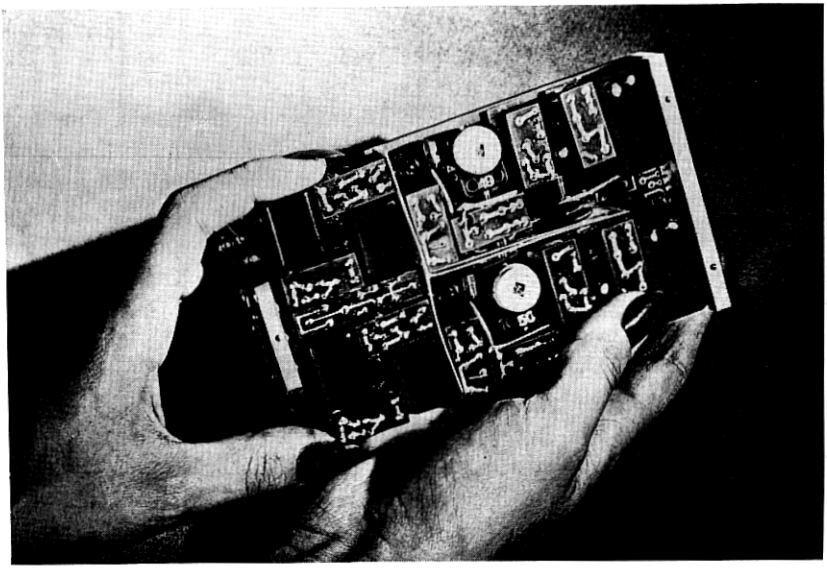

Fig. 12 — Experimental two-way repeater with cover removed.

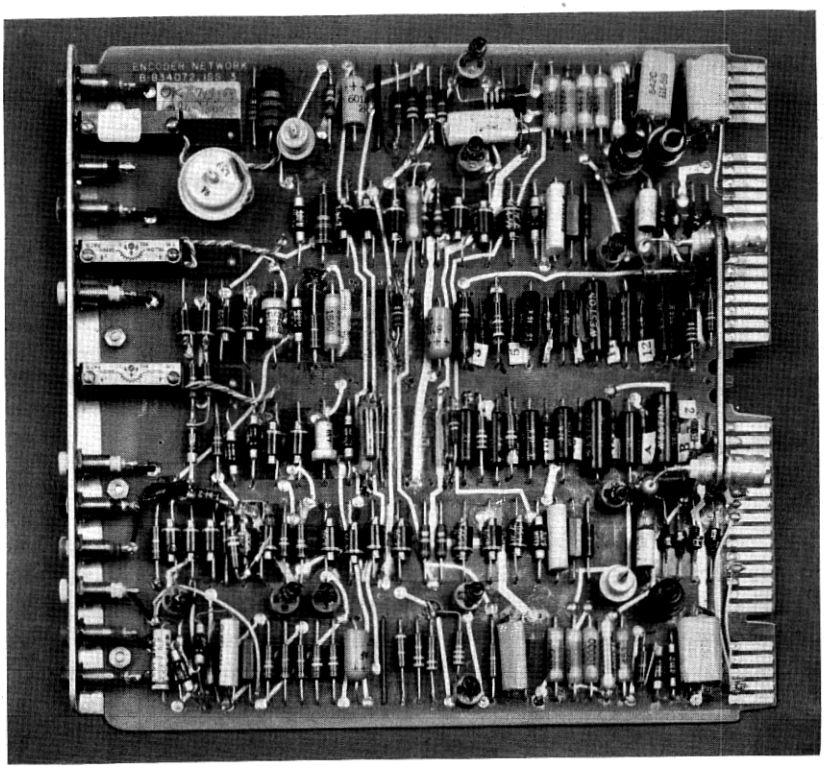

Fig. 13 — Plug-in type printed board used in experimental PCM system.

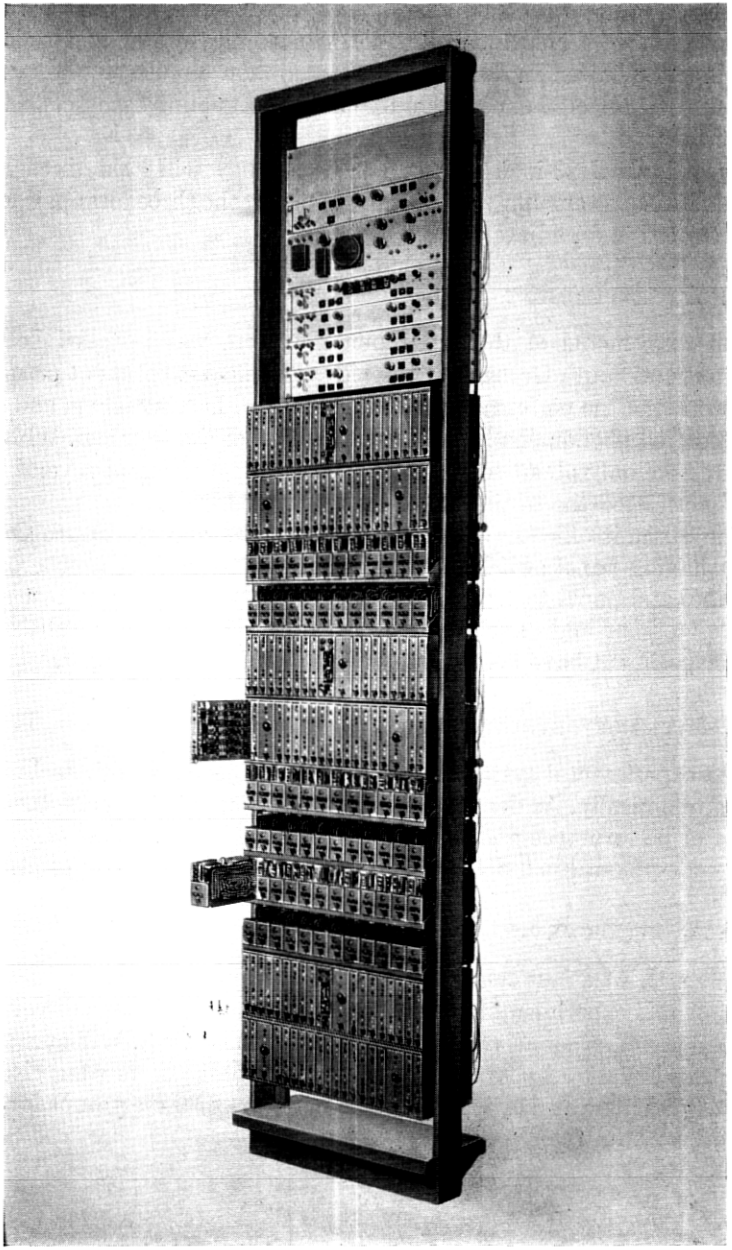

Fig. 14 — Artist's conception of a three-terminal PCM bay.

boards so that a terminal may be partially equipped in the most economical manner. One board per channel, containing hybrid and signaling circuits, is required in addition to the common circuitry. The type of channel unit selected depends on the mode of signaling used between the two offices.

One standard 23-inch by 11-foot, 6-inch bay will hold three PCM terminals. A power supply capable of supplying the three terminals would be mounted in an adjacent bay.

VII. FIELD EXPERIMENT

An early model of the experimental system was installed between Summit and South Orange, New Jersey. This field experiment permitted evaluation of the performance of the repeatered line, signaling, and some unpredicted phenomena in the speech portion of the terminal. While the offices were only about seven miles apart, the provision of several cable pairs permitted the testing of longer repeatered lines.

The Summit office having crossbar switching and the South Orange office having panel switching provided for test signaling from crossbar to panel and panel to crossbar. Loopback tests were used to test crossbar-to-crossbar and panel-to-panel signaling. The general results of the field experiment have been quoted in Section IV of this paper.

VIII. STATUS OF DEVELOPMENT

The experimental system has met design objectives both technically and economically. As described in this and companion papers, the principles of performance and design of such a PCM system are now quite well understood. Final design for manufacture is now nearly completed.

IX. ACKNOWLEDGMENTS

This article has summarized the work of several people. The development of this experimental system was carried out under the direction of E. E. Sumner at the Murray Hill Laboratory and O. L. Williams at the Merrimack Valley Laboratory. Engineering studies were supervised by K. E. Fultz. The author is indebted to members of these groups for their helpful consultation.

REFERENCES

1. Desoer, C. A., B.S.T.J., **36,** 1957, pp. 1403–1428.
2. Shennum, R. H. and Gray, J. R., this issue, p. 143.
3. Mann, H., Straube, H. M. and Villars, C. P., this issue, p. 173.
4. Mayo, J. S., this issue, p. 25.