On the Use of Passive Circuit Measurements for the Adjustment of Variable Capacitance Amplifiers

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In the field of microwave tubes, the cold test plays an important role. However, no attempt in this direction has been made for the variable capacitance amplifier. It is the purpose of this paper to present the theory of a cold test procedure for parametric amplifiers. The cold test is essentially the measurement of the impedance locus of the input, the output and the pump circuits under the no-pump condition, with the diode bias voltage as the variable parameter. From these impedance loci one can evaluate all the important circuit parameters of the equivalent circuit of the parametric amplifier, including the value of the dynamic quality factor of the diode. Using these data, it is relatively easy to design or adjust the circuit so as to give the best noise performance. Since the theory of the cold test procedure neglects the effects of (1) higher harmonics, (2) any parallel conductance of the diode, and (3) circuit losses, the validity of the theory can be established only by experiment. For this reason, this paper also presents some of the experimental results obtained with a 6-kmc degenerate amplifier. The correlation between theory and experiment has proved to be excellent.

I. INTRODUCTION

Although variable capacitance amplifiers have been built and operated successfully, their design has been an art practiced by the individual designer rather than a systematic construction. The designer generally provides various adjustable components in his amplifier and obtains the final optimum result on a trial and error basis. However, the designer can never be free from the fear that just one more adjustable component may considerably improve the noise figure. Furthermore, when the measured noise figure is not as good as expected from some previous

experience, there is no simple way to determine which circuit is the main cause of the poor noise figure, i.e., the signal, the idler or the pump circuit. The poor result might also be due to a poor diode. The cold test procedure goes a long way towards resolving this uncertainty.

In microwave tubes, such as the klystron and magnetron, the cold test plays an important role. However, no attempt in this direction has been made for the variable capacitance amplifiers. It is the purpose of this paper to present both the theory of a cold test procedure for parametric amplifiers and some experimental results on a 6-kmc degenerate amplifier showing the validity and the limit of applicability of the theory. It can be shown[1] that the minimum noise figures of lower-sideband idler-output and circulator type amplifiers, degenerate amplifier and upper-sideband up-converter are all basically determined by a dynamic quality factor of the diode and that, for optimum noise figure operation, each type of amplifier requires certain values of R_s/R_g and R_s/R_L, where R_s is the series resistance of the diode, R_g the internal resistance of the generator and R_L the load resistance. The cold test is essentially the measurement of the impedance locus of the input, the output, and the pump circuits, under the no-pump condition with the diode bias voltage as the variable parameter. From these loci all the important circuit parameters of the equivalent circuit of the parametric amplifier, including the diode dynamic quality factor, can easily be evaluated. Using these data, it is quite straightforward to design or adjust the circuit so as to give the best performance under the restriction of a three-frequency assumption. Further, should a poor noise figure be obtained, one can easily detect from the equivalent circuit where the main trouble lies.

The cold test procedure thus has a large advantage over the conventional trial and error method. It must be pointed out, however, that the cold test checks only the necessary conditions which must be satisfied to obtain a low-noise amplifier. Sufficient conditions are far beyond the scope of this paper, since the present theory of parametric amplifiers completely neglects the effect of higher harmonics. Also, it must be mentioned that if, in addition to the series resistance, there is an appreciable amount of parallel leakage conductance in the diode, the technique discussed here is not directly applicable. Such a diode is regarded as poor and would generally not be used; the theory of minimum noise figure for such a diode has, therefore, not yet been fully developed.

II. EQUIVALENT CIRCUIT OF PARAMETRIC AMPLIFIER

The parametric amplifier which we shall consider is a network with a variable capacitance, and an input (ω_1), an output (ω_2), and a pump

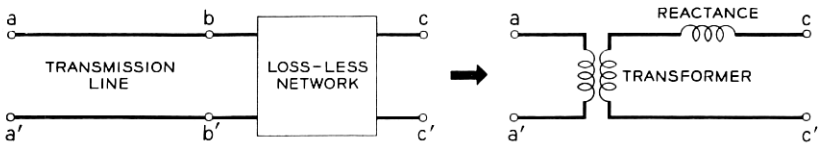

Fig. 1 — Equivalence of two networks.

(ω_p) circuit. Without any loss of generality, we can assume that the input is in the form of a transmission line with a matched generator, and the output a transmission line with a matched load. For a properly designed amplifier the network should have negligible losses except for the diode series resistance. Further, the input, the output and the pump circuits should be isolated from each other except through the parametric action. Therefore, the whole circuit connecting the input terminals to the diode is considered as a lossless two-terminal-pair network at ω_1, and the whole circuit connecting the output terminals to the diode as another lossless two-terminal-pair network at ω_2. By choosing a proper reference plane along the transmission line, each lossless two-terminal-pair network can be considered as a simple combination of an ideal transformer and a series reactance, as shown in Fig. 1 (see Appendix A). Therefore, the equivalent circuit of the amplifier becomes that shown in Fig. 2. For our purpose, however, the transformer can be eliminated as shown in Fig. 3, since only the ratios between the various impedances are important, and not their actual values. For example, the minimum noise figure condition requires a certain value of R_s/R_g, where R_g is the internal resistance of the generator looking back from the diode. R_s/R_g is the diode series resistance normalized to the generator resistance R_g in Fig. 3, and it corresponds to $R_s/(n_1^2 r_g)$ in Fig. 2, which is again the diode series resistance seen from and normalized to the generator resistance r_g, i.e., $(R_s/n_1^2)/r_g$. Thus, there is no difference between Fig. 2 and Fig. 3 as long as the impedances are all measured from the transmission lines.

The pump circuit is yet another lossless two-terminal-pair network, but this circuit does not have to satisfy any stringent requirements.

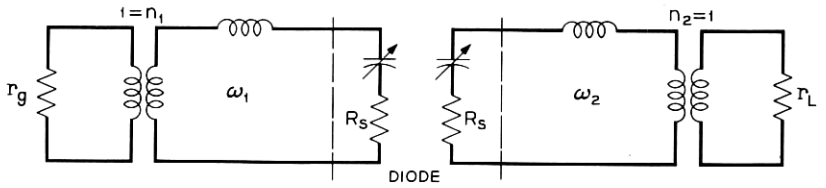

Fig. 2 — Equivalent circuit of the parametric amplifier.

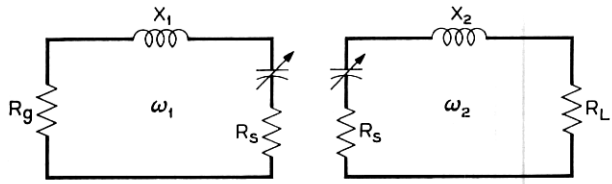

Fig. 3 — Elimination of the transformer in the equivalent circuit of Fig. 2.

The function of this circuit is to provide enough pump voltage across the diode junction without letting the signal and the idler energy escape into the pump generator. The coupling between the diode and the pump input is easily checked in a way similar to that used for the ω_1 and ω_2 circuits.

III. DETERMINATION OF CIRCUIT PARAMETERS

The impedance looking into the network from the input (or the output) is a series connection of a reactance, a variable capacitance and a resistance. If we change the capacitance value by applying a dc voltage to the diode, the impedance changes but the resistive part remains constant. Thus, the locus of the impedance should be a part of a constant resistance circle on the Smith chart. If we set the reference plane arbitrarily, the circle is generally not a constant resistance circle, but it is always possible (under the model assumed) to rotate the experimentally determined circle about the center of the Smith chart until it fits one of the constant resistance circles. This procedure corresponds to the proper choice of the reference plane in the previous section. The resistance value of the circle thus obtained gives R_s/R_g (or R_s/R_L). The mean value of the reactance gives the additional reactance in the input (or output) circuit, i.e., the diode average reactance plus the circuit reactance. The minimum noise figure condition requires that this additional reactance be zero. The locus should, therefore, be located symmetrically on the two sides of the zero reactance line when the bias voltage changes in the same manner as the pump voltage across the diode junction.

Making the open circuit assumption for the unwanted frequencies, the diode dynamic quality factor $\tilde{Q}$ is defined by

$$\tilde{Q} = \frac{1}{\omega 2K_1 R_s} \tag{1}$$

$$\simeq \frac{\text{Total reactance variation}}{4R_s} = \frac{2\Delta X}{4R_s}. \tag{2}$$

The quantity K_1 is defined through the relationship

$$\frac{1}{C(t)} = \frac{1}{K_0} + \frac{1}{K_1} \cos \omega_p t + \cdots \tag{3}$$

where $C(t)$ is a junction capacitance which is a periodic function of time. The value of $\tilde{Q}$ is thus easily evaluated from the impedance locus using (2).

In certain cases, the circle of the impedance locus does not come close to the periphery of the Smith chart, and, thus no appropriate constant resistance circle can be obtained by a rotation of the experimentally determined circle. This indicates either that the network is lossy, or else that the diode has a parallel conductance in addition to the series resistance. In the former case the network should be redesigned or readjusted to eliminate this additional loss. In the latter case the present technique is not directly applicable.

IV. MINIMUM NOISE FIGURE ADJUSTMENT

In addition to the condition that the locus be symmetrical about the zero reactance line, each type of amplifier requires certain values of R_s/R_g and R_s/R_L for optimum noise figure operation. These values are detailed in a previous paper[1] and will be quoted in this section without further reference.

4.1 *Upper Sideband Up-converter*

For the upper sideband up-converter, the minimum noise figure condition is given by

$$\frac{R_s}{R_g} = \frac{1}{\sqrt{1 + \tilde{Q}_1^2}} \tag{4}$$

and

$$\frac{R_s}{R_L} = \frac{1}{1 + \dfrac{\tilde{Q}_1 \tilde{Q}_2}{1 + \sqrt{1 + \tilde{Q}_1^2}}}. \tag{5}$$

The corresponding noise figure and gain are

$$F = 1 + 2\frac{T_s}{T_g}\left(\frac{1}{\tilde{Q}_1^2} + \frac{1}{\tilde{Q}_1}\sqrt{1 + \frac{1}{\tilde{Q}_1^2}}\right) \tag{6}$$

where T_s and T_0 (290°K) are the equivalent noise temperatures of the diode and the source respectively, and

$$G = \frac{\frac{\omega_2}{\omega_1}}{\left(1 + \frac{1}{\tilde{Q}_1\tilde{Q}_2} + \frac{1}{\tilde{Q}_1\tilde{Q}_2}\sqrt{1 + \tilde{Q}_1^2}\right)\left(1 + \frac{1}{\sqrt{1 + \tilde{Q}_1^2}}\right)} \tag{7}$$

From (2) and (4),

$$\frac{\Delta X_1}{R_0} = \left(\frac{R_s}{R_0}\right)\left(\frac{\Delta X_1}{R_s}\right) = \frac{2\tilde{Q}_1}{\sqrt{1 + \tilde{Q}_1^2}} \tag{8}$$

$$\simeq 2, \quad \text{if } \tilde{Q}_1 \text{ is large.}$$

Combining (4) and (8), a numerical calculation shows that the two ends of the locus should be found on the solid line shown on the Smith chart of Fig. 4. The dotted line is an example of the locus. It is worth noting

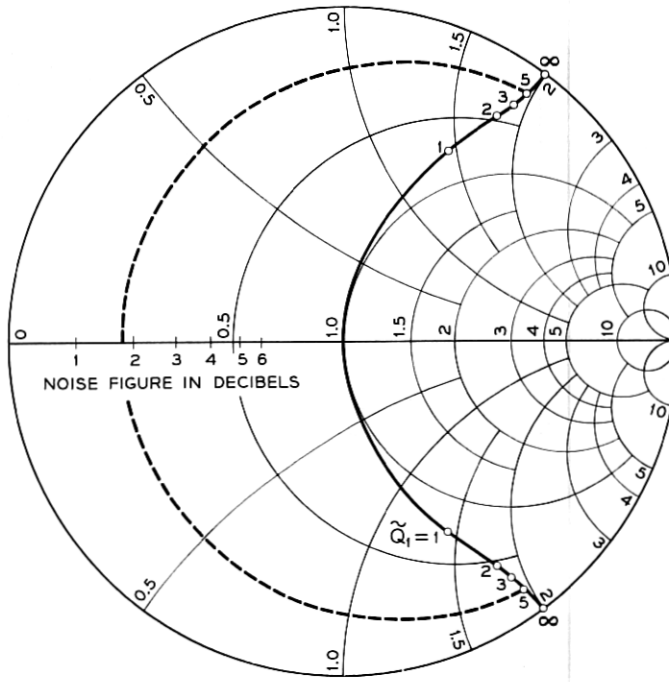

Fig. 4 — Impedance locus of input of up-converter for minimum noise figure. The dotted line is an example. The solid line is the limit of impedance swing.

that in most practical cases $\tilde{Q}_1$ is large, and, hence, the locus should extend nearly from $j2$ to $-j2$. Next let us consider the output circuit. From (5) we have

$$\frac{\Delta X_2}{R_L} = \frac{2\tilde{Q}_2}{1 + \dfrac{\tilde{Q}_1\tilde{Q}_2}{1 + \sqrt{1 + \tilde{Q}_1^2}}}. \tag{9}$$

If $\tilde{Q}_1$ and $\tilde{Q}_2$ are large, as is usually the case,

$$\frac{\Delta X_2}{R_L} \simeq 2. \tag{10}$$

This means that the output impedance locus also should extend from $j2$ to $-j2$.

Whenever the succeeding stage has a poor noise figure compared to the noise figure of the up-converter, the maximum gain condition of the up-converter gives a better over-all noise performance than the minimum noise figure condition. The maximum gain condition is given by

$$\frac{R_s}{R_g} = \frac{R_s}{R_L} = \frac{1}{\sqrt{1 + \tilde{Q}_1\tilde{Q}_2}}. \tag{11}$$

The corresponding noise figure and the maximum gain of the up-converter are given by

$$F = 1 + \frac{T_s}{T_g}\left(\frac{1}{\sqrt{1 + \tilde{Q}_1\tilde{Q}_2}} + \frac{\omega_1}{\omega_2}\frac{1}{\sqrt{1 + \tilde{Q}_1\tilde{Q}_2}}\frac{\sqrt{1 + \tilde{Q}_1\tilde{Q}_2} + 1}{\sqrt{1 + \tilde{Q}_1\tilde{Q}_2} - 1}\right) \tag{12}$$

and

$$G = \frac{\omega_2}{\omega_1}\frac{\sqrt{1 + \tilde{Q}_1\tilde{Q}_2} - 1}{\sqrt{1 + \tilde{Q}_1\tilde{Q}_2} + 1}. \tag{13}$$

Equation (11) shows that both the input and output impedance loci should lie on the same resistance circle of the Smith chart. The reactance variations are given by

$$\frac{\Delta X_1}{R_g} = \frac{2\tilde{Q}_1}{\sqrt{1 + \tilde{Q}_1\tilde{Q}_2}} \tag{14}$$

and

$$\frac{\Delta X_2}{R_L} = \frac{2\tilde{Q}_2}{\sqrt{1 + \tilde{Q}_1\tilde{Q}_2}}. \tag{15}$$

When $\tilde{Q}_1\tilde{Q}_2$ is large, they become

$$\frac{\Delta X_1}{R_g} \simeq 2\sqrt{\frac{\omega_2}{\omega_1}} \tag{16}$$

and

$$\frac{\Delta X_2}{R_L} \simeq 2\sqrt{\frac{\omega_1}{\omega_2}}. \tag{17}$$

In most practical cases, however, because of the moderate noise figure of the succeeding stage, neither the minimum noise figure condition nor the maximum gain condition gives the best over-all noise figure — this is always obtained somewhere between these two conditions. If the noise figure of the succeeding stage is given, the condition for the best over-all noise performance, and, hence, the required impedance loci, are easily calculated.[1] Thus the cold test procedure can also be used to adjust for the best over-all noise figure adjustment.

4.2 *Lower Sideband Nondegenerate Amplifiers*

For the lower sideband nondegenerate amplifiers (both idler-output and circulator types), the minimum noise figure condition for large gain is given by

$$\frac{R_s}{R_g} = \frac{1}{\tilde{Q}_1\tilde{Q}_2 - 1} \tag{18}$$

and

$$R_s/R_L \to \infty. \tag{19}$$

The minimum noise figure is

$$F = 1 + \frac{\frac{T_s}{T_g}}{\tilde{Q}_1\tilde{Q}_2 - 1}\left(1 + \frac{\omega_1}{\omega_2}\tilde{Q}_1\tilde{Q}_2\right). \tag{20}$$

Since $\tilde{Q}_1 = \Delta X_1/2R_s$ from (2), (18) may be rewritten as

$$\frac{\Delta X_1}{R_g} = \frac{2\tilde{Q}_1}{\tilde{Q}_1\tilde{Q}_2 - 1} \tag{21}$$

and so the input reactance should vary from

$$\frac{+j2\tilde{Q}_1}{\tilde{Q}_1\tilde{Q}_2 - 1} \quad \text{to} \quad \frac{-j2\tilde{Q}_1}{\tilde{Q}_1\tilde{Q}_2 - 1}.$$

From (19), the output locus should converge to the infinite resistance circle, keeping the center of the locus on the zero reactance line.

It sometimes happens that because of bandwidth or stability requirements, condition (19) can not be satisfied, i.e., the value of R_s/R_L has to remain finite. The minimum noise figure condition under this restriction, and the corresponding noise figure, are given by (18) and (20) respectively, provided that everywhere $\tilde{Q}_1\tilde{Q}_2$ is replaced by

$$\tilde{Q}_1\tilde{Q}_2\left(\frac{R_s}{R_s + R_L}\right)$$

and that the load and diode temperatures are equal. The reactance variations are given by

$$\frac{\Delta X_1}{R_g} = \frac{2\tilde{Q}_1}{\tilde{Q}_1\tilde{Q}_2\left(\frac{R_s}{R_s + R_L}\right) - 1} \tag{22}$$

and

$$\frac{\Delta X_2}{R_L} = \frac{2R_s}{R_L}\,\tilde{Q}_2. \tag{23}$$

When R_s/R_L is finite, $\tilde{Q}_1$ must be replaced by

$$\tilde{Q}_1\sqrt{\frac{R_s}{R_s + R_L}}$$

to obtain the corresponding noise figure from Fig. 4 of the referenced paper.[1]

4.3 *Degenerate Amplifier*

For the degenerate amplifier, the minimum noise figure for large gain is

$$F = 1 + \frac{T_s}{T_g}\frac{1}{\tilde{Q} - 1} \tag{24}$$

and is obtained when

$$\frac{R_s}{R_g} = \frac{1}{\tilde{Q} - 1} \tag{25}$$

Noting again that $\tilde{Q}_1 = \Delta X/2R_s$ from (2), we have

$$\frac{\Delta X}{R_g} = \frac{2\tilde{Q}}{\tilde{Q} - 1}. \tag{26}$$

A little calculation shows that the locus terminates on the straight lines through the $(\infty, j\infty)$ and $(0, \pm j2)$ points, as shown in Fig. 5. The dotted line is an example of the locus.

The above discussion is entirely based on two assumptions, (*i*) that the unwanted frequencies are open-circuited, and (*ii*) that the reactance variation of the diode junction is sinusoidal. In practice, however, it is difficult to satisfy these assumptions completely, and the actual reactance variation required for optimum performance may be slightly larger than that indicated above. Nevertheless, experiments on lower sideband amplifiers have shown that the effect of improperly terminating the higher sidebands is small as long as the circuit is well detuned at the frequency of the upper sideband. Experiments with an upper sideband up-converter also support the theory, even though in the actual experimental case the lower sideband was not perfectly open circuited. The experimental results on a degenerate amplifier will be discussed in detail in Section VI.

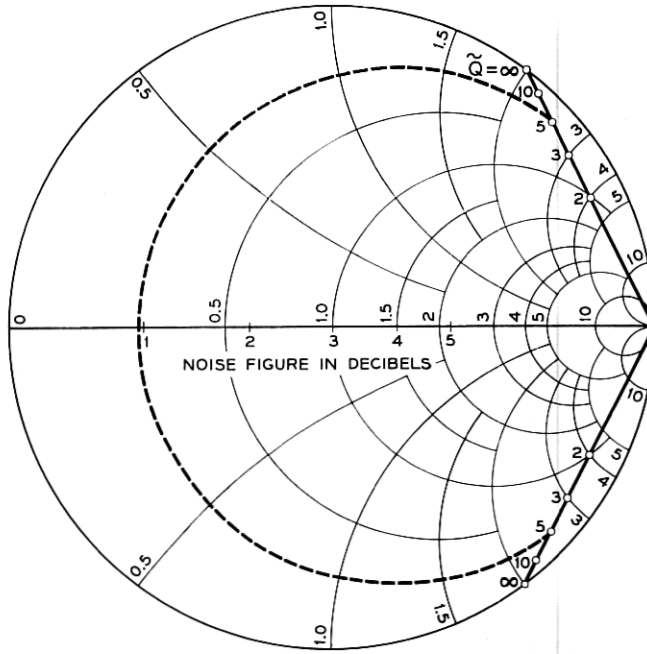

Fig. 5 — Impedance locus of degenerate amplifier with large gain and minimum noise figure. The dotted line is an example. The solid line is the limit of impedance swing.

The best starting point for adjusting an amplifier is to provide about 10 to 20 per cent larger reactance variation than that indicated above, and to test the amplification with reduced pump power. If the amplification is satisfactory, one can decrease R_s/R_g, improving the noise figure. The normalized reactance variation, however, decreases proportionally to R_s/R_g, and accordingly the pump power required for proper amplification increases. If the pump voltage across the diode junction increases too much, additional noise such as microplasma or shot noise becomes effective and the noise figure deteriorates again. Therefore, the decrease of R_s/R_g is stopped just before the noise figure begins to deteriorate.

V. BIAS SWEEPING METHOD

Since a large number of standing-wave measurements have to be made for just one impedance locus, it is a time-consuming job to get the proper locus by adjusting the actual circuit. However, the procedure is considerably simplified by modulating the bias and displaying the output from the standing-wave detector on an oscilloscope. A schematic diagram of the bias sweeping method is shown in Fig. 6. The diode bias voltage is modulated at 60 cps by means of an ac voltage applied through a transformer, and this voltage is also applied to the horizontal amplifier of the oscilloscope. The vertical axis of the oscilloscope shows the output of the standing-wave detector. Thus, if a square-law detector is used, the pattern on the oscilloscope represents the square of the length from a reference point on the periphery of the Smith chart to the locus versus the bias voltage. This relation is shown in Fig. 7 (see Appendix B). If one moves the probe position of the standing-wave detector k wave-

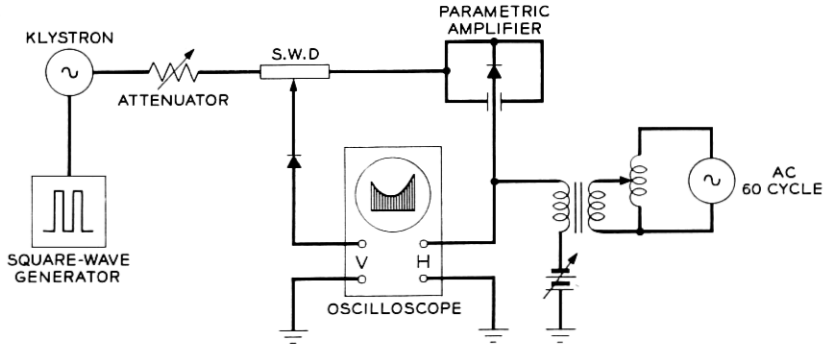

Fig. 6 — Bias sweeping method.

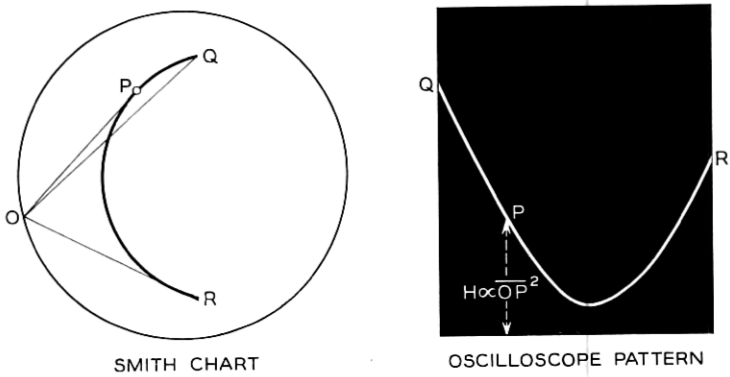

Fig. 7 — Relation between impedance locus and oscilloscope pattern.

lengths towards the load, the reference point moves k wavelengths clockwise along the periphery of the Smith chart (in the direction of the arrow indicating "wavelength toward generator"). Therefore, the pattern changes as shown in Fig. 8. Keeping these relations in mind, observing the pattern on the oscilloscope and moving the probe position of the standing-wave detector, one can visualize the shape of the locus on the Smith chart. After having adjusted the circuit for the proper pattern on the scope, the usual point-by-point measurement can be made, if desired.

The pump circuit can also be checked by the bias sweeping method. The proper impedance variation is an indication of good coupling between the pump input and the diode. No critical adjustment is required

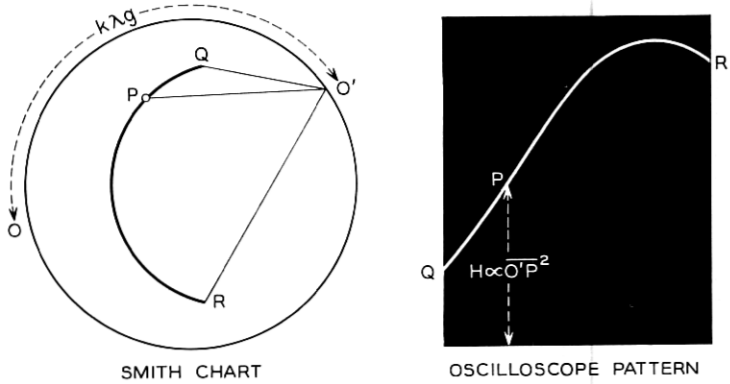

Fig. 8 — Shift of probe position and oscilloscope pattern.

for the pump circuit; however, it is desirable that the locus be reasonably symmetrical about the zero reactance line, and that the impedance swing be reasonably large.

VI. EXPERIMENTAL RESULTS

Since the theory neglects the effects of (*i*) higher harmonics, (*ii*) any parallel conductance of the diode, and (*iii*) circuit losses, the validity of the theory can be established only by experiment. For such a validity check, it is best to start with a degenerate amplifier, since this has the simplest circuit configuration. In this section we shall present some of the experimental results obtained with a 6-kmc degenerate amplifier.

The diode mount and also the noise figure measuring setup are similar to those described by M. Uenohara.[2] To make input impedance measurements, a standing-wave detector is inserted between the diode mount and the circulator. The circuit adjustment is done by the bias sweeping method. After obtaining the desired impedance locus, the locus is plotted on the Smith chart by the usual point-by-point measurement. Figs. 9

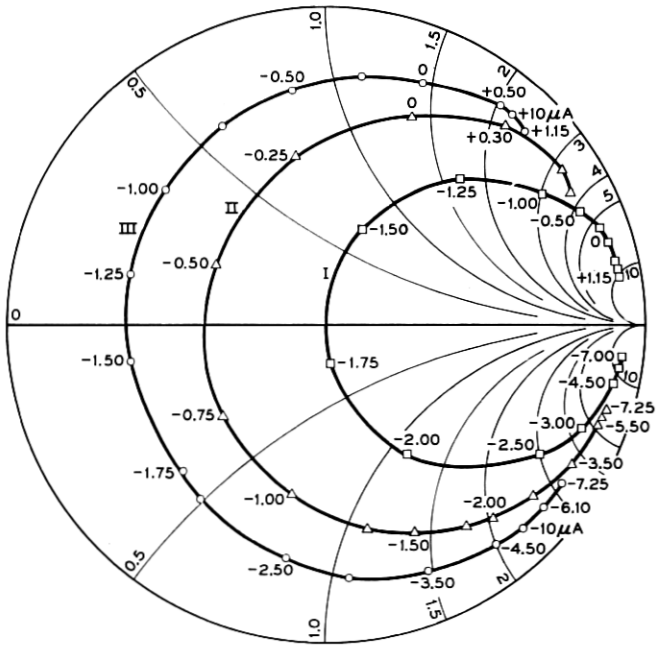

Fig. 9 — Impedance loci of a gallium-arsenide diode. DC bias voltage is applied through a 10,000-ohm series resistance.

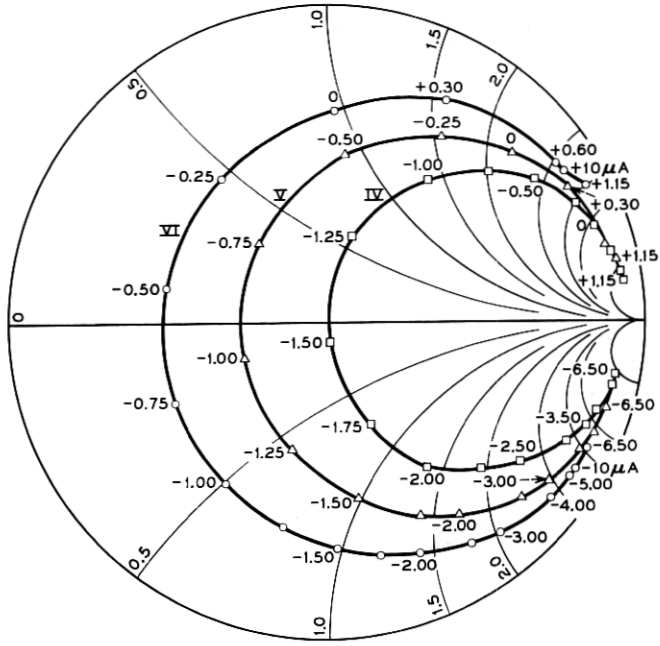

Fig. 10 — Impedance loci of a silicon mesa diode.

and 10 show two examples of such loci, one for a gallium arsenide point-contact diode and the other for a highly doped silicon mesa diode. The corresponding noise figures and the dc bias voltages for amplification are given in Table I. The accuracy of the noise figure measurements is believed to be ±0.2 db. From each impedance locus, a theoretical noise figure is calculated using (24) and (25) and is also given in the Table. The noise figure decreases as the locus moves in the direction of over-coupling. However, if it goes too far, large gain is no longer obtainable.

TABLE I — NOISE FIGURES AND OPERATION BIAS VOLTAGE

Diode Type	Locus.	Noise Figure (db)	Bias Voltage (volts)	Calculated N.F. (db)
Gallium Arsenide (#2499)	I	3.1	−1.75	3.0
	II	1.7	−1.00	1.6
	III	1.0	−2.45	0.9
Silicon (SI-R 73-62)	IV	3.1	−1.50	3.0
	V	2.1	−1.10	2.0
	VI	1.1	−0.95	1.2

This is shown in Fig. 11 for the same diode as that of Fig. 9. For comparison, the locus III of Fig. 9 is here given again. The locus VII gave a maximum gain of 15.4 db, and VIII a maximum of 5.4 db. An attempt to obtain larger gain by increasing the pump power failed. Apparently the loss of the diode increases due to the parallel conductance which comes in when the applied voltage exceeds either the contact potential in the forward bias region or the breakdown voltage in the reverse bias region. The theoretical limit on the length of the locus for the large gain condition is given by the straight lines drawn through the points $(\infty, j\infty)$ and $(0, \pm j2)$, provided that the locus is symmetrical about the zero reactance line. For a given coupling, if the locus cuts these two lines, the reactance swing can be decreased by decreasing the pump power until the locus terminates on these lines, thus giving the correct condition for large gain. If the locus does not extend to these lines, large gain cannot be achieved. The loci VII and VIII in Fig. 11 certainly correspond to this latter case.

The most interesting quantity for a diode is the best noise figure com-

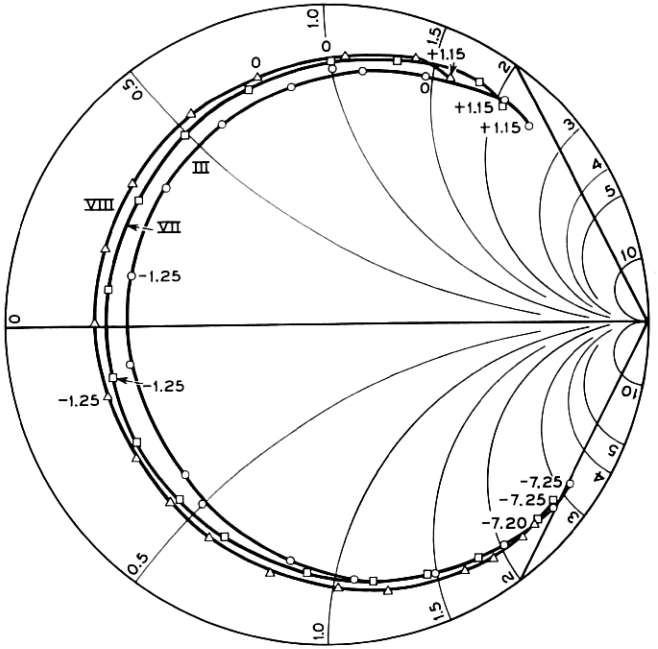

Fig. 11 — Departure from large gain condition. Locus III gives more than 20 db gain, VII 15.4 db and VIII 5.4 db.

patible with large gain. This can be found by changing the locus step-by-step towards overcoupling and measuring the noise figure for each adjustment (as has been done in Figs. 9 and 10) until one gets the optimum noise figure compatible with large gain: beyond this point either the gain becomes small (in our case less than 16 db) or the noise figure becomes worse because of microplasma and/or shot noise. Our final results for ten different diodes are plotted in Fig. 12 against the measured dynamic quality factor $\tilde{Q}$. The quoted values of $\tilde{Q}$ correspond to the reactance variation for a change of bias voltage up to the points where the dc current reaches $\pm 10\mu a$, and these $\tilde{Q}$ values are accordingly designated as $\tilde{Q}(\pm 10\mu a)$ in the Figure. This choice of $10\mu a$ for the limit is made mainly for convenience, and the question remains whether or not this choice is appropriate for all diodes. As diodes are improved, the noise contribution from the parasitic series resistance R_s becomes smaller: the microplasma and shot noise will then predominate, and one may therefore have to change this current limit to a smaller value. For the present diodes, however, the $10\mu a$ limit seems to give an appropriate guide.

VII. SOME REMARKS ON NEGLECTED FACTORS

The theory for the cold test procedure neglects the effects of higher harmonics, the parallel conductance of the diode, and circuit losses.

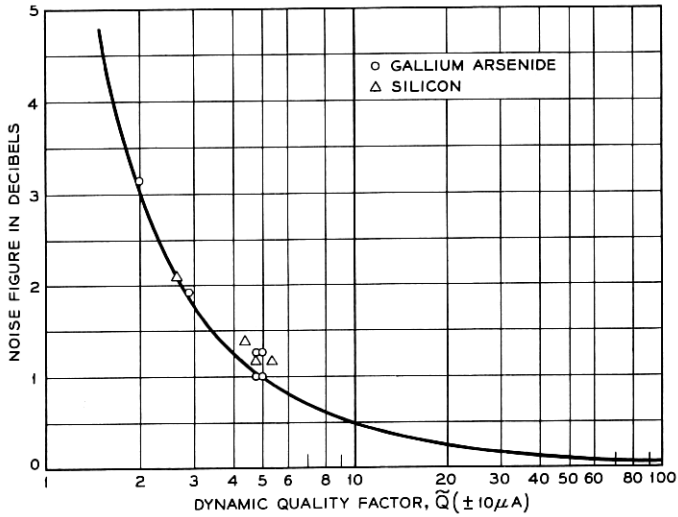

Fig. 12 — Measured noise figure versus measured dynamic quality factor Q $(\pm 10\ \mu a)$.

These effects, however, are actually noticeable in the experiments. Referring to Figs. 9 and 10, strictly speaking the impedance loci are not part of constant resistance circles: extrapolating the circles on which the loci lie, one finds that they do not touch the periphery of the Smith chart. This occurs partly because the diode has a small parallel conductance in addition to the series resistance, and partly because the circuit has finite losses. The series resistance R_s which is read directly off the Smith chart includes some contribution from the circuit itself. It is this R_s which is employed for the noise calculation in the previous section, and, hence, the noise contribution from the circuit losses is partly included in the calculated noise figure.

It will be noted that the operating bias voltage is not at the center of the locus. This is due to the effect of higher harmonics of the reactance variation. To see this clearly, the small-signal reactance of locus III is plotted against the dc bias voltage in Fig. 13. If the pump voltage across the junction is sinusoidal and the operating bias voltage is set at a zero reactance condition, the average reactance is inductive as shown schematically in Fig. 14. In actual practice, a distortion of the pump voltage takes place. As the bias is increased for the forward direction, the capacitance is increased, and, hence, the impedance is decreased. The pump voltage across the junction thus tends to decrease, making the waveform flat. Since it is possible to increase the pump power to produce the same maximum voltage as before without introducing shot noise or

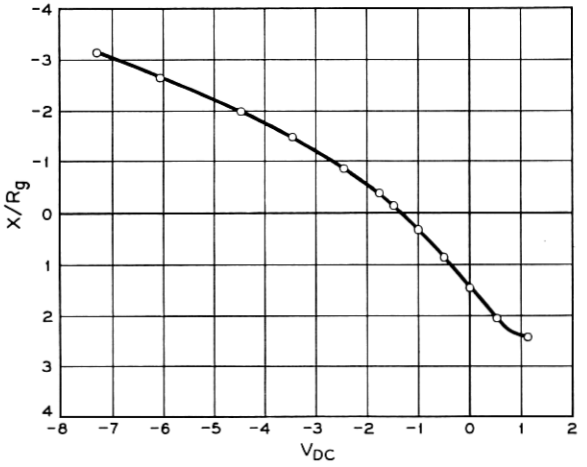

Fig. 13 — Small-signal reactance versus bias voltage (Locus III).

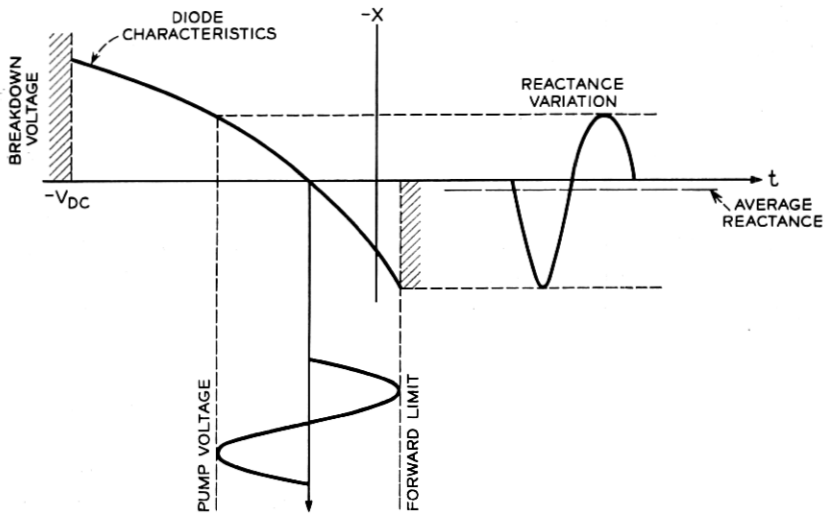

Fig. 14 — Distortion of reactance variation.

parallel conductance, the net result is an increase of the area under the reactance variation curve in the forward bias region. The opposite tendency appears in the reverse bias region, there increasing the area of the opposite reactance swing, but this is insufficient to compensate for the increase in the forward swing. The operating bias voltage must, therefore, be made further negative to cancel the additional inductance. This, then, may be the reason why the best bias voltage for amplification is always found on the capacitive side of the locus.

A rigorous theory for the minimum noise figure would necessarily include the effect of higher harmonics and of the parallel conductance. However, the fruitfulness of further efforts in this direction is doubtful, since the noise contribution which comes from the microplasma produced in avalanche breakdown is at least as great, and an analytical treatment of this is difficult. In our calculation, this is taken care of implicitly by choosing a current limit of $-10\mu a$ when evaluating $\tilde{Q}$.

In the circuit actually used in the experiments, the upper sideband impedance is not necessarily infinite. Whenever the upper sideband impedance becomes low, as indicated by the gain being smaller than that expected from the impedance locus, the shorted plunger or slide screw tuner in the pump circuit was shifted a half or one pump wavelength, thereby detuning the upper sideband without affecting the signal and

pump circuits. The upper sideband is thus expected to be adequately detuned.

VIII. CONCLUSIONS

We have discussed the principle of the cold test procedure for variable capacitance amplifiers, the adjustment of the circuit for minimum noise figure, a simplified method for visualizing the impedance locus on the Smith chart, and the experimental results on a 6-kmc degenerate amplifier. It has been shown that all the important circuit parameters of the equivalent circuit of the parametric amplifier can be evaluated from the cold test result, making the adjustment of the circuit for minimum noise figure relatively straightforward.

For the calculation of the dynamic quality factor, it is suggested that a limiting value for the dc bias current be chosen of $\pm 10\mu a$.

Despite the neglect in the theory of higher harmonics, parallel conductance, and circuit losses, the correlation between the measured noise figures and those calculated from the cold test results is very good, in fact, surprisingly so.

Brief consideration has also been given to certain factors neglected in the simple theory. The best operating bias voltage is always found on the negative side of the locus center, and this is explained qualitatively by the harmonics of the reactance variation.

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APPENDIX A

Equivalent Circuit of Lossless Two-Terminal-Pair Network with a Transmission Line[3]

Consider a lossless two-terminal-pair network with a transmission line on the left-hand side of it. The reflection coefficient at an arbitrary plane on the transmission line is a bilinear function of the impedance Z connected to the right-hand side of the two-terminal-pair network. There are reference planes where the reflection coefficient becomes unity when Z approaches infinity, since in this case the circuit has no losses at all. Take one of such reference planes and consider the reflection coefficient at this plane with an arbitrary impedance Z. It can be expressed

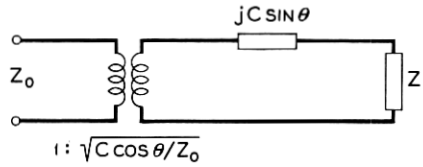

Fig. 15 — Equivalent circuit for a lossless two-terminal-pair network and a certain length of transmission line.

in the form

$$r = \frac{Z + C_1}{Z + C_2} \tag{27}$$

where C_1 and C_2 are complex quantities, because this is the most general bilinear expression for Z for which r becomes unity when Z is infinite. Suppose $Z = jX$ (pure imaginary), then $| r | = 1$, since the circuit is again lossless. Therefore, we have

$$\left| \frac{jX + C_1}{jX + C_2} \right| = 1 \tag{28}$$

for arbitrary real X's. From this relation, we obtain

$$\mathrm{Im}C_1 = \mathrm{Im}C_2 \tag{29}$$

$$| C_1 |^2 = | C_2 |^2. \tag{30}$$

Therefore, using real quantities C and θ, C_1 and C_2 can be expressed in the form

$$C_1 = -Ce^{-j\theta} \tag{31}$$

$$C_2 = Ce^{j\theta}. \tag{32}$$

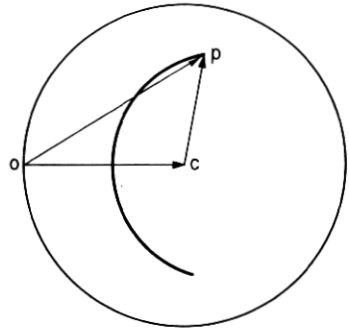

Fig. 16 — Relation between impedance and voltage on Smith chart.

Equation (27) then becomes

$$r = \frac{Z - Ce^{-j\theta}}{Z + Ce^{j\theta}} = \frac{Z + jC \sin\theta - C \cos\theta}{Z + jC \sin\theta + C \cos\theta}. \tag{33}$$

Comparison of this equation and the standard formula for the reflection coefficient in terms of impedance indicates that the same reflection would be given by the circuit shown in Fig. 15. Since Z is arbitrary, this means that a lossless two-terminal-pair network with a certain length of transmission line attached to one side of it is always equivalent to a combination of an ideal transformer and a reactance.

APPENDIX B

Relation Between Impedance and Voltage on Smith Chart

The Smith chart is a reflection coefficient plane in which the constant resistance curves and the constant reactance curves are mapped. Suppose an impedance at a reference plane is given by a point p in the Smith chart shown in Fig. 16, then the vector $\overrightarrow{cp}$ represents the corresponding reflection coefficient, provided that the radius of the Smith chart is unity. The voltage at the reference plane is therefore given by the length of the vector $\overrightarrow{op}$, i.e., a sum of the incident wave $\overrightarrow{oc}$ and the reflected wave $\overrightarrow{cp}$ provided that the incident wave voltage is unity. Keeping the incident wave voltage constant, the change in the length of the vector $\overrightarrow{op}$ is then equivalent to the change in the voltage at the reference plane. If one moves the reference plane k wavelengths towards the load, then the whole impedance locus rotates anticlockwise k wavelengths. However, as far as the length of the vector $\overrightarrow{op}$ is concerned, the same relative effect is obtained when the locus stands still and the point o rotates k wavelengths clockwise (in the direction of the arrow indicating "wavelength toward generator"). Therefore, depending on the probe position of the standing-wave detector, the oscilloscope pattern changes in the manner discussed in the text.

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