No. 1 ESS Logic Circuits and Their Application to the Design of the Central Control

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The central control is composed of thousands of relatively simple logic circuits, intricately interconnected to perform the primary data processing functions of the No. 1 electronic switching system. This paper discusses both the circuit development of the basic modules and their application to the logic design of some of the high-speed arithmetic circuits required in the central control. Special electrical design features, wiring rules, and circuit pack assignment procedures are also described.

I. INTRODUCTION

Companion articles in this issue[1,2,3] discuss the logical organization and diverse responsibilities of the central control (CC) as the primary information processing unit of the No. 1 electronic switching system.

This paper has the objectives of describing the basic building-block circuits which constitute the framework of the central control and illustrating their logic design applications in some of the major functional portions of the unit.

The presentation is divided into three parts:

Sections II–VI deal with the parameters of the semiconductor devices and the characteristics of the basic circuit in which they are integrated.

The logical effectiveness of the resultant configuration is demonstrated in Sections VII and VIII, which trace its applications from fundamental designs to some of the more complex, specialized functions required in the CC.

Section IX discusses circuit packaging techniques and over-all equipment development as applied to the central control.

II. LOGIC CIRCUITS

2.1 *General*

Numerous factors ranging from system philosophy to device physics were considered in the process of selecting the basic semiconductor logic circuits for No. 1 ESS. The paramount objective in this process was to achieve versatile and reliable circuit performance at an over-all minimal cost. In such a large, complex information processor this can be realized only by a concurrent minimization of costs in the broad areas of design, manufacture and maintenance.

2.2 *Building-Block Approach*

The search for the common denominator of minimal cost in these broad areas highlighted the need for a standardized set of building-block logic circuits, not only for use in the central controls, which have the largest concentration of logic circuitry, but also for use throughout the entire system.

Standardization provides the system logic designer with a set of "black boxes" that can be easily interconnected to perform any complex logic function. This facilitates design by reducing the time and cost involved in specifying the logical fabrication of the system.

The minimization of the varieties of building blocks, with their correspondingly higher levels of production, translates to reduced manufacturing costs. Concurrent characterization of devices suitable for many different applications within the system reduces the number of device codes and further benefits the economics of production.

Finally, the advantages to the system user in terms of trouble diagnosis and reduced maintenance costs, particularly in the stockpiling of replacement packages and devices, is considerably improved.

2.3 *Reliability*

The electronic circuits in No. 1 ESS must be intrinsically reliable if the over-all system is to provide uninterrupted telephone service. This means that the components used in the logic circuits must be inherently reliable of themselves and used within conservative limits.

Duplication of major system units is the most important safeguard of reliable, continuous service. To prevent the loss of system control, the central control is fully duplicated. Both units of a duplicated pair contain a large number of circuits whose functions are devoted to continually monitoring all internal data processing and cross-comparing

their operations. Even so, the requirement[1] of a 40-year mean time to the simultaneous failure of duplicated units imposes stringent upper bounds on the allowable failure rate of the basic logic circuits.

To help visualize the circuit failure rates implied by these requirements, the required mean repair time in hours has been plotted against the number of failures per 10^9 circuit hours in Fig. 1.

To achieve what has been established as a reasonable mean repair time for a CC of from one to three hours (including both fault location and replacement times) it is apparent that there must be in the order of 50 to 100 failures or less per 10^9 circuit hours. For individual logic circuits, the semiconductor failure rates must then fall in the range of 1 to 10 failures per 10^9 device hours to meet these objectives.

2.4 *Switching Speed*

The No. 1 ESS system organization requires a number of units to function in real time and share a single control unit. This necessitates the use of fast switching circuits in the control unit in order not to limit the system capability. In switching circuit design, trade-offs are often made between long logic chains which require a small number of logic elements and larger, more complex circuits which have less delay.

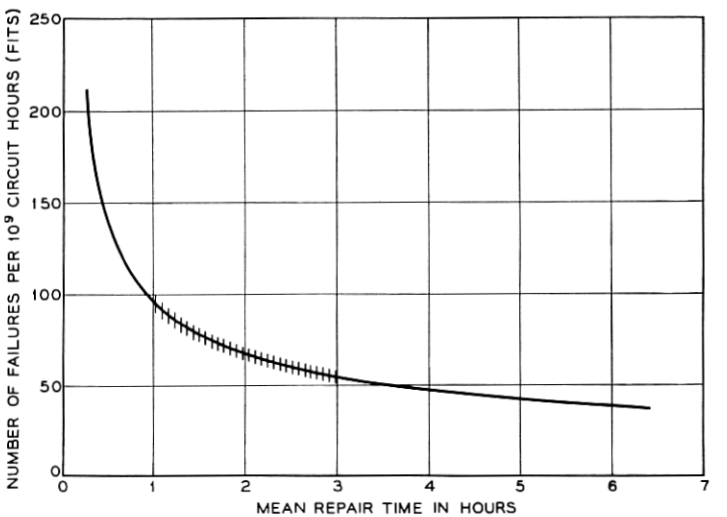


Fig. 1 — Logic circuit failure rate vs mean repair time. Assumptions: duplicated control systems, each containing 12,500 circuits; 40-year mean time to simultaneous failure of duplicated units. Typical circuit elements: 1 transistor, 4 diodes, 4 resistors, 16 soldered connections, and 4 pressure contacts.

Faster switching speeds in the individual devices alleviate the problem considerably, but this is countered by the increasing cost of the devices. These factors are all weighed in deciding upon a satisfactory operating speed.

2.5 *Environment*

For over-all system economy, the logic circuits are designed to utilize the common central-office battery power sources. Since these voltages can decrease by as much as 20 per cent during commercial ac power failure, the logic circuits must be relatively insensitive to supply voltage variations.

The logic circuits are designed to operate reliably over the temperature range of 0–55°C.

2.6 *Silicon Semiconductors*

The low leakage currents and high allowable junction temperatures of silicon devices as compared to germanium have resulted in the specification of silicon semiconductors for all circuits in No. 1 ESS. This eliminates the necessity for an air-conditioned environment. The greater tolerance to temperature variations results in smaller devices for the same power rating, allows higher packing densities for the equipment with a corresponding reduction in lead lengths and floor space, and allows the use of wave soldering on printed wiring boards. Low storage times permit high-speed operation with relatively simple circuit designs. The slightly higher voltage drop characteristic of silicon devices is easily circumvented.

III. SELECTION OF A BASIC GATE

3.1 *Type of Function*

There are many different types of semiconductor logic gates which fulfil in varying degrees the basic requirements outlined in the preceding sections. The selection of the optimum gate for a particular application depends on the relative weight given to factors such as switching speed, component and assembly costs, reliability, allowable tolerances of components and voltages, minimization of device and package codes, logical flexibility, noise margins, and many others.

The building-block logic gates for a system must, first of all, be capable of being interconnected to perform any complex logic function which may be required by the logic designers. This requires that a basic set

of functions be provided. Historically, AND and OR gates together with both inverting and noninverting amplifiers and memory cells (flip-flops) were first used. This was the case in the experimental Morris, Illinois, electronic switching system.[4]

Recently, more complex functions have been combined in the basic block — for example, the various forms of AND-NOT and OR-NOT. These are more efficient in that any one can be used exclusively to construct a complete logic system. A further benefit is that these circuits usually insert voltage or current gain in every logic stage, reducing the variations in impedance levels in a complex circuit and thereby improving speed and crosstalk performance.

3.2 *Low-Level Logic*

After studying the characteristics of many of the widely used gate circuits, the diode-coupled AND-NOT gate[5] was chosen for use in No. 1 ESS. The circuit is generally referred to as low-level logic (LLL). As shown in Fig. 2, the LLL gate consists of a diode AND gate, a biasing circuit to overcome the combined voltage drop of an input diode and the driving transistor's saturated V_{CE}, and an inverting amplifier. The combination of AND plus INVERSION derives the logical AND-NOT function. This circuit has an individual source of base current to avoid the unequal base current problems present in other logic configurations. The diodes are poled in such a manner that large reverse base drive currents can be obtained. These properties result in full utilization of the switching speed capabilities of the transistor. The voltage margins are designable and do not depend solely on device characteristics. All in all, LLL is a high-performance gate yielding a

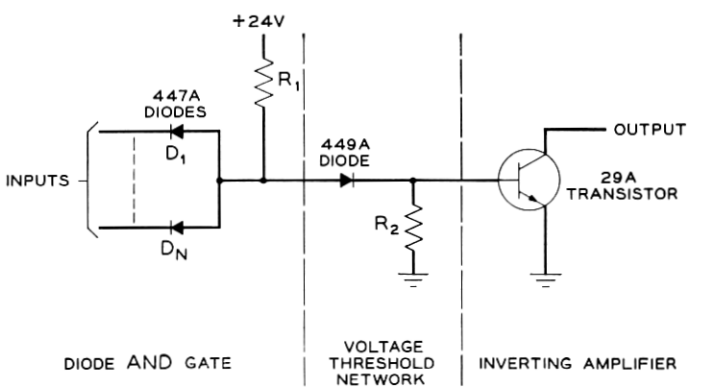


Fig. 2 — LLL circuit.

combination of fast switching speeds, large fan-in and fan-out, and excellent margins.

IV. LLL CIRCUIT DESIGN

4.1 *Worst-Case Design*

The worst-case design philosophy was used for the LLL circuit. This means that the expected characteristics of the gates were predicted on the basis of all circuit parameters being simultaneously at their extreme limits in such a manner as to degrade performance. This approach enhances circuit reliability by insuring that the margins of typical circuits are well within the design limits. For the LLL gate, worst-case design still yields very fast operation with moderately high fan-in and fan-out for relatively wide resistor and supply voltage tolerances.

4.2 *Saturated Operation*

An important consideration in the design of the LLL circuit is the use of a saturating or nonsaturating amplifier design. The primary advantage of the nonsaturating design is the elimination of the delay caused by the storage time of minority carriers in the transistor during turn-off. The significance of storage time is very much a function of the particular transistor employed and the need for speed in the system. Nonsaturating designs are complex, costly circuits which result in larger output voltages when the transistor is conducting. Also, biasing of the transistor in its active region not only increases power dissipation in the device, but also causes the circuit to be more sensitive to noise and prone to oscillation.

Part of the apparent speed advantage of the nonsaturating circuit is lost because of the necessarily higher threshold voltages. For many high-speed silicon switching transistors the storage times are so short relative to their rise and fall times as to be almost negligible in an LLL-type circuit. Furthermore, since approximately half of the stages in a logic chain are turning ON and half are turning OFF at any one time, only half the improvement in turn-off delay can be deducted from the average delay per stage. These considerations led to the selection of a saturating amplifier design.

4.3 *Biasing Network*

The major item for design in the LLL gate is the biasing network. Once a method for performing this function is selected and the element

is properly designed, the characteristics of the gate are largely determined by the inherent capabilities of the semiconductor devices, ambient operating conditions, and the tolerances of the resistors and power supply voltages.

The primary function of the biasing network in an LLL gate is to insure that its transistor will not conduct when any input to that LLL is held low by a conducting transistor in the prior stage. This requires that the biasing circuit keep the base-emitter voltage below the minimum threshold of the transistor for the maximum sum of the diode voltage drop and the V_{CE} of the saturated transistor.

The biasing network has three other important functions. First, the design should cause relatively large reverse base current flow when the transistor is switched from ON to OFF. This is necessary to obtain minimum turn-off time. Second, the biasing network should provide a noise threshold to the amplifier to prevent small transient voltage perturbations from falsely turning on the transistor. Third, the network should be designed so that the voltage across it remains as low as possible when current flows from R_1 into the base of the transistor (see Fig. 2). This minimizes the voltage swing required at the gate input.

The voltage biasing element in the LLL circuit consists of three silicon junctions in series. The three junctions provide approximately a two-volt threshold to the amplifier without the need for a second power supply. Resistor R_2 across the base-emitter junction of the transistor provides a relatively low-impedance shunt for the small forward current in the multijunction diode when the input to the circuit is low. This improves the noise margin by insuring a low potential at the base of an OFF transistor. The signal voltage swing is minimized since the difference between the threshold voltage and the forward-biased voltage drop of the multijunction diode is small. The reverse breakdown voltage of the three junctions is very high to prevent any reverse dc current. The necessary reverse transient drive is obtained by designing the multijunction diode to have a relatively long recovery time. Thus if an input to an LLL circuit whose transistor has been conducting suddenly goes low, the voltage across the diode cannot change instantaneously. For a brief time the base of the transistor is made negative and reverse base current is drawn through the temporary low reverse impedance of the multijunction diode. After recovery the diode reverts to a high impedance and prevents noise from being transmitted into the base node. To further insure this, the net capacitance of the three junctions in series is kept small.

4.4 *Dummy Load Resistor*

The LLL circuit shown in Fig. 2 has one serious deficiency. In the OFF state the collector node is at an indeterminate potential between two high impedances which are presented by the OFF collector and the nonconducting input diodes in the driven circuits. Not only does this make the node sensitive to noise, but it also slows down the turn-on of the following stages, since collector node stray capacitance must be charged by the internal gate resistors of the driven LLL circuits. The addition of a dummy load resistor from the collector node to a voltage above the threshold of the driven inputs provides a charging current for the capacitance, defines the OFF state voltage and provides a noise margin in this state, and limits the depth of saturation by establishing a lower bound for collector current.

4.5 *Operating Levels*

The choice of current and voltage levels for the LLL circuit is influenced by many of the parameters discussed earlier and ideally should be made for each system and device selection. In general, the selection of low impedance levels improves speed and capacitive crosstalk performance while higher levels result in lower power dissipation (allowing higher packing densities), improved device reliability, and fewer inductive interaction problems. In high-speed circuits the mechanical embodiment of individual circuits and of whole equipment units is significant because of its primary effect upon stray capacitance and inductance.

The impedance level chosen for the logic circuits in No. 1 ESS was largely determined by the stray capacitance anticipated at collector nodes and by estimates of wiring inductance. To charge an estimated maximum node capacity of 150 pf to the threshold of an LLL circuit in 50 nsec implies a charging current of about 10 ma. In the worst case (fan-out of one), approximately 75 per cent of this current is assigned to the dummy load and 25 per cent to the internal gate of the driven circuit. This guarantees the 10 ma for the minimum fan-out case and keeps the ratio of maximum to minimum collector current low. The choice of a collector supply voltage in the 4- to 5-volt range provides sufficient margin for noise and establishes the OFF collector impedance at about 500 ohms. The current and voltage levels chosen assure fast switching speeds for the low-power semiconductor devices described in Section V. In addition to these considerations, the effects of stray capacitance and inductance on interaction between circuits (crosstalk) had to be evaluated for the packaging and wiring arrangements used in No. 1 ESS.

4.6 *L and C Crosstalk Effects*

In addition to degrading rise times, stray capacitance between signal leads can cause interference between circuits. At the impedance level chosen, these effects do not significantly alter performance in this system.

Wiring inductance can affect circuit performance in two ways. Series lead inductance causes longitudinal voltage drops due to the rapid change of signal current. The allowable length of wire depends upon its inductance, the noise thresholds of the circuits, the operating current levels, and the required switching speeds. The wire inductance can be reduced by using twisted-pair wire for long interconnections. In addition to the series inductance problems, the mutual inductance occurring between parallel wire runs can cause interference between circuits.

The interactions of the L and C effects, together with the complex wiring patterns and nonlinear waveforms occurring in logic circuits, make an exact analysis of the net effects very difficult.[6] Analytic studies of simplified models in conjunction with laboratory measurements were utilized to formulate the following set of wiring rules to insure that the physical wiring patterns would limit the crosstalk to acceptable levels.

4.7 *Wiring Rules for Interconnecting Logic Circuits*

(1) Leads must be as short as possible, using horizontal and vertical paths

(2) wires following the same path should be loosely constrained, i.e., not laced into a cable

(3) a single wire should be used to tie the points of a node together and to a dummy load resistor where:

(a) the total node wiring is less than 6 feet and

(b) parallel runs do not exceed 3 feet

(4) twisted pairs must connect points of a node together and to three dummy loads in parallel at the driven end where:

(a) the total node wiring exceeds 6 feet and

(b) parallel runs exceed 3 feet but in no case exceed 10 feet

(5) when two LLL circuits are interconnected to form a flip-flop, they must be on the same circuit pack.

V. DEVICE CHARACTERISTICS

5.1 *General*

The characteristics of each of the semiconductors used in the LLL circuit are shown in Tables I–III. Both the input diode and the multi-

junction diode are specifically characterized for the LLL circuit. The transistor, on the other hand, is characterized for use in many different applications in a variety of circuits in No. 1 ESS.

The reliability of these devices when used in the LLL gate has been predicted on the basis of step-stress aging experiments.[7] The studies indicate that failure rates will be less than 10 in 10^9 device-hours for the transistor and less than 5 in 10^9 device-hours for the diodes. These rates are adequate to meet the reliability objectives discussed in Section 2.3.

The variations of specific parameters over the temperature range of 0–55°C were considered in establishing specific limits, although all limits are specified at 25°C to facilitate testing.

5.2 *29A Transistor*

The most important parameters of the transistor employed in the LLL circuit are presented in Table I.

The choice of operating level in the LLL circuit restricts the maximum collector current, collector voltage, and power dissipation to well below the maximums allowable. In general, these margins have been utilized to improve reliability in the logic circuits. In a number of cases the extra capability has been utilized in the design of scaled-up versions of the LLL circuit which satisfy the need to drive high fan-out situations within the logic and to drive cables to remote units.

Although the specified limits are important in determining worst-case performance, a knowledge of the distribution of parameters is necessary to predict typical behavior. Distributions of some of the more significant parameters are given in Figs. 3, 4, and 5. From the figures it is obvious that all of the limits specified are well within the device capability, which assures a high yield in production with resultant economies.

TABLE I — 29A TRANSISTOR SPECIFICATIONS

$BV_{CEO} \geqq$ 30 v	I_C = 5 ma, I_B = 0
$BV_{EBO} \geqq$ 7 v	I_C = 0, I_E = 10 μa
$h_{FE} \geqq$ 30	I_C = 5 ma, V_{CE} = 1 v
$V_{CE} \leqq$ 0.5 v	I_C = 50 ma, I_B = 2 ma
$V_{BE} \leqq$ 1.1 v	I_C = 50 ma, I_B = 2 ma
$C_{ob} \leqq$ 6 pf	I_E = 0, V_{CB} = 5 v
$C_{ib} \leqq$ 10 pf	I_C = 0, V_{EB} = 1.5 v
$T_{on} \leqq$ 65 nsec	I_C = 35 ma, I_B = 1.5 ma
$T_{off} \leqq$ 65 nsec	I_C = 10 ma, I_B = 2.5 ma, V_{BER} = −0.9 v
$\theta_{J\text{-}C}$ = 0.33°C/mw	

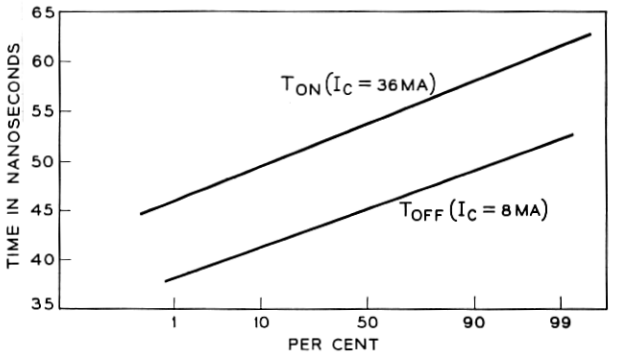


Fig. 3 — Typical switching speed distributions for worst-case conditions for 29A transistor.

5.3 *449A Multijunction Diode*

Table II lists the parameters of the multijunction diode used in the biasing network of the LLL circuit. The minimum forward voltage specification guarantees an adequate noise margin under the worst (high-temperature) conditions for the OFF state. The maximum limit assures a low drop in the conducting state, which provides an efficient transfer of current into the base of the transistor when it is turned ON.

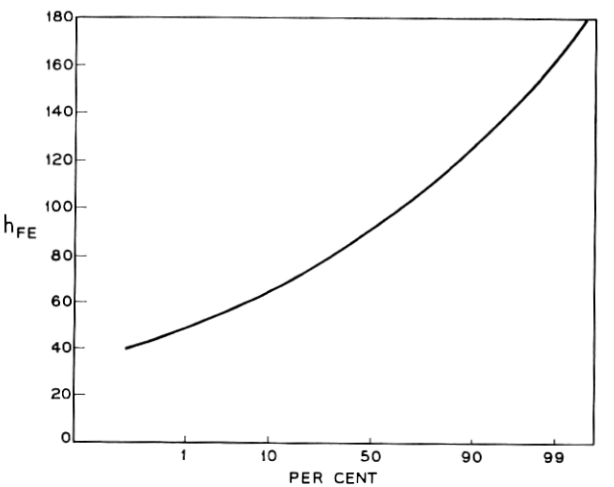


Fig. 4 — Typical h_{FE} distribution for 29A transistor: I_C = 5 ma, V_{CE} = 1 v, circuit design limit $h_{FE} \geqq 22$.

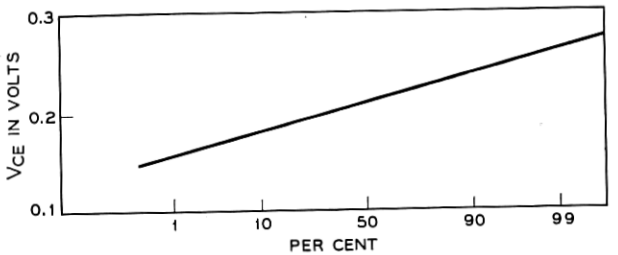


Fig. 5 — Typical V_{CE} distribution for 29A transistor: I_C = 50 ma, I_B = 2 ma specification limit ≦ 0.5 v.

Specifying the minimum stored charge guarantees that sufficient base current can be drawn during turn-off of the slowest 29A transistor. The upper limit on the total capacity across the three junctions limits noise transmission to a satisfactory level.

5.4 *447A Logic Diode*

The parameters of the 447A diode are given in Table III. The forward voltage drop, typical for a small silicon computer diode, is easily accommodated by the threshold created by the multijunction diode and the transistor base-emitter junction. The reverse breakdown is higher than necessary for the circuit, but improves reliability and allows for other applications. The reverse leakage current is so small as to be negligible for any reasonable fan-in.

The upper limits on capacitance and reverse recovery time are necessary to assure obtaining the full speed capability of the transistor. Consider the circuit in Fig. 6. If both Q_0 and Q_1 are conducting, current through R_1 will be shunted through Q_0 to ground and the current in R_2 passes through Q_0 and Q_1 in parallel; therefore Q_2 and Q_3 are nonconducting. If Q_0 is suddenly turned OFF, the shunt path to ground for I_1 will be removed, allowing Q_2 to turn ON. On a transient basis, however, diode D_2, which serves to isolate the collector nodes, can have a

TABLE II — 449A MULTIJUNCTION DIODE SPECIFICATIONS

$V_F \geqq$ 1.53 v	I_F = 70 μa
$\leqq$ 2.3 v	I_F = 2.5 ma
$\leqq$ 2.85 v	I_F = 20 ma
C 15 pf	V_F = 1 v
Stored charge $\geqq 0.4 \times 10^{-9}$ coul	I_F = 2 ma, I_R = 10 ma

TABLE III — 447A LOGIC DIODE SPECIFICATIONS

$BV \geqq 40$ v	$I_R = 5\ \mu a$
$I_s \leqq 25$ na	$V_R = 20$ v
$V_f \leqq 1$ v	$I_f = 10$ ma
$C \leqq 3.5$ pf	$V_R = 0, f_0 = 100$ kc
$t_{rr} \leqq 4.0$ nsec	

low reverse impedance for a time equal to its recovery time. As long as the low reverse impedance condition persists, the current from R_1 can "leak" through D_2 as indicated by I_3 in the figure. This interaction between nodes causes no logical error but does introduce an absolute delay in Q_2's turning on. In a fast system such delay is not tolerable. The capacitance of the diode allows a similar interaction. In addition, the capacitance can transmit noise into the internal AND gate node and also degrade rise times at this node by its shunt effect on the current from R_1. The specifications on the 447A diode are such as to make these effects almost negligible.

VI. SUMMARY OF LLL CHARACTERISTICS

The outstanding characteristics of the LLL circuit designed for No. 1 ESS are summarized in Table IV.

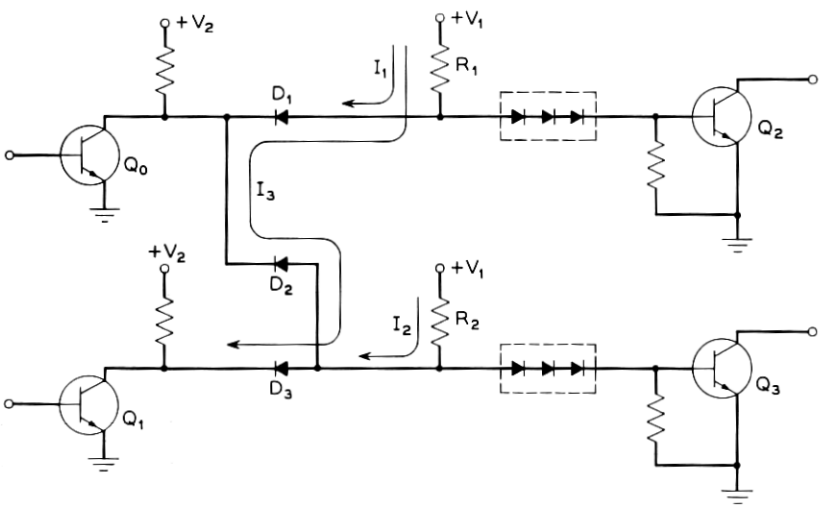


Fig. 6 — Diode recovery effect.

TABLE IV — LLL CHARACTERISTICS

Parameter	Range	Typical Value
Signal levels		
high (1)	4.0–5.1 v	4.6 v
low (0)	0.1–0.5 v	0.25 v
Fan-out	1–8	4
Fan-in	1–20	4
Turn-on delay	10–65 nsec	35 nsec
Turn-off delay	10–65 nsec	35 nsec
Noise margins		
high	1.6–3.6 v	2.5 v
low	1.0–1.5 v	1.2 v
Circuit margins		
resistor tolerance	±20%	
voltage tolerance	±10%	
Power consumption	37–140 mw	76 mw
Operating temp. range	0–55°C	

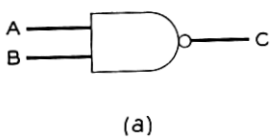
VII. LOGIC DESIGN

7.1 *Applications of LLL in Logic Designs*

It was mentioned earlier that LLL gates can be used exclusively to synthesize any logical combinaton possible with AND, OR, and NEGATION. The gate performs the AND-NOT function for the convention that a "high" or +v signal is a logical 1 and a "low" or ground signal is a logical 0.

The standard logic symbol for the LLL circuit is shown in Fig. 7 along with a function table defining its properties.

There are many ways in which complex logic circuits can be synthesized using LLL. One of the simplest approaches is to perform the original logic design in terms of the more familiar AND, OR, and NOT functions and then to substitute LLL equivalents for each of the original functions.



(a)

A	B	C (OUTPUT)
0	0	1
0	1	1
1	0	1
1	1	0

(b)

Fig. 7 — Building block logic.

The basic equivalent circuits and several other important configurations are shown in Fig. 8.

In using the substitution procedure, the following two rules should be repeatedly applied until further simplification is impossible:

(1) cancel (remove) tandem pairs of single input LLL gates since two inverters in series perform no net logical function;

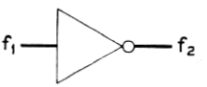
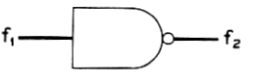
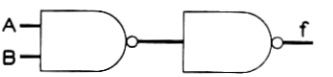
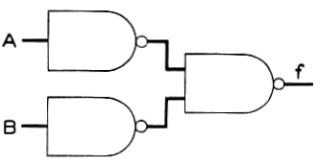
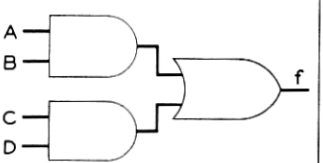
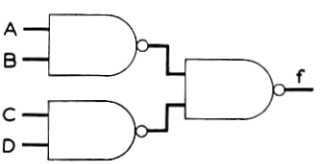
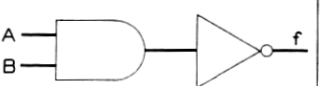
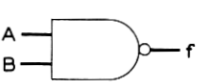
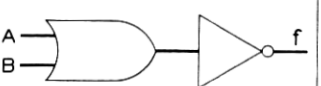
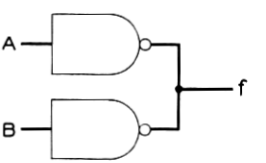
FUNCTION	AND, OR, NOT CIRCUIT	LLL CIRCUIT
INVERSION: $f_2 = f_1'$		
AND: $f = AB$		
OR: $f = A + B$		
AND – OR: $f = AB + CD$		
AND – NOT: $f = (AB)'$		
OR – NOT: $f = (A + B)'$		

Fig. 8 — Equivalent logic circuits.

(2) when two or more LLL gates drive a common gate and this gate is their only load, the outputs of all of the driving gates can be tied together and applied to a single input of the driven gate.

The example in Fig. 9 illustrates this process of simplification.

Several of the examples highlight the common connection which is

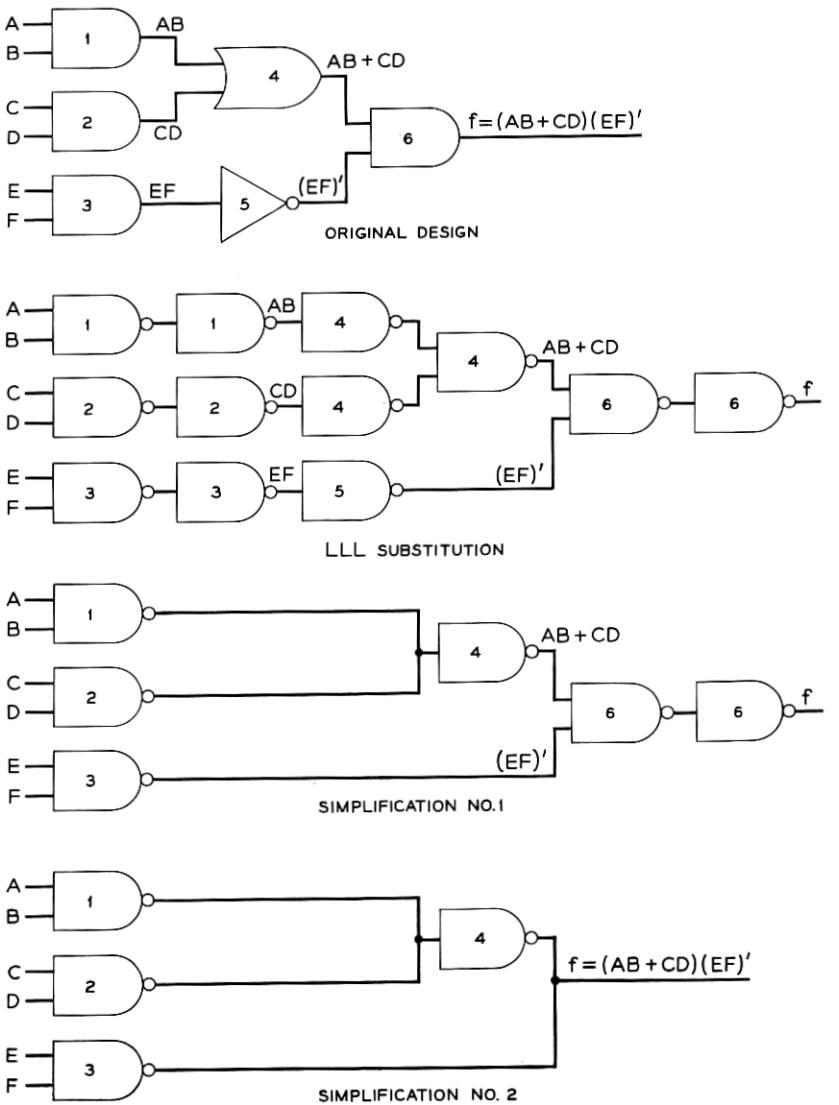


Fig. 9 — LLL simplification process.

made between the outputs of transistors which are driving a common input. An AND function is effectively formed here, since all transistors connected to the junction must be nonconducting in order that the output be high (logical 1). The use of this technique has resulted in the savings of several thousand logic diodes in the central control alone. The number of transistors which can be connected in this way is limited by the adverse effect on switching speed which is caused by the increases in inductance and capacitance.

Another approach in using LLL in logical designs is the "inhibit" technique. A simple example illustrates this approach in the design of a match circuit. In such a design, the output should be high when the two input variables (A and B) have the same state. Fig. 10(a) illustrates this solution. Conversely, one can think of the match function as requiring a high output except when A and B mismatch, in which case the output should be inhibited. This leads to a solution utilizing one LLL for each input combination which is to inhibit the output [see Fig. 10(b)]

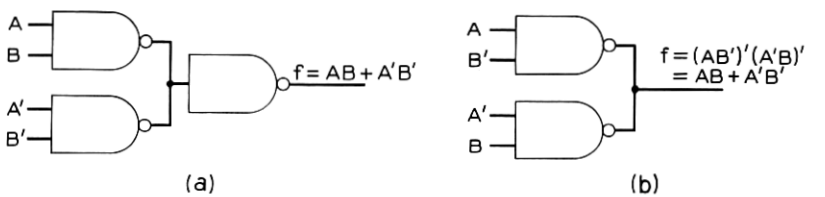


Fig. 10 — LLL match circuits.

7.2 *The LLL Flip-Flop*

Throughout the switching system, and particularly within the CC, there is the need for temporary memory facilities in the form of flip-flops. These are readily constructed by cross-connecting two LLL gates as shown in Fig. 11. The circuit operates as follows: gating functions insure that inputs A and B are both held in the high state when the

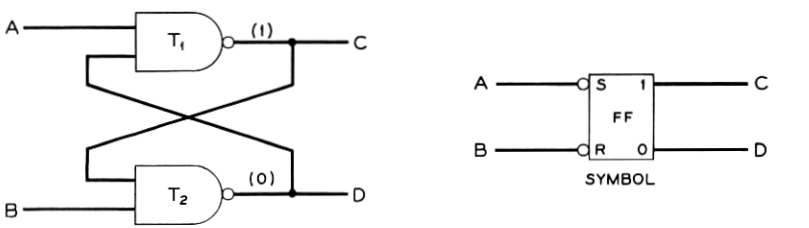


Fig. 11 — LLL flip-flop.

flip-flop is quiescent. Assume that the "set" output is high ($C = 1$) and accordingly $D = 0$. Any change in the state of A is ineffective, since the cross-connected input from D keeps T_1 nonconducting. However, if B goes to 0, the base drive for T_2 is removed, and D will go high, providing drive for T_1 and causing C to change from 0 to 1.

7.3 *Binary Counters, Shift Registers and Cable Pulsers*

In addition to the basic LLL gate and flip-flop, special circuits for binary counters and shift registers are also required. These consist of steering gates appliqued onto the LLL flip-flop to provide nonracing counting and shifting functions. "Nonracing" means that correct operation is independent of input pulse width as long as the width is greater than the minimum allowed, which here is approximately 0.25 microsecond.

The binary counter circuit is shown in Fig. 12. As can be seen, memory is provided by an LLL flip-flop, which has been modified to include direct connections to the transistor bases. Two steering networks and a

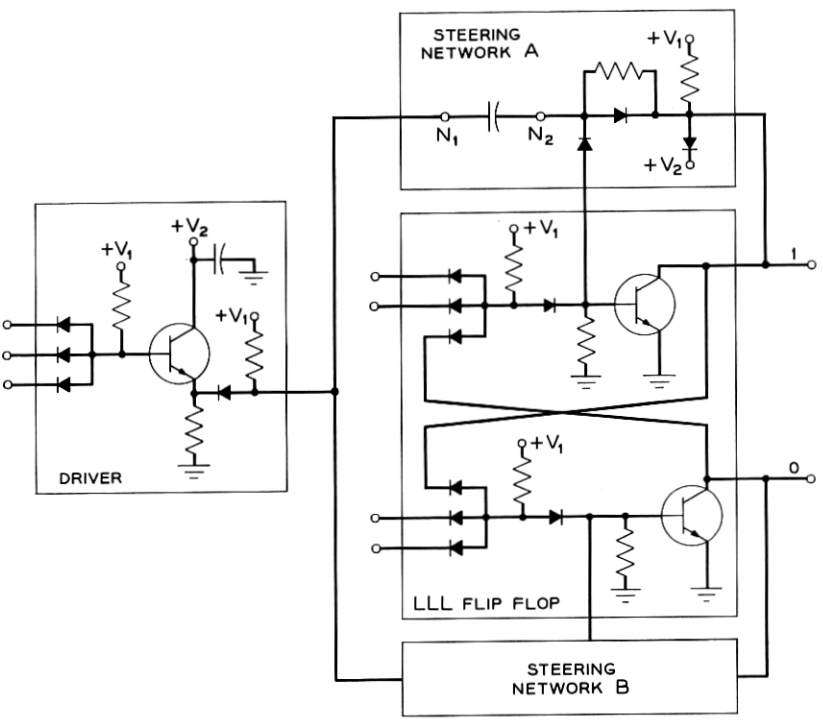


Fig. 12 — Binary counter.

special driving circuit have been added to obtain the nonracing binary counting action.

The design is such that if all inputs to the driver become high coincidently for longer than 0.25 microsecond, the flip-flop will reverse its state when any input returns to the low condition and remains there for at least 0.2 microsecond. In the steady-state condition, the N_2 points in the networks are at approximately the same potential as the output voltage of that side of the flip-flop to which they are connected (either +4.5 or approximately zero volt), while the other sides of the capacitors (points N_1) are near ground potential. When all driver inputs go high, the emitter follower drives the N_1 points to near +4.5v and the N_2 points remain at their original voltage levels. When the output of the driver goes low due to an input going low, the N_2 points attempt to drop by 4.5 volts. That N_2 which was originally at +4.5v will drop to near ground potential, while the other N_2 will go negative and forward bias the diode connected to the base of the transistor on its side of the flip-flop, turning it OFF. Since this transistor was originally ON, the flip-flop will change state. The N_2 points in both networks will return to the new output voltage states as the capacitors in the networks charge to their new voltage values. The next pulse from the driver will repeat the process, except that the opposite transistor will now be the one which turns OFF.

The shift register cell is almost identical to the binary counter, except that the two steering networks are driven by individual drivers which have one common shift control input. The two drivers have individual data inputs which are connected to the complementary outputs of the preceding stage in a multistage shift register. In this way only one driver output will be activated when the shift control input goes high and the cell will be forced into the original state of the preceding stage when the shift signal goes low.

The LLL gate has one other important application in No. 1 ESS. It is used (at a higher current level) as the basic cable pulser for the interframe bus communication system (see Fig. 13). The bus receiver circuits which are designed to drive standard LLL gates are also shown. This application is described in detail in a companion paper.[2]

VIII. LOGIC DESIGN IN THE CENTRAL CONTROL

8.1 *General*

By far the largest use of logic circuits in No. 1 ESS is made in the central control (see Fig. 14). Some feeling for the size and complexity

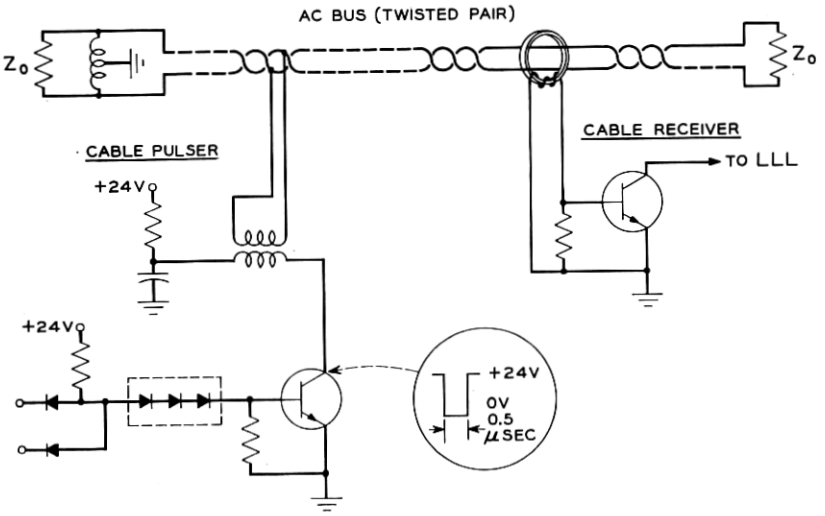


Fig. 13 — LLL gate used as a cable pulser.

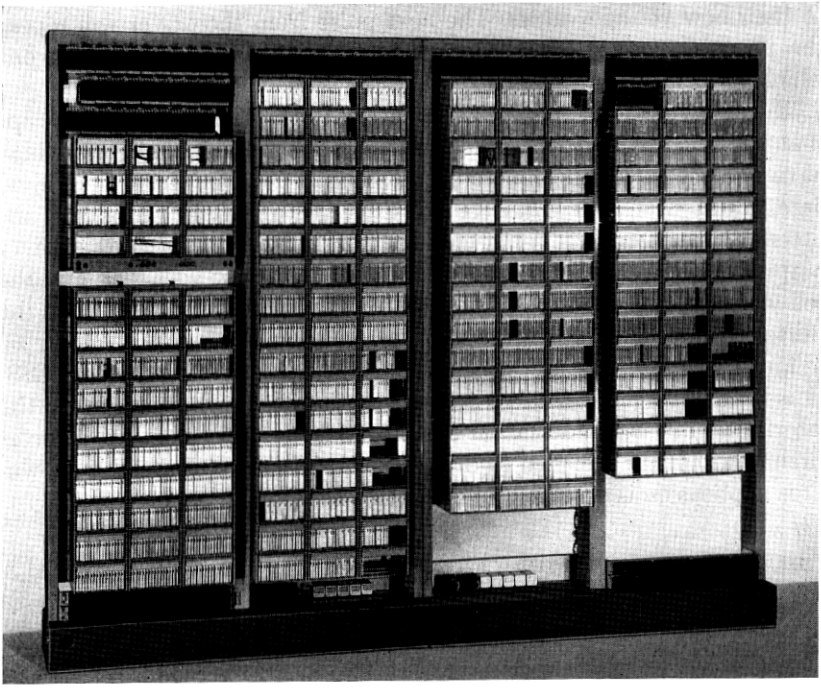


Fig. 14 — Front view of central control.

of the unit is found in the fact that the circuitry for a pair of duplicated CC's, while contained within about 5 per cent of the volume of a typical 10,000-line telephone office, contains about 50 per cent of the semiconductor devices. The statistics of Table V show the CC in perspective with the rest of the system.

Because of its size, it is impractical to discuss all of the details of the basic data processing circuits of the CC within the scope of this paper. The majority of circuits are used in translating program instructions, providing internal flip-flop registers between which data routinely shuttle, communicating with peripheral equipment, and performing routine maintenance checks. These circuits contain a high degree of design repetition and their implementation is fairly straightforward. Most of the real processing of data takes place in a small portion of the machine known as the "arithmetic system." The functions of this unit will be developed in detail, as an illustration of the over-all logic design and equipment layout techniques that have been employed.

8.2 *Arithmetic System*

In the process of completing telephone calls and diagnosing system troubles, the central control is called upon to manipulate both arithmetic quantities and logical quantities which are characterized in binary form. Arithmetic numbers contain 23 bits, labelled 0 to 22 in ascending order from the least significant at the right to the most significant at the left. Positive and negative numbers are permissible and are distinguished by the state of bit 22, the sign bit. Since the central control has a capacity of 23 bits, including the sign, the largest number therefore cannot exceed $2^{22} - 1$ ($= \pm 4{,}194{,}303$). For positive numbers, the sign bit is 0. Negative numbers are the "ones" complement of the equivalent positive value and contain a 1 in the sign bit. For example, $+1$ is 000 $\cdots$ 001, and -1 is 111 $\cdots$ 110. Both $+0$ (000 $\cdots$ 000) and -0 (111 $\cdots$ 111) can exist in this number system.

One of the chief constituents of the arithmetic system is a parallel

TABLE V — RELATIVE COMPLEXITY OF CENTRAL CONTROL

Item	No. of Items in Two CC's	% of Total	No. of Items in 10,000-Line No. 1 ESS
Circuit packs	4,716	37.0	12,600
Transistors	27,142	49.0	55,000
Diodes	89,934	54.0	160,000
Wire-wrapped connections	173,200	13.0	1,300,000
Equipment bays	8	5.0	147

binary adder circuit which generates the algebraic sum or difference of two or more 22-bit signed numbers in an interval of less than 1 microsecond. Addition is performed conventionally by summing corresponding bits of a number and combining them with carries that might have been generated in less significant bit positions. Subtraction is performed by the use of addition of complements with end-around carry. That is, the subtrahend is first complemented and then added to the minuend. A carry from the most significant bit sum is returned to be re-added to the lowest-order bits.

Another function of the arithmetic system is the ability to perform the purely logical functions of AND, OR, and EXCLUSIVE-OR upon two 23-bit quantities.

The arithmetic unit also has provision for shifting or rotating the positions of the bits of a binary word within a register. A shift register circuit is available which can move a word in either the right or left direction by any integral displacement of from 0 to 23 positions. A special mode rotates only 16 bits of the word, while leaving the others undisturbed. A complete shift cycle requires approximately 3.5 μsec.

8.2.1 *Block Diagram*

A simplified block diagram of the arithmetic system is shown in Fig. 15. The elements divide into two categories, namely, those concerned with the additive-type functions and those relating to rotational functions.

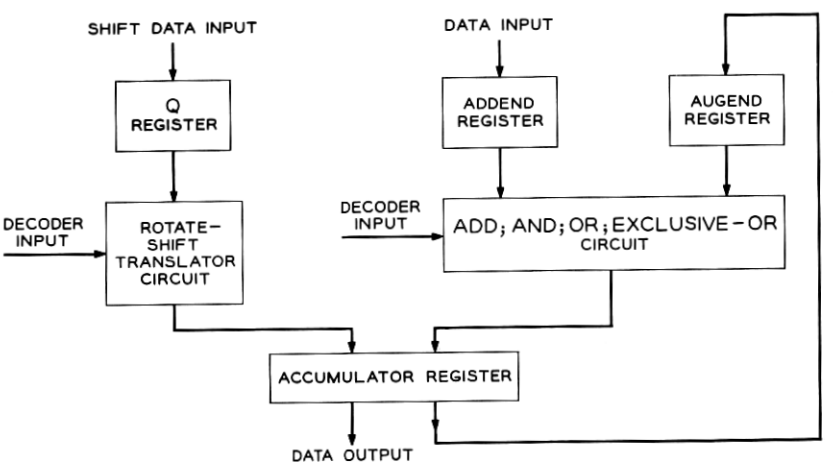


Fig. 15 — Block diagram of arithmetic system.

The circuit requirements for the additive functions are quite simple. Two flip-flop registers, the addend and augend, act as transient memories into which are inserted the incoming operands. The block labelled ADD, AND, OR, EXCLUSIVE-OR contains the logic to produce all of these functions. Finally, a register is required to hold the resultant. This is the accumulator.

The accumulator is constructed of LLL shift register circuit packs (Section 7.3) to provide greater flexibility than mere flip-flop memory. Steering networks associated with each side of the internal flip-flop allow tandem, race-free connections to other bits in the register. Upon command, the value of any bit in the register can be transferred to any other bit position to which it has been wired. The logic to interpret the shift-rotate commands and to translate the amount of displacement is contained in the rotate-shift translator. The Q register is a 6-bit flip-flop group which holds the shift-rotate translator data while the operation is taking place.

8.2.2 *Accumulator Input Registers*

The addend and augend registers consist of 23 LLL flip-flops with associated input gating. All new data are introduced into the arithmetic system by way of the addend register, which connects to the central control's main transmission artery — the masked bus. The augend register has two input options. It may be "reset" to zero by a signal from the order decoders, or it may be set up to the contents of the accumulator register. The latter path provides the ability to accumulate a sum by the process of repeatedly adding new numbers to the earlier totals. Since both input registers are connected to the adder circuit without gating, the adder continually monitors the sum of the register contents.

8.2.3 *Adder Circuit*

The inherent slowness of binary adders arises from the fact that "carries" which are generated in low-order bits create an appreciable delay by propagating serially toward the more significant bit positions. A complete sum cannot be available until all carries have been terminated. An adder circuit was developed which partially overcomes this problem and achieves the required speed without an unreasonable increase in circuit components. The circuit makes use of the group-carry concept, whereby all the carries within a prescribed group of bits are generated simultaneously and propagation is restricted to occur only between the adjacent groups.

When adding the corresponding bits of two binary numbers X and Y, a carry is obtained whenever both bits x_i and y_i are 1; or when either x_i or y_i is 1 in conjunction with a "carry in" from the adjacent lower-order bit. The relation can be expressed as:

$$C \text{ out} = X_i Y_i + (X_i + Y_i)C_{i-1} .$$

In order to take advantage of the inversion property of the LLL circuit, it is convenient to complement the expression to obtain

$$C' \text{ out} = X_i'Y_i' + (X_i' + Y_i')C_{i-1}'.$$

Now, the "carry out" from the ith position will be the "carry in" to $i + 1$, so that C_{i+1}' can be expressed as

$$C_{i+1}' = X_{i+1}'Y_{i+1}' + (X_{i+1}' + Y_{i+1}')C_o'.$$

Substituting the value of C_o and simplifying yield the product-of-sums expression:

$$C_{i+1} = (X_{i+1} + Y_{i+1})(X_i + Y_i + X_{i+1}Y_{i+1})(C_{i-1} + X_iY_i + X_{i+1}Y_{i+1}).$$

Let

$$A_i = X_i + Y_i$$

$$B_i = X_iY_i .$$

Then

$$C_{i+1} = A_{i+1}\,(A_i + B_{i+1})(C_{i-1} + B_i + B_{i+1}).$$

If the process is continued for successive carries, a general expression for the nth carry is obtained in terms of the input:

$$C_n = A_n\,(A_{n-1} + B_n)(A_{n-2} + B_{n-1} + B_n)(\cdots)\cdots$$

$$\cdots (A_2 + B_3 + \cdots + B_{n-1} + B_n)(C_{in}\,A_1 + B_1 + B_2 + \cdots + B_n).$$

The equation consists of n product-of-sum terms whose complexity increases in a pyramidal pattern. For example, the term $(A_1 + B_2)$ would appear as the second factor in generating the carry C_2. It re-appears, in union with B_3, as the third factor of C_3. This new factor, $(A_1 + B_2 + B_3)$, combines with B_4 as the fourth product of C_4, and so on. Each product term in every carry expression follows a similar growth pattern. These combinations are suited to LLL circuitry in that the highly repetitive B terms need only be generated once and can be combined successively (within fan-out limitations) to form a series of carry outputs.

Although any number of carries can be generated simultaneously in a two-stage logic circuit by implementing the above equations, the number of LLL gates required quickly becomes excessive when more than about 15 carries are generated. The curve of Fig. 16 summarizes the circuit requirements for multibit adders of any size up to 25 bits. It is useful in predicting the circuit complexity for tandem arrangements of carry groups to obtain a desired addition speed. The curve is divided into two areas. The portion with the larger delay occurs for group sizes greater than 11 carries and is occasioned by the fact that an extra logic stage is necessary to satisfy the fan-out limitations of the LLL circuit. The minimum delay of four logic stages includes the two stages for addition in the sum circuit, and applies to the first group of a tandem arrangement only, since the carries in adjacent groups are completed concurrently with the preceding sum. Therefore, each subsequent carry group after the first contributes only two delays to the total addition time. On this basis, an adder with two group carries requires six delays, one with three groups requires eight delays, etc.

Fig. 17 compares the circuit component requirements with the delay for several possible 23-bit end-around carry adders. Point A on the curve indicates that approximately 800 LLL gates are needed to design a circuit which generates all bits simultaneously and produces a sum in 5 stages of delay, ≈300 nsec. At the other extreme, point D describes the conditions of a quasiparallel adder where the carry propagates on a bit-by-bit basis. B shows the condition for which the carries are divided

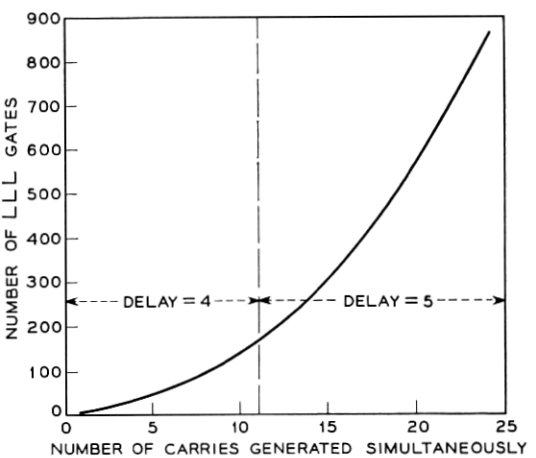


Fig. 16 — LLL circuit requirements for parallel carry adders.

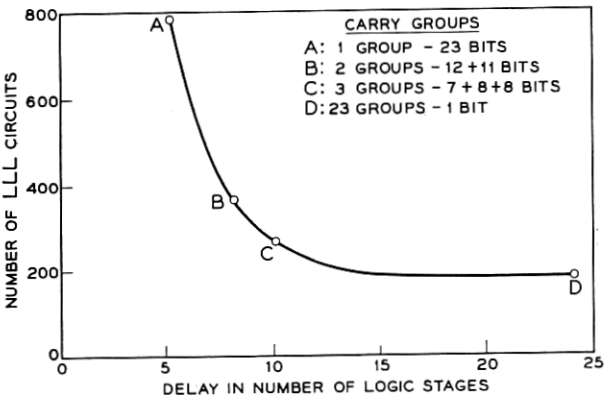


Fig. 17 — Circuit requirements and delay of 23-bit adders.

into groups of 11 and 12 bits, and indicates better than 2:1 savings in equipment over the circuit in A at the cost of ≈200 nsec. Point C defines the central control adder. It requires 270 LLLs and has a delay of 650 nsec, determined on the basis of 65-nsec worst-case transistor switching speed.

The block diagram of Fig. 18 shows the adder circuit used in the central control. For maximum economy in satisfying the speed requirements, the carry circuit is divided into three groups: one produces

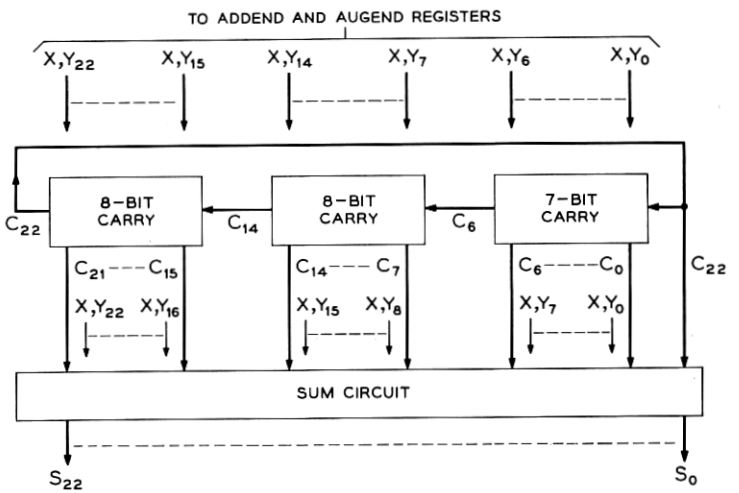


Fig. 18 — Block diagram of adder.

simultaneous carry outputs from seven bits, the other two groups from eight bits apiece. A single carry propagates from one group to the next in tandem, with the third group rejoined to the first in order to provide the end-around-carry connection. With each group after the first contributing the delay of two logic stages, and an added two stages of delay caused by the end-around-carry provision, the maximum propagation time is that of ten stages or, at worst, 650 nsec. Maximum propagation delay occurs when a carry terminates in the same group from which it had originated, after having propagated through the other groups. The addition of $+1$, $(00 \cdots 01)$, to -0, $(11 \cdots 11)$, is an example where the initial carry in the least significant bit causes a carry to ripple through all succeeding bits, until the end-around connection returns it to the origin where it terminates. The correct result is, of course, $00 \cdots 01$, or $+1$.

The end-around-carry connection between carry groups constitutes a feedback loop which can give rise to oscillation when two binary numbers, one of which is the exact complement of the other, are to be added. The problem exists because the carry circuit reflects the momentary conditions of its input registers at all times. The closed loop constitutes a delay line which can inject a remembered carry indication at the exact moment when a register is changing state. Normally, the circuit stabilizes when the register state has settled down due to the further generation of new carry terms, but when the numbers are complementary, no carries are initiated and the remembered carry could continually circulate or at least introduce an error. This problem is eliminated by inhibiting all carries (opening the feedback loop), during the transition period of either of the input registers.

The sum circuit combines the carries with the operand bits in the two-stage logic circuit shown in Fig. 19. The first stage of the circuit combines the inputs in four LLL gates as a sum-of-products which when inverted yields:

$$\text{SUM}' = X_iY_i'C_{i-1} + X_i'Y_iC_{i-1} + X_iY_iC_{i-1}' + X_i'Y_i'C_{i-1}'.$$

The output of this stage remains at the common-collector potential ($+4.5$ v) when at least one input to every product term is at ground potential. Logically, the equation states that the sum is 0 whenever any two of the operand bits or the input carry are both equal to 1, or when all three are zero coincidently.

An inverter amplifier stage is used to make the complementary sum output available to the connecting logic.

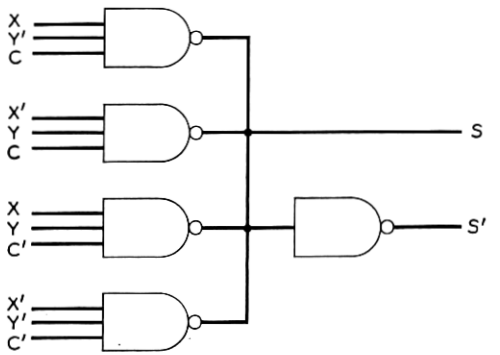


Fig. 19 — Logic diagram of sum circuit.

8.2.4 *Special Logic Functions*

The sum circuit logic contains each of the four possible combinations of the input variables X and Y in product with a carry term or its complement. By forcing the carry terms to become high ($C = C' = 1$), the equation for the sum degenerates to

$$\text{OUTPUT}' = X_iY_i' + X_i'Y_i + X_iY_i + X_i'Y_i'.$$

When appropriate control functions are introduced into each product term, the result can be expressed as

$$F' = f_1X_iY_i' + f_2X_i'Y_i + f_3X_iY_i + f_4X_i'Y_i'.$$

This is the familiar expansion of two variables; it can generate any of the sixteen functions of X and Y, depending on the values assigned to the control functions.

Control inputs were added to the LLLs in the sum circuit to generate the logical combinations required in the CC. The condition that $C = C' = 1$ was satisfied by grounding inputs to the appropriate logic packages in the carry circuit. Fig. 20 shows the sum circuit with the control inputs to generate logical AND, OR, and EXCLUSIVE-OR. None of the functions here required the condition of $f_4 = 0$; therefore it was not provided. To obtain a high output when performing the AND operation, we let $f_3 = 0$. Then

$$F'_{XY} = f_1XY' + f_2X'Y + X'Y'.$$

When $f_1 = f_2 = f_3 = 0$:

$$F'_{(X+Y)} = X'Y'$$

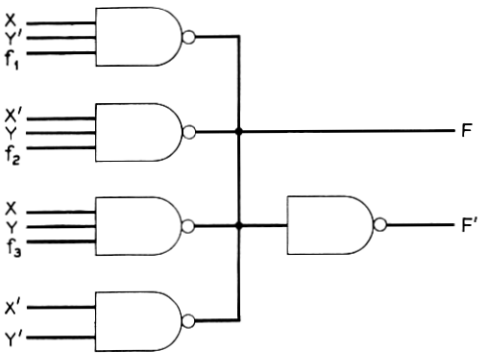


Fig. 20 — Modification of sum circuit to generate special logic functions.

which is high only when the bits satisfy OR logic. Finally, to obtain EXCLUSIVE-OR, let

$$f_1 = f_2 = 0:$$

$$F'_{(X \oplus Y)} = f_3 XY + X'Y'$$

which is accordingly high for $XY' + X'Y$ as required.

Since the carry circuit is inoperative when forming the logical combinations, the delay time is merely that of the two-stage sum circuit or 130 nsec maximum.

8.2.5 *Shift-Rotate Functions*

When manipulating data in the central control, it frequently happens that particular bits of information are not located in the bit positions that are most convenient to use. This commonly comes about, for example, when several small data words are packed together into adjacent bits of a larger memory word. Product masking is effective in isolating the desired data word from the rest of the group, but does not affect the relative bit positions. To provide the ability to relocate all bits of a word in some specified manner, shift register features have been designed into the accumulator.

The two basic types of operation in the accumulator register are rotation and shifting. Full rotation indicates a displacement of the 23 bits of a word by any instructed amount from 0 to 23 positions. Those bits which pass through one end of the shift register are reinserted into the other end so that no information is erased in the process. A modified,

form of rotation is confined to be effective only within a selected group of sixteen bits. In both cases, the rotation can be specified to be in either a left or right direction. Shifting is also a displacement of all 23 bits in either direction, but here the bits are forced out of the end of the register and the vacated spaces at the opposite end are replaced with zeros.

The accumulator is activated by synchronous commands from the rotate-shift translator, which receives the basic instruction from the order word decoder and a 6-bit descriptive word from the Q register. The five least significant bits of this word are the binary equivalent of the amount of displacement; the sixth, the sign bit, determines the direction of motion. When the sign is 0 (plus), motion is to the left; when it is 1 (minus), motion is to the right. In the latter case, the accompanying five bits are in complement notation and signify a negative number. To obtain the true displacement of a negative quantity, the rotate-shift translator must recomplement these five bits.

The program instruction itself can also specify that the shift or rotation take place in complemented form. That is, under the influence of a "shift complemented" instruction, not only will the magnitude of the displacement be complemented, as in the case for negative numbers, but the direction of the motion will also be reversed. Table VI summarizes the various forms of motion which are obtained.

8.2.6 *Derivation of Shift Mechanism*

Only 4.0 microseconds may be allotted to the shifting operation, so that the output of the accumulator can be available for some other operation in the cycle following the shift instruction. This interval includes the time absorbed in receiving and translating the instruction and the description of motion, as well as that allowed for the mechanics of shifting and register settling. Conventional series shift registers, in

TABLE VI — TRANSLATION OF SHIFT-ROTATE INSTRUCTIONS

Instruction in Order Word Decoder	Q Register Shift Code		Bit Motion in Accumulator
	Sign Bit	Magnitude	
Shift	0	00001	1 pos. to left
Rotate	1	11110	1 pos. to right
Rotate 16 bits only			
Shift complement	0	00001	1 pos. to right
Rotate complement	1	11110	1 pos. to left
Rotate 16 complement			

which a single position shift of all bits is triggered by successive clock pulses, were thereby ruled out. Instead, a semiparallel operation was used which allows all bits to be relocated by discrete groups. This reduces the number of shift operations.

Shifts involving any number of positions, within the 23-bit capacity of the accumulator, can be formed by successively adding together any three of the integers 0, 1, 4, 7, and 8, if we include the possibility of using an integer repeatedly. For example: $19 = 4 + 7 + 8$; $9 = 7 + 1 + 1$, or $9 = 8 + 1 + 0$; $3 = 1 + 1 + 1$; and so on. Based on shift groups of these values, all accumulator movements are realized as a combination of, at most, three jumps. The 0 group is trivial, of course, since it requires no shifting action.

After determining the direction of motion and performing any resultant complementation, the shift circuit translates the binary magnitude of the remaining five bits and sorts the results into the four categories. Each bit in the accumulator shift register is connected to its neighbors on both sides which are 1, 4, 7, and 8 positions away. Fig. 21 is a sketch of the bit positions of the accumulator showing the shift register connections for bits 10 and 17. Each bit provides an input to eight other positions, four on each side, to allow bidirectional motion. Bit 17 illustrates the circular nature of the rotation process, whereby a left rotation of 7 positions causes bit 1 to assume the value of bit 17. All bits of the register would be connected similarly for the shift orders and 23-bit rotation orders.

Further interconnections are required for the 16-bit rotation instructions that confine the rotation process to the particular 16 bits between positions 6 and 21. As shown in Fig. 22, a left rotation of 7 positions from bit 17 in this mode requires a connection to bit 8. Similarly, bit 10 is connected to bit 19 as well as to its other destinations. Double connections are shown between bits 10 and 18, and bits 17 and 9, to indicate that these destinations are equidistant from the source bits in

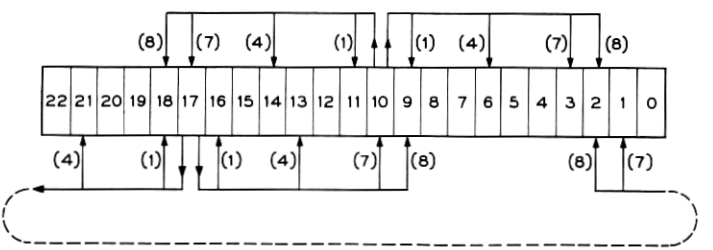


Fig. 21 — Interconnection of accumulator bits for rotate-shift functions.

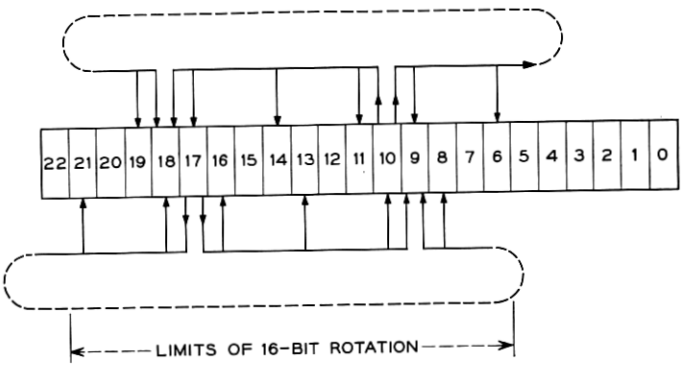


Fig. 22 — Bit interconnections for 16-bit rotation mode.

both directions. Bit 18, for example, assumes the state of bit 10 either in response to the instruction "shift (or rotate) all bits 8 positions to the left," or in response to "rotate 16 bits a distance of 8 positions to the right." These and similar patterns for other bits are redundant entry conditions and have been logically simplified in the final design.

Both the translated shift description and the bit interconnection logic are assembled in the final stages of the shift-rotate circuit. The results are combined with the three required clock pulses to trigger the synchronous operation of the shift register. Fig. 23 is a timing diagram illustrating the sequence of events which occur as a result of a shift or rotate instruction. During the initial 0.75-μsec interval, the instruction is recorded and the Q register is loaded with the 6-bit word that defines the direction and amount of shift that is to be applied to the binary word in the accumulator. Suppose that a shift instruction had been given, specifying that all accumulator bits be displaced 13 positions to the left. In binary form, the 6-bit description is 001101,

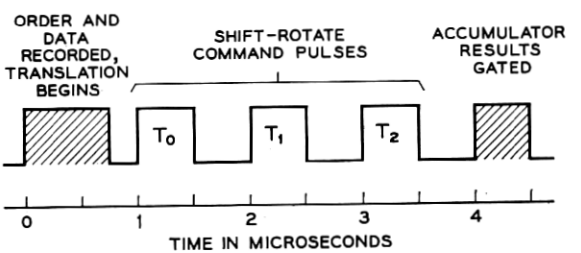


Fig. 23 — Timing diagram for shift register.

where the most significant bit signifies that motion is to be to the left. The shift translator decomposes the binary code into commands of jumps of 1, 4, and 8 positions. The first clock pulse of the chain, T_0, combines with the "shift 1" command, and the circuits in the accumulator prepare to respond. Activity commences on the downward swing of the T_0 pulse, causing all bits to move simultaneously one position to the left. At the same time, a 0 is inserted into bit 0. The ensuing 0.5 μsec interval allows the shift register stages adequate time to settle down in their new states. T_1 is combined with the "shift 8" signal. At its conclusion, all bits move 8 positions to the left, with 0's being inserted into the vacated spaces at the right. Finally, T_2 combines with "shift 4" to complete the action. Within 0.5 μsec after T_2, the new accumulator contents are gated out and the register is available for other use.

Table VII shows the translation of the shift magnitude from binary to the 1, 4, 7, 8 code and indicates the interval when each jump occurs. There are several limiting conditions which have not been previously

TABLE VII — TRANSLATION CODE FOR SHIFT-ROTATE

Shift-Rotate Code	Displacement	Jumps/Unit Time		
		T_0	T_1	T_2
0 0 0 0 0	0	0	0	0
0 0 0 0 1	1	1	0	0
0 0 0 1 0	2	1	1	0
0 0 0 1 1	3	1	1	1
0 0 1 0 0	4	0	0	4
0 0 1 0 1	5	1	0	4
0 0 1 1 0	6	1	1	4
0 0 1 1 1	7	0	0	7
0 1 0 0 0	8	0	8	0
0 1 0 0 1	9	1	8	0
0 1 0 1 0	10	1	1	8
0 1 0 1 1	11	0	7	4
0 1 1 0 0	12	0	8	4
0 1 1 0 1	13	1	8	4
0 1 1 1 0	14	0	7	7
0 1 1 1 1	15	0	8	7
1 0 0 0 0	16	8	8	0
1 0 0 0 1	17	8	8	1
1 0 0 1 0	18	7	7	4
1 0 0 1 1	19	7	8	4
1 0 1 0 0	20	8	8	4
1 0 1 0 1	21	7	7	7
1 0 1 1 0	22	7	7	8
1 0 1 1 1	23	8*	8*	8*
1 1 0 0 0	None			

* Results in resetting accumulator on shift instruction. No action on rotate instruction.

discussed. When either 0 displacement or a magnitude greater than 23 is specified, the shift-rotate mechanism is inhibited. An exception is the 16-bit rotation instruction, which rotates the bits "modulo 16," i.e., $n - 16$ positions.

IX. EQUIPMENT DESIGN

9.1 *General*

Apparatus counts based on early block diagrams showed that the central control would be so large as to require precise control of logic circuit locations and their interconnections. With these concerns in mind a "breadboard" version of the central control's arithmetic system was built and tested. This unit, dubbed SPADE (Stored Program Arithmetic Digital Exerciser), contained wired LLL circuit packs tailored to meet many different combinational patterns and utilized point-to-point wiring between connector terminals.

SPADE provided the testing ground for prototype semiconductors, LLL combinational patterns, and many system concepts. The four-bay central control reflects the circuit pack designs, wiring patterns, and logic pack arrangements resulting from these early studies.

9.2 *LLL Circuit Packs*

Plug-in circuit packs[8] to accommodate the various combinations of gates, flip-flops, etc., were designed to allow rapid isolation and replacement of suspect components, thereby facilitating system maintenance. The design approach was to provide accommodations for various quantities of separate, independently accessed LLL gates on specific packs. Logic combinations are formed by interconnecting suitable gates at the plug-in connector terminals. This approach is in contrast to that of designing a large variety of low-usage packs in which the gates are internally wired to generate specialized functions.

To achieve high density, it is important to place as many logic gates as possible on a circuit pack and to use them with the greatest efficiency. The controlling variables in the design are the circuit pack area and the number of connector terminals available (28). With these limitations, the most densely packed logic element contains eight two-input gates. This pack, shown with its apparatus mounting in Fig. 24, has the largest usage in a No. 1 ESS office. Table VIII contains a listing of other LLL-type circuit packs used in the system, predominantly in the central control.

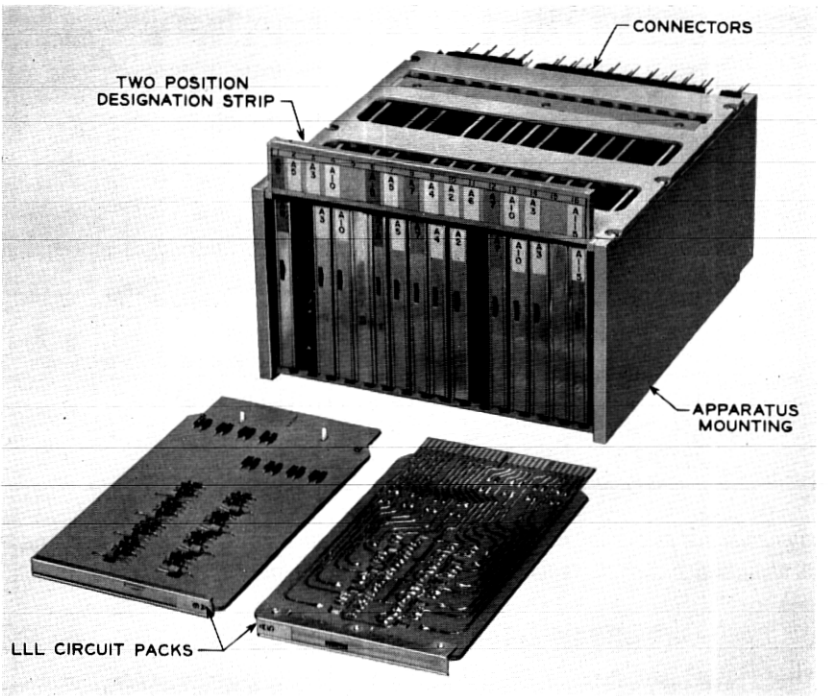


Fig. 24 — LLL circuit pack and mounting.

A measure of the success of logic circuit standardization is best illustrated by the fact that sixteen logic circuit packs, making up about 10 per cent of the entire No. 1 ESS catalog, account for more than 50 per cent of the packages and 70 per cent of the semiconductors used in a typical office. In the No. 1 ESS office at Succasunna, New Jersey, 6,675 of these sixteen types are required, the duplicated central controls alone accounting for 4,036.

Previous sections have pointed out that LLL gate outputs can be connected together (with certain restrictions) to form a common driving AND node. When this is done, a single dummy load resistor (Section 4.4) is sufficient to maintain the proper operating conditions for the combined circuits. To facilitate this use, the resistors are omitted from the logic packs and are assigned instead to resistor packs. These contain twenty-four separate collector resistors commonly connected to the +4.5-v collector source. A single LLL gate then receives its base drive through its own internal base resistor supplied from a common +24-v

TABLE VIII — LLL-TYPE CIRCUIT PACKS

Code		Description
A1	2	9-input LLL gates
A2	3	7-input LLL gates
A3	4	5-input LLL gates
A4	6	3-input LLL gates
A5	8	1-input LLL gates
A6	8	2-input LLL gates
A15	8	1-input LLL gates (individual power connections)
A7	8	1-input high fan-out LLL gates
A8	8	2-input high fan-out LLL gates
A11	1	binary counter stage
A13	2	flip-flops with input gating
A14	1	shift register stage
A18	8	high-sensitivity bus receivers
A19	8	bus receiver amplifiers
A21	8	bus driver transformers
A177	8	bus driver LLL gates

power terminal on the connector and its +4.5-v collector source through an assigned external resistor at the collector output terminal.

9.3 *Circuit Pack Interconnection Practices*

The interconnection of logic gates to generate a circuit function is dependent upon the over-all circuit organization and the diagnostic and maintenance techniques which are applied in its operation.

Because of its word-organized design, faults and errors in a CC are most easily diagnosed to the troublesome bit position in a word. It seems only natural, then, that as many logic gates as possible associated with the same bit of a word be assigned to the same circuit pack. In effect, this approach to logic gate assignment keeps to a minimum the number of circuit packs which must be tested to isolate a particular fault. Unfortunately, assigning logic gates to circuit packs on a word-bit basis is often incompatible with the approach which assigns logic gates on the basis of achieving high circuit pack density. As a result, it is often necessary to compromise and to assign two or more bits to the same circuit pack.

Output leads from flip-flops, binary counters, and shift registers are critical because of their internal cross-connections to inputs; therefore the total wire length is restricted to a maximum of three feet. To some degree, this requirement also affects the assignment of logic gates to circuit packs. The following are examples of circuit pack assignment practices as applied to the central control.

Fig. 25(a) shows a common-collector configuration where all logic

gates can be assigned to the same circuit pack if no input lead from a register exceeds three feet.

Fig. 25(b) shows a common-collector configuration where all logic gates are not assigned to the same circuit pack. These logic gates are assigned to three different circuit packs as follows: one 7-input logic gate to an A2 circuit pack, three 5-input logic gates to an A3 circuit pack, three 3-input and two 2-input logic gates to one A4 circuit pack. In this case, the 3-input circuit pack is used where the circuit logic requires 2-input gates. Had the 2-input gates been assigned to an A6 pack, four types of circuit packs would have been required for this word bit, rather than three.

9.4 *Frame Wiring Methods*

During the brassboard development stage it became evident that the shop and field wiring practices of relay switching systems could not be

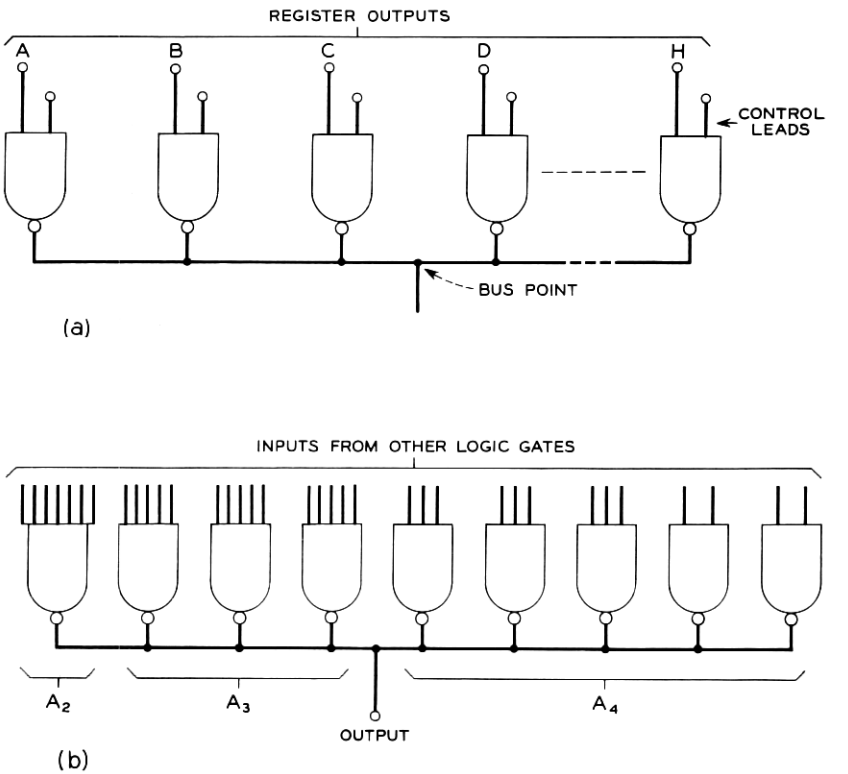


Fig. 25 — Common-collector configurations.

used for the high-speed pulse circuit wiring of central control. The lengths and parallel spacings of signal wires had to be controlled to minimize electrical interference (crosstalk) between circuits. This resulted in circuit pack placement restrictions and the development of new wiring methods suitable for this type of equipment.

Where high densities of circuit packs and wired interconnections exist, special wiring procedures are employed which dictate specific routings for surface wiring, loose wiring, and local cables. This eliminates the shop wiring variability that could appear in surface wiring by different operators.

The individual mounting plates are first surface-wired in the shop and verified with a dc test. The associated mounting plates of a unit are next surface-wired together. The loose wiring support details are then mounted on the units, and the units in turn installed on the bay or frame. A preformed loose wiring harness is mounted on the support details and the leads are terminated.

The loose wiring support details are epoxy-coated metal combs and fingers which are grounded to the mounting plate via their mounting screws. These provide an extension of the ground plane to minimize inductive coupling between the loose wire signal paths. The high wiring density shown in Fig. 26 requires the use of no. 26 gauge wire.

An analysis of the CC wiring disclosed the following distribution on the four-bay frame:

(a) surface wiring per mounting plate (average): 450 wires between connectors on the same plate, and 100 wires between connectors on different mounting plates of the same unit

(b) loose wiring per mounting plate: 50 wires between connectors on different units.

(c) local cable wiring per mounting plate: four wires to fuse panel

(d) interframe loose wires between bays 1 and 2: 750 wires.

Approximately 43,300 wires or 86,600 wrapped connections are required within the four bays.

9.5 *Grounding Techniques*

Because of the rather small voltage swings necessary to control the transistor circuits, and the speed with which they react, the grounding technique is very important. A very low impedance (inductance) ground plane is required to prevent excessive noise voltages (a few tenths of a volt) from being generated by the high-speed switching circuits in the CC. For this reason, the equipment frame is utilized as

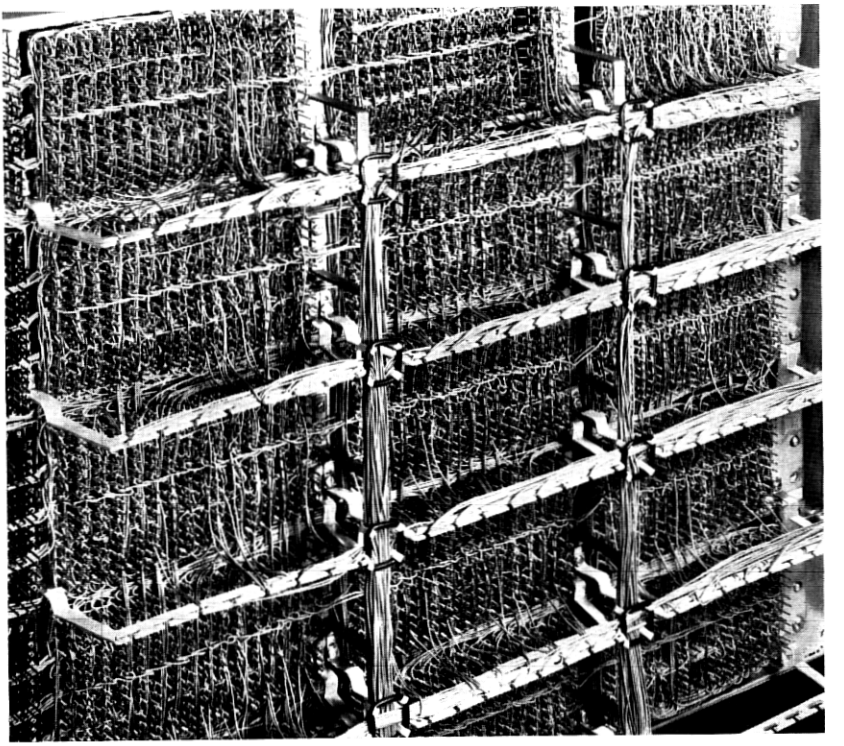


Fig. 26 — Photograph of central control wiring.

a circuit ground. A ground terminal intimately connected to the frame is located immediately below each circuit pack. Each circuit pack has its circuit ground tied into frame ground with a wire approximately three inches in length. These precautions have reduced the ground noise internally generated in the CC to a level where it is not a problem. The power and grounding arrangements in the system are relied upon to keep extraneous circulating currents from creating disturbing voltage drops in the framework.

X. SUMMARY

The design of the central control has been discussed in terms of its influence upon the design of building block logic circuits and their utilization in performing some of the specialized functions which are carried out in the process of controlling a telephone switching system. The complexity of the unit made a detailed description of each internal

circuit beyond the scope of this paper; therefore many features have had to be omitted.

The emphasis for reliability has been perhaps the most important factor dictating all CC design decisions. A major part of the circuit and equipment design effort was directed toward enhancing dependability by prescribing inherently reliable circuits, components, and equipment. The logic circuit design provides standardized but versatile building blocks with fast, low cost performance. Over 10^9 LLL gate hours have been logged during the No. 1 ESS preoperational phase. The failure rates during this phase are, as might be expected, higher than will be experienced when installation troubleshooting is completed. Based on current reliability predictions, about one component failure per operating month is anticipated in each CC. Because of the internal fault recognition and self-diagnostic maintenance features of the system, along with the provision for rapid repair by circuit pack replacement, this failure level is sufficiently low to insure the requisite system dependability.

XI. ACKNOWLEDGMENTS

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