No. 1 ESS Program Store

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Line and trunk translation data and operating programs for No. 1 ESS are stored in a large semipermanent memory. This memory is provided by modular units known as program stores. Each program store provides 5.8 million bits of randomly accessible permanent magnet twistor memory organized into 131,072 parallel words. The information is stored in the state of small magnets affixed to aluminum cards. Each card contains 64 forty-four-bit words.

Each store is designed to operate over a duplicated common bus system for both normal and diagnostic operations. The stores have a cycle time of 5.5 μsec. Such stores are an attractive and economical solution to the problem of providing large storage capacity for information which must be protected against accidental change.

To provide an efficient and routine method for updating the information content of such stores, offices are provided with card writing equipment. This includes both card handling equipment and card magnetizing equipment under system control.

I. GENERAL

1.1 *Storage Requirements*

No. 1 ESS is under control of a very large program. The complete program may require a storage capacity in excess of 4 million bits. In addition, the office must store a considerable amount of data about each line and trunk. Such data as directory number, class of service, special feature lists, etc. must be available internally to the system. The storage needs for these items are variable with office size and range from 1 to 14 million bits. This program and translation information together constitute (a) the knowledge necessary to perform the telephone switching function and (b) the memory of the service commitment to each customer. To ensure service continuity this information must be

protected from accidental destruction by either equipment malfunction or operator error.

The system must have direct and immediate access to all of the information. However, it will be noted that the system does not require the direct capability of altering the information. This is because the information and its changes are generated externally to the system, as by a program designer or the telephone business office. What is required is a suitable way of introducing the information changes into the system.

To meet this need of an economical, high-capacity, random-access memory, No. 1 ESS uses permanent magnet twistor modules as basic storage elements. These provide a memory that is fundamentally "read-only" while at the same time providing a simple and straightforward way of replacing old information with new. As desired, no electrical malfunction can alter the information content.

1.2 *Store Objectives*

Twistor modules, with their circuitry, form an ESS unit designated a "program store." The general objectives set for the development of program stores are given in Table I. The word size of 44 bits allows 37 bits of information and 7 bits of redundant encoding.[1] The high-reliability requirement, coupled with past experience in the Morris, Illinois, ESS trial, indicated strongly the desirability of high redundancy in program information. The coding used includes a Hamming single error correcting code plus an over-all parity, both taken over the data and its storage address. While with equipment operating normally this much redundancy may seem extravagant, the ability to operate under serious degradation of circuit or memory, as well as the enhanced ability to detect and isolate malfunction, is felt to more than repay the cost.

The capacity of 131,000 words represents the basic storage needs of a small office. It was felt that this size also represented about the largest size that could be achieved with common-access circuits. The cycle time of 5.5 μsec was essentially determined by the over-all system,

TABLE I — ESS PROGRAM STORE OBJECTIVES

Word size	44 bits
Capacity	131,000 words
Speed	5.5 μsec
Cost	low
Reliability	high
Maintenance	automatic
Power	battery
Environment	non-air-conditioned

including the twistor modules, but did not represent an attempt to build the fastest store possible. Low cost is of course an inherent objective; an over-all economic balance in the system dictated the need to achieve a cost per bit of the order of one-fifth that of the system's variable memory.

Programmed fault diagnosis is an essential feature of an ESS. In the case of a program store, the interaction between the fault and the fault-detection program can be especially severe. This requires that advance planning and coordination between the circuit, system, and programming engineers be especially effective.

The requirements of battery power and non-air-conditioned space are office-wide. They provide somewhat more of a challenge in the case of the program and call stores, where temperature-sensitive devices and nondigital circuits occur.

The over-all objectives, at the time they were established, represented a goal that would require significant device and circuit development. This article reports the successful attainment of that goal.

1.3 *Devices*

1.3.1 *Semiconductors*

As in the remainder of the system, in digital or low-level applications the store used the single code of transistor developed for No. 1 ESS. However, it was clear at the outset that a fast, higher-powered transistor and companion diode would be required for program store access. For this purpose the 20D transistor and 426AC diode were developed. The 20D transistor, which can handle 1.35 amps with $\frac{1}{3}$-μsec switching times and a breakdown voltage of 50 volts, also proved a suitable transistor for other fast, high-power needs of the system.

1.3.2 *Twistor Modules*

The permanent magnet twistor memory has been previously reported.[2,3,4,5] The twistor modules used in ESS were a further development of the module described in Ref. 4. The front and rear views of a module are shown in Fig. 1. On the rear is a 64 × 64 biased-core switch matrix. A particular core is switched by the combined action of a horizontal and vertical half-select current overcoming a common bias current. Each core is coupled to a strip solenoid referred to as a "word solenoid" (see Fig. 2). The word solenoids are attached to the surface of an insulating board over which have been placed thin sheets of permal-

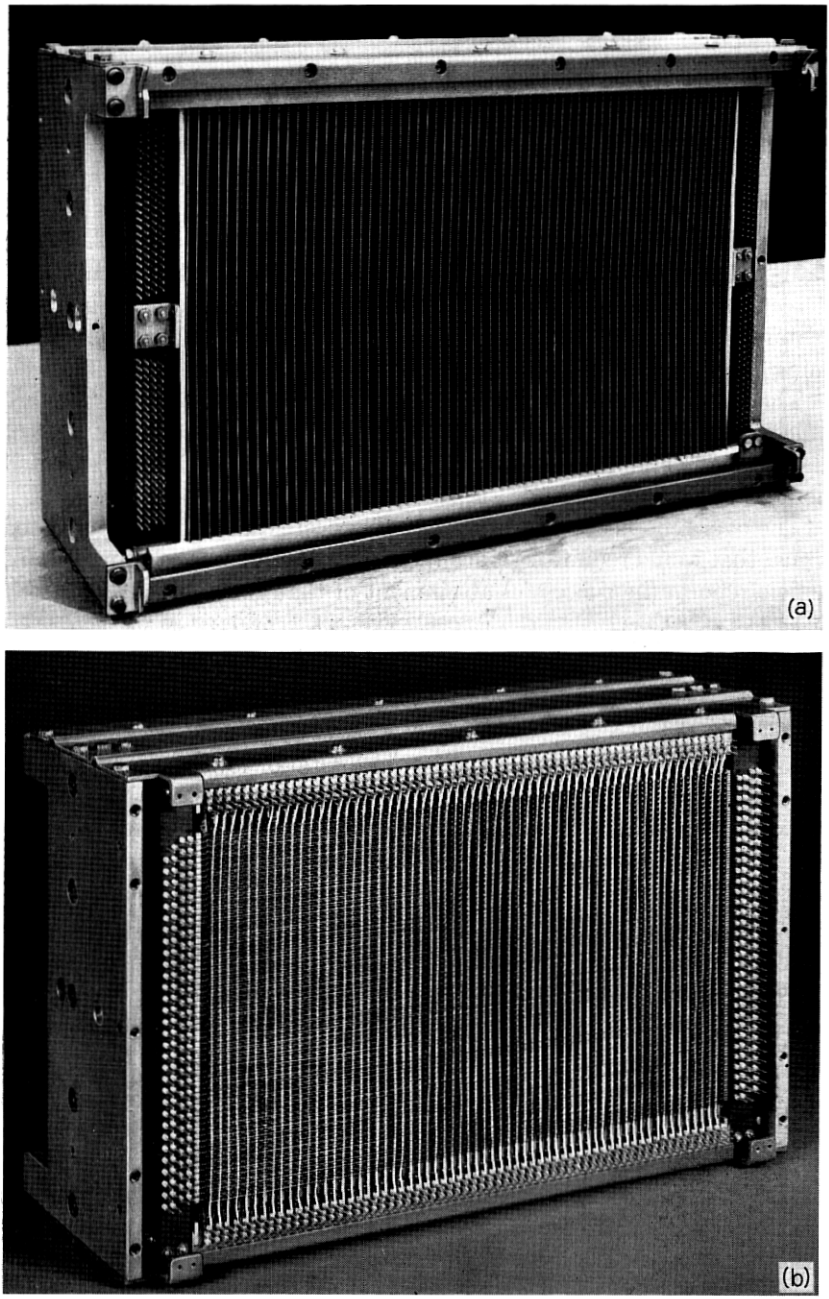


Fig. 1 — (a) Front (card insertion side) of a 1A twistor memory; (b) rear (core access side) of memory.

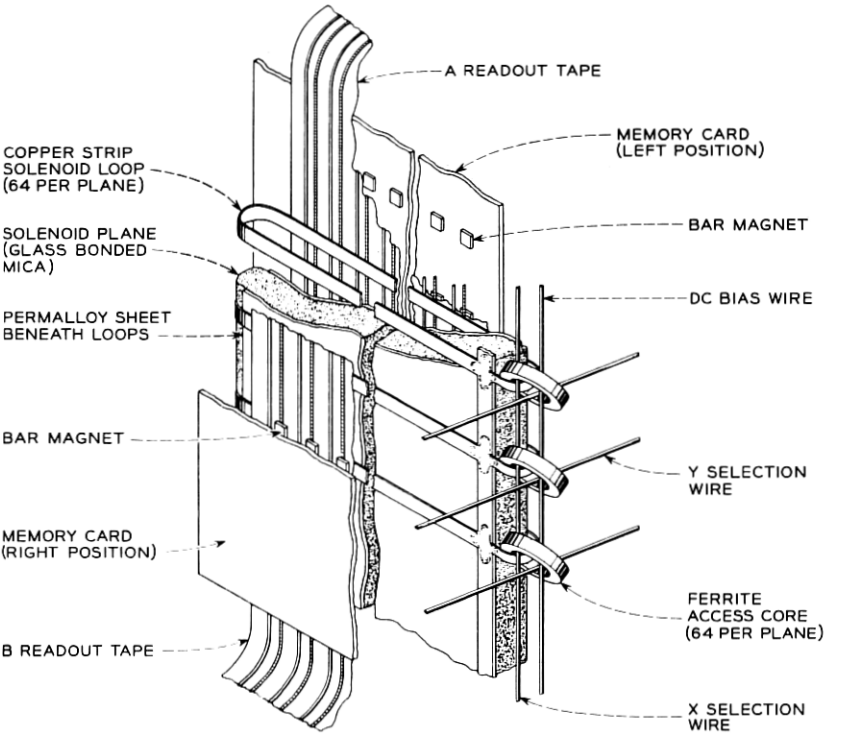


Fig. 2 — Cutaway schematic showing the basic elements of permanent magnet twistor memory.

loy. Each module contains 64 boards, each with 64 solenoids. Through the module, accordion fashion, run two flat plastic belts, each containing 44 twistor wires and 44 adjacent return wires. A section of each tape is cemented to one side of each board. Each of the modules provides space for 128 magnet cards, one of which is shown in Fig. 3. Each aluminum card carries 64 columns of 45 thin permanent magnets. Each column represents a word and each of the first 44 magnets, a bit of the word. (The 45th row is not used in this application.) When magnetized, each magnet represents a stored "zero." A demagnetized magnet represents a stored "one." When all cards are in place in the module, a magnet appears over each intersection of a twistor wire and word solenoid. If the magnet is magnetized, it fully saturates a region of the twistor wire beneath it. The magnets are always magnetized in the same direction as the initial field of the word solenoid.

When an individual word solenoid is selected by applying a half-

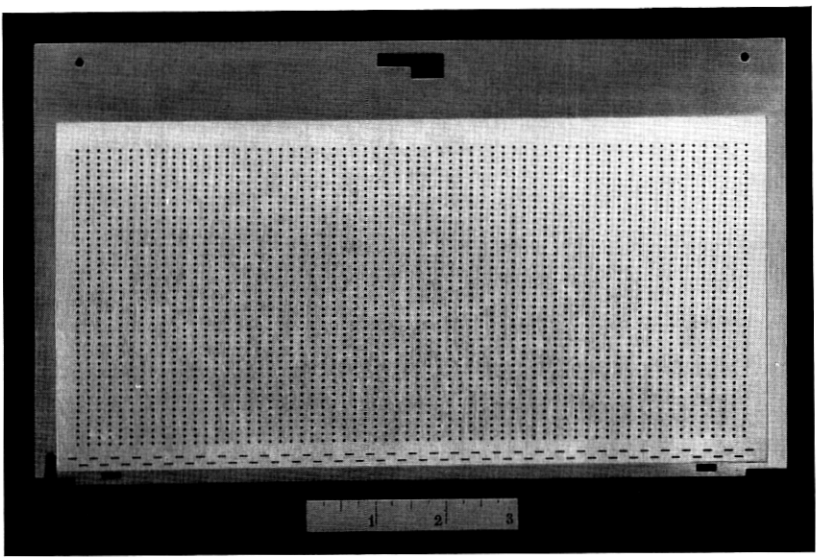


Fig. 3 — Twistor memory card.

select current to individual horizontal and vertical access wires, a current pulse is induced in the word solenoid. The resulting magnetic field acts on the twistor wire. Because of the orthogonal geometry no significant voltage is induced in the wire unless the magnetic material of the twistor wire is switched. This can occur only at the sites containing nonmagnetized magnets. When the half-select currents are removed, the common bias current switches the selected access core back to its initial state. The resulting word solenoid pulse restores initial twistor wire conditions.

It will be seen that the selection of a single word solenoid causes a readout of 88 bits. Within the readout circuits, it is thus necessary to select the 44 bits associated with the desired magnet card.

For uniform outputs from the memory, the magnetic field applied to the twistor wire should completely switch its magnetic material. In these modules the magnetic field produced by the solenoid is concentrated onto the twistor wire by two mechanisms. The first is the underlying permalloy sheet, which provides a low-reluctance return path for the field; the second is the conductivity of the magnet card, which produces, by eddy currents, a magnetic barrier above the twistor wire. These two mechanisms help to reduce the drive currents required and the interaction between bits.

In these modules, a 2.62 ampere-turn bias and half select are used. These produce a "one" output at the end of a twistor pair of 2.5 mv

across 300 ohms (far end short-circuited). For a bit with a magnetized magnet, essentially no output is generated in the twistor wire. However, because any selected access core is always accompanied by 126 half-selected cores, some "shuttle" or "delta" noise may be generated due to the summation of small voltages at each of these solenoids. This delta noise is information dependent. It may subtract from a "one" signal as well as create a "zero." The modules used are designed to insure a 2.5-to-1 ratio of "one" to "delta" for worst drive, temperature, and information pattern over the complete population of manufactured modules. Under nominal conditions of drive and temperature almost all bits will exceed 5-to-1 with worst pattern.

1.4 *Store Organization*

A complete program store is shown in Fig. 4. The store circuitry contains three major divisions: access, readout, and control. Each of these will be treated in detail in this article. The function of each is as follows:

1.4.1 *Access*

To achieve the required capacity, 16 twistor modules are used in the store. These are arranged in a 4×4 array which results in a 256×256 access core matrix. The access circuits must provide this array two pulses of accurately controlled shape, amplitude, and coincidence to cause the readout of the desired word.

1.4.2 *Readout*

The readout section must provide the amplification of the low-level twistor signals and the selection and sampling necessary to provide the binary output word. The twistor wire signals all appear on terminals on the front surface of the modules. Because of the large area of the core matrix and the low level of the twistor signals, the readout leads must be well shielded to avoid interference. Ideally, the 88 twistor pairs from each module could be paralleled before amplification, since only one solenoid is accessed at a time. For two reasons, this is not done: first, it would result in a considerable reduction in available output power; second, and more importantly, the delta noise would be several times that from a single module. On the other hand, individual handling would require 1408 preamplifiers. In the interest of economy a compromise solution is used. The modules are paralleled in groups of four. Each module in the group is chosen from a different row and column so that no delta noise penalty is incurred. The 6-db loss in power is not great enough to significantly degrade signal-to-noise performance.

The selection of the desired group of 44 pairs from the four groups of 88 pairs is made after a small amount of amplification. A single group of

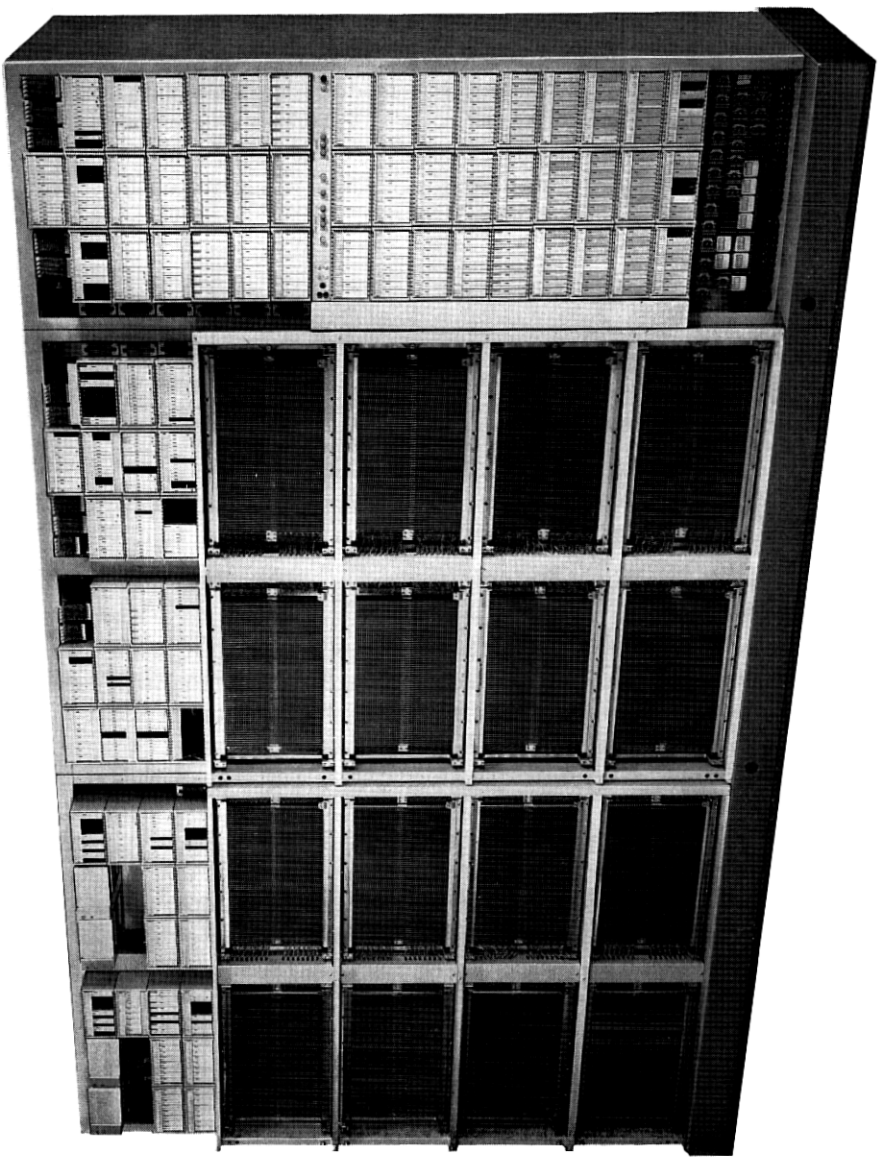


Fig. 4 — No. 1 ESS program store.

44 readout amplifiers and samplers is used to generate the final quantized one and zero signals. (See Fig. 5.)

1.4.3 *Control*

These circuits must provide all of the communications with the remainder of the system, both for normal action and maintenance. Additionally, they must make continual checks to detect abnormal conditions and initiate diagnostic action. Duplicate communication circuits to the central controls are provided. This duplication requires control circuits which must have further communication paths. To provide flexible growth a common bus system is used for all stores. Thus each store must have circuits for recognizing coded bus signals before responding. To insure that effective automatic diagnosis is possible, logical separation of circuit faults must be made possible by judicious provisions of circuit and communication redundancy. An indication of the complexity of this function is that nearly one-half of the store circuitry is in this section.

1.5 *Card Writing*

The insertion of information into the program store requires the magnetizing or demagnetizing of individual magnets. To meet the

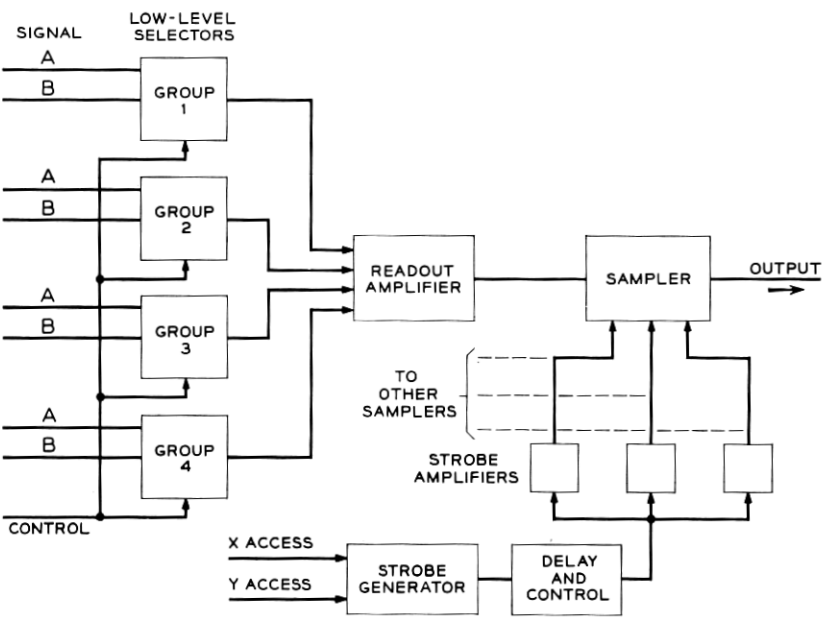


Fig. 5 — Readout block diagram.

system objective of a simple and straightforward method for accomplishing this, two auxiliary units are used: (1) the magnet card writer, which provides a mechanism for handling cards and a movable magnetic head for magnetizing or erasing magnets, and (2) a card loader which provides an automated method of removing or inserting a full module of cards from or into a store and supplying them to the card writer.

The card writer is used by the system as a peripheral unit. It is supplied information based on old program store information modified by the changes desired. Using this information the card writer magnetizes and erases a spare set of cards. Once prepared, this set may be substituted for the old set in the program store. This process of updating translation information in the office is straightforward and insures that the new information is correct before the old information is destroyed.

II. STORE ACCESS

2.1 *General Philosophy*

2.1.1 *Coincident-Current Word Selection*

Word selection is obtained in the No. 1 ESS program store by means of a coincident-current selection method utilizing a ferrite biased core switch. Normally, all of the access core switches are biased with 2.62 ampere-turns, which in the absence of other drives causes the ferrite core to be in a state of saturation. The core has a squareness ratio, B_r/B_{max} ,

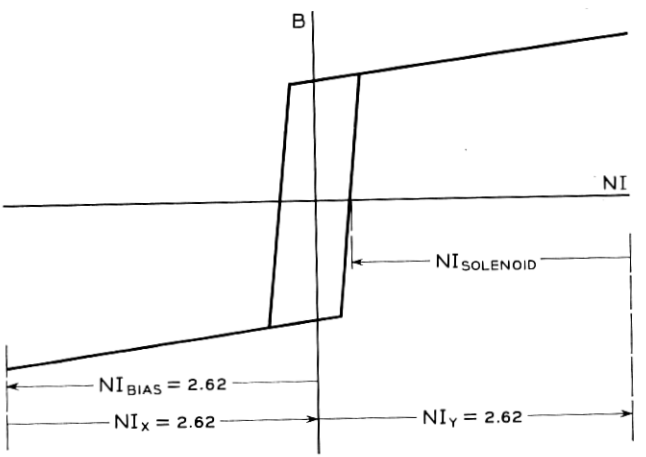


Fig. 6 — Operation of biased core switch.

of about 0.95, together with a coercive force (H_c) of about 0.2 oersted. Thus the state of the core is much as shown in Fig. 6. Also shown are the driving forces, NI_x and NI_y, applied to the biased core switch. It is obvious from the figure that either drive by itself is insufficient in magnitude to cause any switching action in the core. On the other hand, if both drives are present at the same time, the core will begin to switch. During the switching interval, a voltage will be induced in the solenoid winding which will cause a current in this winding that will flow in a direction such as to oppose the drive current. Thus the magnitude of the ampere-turns drive in the solenoid is equal to the sum of the two drives minus the bias, the coercive force, and appreciable losses due to high-speed switching of the core.

If the drives were maintained on the biased core switch, the core would eventually saturate. For the duration of the pulse required (2 μsec), a 400-mv-μsec core provides ample margin for worst-case considerations of temperature, drive currents and solenoid impedances. Normally, the core is only partially switched at the time the drive currents are removed. Upon removal of the drive currents, the bias current switches the core back to its initial, or set, state. This results in a reverse current flow in the solenoid winding that resets all the twistor wire bits. Such action points out one great advantage of the biased core switch for memory access: unipolar drive currents in the core lead to bipolar pulses in the solenoid. This provides for automatic resetting of the memory word bits after interrogation.

2.1.2 *Size of Access Matrix*

The size of the access matrix is necessarily a balance between economy and peak power requirements. Generally speaking, the cost of memory on a per bit basis is less as the size of the memory increases. This is particularly true of coincident-current access memories. The larger memories, however, require an increased drive power which results in several problems. One is the problem of generating the high-power drive pulses while meeting the system cycle time and another is the problem of interference between the access and readout signals.

The No. 1 ESS program store has a single access system. The access matrix is 256 $\times$ 256. That is, there are 256 X-drive windings and 256 Y-drive windings, together capable of selecting one of the 65,536 cores used as biased core switches. The load presented by the winding consists of three parts. The primary load consists of the air inductance of the access winding itself. The secondary load is the shuttling of the 255 cores which are not driven by the other set of drive windings. Of little con-

sequence is the load presented by the selected core. This is not to say that the core properties are not of great importance. The squareness ratio determines the load presented to drivers when the 255 cores are shuttled. The smallest core that has the requisite output is desirable, since larger cores increase the shuttling load.

The choice of the number of turns to be used on the biased core switches for the drive windings is dependent on several factors. The most important factor is the semiconductor to be used and its ratings. The 20D transistor is specified primarily for its needs in the access circuitry. The transistor has to have fast turn on and off times, with 1.35-amp current capability, and be able to interrupt a 50-v level without breaking down. These are approximately the values of current and voltage encountered with two turns per core. Operation with three turns requires excessive voltage ratings on the transistors and lowers the resonant frequency of the drive winding into the frequency band used by the pulse drivers. Single-turn operation would be desirable if an adequate transistor were available. Its advantages do not appear sufficient to warrant paralleling three 20D transistors, since this would entail added cost and circuit complications. As a result, a two-turn winding was chosen.

The circuit access matrix for one axis is shown in Fig. 7. It is basically a simple diode matrix with 16 access switches on each side of the matrix. A closure of one access switch each in the upper set and the lower set will establish a path through the matrix, thus selecting 1 out of 256 drive windings. As mentioned previously, each of the drive windings drives 256 cores. The matrix diodes prevent sneak paths from occurring which would subtract from the current pulse desired in the selected winding. They are normally back-biased to a voltage slightly higher than the peak drive voltage. This protects the access switch from a transient turn-on problem that could degrade the shape of the leading edge of the drive pulse. The diodes above the upper switches and below the lower switches also serve to protect the transistors of the associated switches from voltage pulses which could turn on a switch on a transient basis. These diodes are also normally back biased.

2.1.3 *Access Waveform*

Fig. 8 shows the basic waveforms of current and voltage as related to the twistor modules. Traces (a) and (b) represent the drive currents, I_x and I_y, that drive a particular core in the memory. Trace (c) shows the current in the word solenoid. The solenoid current shows the bipolar pulse characteristics plus the exponential recovery portion. The ex-

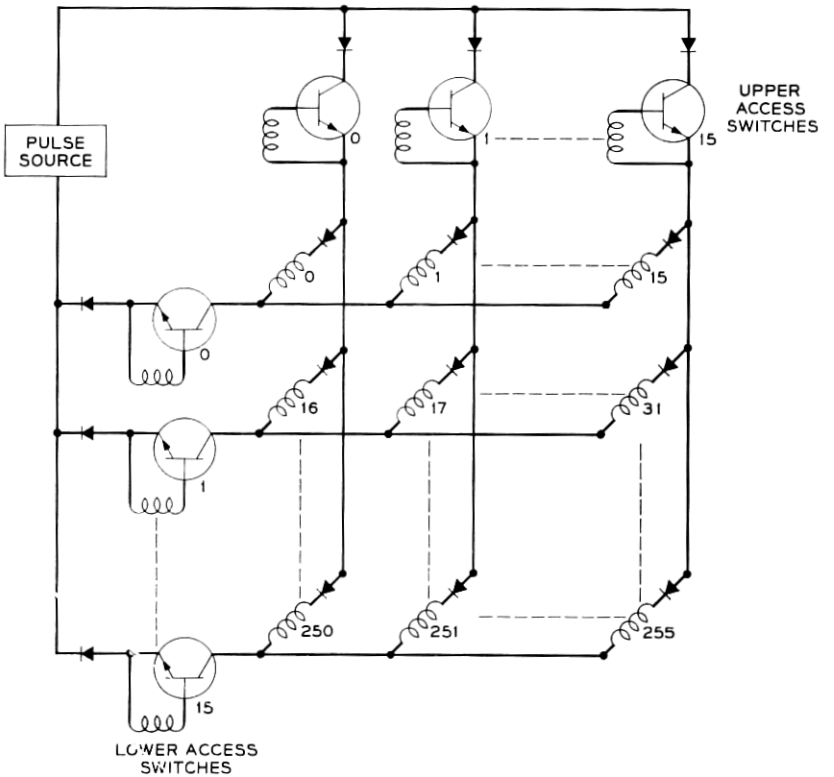


Fig. 7 — Access matrix for one axis of selection.

ponential decay occurs when the biased core switch returns to saturation. At this time the core is essentially a short circuit to the word solenoid. Thus the inductance and resistance of the solenoid determine the rate of decay of the solenoid current. This L/R time is important, since another interrogation cannot be started until the solenoid is nearly recovered. The program stores are operated at a 5.5-μsec cycle rate in the No. 1 ESS system but could be operated as fast as 4.5 μsec without degrading the solenoid current waveforms.

The drive currents are "on" for 2 μsec in the program store. This is primarily so that the readout can be detected before the transient caused by turn-off occurs in the readout circuitry. The approximate waveform of readout from the memory is shown as trace (d). It is included for timing reference only and is explained in some detail in the readout section of this article. The drive currents must be left on long enough to

switch enough flux in the biased core switch to insure a sufficient reverse current in the word solenoid to reset the twistor bits.

The rise and fall times of the drive currents are approximately 0.5 μsec. The shape of the current waveform is nearly trapezoidal in order to obtain the desired current level in a minimum amount of time without exceeding the drive transistor voltage limits.

2.2 *Current Pulse Generating System*

2.2.1 *Basic System*

The basic current pulse generating system for one axis consists of a constant-current source connected to a parallel circuit consisting of the load (access matrix) and a normally closed switch, as shown in Fig. 9. Normally the current source feeds current through the closed switch, A. When switch A is opened the current is forced to flow through the load and the normally closed B switch to ground. This presupposes that the proper access switches in the load section have been closed prior to opening switch A. Since the load is primarily an inductance, it is necessary to limit the voltage across the parallel circuit to prevent damage to switch A. For this purpose, limiter A is placed directly across switch A. Thus, when switch A opens, the limiter takes all of the current but places a fixed voltage across the load and switch A, causing a linear

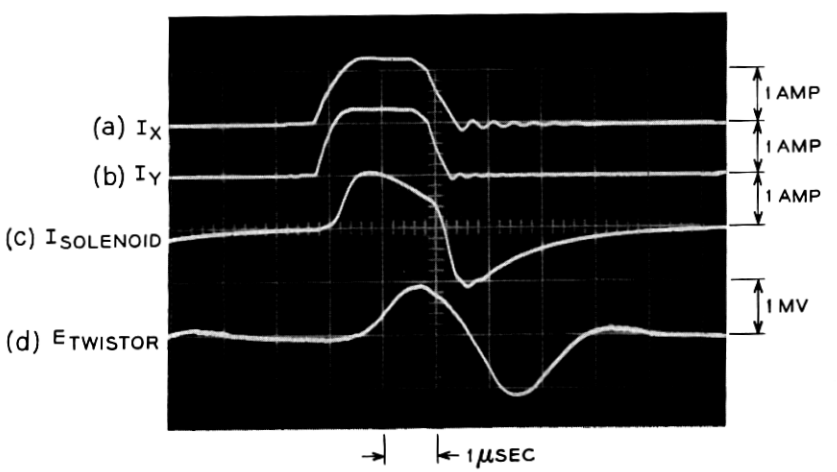


Fig. 8 — Access waveforms; (a) horizontal select current, 1 amp/division; (b) vertical select current, 1 amp/division; (c) drive solenoid current, 1 amp/division; (d) twistor output, 1 mv/division; horizontal scale, 1 μsec/division.

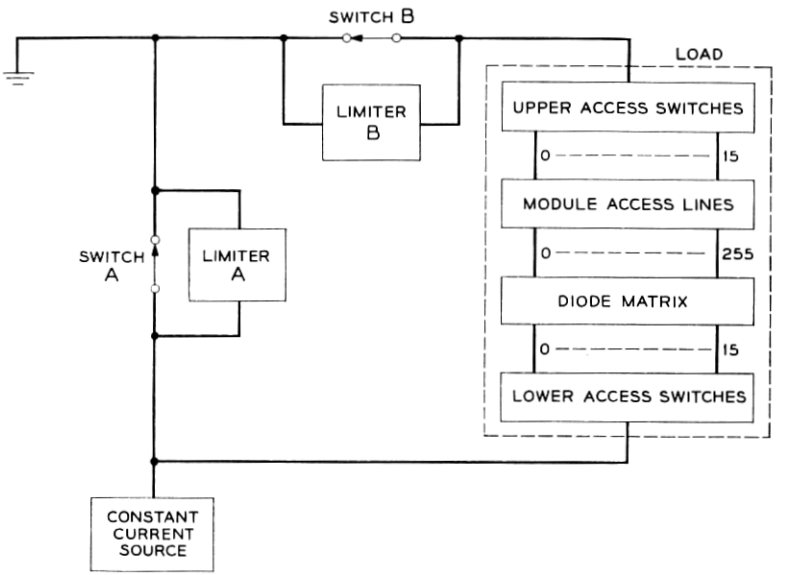


Fig. 9 — Basic access pulse generation.

buildup of current in the load. This continues until the load current equals the source current, at which time the load current remains fixed and the voltage on the parallel circuits drops to a low value determined primarily by voltage drops of the various semiconductor devices.

This mode of operation is uniquely suited to the twistor. In the twistor the inductances of the drive lines are all well matched and independent of the memory contents. Thus the application of a constant voltage results in accurate control of the rise time.

A similar method is used to effect turn-off. Again referring to Fig. 9, switch B is opened and switch A is reclosed. The inductance of the load must now drive limiter B. Thus a constant reverse voltage occurs across the load until the load current drops to zero. Switch B can then be reclosed and the access switches opened. With this method only switches A and B are used to make and break the current paths. The access switches are merely used to route the current pulse to the proper drive line.

2.2.2 *Switches A and B*

Switches A and B are identical circuits. They are both normally closed switches utilizing a pair of 20D transistors in the output stage and

operated in an antisaturation circuit to provide fast turn-off by elimination of the storage time inherent in saturated transistors. The basic circuit is shown in Fig. 10. The input stage is compatible with LLL and is driven from timing chain flip-flop circuits used as gate generators. The second stage is connected across the base-emitter terminals of the Darlington-connected output stages. This connection allows very fast turn-off even when driving inductive loads. The voltage transient that occurs as the switch is opened drives the second stage harder into saturation, preventing the power stages from turning on again.

The paralleling of the output stage is necessary in this circuit to keep the junction temperature below 100°C in the worst case, since these switches work in a nonsaturating mode and may run at 100 per cent duty factor.

2.2.3 *Limiter*

The basic limiter circuit is shown in Fig. 11. The limiter is a floating limit circuit. That is, both ends are free while the circuit is in a limiting mode and the capacitor, C_1, controls the limiting voltage. In its quiescent state, the −40-v regulator controls the voltage across C_1. The transistor used is a 20D with a resistor in its collector to lower the transistor power dissipation when the peak current of 1.35 amps is being limited. The limiter is expected to limit the voltage across its corresponding switch and carry a 0.5-μsec triangular current pulse every 5.5 μsec. A pulse transformer is provided in the collector circuit of the limiter. It produces

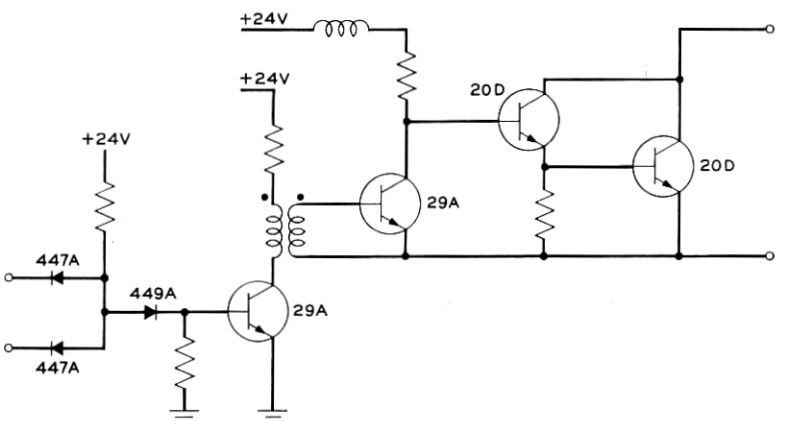


Fig. 10 — Circuit schematic — switches A and B.

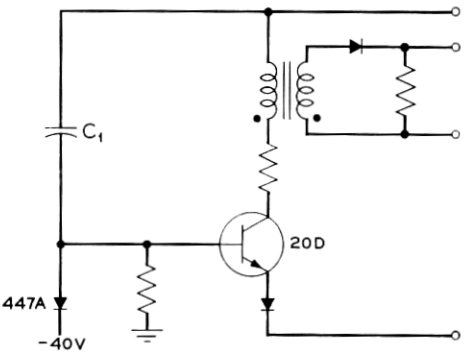


Fig. 11 — Circuit schematic — limiter.

a pulse used for maintenance checks on the access circuitry. The limiters for one axis are mounted on a common plug-in board.

2.2.4 *Access Switches, Voltage Pulser, and the Diode Matrix*

The access switch is a normally open switch used to select a current path through the diode matrix. The basic circuit for the access switch is shown in Fig. 12. The input stage is basically an LLL stage with 5 inputs. Four of the inputs are from the address register and provide the 1-of-16 selections required. The fifth is a gating input that controls the closing and opening times of the selected access switch. The collector of the input stage contains a 3-to-1 stepdown pulse transformer to drive the base of the output stage. This transformer coupling allows the output stage to float relative to the input stage. The transformer is designed to cause a 20 per cent droop in the current pulse applied to the output stage. This causes a negative drive to the base of the output stage to improve its turn-off characteristics when the input stage is turned off. The connections of the upper access switches for one axis are shown in Fig. 13. The capacitors (C_s) shown on the emitters of access switches represent the stray wiring capacitance of approximately 3000 $\mu\mu$f. The capacitance is charged to negative battery voltage to back-bias the diode matrix. Thus, when an upper axis switch is selected, it must discharge the 3000 $\mu\mu$f capacitance. To prevent this discharge current from exceeding the switch ratings, a filter is provided to limit the current surge to 1.35 amps at 50 volts. This allows the capacitance to be discharged in about 0.25 μsec. For this reason, the upper access switches are turned on 0.25 μsec before the lower access switches and switch A, which initiates the main drive pulse. Conversely, switch B is opened

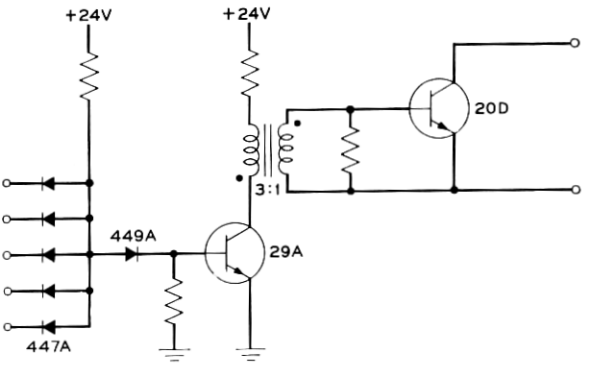


Fig. 12 — Circuit schematic — access switch.

0.25 μsec before switch A is closed, which forces the selected path to recharge its capacitance back to the level set by limiter B. The capacitance is charged the rest of the way to battery voltage by the action of the voltage pulser. The voltage pulser is identical to switches A and B; it is opened just prior to the initiation of a drive pulse and closed after the access switches have all opened. The voltage pulser connects the emitter side of each upper axis switch (and its associated capacitance) through a diode to battery.

The voltage pulser contains, as do switches A and B, a pulse trans-

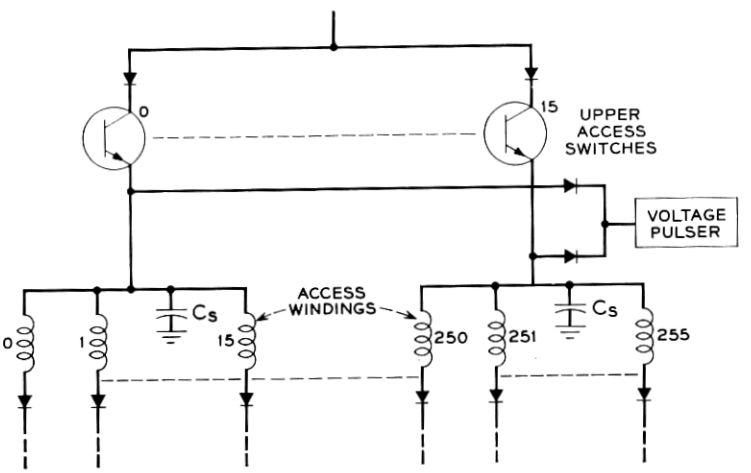


Fig. 13 — Partial schematic — access matrix showing stray capacitance load handling.

former to provide a voltage pulse representative of the switched current. This is used for diagnostic and maintenance purposes.

2.2.5 *Bias and Drive Current Regulator*

The bias and drive currents are regulated by identical plug-in current regulators. The currents at which the regulator operates, 1.31 amps for drive and 2.62 amps for bias, are determined by the socket interconnections. Because of the large amounts of power that must be handled, the regulator output stage is operated as a high-speed switch rather than in a linear mode. The average output current is controlled by adjusting the percentage dwell time of the switch closure. In this mode of operation the 20D transistors are either cut off or in saturation except for the short time required to transfer from one state to the other. Thus the power dissipation of the transistors is a small fraction of the power that is controlled.

The operation of the regulator can be seen from Fig. 14. The transistor switch and the resistor, R_s, are connected in parallel. This combination is then connected in series with the reference resistor R_R and the choke L. Feedback control is used to control the "on" and "off" times so as to generate the desired dc average current. (The resistance of R_s must be chosen large enough so that the highest steady-state voltage across it causes less than the desired regulator output current to flow into L.) Thus, the regulator's output current has an ac component; however, this component can be made quite small. The amplitude of the ripple component of the regulator's output current is controlled by the reference resistor value, the difference amplifier gain, and the Schmitt trigger's "window" or difference between "on" and "off" trigger voltage. The ripple frequency depends primarily on the above items plus the value of L_F but is also a function of the average battery and load voltage. The

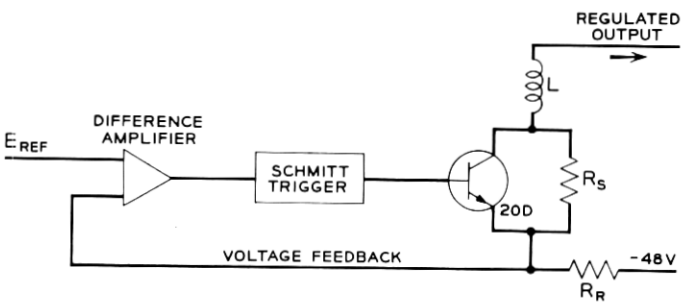


Fig. 14 — Access current regulator.

regulators operate at a nominal frequency of 50 kc with less than 1 per cent peak ripple. The choke serves to maintain constant current during transients too rapid for the regulator to handle directly.

Since the actual drive seen by a biased core switch is the sum of the X and Y drive currents minus the bias current, it is important that the bias and drive regulators do not drift in opposing directions and thus cause additive errors in the net drive. To prevent this occurrence, tracking circuits are provided that cause the output of each bias regulator to equal the sum of the X and Y drive regulator outputs within 1 per cent, ripple not included. The tracking circuit is composed of magnetic amplifiers driven with a 1-kc carrier current. A fail-safe tracking check detector is provided for diagnostic checking of the tracking circuitry.

2.3 *Access Timing*

The more important timing functions for the access portion of the program store are shown in Fig. 15. The various timing gates are generated by setting and resetting various flip-flops under the control of the access timing chain. Also included in Fig. 15 are some of the currents that are generated by these timing functions.

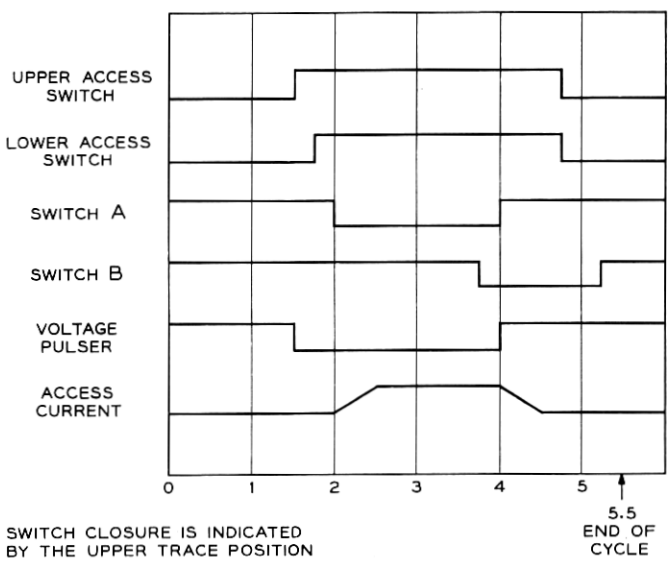


Fig. 15 — Access timing for one axis.

III. STORE READOUT

3.1 *Signal Selection*

As previously mentioned, in each group of four modules corresponding readout wires are paralleled. This results in eight groups of forty-four wires, of which only one contains the desired information. The other groups contain unwanted information or noise which must be suppressed. The selection of the desired group takes place in the low level selectors (LLS).

The LLS (see Fig. 16) accepts two twistor pairs, both associated with the same bit of the words common to an access solenoid. The two inputs are amplified and one is selected. The selection is made as early in the store cycle as possible so that selection transients will not interfere with the readout signals. The design of the LLS is such as to avoid in-service gain adjustment.

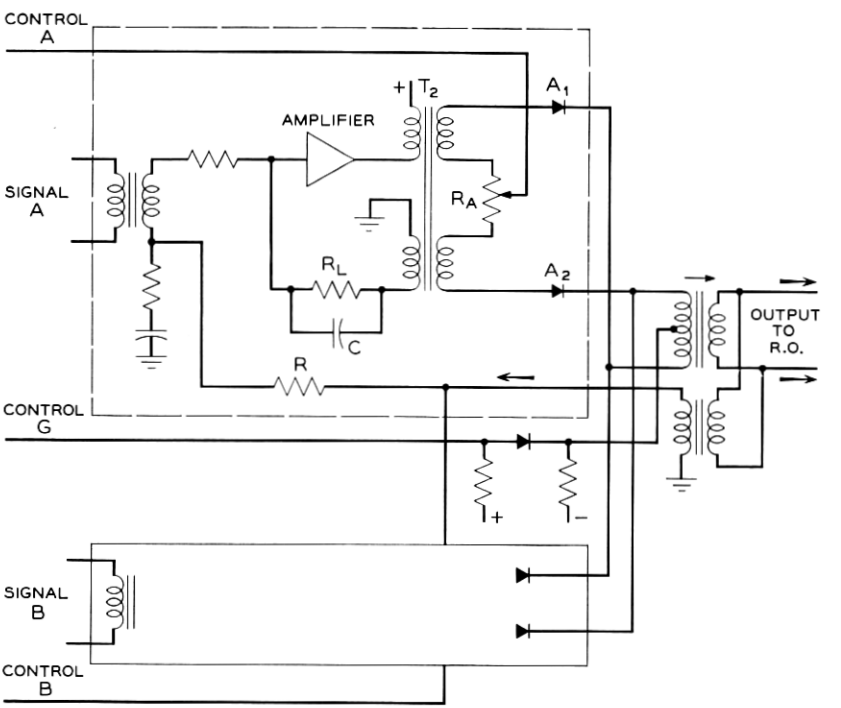


Fig. 16 — Circuit schematic — low-level selector.

The input signal is transformer-coupled to give good common mode rejection and to improve the impedance match. There are two stages of amplification with two feedback paths. There is a local feedback path, R_LC, and an over-all feedback path, R. The local path controls the high-end frequency response and gives the amplifier a low output impedance working into T_2. The over-all feedback path controls over-all gain and improves the low-frequency response.

Selection of signal A is made by making control A positive, control B ground, and G ground. With control A positive, equal currents flow through diodes A_1 and A_2. To avoid the requirement for matched diode pairs, R_A is provided to equalize currents. Since the currents are equal, only a minimum transient occurs when a path is selected. The signal at diodes B_1 and B_2 is sufficiently small that the diode threshold blocks the signal B.

Over a store cycle, the signal from the twistor memory goes both positive and negative and averages to zero. To avoid generating a dc component in the LLS, the path selection cannot be changed until the complete signal has passed. To accomplish this, a separate buffer register holds the selection information from cycle to cycle.

The LLS has a very large amount of feedback. In addition, the feedback resistors are very precise and have excellent long-term stability and tracking. The combination assures gain stability of a few per cent over the life of the circuit.

3.2 *Signal Amplification and Sampling*

Each of the 44 readout amplifiers shown in Fig. 17 accepts the outputs from four low-level selectors and provides the necessary gain to operate the sampler. The four LLS outputs are mixed by four resistors, R_1 to R_4, operating into the emitter of Q_1 and the feedback resistor, R_F. The mixing point is a very low impedance compared to the 100 ohms of R_1 to R_4. The readout amplifier has a large amount of feedback which provides frequency shaping and gain stability. Its long-term gain is constant to approximately one per cent. The signal at the output of the readout amplifier is bipolar and has a nominal amplitude of one-half volt for a one. A typical readout for several bits is shown in Fig. 18. Because of the wiring pattern, one-half of the ones have an initial positive loop, while the other half have an initial negative loop. Typical delta noise zeros shown are representative of a severe pattern interaction. The polarity of the zero is information-dependent and may be of either polarity at a given address.

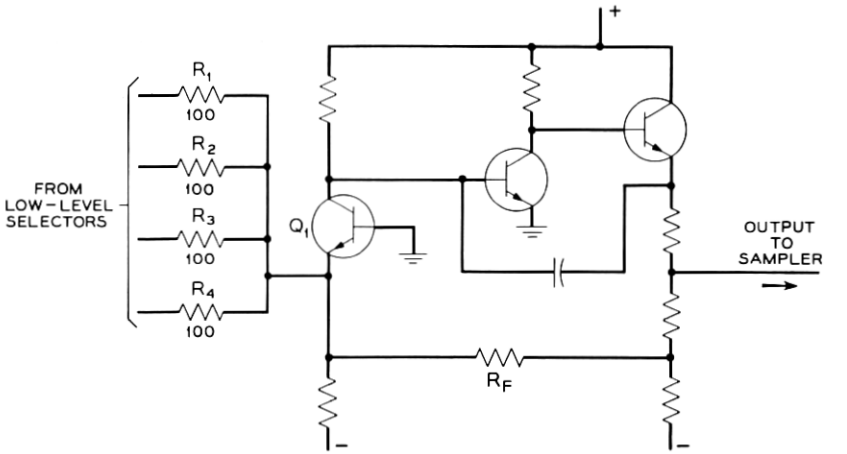


Fig. 17 — Ci rcuit schematic — readout amplifier.

A sampler (see Fig. 19) must make the decision as to whether the output is a one or a zero and quantize the output.

In designing the sampler certain characteristics of the signal were exploited. One of these characteristics is that the delta noise passes through zero near the time the one signal reaches a peak. Advantage was taken of this characteristic by placing a very narrow strobe at the delta noise zero crossing, as shown in Fig. 18. Another characteristic of the signal is that at a given address the one is of a known polarity. The sampler is designed to observe only this polarity, so that delta noise of the opposite polarity, no matter how large, cannot generate an output.

The two-stage input amplifier provides gain and a very low output impedance. The low output impedance is necessary because the load is variable, depending on the size of the signal. There is no load on the amplifier until the strobe occurs and no load then unless the signal exceeds the threshold. The low output impedance of the amplifier makes it possible to deliver enough power to trigger the output if the signal only slightly exceeds the threshold. This leads to high stability. The low impedance also prevents modulation of the signal by the sample pulse.

The strobe pulse, correct for the polarity of "one" being sampled, is supplied to each sampler at the correct time. The amplitude of this pulse is not critical. If the signal exceeds the threshold reference, diode D_1 is back-biased and the voltage change is coupled by C_1 to the output transistor, Q_1. Since Q_1 is biased in a Class A region, any minute voltage change is amplified and fed back to the base. This feedback path is

activated 0.25 μsec before the narrow strobe pulse. The purpose of this feedback path is to guarantee full quantization of "one" outputs and to lengthen the pulse to the standard half microsecond used for bus communication. Once regeneration starts it can be terminated only by opening the feedback path. The feedback path cannot cause regeneration in the absence of an input pulse.

3.3 *Strobe Timing and Generation*

In the laboratory, optimum strobe time can easily be set for a particular set of circuits. It is more difficult to design circuitry which will produce the strobe at the correct time for any combination of access or readout circuitry. To accomplish this, the strobe timing must be referenced as closely as possible to the start of the access current flow. Fig. 20

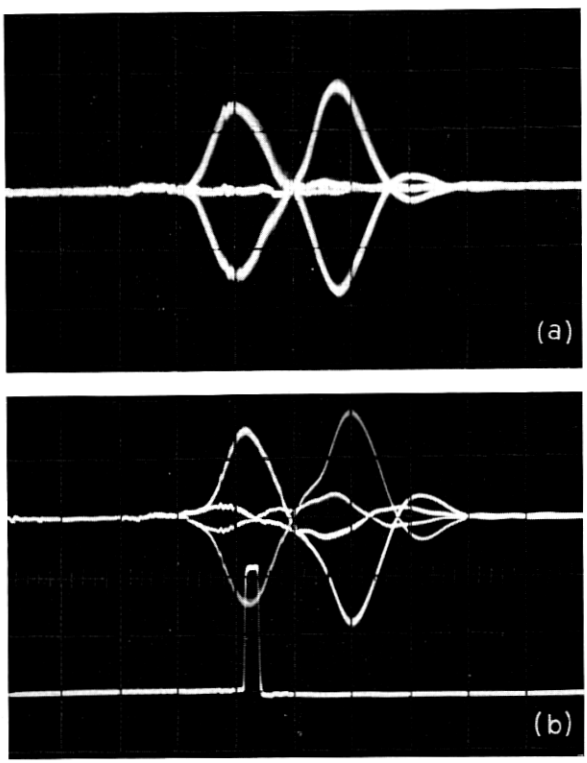


Fig. 18 — Readout waveforms: (a) typical readout; (b) readout with high "delta" noise.

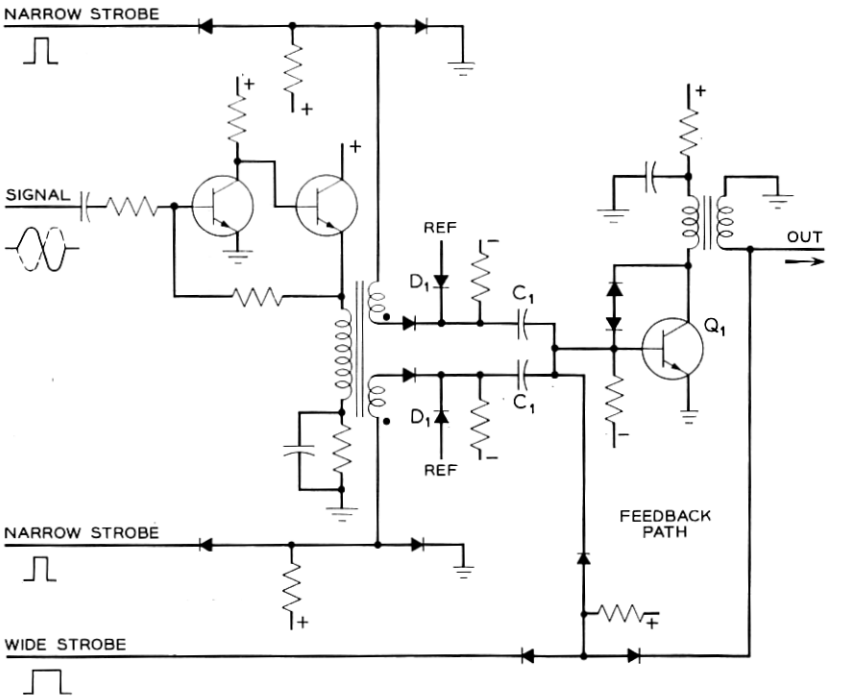


Fig. 19 — Circuit schematic — sampler.

shows the strobe generating circuitry. Three pulses must be generated: a narrow strobe of 0.25 μsec duration, a wide strobe that starts 0.25 μsec before the narrow strobe and ends 0.25 μsec after the end of the narrow strobe, and a 0.5-μsec sync pulse starting with the narrow strobe.

The readout signal occurs at a fixed time after the start of the access current. The beginning of access current for both axes is monitored by the strobe generator; only when both X and Y currents have started is the strobe circuitry initiated. This avoids the delay time variability of the access circuitry. The initiating pulse is delayed the proper amounts to set flip-flops 2 and 3, which initiate the narrow and wide strobes respectively.

The strobe amplifiers are relatively powerful, since they must drive 44 samplers. The strobe amplifiers each have an auxiliary output; these are added logically to start the timing of the wide strobe termination. This approach assures that the width of the pulse output of the sampler is 0.5 μsec.

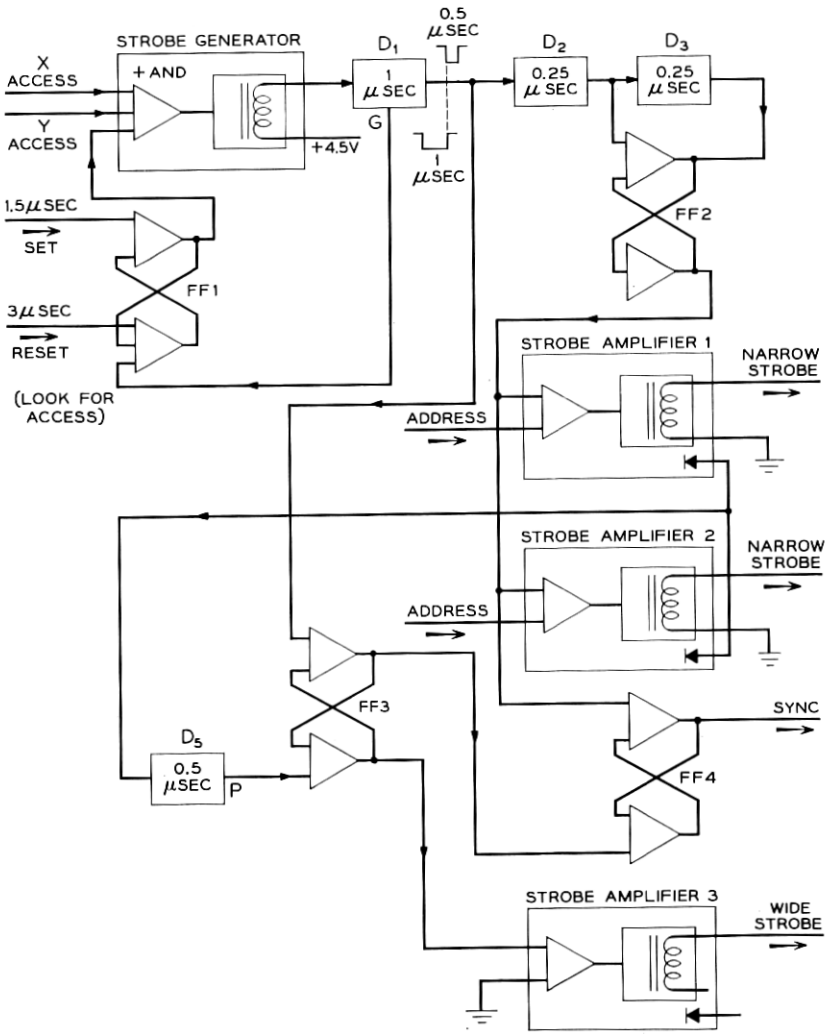


Fig. 20 — Strobe generation.

IV. CONTROL

4.1 *Communications*

The principal communication path of a program store is a duplicated two-way bus system connecting all program stores and both central controls. These buses carry the necessary addressing and control information required to read a particular word from a particular store or pair of stores, or perform a control function on a particular store. The buses also carry the reply from the program store containing either the desired stored word or, in special control modes, the states of various flip-flops. The signals are sent as 0.5-μsec pulses on a balanced line for binary ones and no pulse for zeros. The busing arrangement is described in more detail elsewhere in this issue.[8]

The program store also receives inputs from the central pulse distributor, the signal distributor, and the master control center and sends outputs to the master scanner. The inputs from the central pulse distribution are direct connections to each store, as opposed to a bus, and consist of either positive or negative 0.5-μsec pulses. These pulses must be accompanied by a pulse on a sync bus to be effective. They are used to set or reset various control flip-flops in the program store.

The inputs from the signal distributors are relay contact closures used to control special relay circuits or lights in a particular store. The inputs from the master control center are also dc contact closures. These inputs provide manual override control of the program store and can be used to force a particular store or stores off-line or to force a store to listen on a particular bus from central control.

The outputs from the program stores to the master scanners are divided into two groups. One group consists of direct wires from each store to a scanner ferrod and is used primarily to detect the status of various control relays and flip-flops in the store when they cannot be interrogated over the bus system. The second group is another common bus system to which any program store may be connected. This 48-pair monitor bus terminates in a bank of ferrods in the master scanner. When so ordered by the signal distributors, a program store will connect a group of test points to the monitor bus. This operation is used for maintenance checks of the voltage and current regulators and other dc levels throughout the store.

4.2 *Codes and Modes*

Each program store has its memory field separated into H and G halves. Each program store half will have a numerical code wired into

the store at the time of installation. This allows an office to operate with an odd number of stores and yet provides full duplication, as shown in Fig. 21. As can be seen, duplicate information (identified by the same numerical code) is always provided in the logically adjacent store. That is, information field 2 in the H side of store 2 is duplicated in the G side of store 1, and so forth. Normally, all H-half outputs will communicate on one bus to central control and the G-half outputs on the duplicate bus. Thus, when a particular information word is requested, the two stores containing the word will interrogate the required memory location and answer back on separate buses. If one of the program stores should fail, then the store carrying the duplicate information would be arranged to answer on both buses to provide duplication. The decision as to which bus or buses to answer on is made by system programs and sent to program stores as control orders.

Along with the address and code bits sent by the central controls on the program store buses are several mode bits which establish the type of operation desired of a store. Four modes of operation are decoded from these bits by the program stores. They are normal, maintenance H, maintenance G and control. If a normal mode is recognized, the stores (or store) that also recognize the code bits will send back the desired memory word. If a maintenance mode H is requested, only the store that recognizes the code bits as being the code of its H half will answer. Similarly, for a G mode, only the store that recognizes the code bits as being the code of its G half will answer. The control mode order affects only the store that recognizes the code bits as being the code of its H half. The control mode is not a memory read operation. The control mode is subdivided into two submodes, the control write and the control read. This selection is made by an additional wire pair in the bus system. In the control write mode, the address leads are used to write, dual rail, into various flip-flops within the store. Some of the address leads select which bank of flip-flops will be written; others contain the information to be written. In control read, the states of various flip-flops throughout the

Fig. 21 — Program store duplication.

store are sent back to the central controls. The address bits are used again to select which bank of flip-flops is to be interrogated. The control mode constitutes a powerful maintenance and diagnostic tool by providing a means of writing into and reading out of most of the control and maintenance flip-flops of the program stores.

4.3 *State Flip-Flops*

In order to control the store communications, several basic state flip-flops are provided. One group of such flip-flops controls the store routing. For example, one of the flip-flops selects the input bus on which the store should receive address and control information. This flip-flop is normally controlled by the central pulse distributor, but may be controlled by the master control center. Four flip-flops are used to control the normal store output to the buses. The H and G halves are each controlled by two of these flip-flops, which are normally set and reset by a control write operation.

In addition to the foregoing, two trouble flip-flops are provided that can prohibit the store from either sending or receiving on either or both of the buses. These can be set by the store itself, the central pulse distributor, or the master control center.

In addition, the office contains an emergency-action circuit which can set the state flip-flops. This circuit is activated whenever the system stops, and sets one of the stores containing program information to communicate on one of the buses and the store containing duplicate program information to communicate on the other bus. In offices with more than two stores, the remaining stores are disconnected from the buses. Following similar action with other units, the circuit attempts to restart the system.

4.4 *Timing*

The store timing is initiated by a sync pulse on the input bus from central control. The pulse is then delayed in each of two independent timing chains. One chain is used primarily for access timing, while the other is primarily used for control circuit timing. The two timing chains provide reliability in that critical communication control circuits are wired to both chains so that a failure of one timing chain does not cause a breakdown of communications and thus allows diagnostic programs to use the control mode feature to check the timing chains. Having two chains also makes it possible to check the accuracy of one timing chain against the other. The timing chains consist of a series string of delay gate

generators (DGG). The DGG's are available with delay times ranging from 0.25 μsec to 1800 μsec, all of which use the same printed wiring board but have a different timing capacitor. The DGG consists of two monostable multivibrator circuits connected as shown in Fig. 22. The first three transistors comprise one monostable circuit with a negative input signal used to trigger the circuit. This circuit generates an accurate gate pulse whose width is equal to the desired delay. The output of this circuit is applied to the final transistor, which turns on at the end of the gate pulse for approximately 0.5 μsec. Thus the output of a DGG is a negative-going pulse with a width of 0.5 μsec delayed by a fixed amount from the input negative pulse. The DGG has several diodes for temperature compensation and can be set to better the 0.1 per cent. The long term drift of the DGG is expected to be less than ± 5 per cent of the delay value. A DGG can drive up to five input loads which may either be LLL circuits or other DGG's.

The DGG's on the access timing chain are used primarily to set and reset gating flip-flops which are in turn used to control access timing gates such as required for the access switches or switch A.

The timing chains are checked against each other at several places along the chains, including the ends, to ensure agreement in the two chains. In addition, circuits are provided to check the output level of each DGG to ensure that it is normally in its high state and not loaded

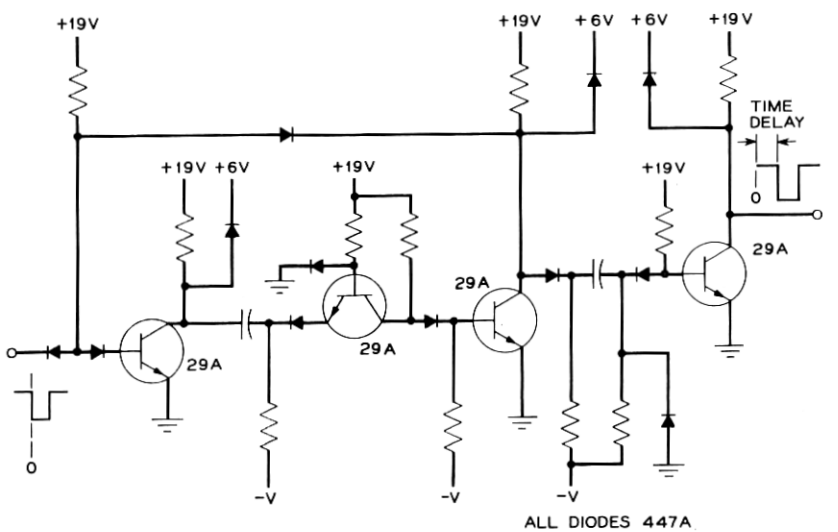


Fig. 22 — Circuit schematic — delay gate generator.

down by some other package with an input problem. Also, the operation of either timing chain can be inhibited to check the check circuits.

4.5 *Power*

The program store obtains its power from the +24-v and −48-v office batteries. This power is filtered and switched at the store. Separate power is provided at the store to power the card loader when the latter is connected to a store.

The program store draws essentially a constant load of almost 1000 watts from the battery plant. The actual battery drains are 18 amps on the +24-v bus and 12 amps on the −48-v bus. The power is filtered by a double L-section filter at the store input terminals both on the +24-v bus and the −48-v bus. The filters serve both to prevent noise spikes from entering the store and prevent power turn-on and -off transients from interfering with other operating units. The filter is so damped that the turn-on current increases smoothly to its operating value with no overshoot.

Several voltage regulators are used in the program store. A 4.5-volt regulator is used to supply the LLL stages as well as the low level selectors. Also +19- and −40-volt regulators are provided to supply several special circuit packs.

The +4.5-volt regulator is a high-efficiency "off-on" regulator which can deliver 1.5 amps at 4.5 volts while drawing about 0.4 amp from the +24-v bus. A basic diagram of the regulator is shown in Fig. 23. The output stage consists of a choke input filter which is either being charged by the 20D transistor connected to +24 volts or is being discharged by being forced to draw current from ground through the diodes. The "off-on" operation of the 20D is controlled by the output of the Schmitt

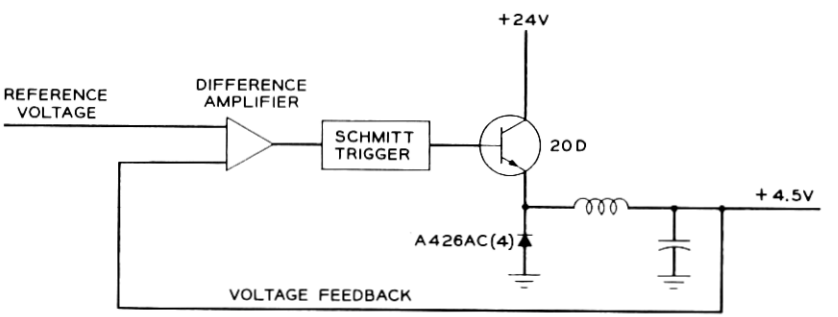


Fig. 23 — Circuit schematic — 4.5-volt regulator.

trigger, whose input is an amplification of the difference between a Zener reference stage and the regulators' output voltage. The feedback is so controlled that regulator "off-on" frequency is about 50 kc, with the 20D transistor being on about 20 per cent of the time. This type of regulator has the advantage of providing good regulation with high efficiency and low power dissipation in the semiconductors. The operation of this circuit is similar to the operation of the bias and drive current regulators described in Section 2.2.5.

The +19- and −40-volt regulators are conventional series linear control regulators. Since many of these regulators are used in each store, special reference regulators operating at +17 and −38 volts were made for the +19- and −40-volt regulators respectively. This circumvents the need of providing a Zener reference for every regulator package. Actually, two reference units for +17 and −38 volts are provided to facilitate maintenance and diagnostic checks.

The voltage regulators are checked for the correct voltages by means of the scanner monitor bus. The general method of testing the +19-volt regulators is indicated in Fig. 24. Since the regulators are cross checked against another regulator and reference unit, the failure pattern is unique for each regulator. To ensure that the check circuits are operating properly, the 19-volt check regulator outputs can be shifted by operating

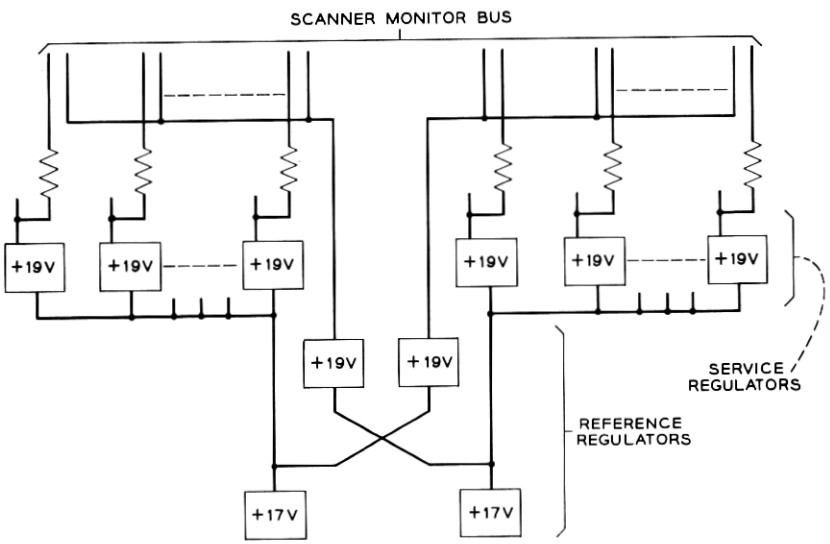


Fig. 24 — Regulator diagnostic checking.

a signal distributor input to give trouble indications of all associated regulators. The −40-volt regulators are tested in the same manner as the +19-volt units. The +4.5-volt regulators are checked two against one on the scanner bus, since only three are required per store.

V. MAINTENANCE

5.1 *Maintenance Philosophy*

The program store maintenance and diagnostic check circuits were designed along with the operational circuits. Each circuit, including the maintenance circuits, became the subject of a detailed study to ensure that a fault could be readily localized to, in most cases, a single circuit package, and in the worst case no more than three circuit packages. The effect of the failure of any semiconductor device used in the store was scrutinized to ascertain that the diagnostic checks provided could localize the fault. In general, the maintenance and diagnostic system can be divided into three sections. The first section is the all-seems-well (ASW) section. An ASW pulse is returned along with every readout from the program store to central control and indicates the success of all internal store checks. The second section makes use of the control read and write modes to diagnose and test the stores' condition. The third section is composed of the direct scan point that checks various states within the store and the monitor bus, which can be used to check many points within the store, as previously discussed.

5.2 *All-Seems-Well Circuit*

The ASW circuit provides an extremely powerful check on a store's condition. The ASW pulse indicates that: (1) the mode decoder has received a valid code, (2) the timing chains are both in step, (3) the address register and other control flip-flops were reset at the beginning of the cycle, (4) one and only one X and Y access drive winding was pulsed (for modes other than control), (5) the access pulses were of the proper amplitude, and (6) only one readout group was selected. Thus the ASW signal is derived from the status of several individual circuits. The failure of the central control to receive an ASW signal from a program store will generate a system attempt to reread the desired word. If the failure continues, the store will be checked by a diagnostic routine to isolate the faulty unit.

5.3 *Read Control and Write Control*

The control modes together with a circuit known as "freeze reset" comprise a powerful diagnostic tool for checking the program store.

When a control read (CR) or a control write (CW) is recognized by a program store, it knows the system wishes either to interrogate the state of a set of store flip-flops or to write into a set of flip-flops rather than to perform a memory operation. For example, the system can, in CW, write into a flip-flop that normally is set when an access failure occurs. This should result in an ASW signal failure if the ASW circuitry is functioning properly. The pulse detectors that check the amplitude of an access pulse can be forced to indicate either high or low as desired to check that these circuits are functional.

A CW command can also be used to place the freeze reset circuits into operation. In this type of operation, many of the flip-flops which are normally reset at the end of each system cycle (5.5 μsec) are blocked from being reset. Thus the address register, for example, can be filled and its contents checked by a CR, an operation which could not otherwise be checked. Also, the freeze reset operation can be used to localize the cause of an ASW failure. The store is placed in a freeze reset condition by a CW; then a maintenance operation is called for. This latter operation will cause the memory to be interrogated. If the ASW indicates a failure on this operation, a flip-flop for the defective circuit area will have been set and will not reset at the end of the cycle. Thus this flip-flop can be read with a CR command to localize the fault. The freeze reset condition is restored to normal by a CW command.

To localize a fault to a specific package it is often necessary to run a special sequence of instructions and determine the pattern of ASW failure indications. For example, an open diode in the group select flip-flops could cause two readout groups to be selected at the same time. The ASW circuit will indicate the program store failure, the control mode and maintenance mode operation will determine what section of the store is causing the failure (in this case the group select flip-flops), and then a simple four-step pattern will determine which of the four group selects are in trouble, since the ASW signal will indicate a failure except when the faulty package is selected.

5.4 *Direct Scan Points and the Monitor Bus*

The slowest maintenance access, but the most direct, is the use of scan points.

Each store has 17 direct scan points, most of which are used to deter-

mine the state of the more important control flip-flops such as the code, trouble and bus receive flip-flops.

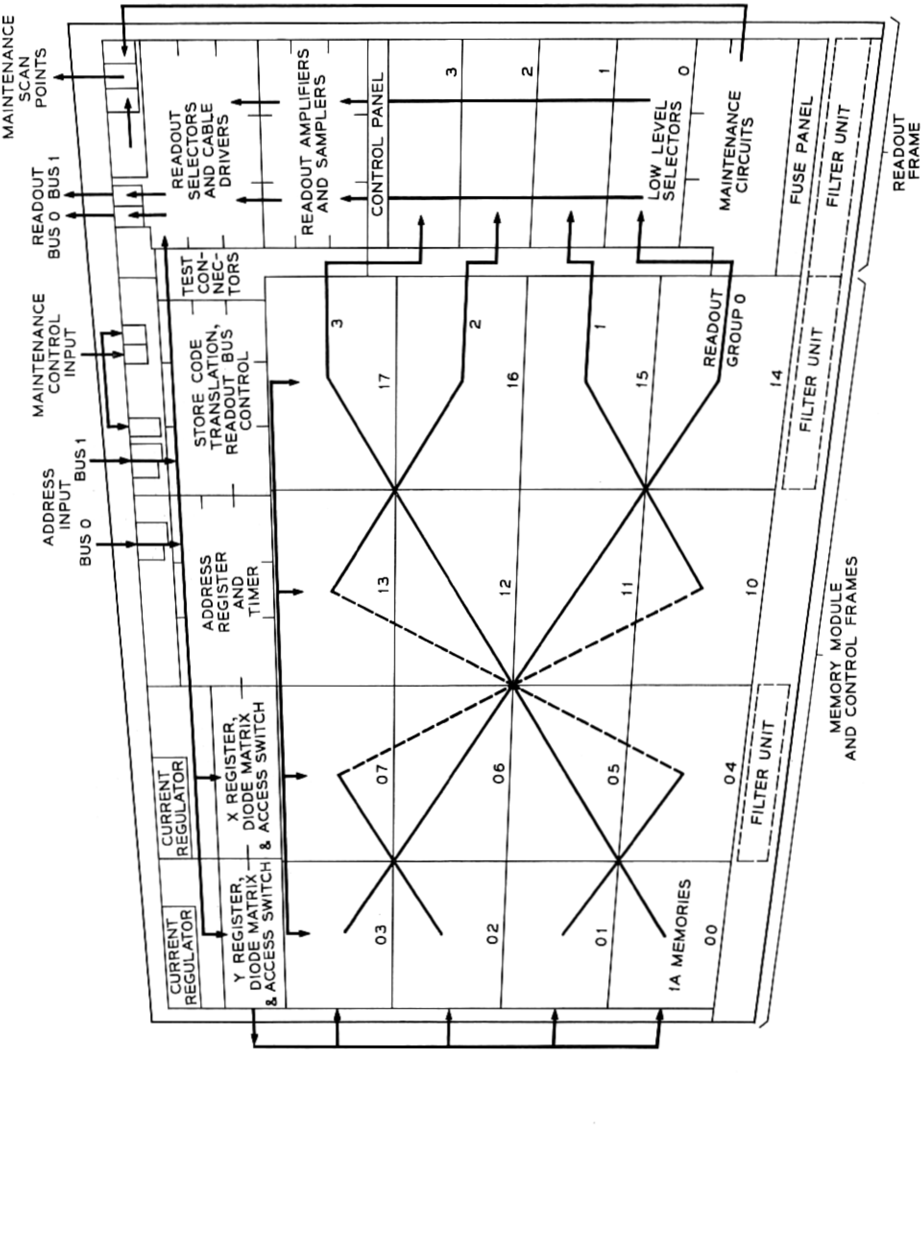
The direct scan points are also used to check the store manual control pushbuttons and power alarms as well as checking the states of relays controlled by the signal distributor, as discussed later. It is necessary to have direct scan points on functions such as the code detectors, since the store will not answer on the main communication path if it cannot recognize its codes, making the previously discussed diagnostic checks useless.

The scanner monitor bus is a 48-wire pair bus common to all the program stores within an office. The bus can be connected to points within a store by operating banks of relays under the control of the signal distributor. Each store has two banks of relays used to test the bus and connections to it, and three banks of relays to test various points within the store.

All of the store voltage and current regulators are checked by means of the monitor bus. The monitor bus is also used to check many flip-flops to aid in trouble diagnosis. In particular, the monitor bus is used to check the many packages whose failure could cause the store to become inoperative. The failure of a store to generate an access pulse in one axis could be caused by several different packages, most of which cannot be checked by a control read operation. The scanner monitor bus provides an inexpensive method of checking these packages.

VI. STORE EQUIPMENT[6]

The functional arrangement of the program store equipment is suggested by the flow chart, Fig. 25. Here the principal routes of information flow are superimposed on the equipment layout of the store. The address input signals are received by the pulse transformers in centrally located terminal strips at the top. These signals are then routed via the address register and timer unit to the X and Y drive circuits at the left and to the readout selectors at the right. The 256-point Y-select matrix reaches the select windings of the 16 memory modules with a vertical cable at the left end, while signals from the X-select matrix are distributed to the vertical select windings by means of a horizontal cable above the memory modules. These cables are shown in the rear view of the store in Fig. 26, together with the short horizontal jumpers which multiple the Y-select windings of the individual memory units and vertical jumpers which multiple the X-select windings. Thus, the desired 256×256 coordinate selection is achieved through short, direct wiring in a rectangular array.


MAINTENANCE SCAN POINTS
READOUT BUS 0 BUS 1
MAINTENANCE CONTROL INPUT
ADDRESS INPUT BUS 0 BUS 1
READOUT SELECTORS AND CABLE DRIVERS
READOUT AMPLIFIERS AND SAMPLERS
CONTROL PANEL
LOW LEVEL SELECTORS
MAINTENANCE CIRCUITS
FUSE PANEL
FILTER UNIT
READOUT FRAME
TEST CON-NEC-TORS
STORE CODE TRANSLATION, READOUT BUS CONTROL
ADDRESS REGISTER AND TIMER
CURRENT REGULATOR
X REGISTER, DIODE MATRIX & ACCESS SWITCH
Y REGISTER, DIODE MATRIX & ACCESS SWITCH
READOUT GROUP 0
1A MEMORIES
MEMORY MODULE AND CONTROL FRAMES
00
01
02
03
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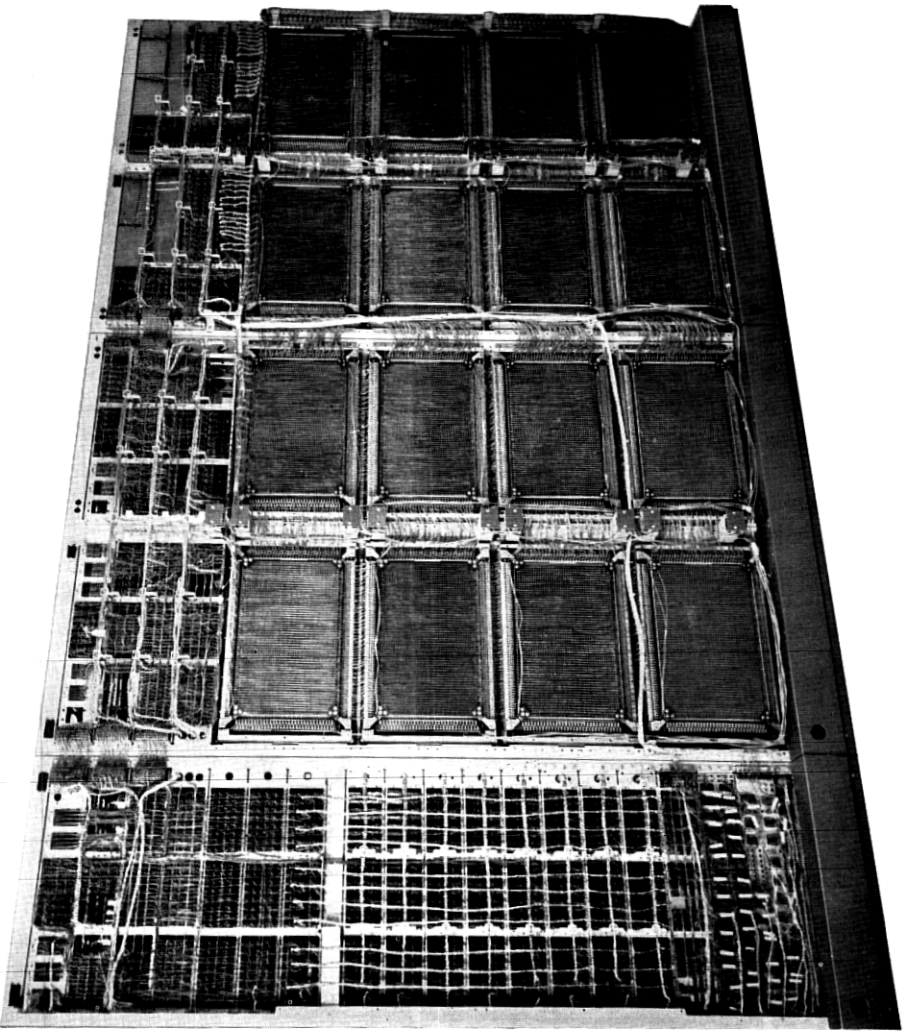

Fig. 26 — Program store — rear view with shield removed from readout bay.

For readout, the memory modules are arranged in four groups of four modules each. The twistor tapes for the four modules within each group are multipled in parallel. To minimize noise associated with half-selected addresses, no two memory units of a group are located in the same horizontal row or vertical column. The memory modules are associated as shown in Fig. 25, with readout connections to the four groups of low-level selectors at the right. These connections, as well as the interconnections between modules, are made with 26-gauge BY wire in close-twisted pairs ($\frac{1}{2}$-inch lay). These wires are precabled and routed through horizontal and vertical metal ducts between the memory units, and a vertical duct between the units and the low-level selectors. Special care has been exercised in the design of these cables and ducts to facilitate cable replacement, if necessary, in the event a memory unit should require replacement. The ends of the cables which terminate on the low-level selectors are distributed in the eight horizontal branches which appear in the left-hand bay of Fig. 26. The two branches associated with each readout group reach 44 circuit packs, which receive the 44-bit readout signals from each of the two twistor tapes associated with a readout group.

After selection, the readout signals are carried upward on the 11 vertical cables (four bits per cable) to the readout amplifiers and samplers, to the cable drivers and thence to the readout terminal strips at the top. The quality of the readout is due in considerable measure to the orderly and functional organization of this equipment.

VII. CARD WRITING

7.1 *Objectives*

The card writer is provided to rewrite, as necessary, magnet cards containing translation information for the office. It must be economical and reliable. It must not burden the real-time capabilities of the office while writing cards or require a high degree of operator skill. The procedure followed in writing cards should not destroy an existing module of cards until the new set is written and verified. Because there is no requirement of 100 per cent up time, duplication of communications, power, and equipment is not required.

The card writer must keep up with the writing requirements of a large office. Such an office, containing 6 stores, may require that $4\frac{1}{2}$ stores be rewritten each week. The card writer is designed to accomplish this in less than 18 hours of machine time.

The objective at the outset was to write the cards so well that no store margins were deteriorated due to marginal cards.

Every effort was made to design the writing process in such a way that no preprocessing such as bulk magnetization or demagnetization is needed and that the card will be correctly written regardless of the prior state. Accomplishment of this objective permits single-word writing, which is useful during program debugging.

7.2 *System Requirements*

The card writer magnetizes or demagnetizes the bits on a card by passing a head across the card. The system must provide the information to the head at the proper times. This requires suitable communication between the card writer and the system. The time between successive words is 13 milliseconds. This is slow enough that a scan point can be set by the card writer as soon as a word is written and the system can pick up the scan point on a routine scan and deliver a 44-bit word before the head reaches the next word.

Between each card writing operation approximately two seconds elapse while the system assembles the information for the next card. There is no check on the information written until the cards are inserted in the store. Every effort is made to assure a well written set and to complete the writing even when the system has difficulty delivering words on schedule. Some troubles, such as failure to receive a word when requested, cause the card writer to repeat the card. If three tries fail to write a card successfully, the process is aborted and an alarm sounded. Other troubles cause the process to be immediately aborted. In general, any indication of an incorrectly written module leads to termination during the card writing process. This follows the general philosophy of not putting suspect cards into operating stores even for checking purposes.

7.3 *Equipment*

The memory card writer, shown in Fig. 27 with a card loader attached, contains a centrally located card writing mechanism with circuitry above and below. The logic unit above is functionally arranged with terminal strips and sequence control circuits at the top and with registers and write control circuits between these and the control panel. A group of relays to control polarity of the writing heads and the writing head connectors are mounted just below the control panel on the sub-frame of the card writing unit. The lower part of this subframe supports a group

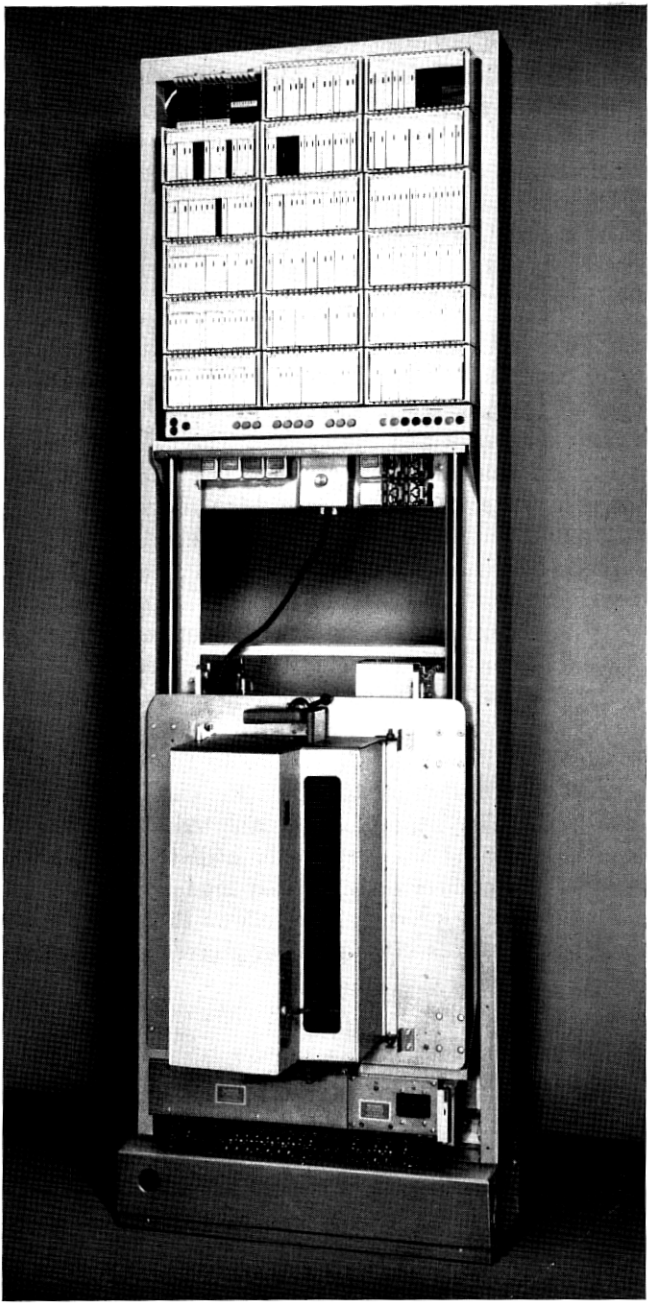

Fig. 27 — Memory card writer — front view with card loader attached.

of relays which control the mechanical sequences of the writing unit and power control circuits.

When a card loader contains a set of cards which are to be written, it is mounted on the memory card writer by clamping it in a vertical position to a carriage which forms a part of the card writing unit. This carriage is mounted on vertical rails at the sides which permit it and the attached card loader, to be indexed upward as successive cards are written. In Fig. 27 the carriage and loader are in a partially raised position.

At each index position, a pair of fingers on the card writing unit reaches forward, seizes the card in that location and draws it backward over a horizontal writing table to a fixed stop position. The card writing head then passes in a smooth, continuous motion across the card (Fig. 28). In this figure, a guard rail which prevents accidental interference between the fingers and the writing head has been removed for better visibility.

During its travel, which requires approximately one second, the head magnetizes the initializing magnets, senses the position of these along the length of the card, and magnetizes or demagnetizes each of the 2880 bit magnets. After passing the length of the card in a right-to-left direction (viewed as in Fig. 28), the head is returned to its normal position at the right, the fingers push the card back into the loader, the fingers disengage the card and return to an intermediate position, the loader indexes upward, and the cycle is repeated.

In the loader, the magnet sides of the cards face alternately downward and upward, corresponding to the alternately right and left directions which these cards face in the program store. Since only upward facing cards can be written, alternate cards are first written with the loader oriented as shown in Fig. 27. This sequence is called "pass A." When completed, the carriage and loader are automatically returned to the downward position and a buzzer sounds to alert the operator that pass A is complete. The loader is then inverted, end for end, reclamped to the carriage, and pass B is started, during which the remaining cards are written. The carriage is again automatically returned to the normal start position and the buzzer signals the operator that writing is complete.

The card writing unit and card writing head require moderately high precision in mechanical construction for satisfactory card writing. Sensing the initializing magnets to synchronize the writing function is done primarily to ease the mechanical tolerances for positioning the card in the longitudinal direction. The design incorporates fail-safe and interlock features to avoid or limit damage in the event of power failure or com-

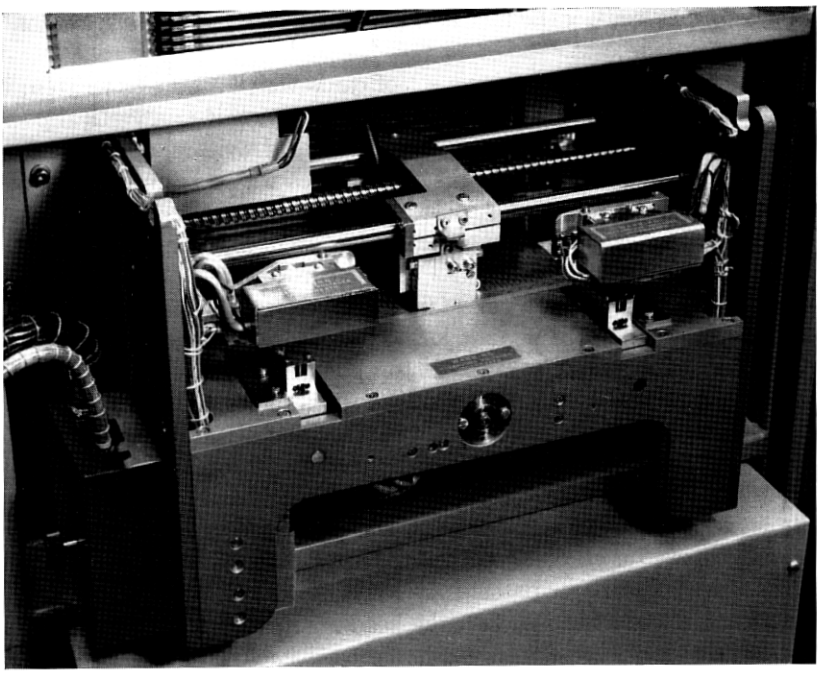

Fig. 28 — Memory card writer — rear view of writing mechanism.

ponent failure. The writing head and finger assemblies are designed for easy replacement in the field since they are more vulnerable to damage than some other parts because of repeated contact with the twistor cards. Also, the central mechanism portion of the writing unit, together with the writing head, have all electrical connections on a plug-in basis and can be removed from the frame for servicing or replacement by disconnecting two connector assemblies and removing four screws.

The card loader (see Fig. 29) is used to insert the twistor cards into and to withdraw them from the memory modules in the program store, to support the cards on the memory card writer during the writing operation, and to transport cards between the program store and the memory card writer. At the program store, the loader always inserts or withdraws all 128 cards of a set simultaneously, using a motor drive mechanism. The loader is controlled by means of three pushbuttons and a lever at the right, which is used to engage or release cards from the drive mechanism. In addition, an adjustable indicator assists the operator in keeping track of the particular store and module number with which he is working. Each memory module carries preadjusted brackets and

registration details which support the loader in accurate relationship with respect to the twistor planes in the memory. Moderately high precision is needed in control dimensions for the loader, memory module, and twistor cards for the loading and unloading operations to be carried out satisfactorily.

7.4 *Circuitry*

Successful card writing depends on accurate positioning information, which must be obtained from the initializing magnets. A head precedes the sensing head to magnetize these magnets. The initializing magnets are very long (130 mils) compared to the desired positioning accuracy (± 5 mils). The position sensing head has a special shape which develops a large pulse just as the head is centered over a magnet. Fig. 30 shows the sensing head and the relationship of the two gaps to the ends of the magnet. Only when the head is centered does the flux change through the two coils at the same time in an aiding sense.

Since there is a double row of initializing magnets, two heads are used alternately. The voltage from each head is amplified and sensed in an

Fig. 29 — Card loader in use on program store.

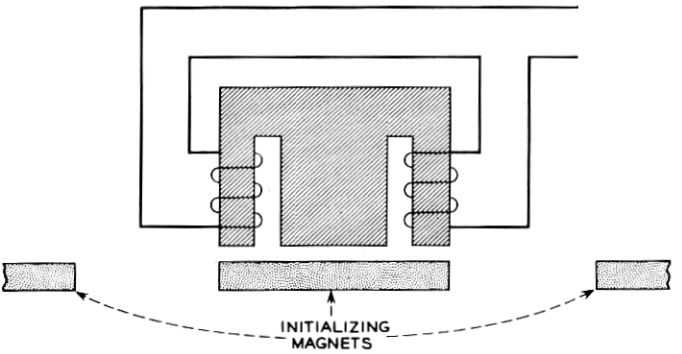

Fig. 30 — Position sensing head.

amplitude discriminator. To avoid false triggering, particularly during writing, the discriminators are enabled shortly before the proper head is at the expected position and are disabled as soon as writing is initiated.

Writing begins just as the write heads are approaching the center of a bit magnet. A relatively high frequency is used to magnetize or demagnetize the magnet. The basic waveform generated is a 20-kc sine wave which initially drives the heads into saturation and is gradually reduced in amplitude. The heads saturate at about 2 amperes of current at 26 volts peak amplitude. If it is desired to magnetize a bit, the waveform is altered during a saturated cycle just as the current crosses zero. The next current maximum is enhanced, and the current is forced to remain in the direction of that maximum. If the bit is to be demagnetized, the waveform is left on until the head is well off the magnet. The 20-kc waveform, Fig. 31, is developed by the circuit of Fig. 32. The head and two capacitors, C, form a resonant circuit which is in series with a Zener diode-capacitor network. The transistors are triggered "on" alternately for about 6 μsec, one each half cycle. The waveform reaches a peak in two to three cycles, at which time the head saturates. At this time the waveform is altered if the bit is to be magnetized, or made a zero.

To completely erase a bit magnet is difficult. Any biasing, either of unbalanced current through the head, or flux from an adjacent head, leaves a residue of flux in the magnet. Even a few milliamperes of unbalanced current can upset the erasure. It is difficult to obtain this degree of balance when the peak currents through the head are amperes. The Zener diode-capacitor network prevents slight differences in average voltages on the two sides of the head from causing unbalanced currents to flow but allows dc to flow through the head while magnetizing. During

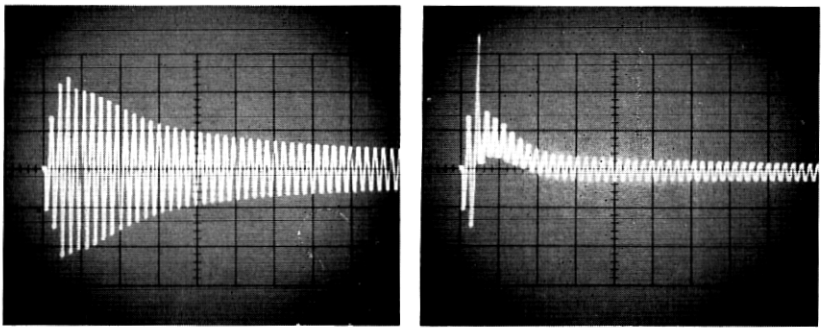

Fig. 31 — Basic demagnetize and magnetize waveforms.

the time the head is in saturation, exact balance is not maintained. Balance is recovered once the head is out of saturation, which occurs while the head is still over the bit magnet.

Biasing due to magnetizing adjacent magnets is avoided by essentially terminating the magnetizing currents during the early part of the demagnetizing period.

Additional circuitry is used for controlling the writing and mechanical sequencing of the unit. There are LLL circuits to check the count and

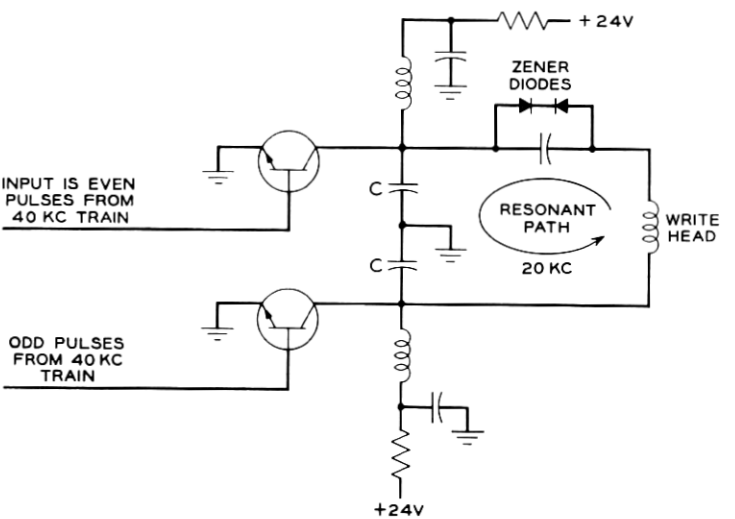

Fig. 32 — Circuit schematic — write head driver.

register the bits to be written. The control of the motors and solenoids is mainly by relay logic.

There are two drive motors, each 208-volts, 3-phase, 60-cycle. Both motors must be abruptly stopped, the head motor when at the home position and the finger motor when full forward and when full back. This braking is supplied by passing a direct current through two of the phases of the motors. The current is initially supplied by a large surge from a capacitor and is capable of stopping a 3600-rpm, fractional-horsepower motor in less than a revolution. The direct current is then allowed to decay to a value within the rating of the motor.

7.5 *Translation Changes*

Changing the translation information which is stored on the twistor memory cards is accomplished in the telephone office with the aid of two card loaders, the memory card writer frame, and a spare set of 128 twistor memory cards which is usually stored in one of the card loaders. The procedure normally followed in updating translation information is as follows:

(1) The first module to be rewritten is selected and an instruction is typed to the system identifying this module.

(2) A card loader containing the spare set of cards is mounted on the memory card writer in the pass A position and appropriate buttons are pressed to initiate the writing. On signal, the loader is inverted for pass B and the remaining cards in this set are written.

(3) The first store in which the module is to be updated is removed from service by means of the "request inhibit" button on the control panel.

(4) On signal that the store is out of service, the cards are removed from this module by means of the second card loader and are immediately replaced with the newly written cards in the first loader.

(5) The verify button is depressed, and upon a signal that the new cards are correctly written, the store is returned to normal service.

(6) Steps (2) to (5) are repeated in order to rewrite cards in the memory module containing the duplicate of this information.

A simplified diagram for changing information for a single set of cards in one program store is shown in Fig. 33. The machine time required for processing a set of 128 cards in the memory card writer is approximately 10 minutes, and time required by the card loader for inserting or withdrawing a set of cards from a memory module is approximately $\frac{1}{2}$ minute each. Including manual operations, a total time of about 12 minutes is required to update information in a single memory module. However,

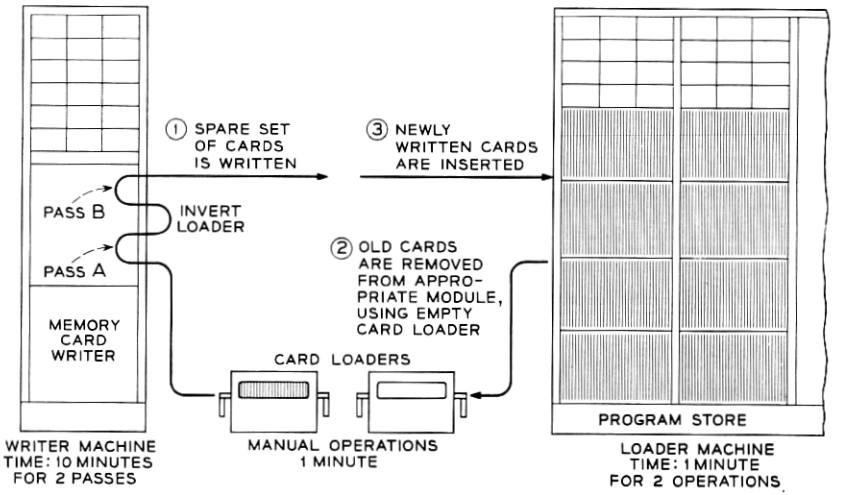

Fig. 33 — Card writing sequence.

it is seen that the down time during which the store being changed is unavailable to the system is only a little more than one minute per module.

In the event that a set of cards is incorrectly written, this is indicated after insertion into the store by the failure of the "verify" lamp on the control panel to light. In this case the new cards are immediately removed and replaced with the old set, and the store is returned to service.

7.6 *Program Changes*

In an operating office there is seldom an occasion for writing program information. However, during system debugging work this is the primary use of the card writer. To facilitate this operation a special laboratory machine called a tape reader assembler and processor (TRAP) was developed.

TRAP contains a conventional digital tape transport, a small core buffer memory, and a moderate amount of logic. Ordinarily, TRAP is supplied with a tape prepared on a commercial data processor containing the program information in the order the card writer will write it. TRAP reads the tape into the buffer and supplies a word at a time to the card writer.

An alternate mode of operation of TRAP permits the writing of a single word on a card. This is of considerable usefulness in making short program corrections.

The modifications to the card writer for TRAP operation involve the addition of several special circuit packs. These are not normally provided in an operating office.

VIII. PERFORMANCE

The program store is designed to operate over wide battery voltage limits (42 to 52 v) and ambient temperatures (32°F to 115°F) with any stored pattern of information. The evaluation of a unit of this size to assure it has met its design objectives is far from an incidental part of the development program. Ultimately the full evaluation requires operation with a complete ESS. To achieve a simulation of such operation a test set was developed to operate the store and analyze its outputs. The large number of variables involved in such an operation is clear from the control panel of the test set (Fig. 34).

Because the store has a read only memory, evaluation with different patterns of information is laborious. In lieu of actual worst-case patterns, a limited number of worst-case repetitive patterns is used. To ensure that under actual worst-case patterns the store will retain margin, the one-to-zero ratio must remain above 2.5 to 1 for the repetitive patterns. A very large number of tests of this type were carried out on a prototype store at varying conditions of temperature and worst tolerance circuits. These led to changes in both circuits and modules during development. Four stores of essentially final design have been operated for more than five store years in an actual system environment. As would be expected from the worst-case design approach, this operation has uncovered no case of errors not associated with failures of circuit or writing.

Circuit failures have been gratifyingly low despite the usual initial troubles encountered in first manufacture of a complex system. The average failure rate has been one package a week, but has shown suspicious bunching that pointed toward inexperienced debugging techniques. The mean time to failure has steadily risen during the interval.

Card writing performance has been generally excellent. The objective of erasing or writing to a point where no decrease in store margins could be assigned to card writing has been consistently realized. This required a ratio of 26-to-1 in magnet field strength between a zero and a one. Forty-to-one (2 gauss to 80 gauss) is generally obtained.

Error-free writing has not been as easy to obtain. A bit error rate exceeding 1 in 10^7 has been routinely achieved but at this rate to produce error-free modules requires rewriting one in ten. Most errors have been due to communication or mechanical problems. It is expected that an improvement of a factor of 10 will be achieved before the initial service

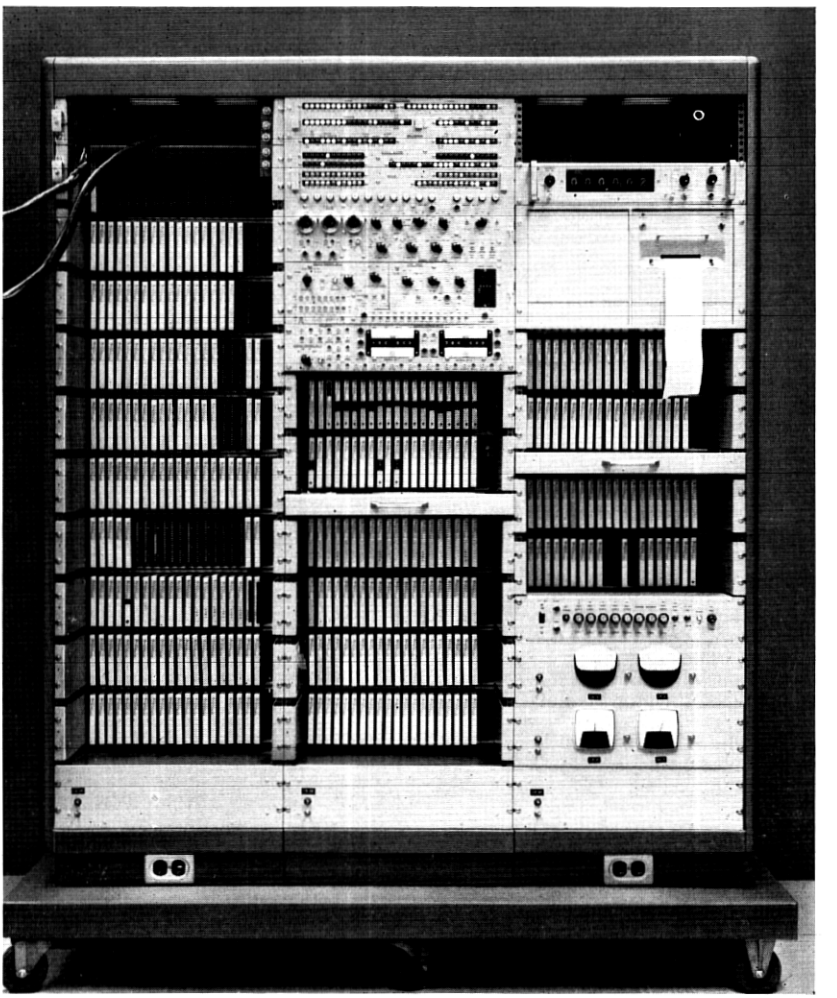

Fig. 34 — Program store test set.

date. This improvement is desired mainly to eliminate the nuisance effect of errors, since the system can tolerate a small number of errors in translation information through the recent change mechanism which allows any program store translation word to be superseded by a call store entry.

The program store has been evaluated against all of its initial objectives, and in all cases has met or exceeded them. A separate evaluation of the memory modules has been carried out and reported.[7]

IX. ACKNOWLEDGMENTS

The design of the program store has involved a large number of people, both directly and indirectly. It is not possible to acknowledge individually all of the many contributors but we are well aware that without them the development could not have been a success. The authors wish especially to acknowledge the excellence of the twistor modules developed under the direction of L. W. Stammerjohn and J. J. Suozzi.

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