No. 1 ESS Call Store — A 0.2-Megabit Ferrite Sheet Memory

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A call store is an 8,192-word, 24-bit per word memory system using multi-aperture ferrite sheets in a destructive-readout, coincident-current configuration and operating in a 5.5-microsecond read-write cycle. It is designed for 40-year life and operation in ambient temperatures from 32°F to 115°F.

The paper describes in detail the memory medium and memory circuits. General description is given of call store usage on the common bus in the No. 1 ESS and the maintenance and diagnostic features provided. Finally, a discussion of testing and test pattern philosophy is included, along with results measured on production stores.

I. INTRODUCTION

1.1 *System Requirements*

As the name of the call store implies, its prime function is to provide the read-write or erasable storage for all the call-related temporary information processed by the No. 1 electronic switching system (ESS).

Aside from the conventional call processing functions,[1] other common system functions involving administration, maintenance, AMA and TTY buffering and network simplification (by map and queue techniques) are also assigned to the call store. This concentration of system functions has imposed rather large capacity requirements on the store. Of course the total number of bits required is a function of both the number of lines in the office and the number of calls per busy hour. A range of 100,000 to 4,000,000 bits is required to cover the gamut of office sizes and calling rates envisioned for No. 1 ESS. To achieve a compatible solution, a specific store size is required to provide a modular building block with few stores in small offices and many in large offices.

Maintainability and dependability considerations imposed rather extensive requirements[2] on the call store. A duplication scheme to permit

economic growth by single stores requires splitting the memory in each store into two halves or two information blocks, with common access circuitry used for both. Each information block is then duplicated in another store.

Furthermore, high-speed and reliable communication between the call stores and the central controls, as well as the high-speed switching of duplicated information blocks, calls for the use of a bus system.[3] All the call stores in the office share the same set of signaling and addressing leads, with each call store on the bus capable of recognizing its own name code (sent as part of the address) and responding with the addressed word. Each store must communicate over either or both duplicated buses as directed by the central control. Furthermore, the central control must have the option of changing or rerouting these central control-call store bus assignments at system cycle speeds, thus bypassing faulty individual stores or buses to achieve an operational system.

Special maintenance control modes are required to permit use of the normal communication bus for the interrogation of various internal test points within the store and also the alteration of the operational features of various internal circuits. Separate monitor and direct scanning buses with access to additional internal points are also necessary to allow alternate channels of interrogation. The system requires verification of proper operation and transmission. This is accomplished by a parity check on each address received, as well as tests of a number of internal store circuits.

Finally, the call store must be designed against a 40-year life requirement with no program or environmental restrictions. These requirements dictate redundancy and safeguards against catastrophic failure, so that failures can be rectified by maintenance. Standardized plug-in circuit packages must be used to make failed components readily accessible and rapidly reparable.

II. DESIGN OBJECTIVES

2.1 *Memory Medium*

The basic memory medium selected for the call store is the multibit ferrite sheet with a 16 × 16 array of holes.[4,5] A copper conductor is evaporated and subsequently electroplated onto the sheet in a pattern forming the equivalent of a copper wire threading through all 256 holes in series.

The plated lead on the homogeneous sheet is a prime factor in achieving low memory module fabrication costs, since this eliminates the tedious

hand wiring operation that would be necessary to interconnect 256 discrete memory elements in an equivalent manner and lends itself to automated high-level manufacturing techniques. Also, the precise geometry of the ferrite sheet permits easy registration of holes in large stacks, and this simplifies and reduces the cost of the few hand wiring operations that remain.

The use of ferrite sheets also reduces the number of soldered connections over the use of discrete memory elements by a factor of 5 to 1. This is extremely significant in large-scale memories and enhances the over-all reliability and dependability.

To achieve these benefits in terms of cost and reliability, a considerable initial device development effort was required, which, based on present-day yields and performance, was well worth the effort.

2.2 *Store Characteristics*

The organization of a single call store is chosen to provide a capacity of 8192 words of 24 bits, or a total storage capacity of 196,608 bits. This appears to be a size that satisfies the minimum requirements of small offices and provides the growth flexibility for the larger offices. The 24-bit word length and the 5.5-μsec cycle are dictated by general system considerations and do not represent an attempt to realize the maximum capabilities of the memory. A median-size office of 10,000 lines having a calling rate of 13,000 calls per busy hour would require only two basic call stores. Of course, two additional units would be added for duplication purposes. Many smaller offices would require only one call store and one duplicate, while large offices would require up to 40 total stores.

The 768 ferrite sheets necessary to provide the 196,608 bits are wired for coincident-current access. A 13-digit binary address is necessary to control the access selection.

2.3 *Environment*

The call store must be operational over an ambient temperature range of 32°F to 115°F without recourse to environmental control.

2.4 *Simplified Block Diagram*

The simplified functional block diagram of the call store is shown in Fig. 1. There are four major blocks: the memory module, the memory circuits, the logic and sequence circuits, and the maintenance circuits.

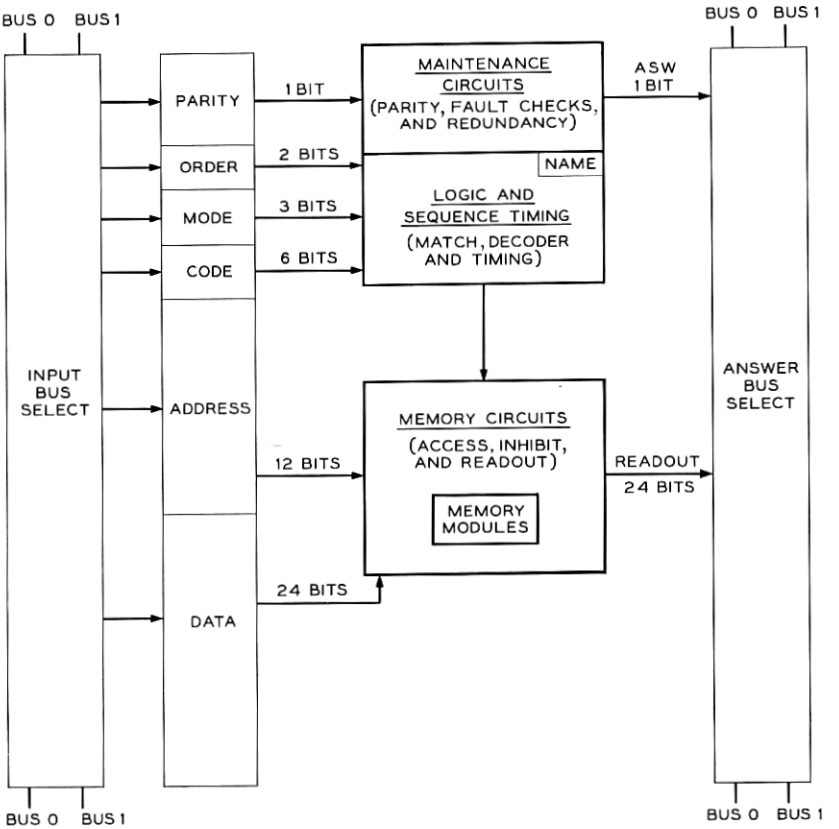

Fig. 1 — Simplified functional block diagram of call store.

2.4.1 *Memory Modules and Memory Circuits*

The ferrite sheet memory modules are surrounded by the memory circuits. A 12-bit memory location address directs the access circuits to switch the 24 "holes" desired in either of the two information blocks in the store. A single bit is derived from the name code to select one of the two information blocks. The readout signals from the memory are amplified and returned on the answer bus.

In the "write" mode the data register is set by the 24-bit data pulses received via the input bus.

In the "read" mode the data register is used for buffer storage of the readout, which is then rewritten into the memory.

2.4.2 *Logic and Sequence Circuits*

The logic and sequence control circuits decode the incoming 6-bit name code, the 2-bit read or write order, and the 3 mode bits to determine whether or not the call store should respond and in which mode of operation. Internal timing circuits are also included in this block.

2.4.3 *Maintenance Circuits*

The maintenance circuits check the correctness of the single parity bit generated over both the code name and address. These circuits also verify a number of internal store test points, and if these and the parity are all satisfactory an "all-seems-well" pulse is generated and sent on the answer bus.

Aside from the basic read and regenerate and erase and write modes, other modes are added to facilitate the maintenance of the store.

First, a "maintenance" mode is added in which the store responds as a memory but most of the flexibility in store selection and in store response is eliminated. Only one store can respond, and the store address is uniquely pinpointed by the incoming address.

A "control read" mode permits the interrogation of test points within the store. It accomplishes this by bringing the test data from the selected test points through the data register out on the answer bus.

A "control write" mode allows central control to alter the internal control states in the store. Special data and address codes are used to internally manipulate all the circuitry without actually switching the memory. Thus central control is able to electronically change the particular memory assignment or code name of a store.

The three major circuit blocks, along with the memory modules, will be discussed in detail in the following sections.

III. MEMORY

The basic storage device is a multiaperture ferrite sheet approximately 1 inch square and 30 mils thick. Each sheet contains a 16-by-16 square array of holes 25 mils in diameter, placed on 50-mil centers. The material used in this device is a mixed magnesium-manganese ferrite similar to those used in square-loop toroids but with a higher Curie point, which allows an extended temperature range. Square hysteresis loop characteristics of 1.9 oersteds coercive force, 1800 gauss saturation flux density and 0.97 squareness ratio are the governing parameters of the material. However, behavior of the material surrounding a hole is also influenced by

neighboring material and magnetic field distribution. Each hole, when excited by approximately 250-ma coincident-current pulses, acts as a square-loop memory core with the field constrained to the annular region immediately surrounding each hole. Interaction effects are reduced by generating opposing fields in neighboring holes. In this application the typical disturbed "one" output of a switched hole is 75 millivolts with 0.9 μsec switching time.

A printed copper conductor linking all the holes on a sheet is one of the four necessary conductors (see Fig. 2). The three remaining wire conductors are threaded after the ferrite sheets are mounted into stacks.

3.2 *Constraints of Large Coincident-Current Ferrite Sheet Memories*

Three of the four conductors combine to form a standard coincident-current access.[6] In this application there are 128 X coordinates and 64 Y coordinates whose product (8,192) equals the number of words in the memory. Simultaneous half-read currents, I_d, along one of the X and one of the Y coordinates, are sufficient to fully switch the selected holes of an address to the read or "zero" state but will not disturb any of the many holes half-selected by X current and Y current. Subsequent re-

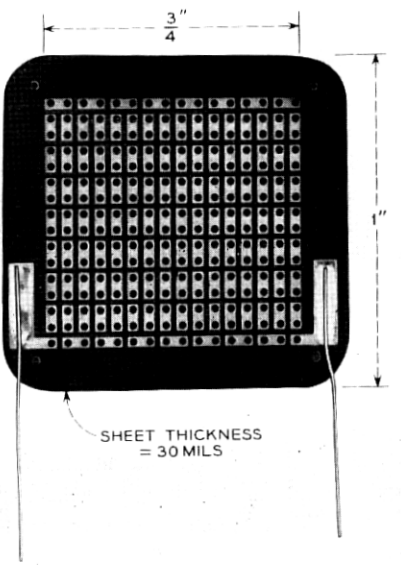

Fig. 2 — Ferrite sheet.

versal of current on the same conductors switches the previously selected address to a write or "one" state unless a separate read direction half-drive, called an "inhibit current," is applied on another conductor. For a 24-bit word there are 24 distinct bit planes, each containing an inhibit conductor and a sensing or read conductor; both are coupled through all the 8,192 address-location holes.

The major constraint in coincident-current memories is on the sense wire noise voltages due to the accumulation of signals across holes excited by the half-current drives. Attempts are made to cancel these signals by directing half the sense and drive lead hole intersections positively and the remaining half negatively. However, the positive and negative noise voltages, which are functions of information storage, past history and addressing sequences in other sections of the memory, do not cancel exactly, leaving a residue called "delta noise." A byproduct of delta noise is the large and variable load imposed upon the X, Y and inhibit drivers. The impedance to a driver, due to the summation of the inductances of each hole which is pulsed by the driver, is a function of the information stored and the remanent state of flux. These factors are, in turn, a function of the memory contents and the prior addressing sequences. The variable-load inductance, as well as the large interwinding capacitances, forms complex transmission lines that impose severe design problems on the drivers.

Methods of generating delta noise and driver loading variations are discussed in Section 9.2.

A unique problem to the ferrite sheet is the interbit reaction due to magnetic coupling of flux between the holes. To combat interhole coupling, special flux constraining wiring patterns are used which limit the fields to annular regions about each hole. (See Fig. 3.) The constraint is simply generated by guaranteeing that any hole selected with a full drive during read or write intervals is countered by an opposite half drive in the nearest neighbor holes. Therefore special wiring rules, covered in the next section, are applied.

The fixed 16-by-16 array of holes imposes another constraint, because this size must be used as the basic building block. But this larger-size sheet reduces the number of connections and improves reliability. The 24-bit per word application necessary in No. 1 ESS is achieved by coupling the sense wire through two adjacent rows for each bit; the 16 rows in a sheet can be subdivided into 8 row pairs which allow 8 bit planes. The full complement of 24 bits is formed by using 3 stacks of sheets, each stack supplying 8 rows of paired bit planes. This folding of the read or inhibit plane complicates X-plane wiring because two sep-

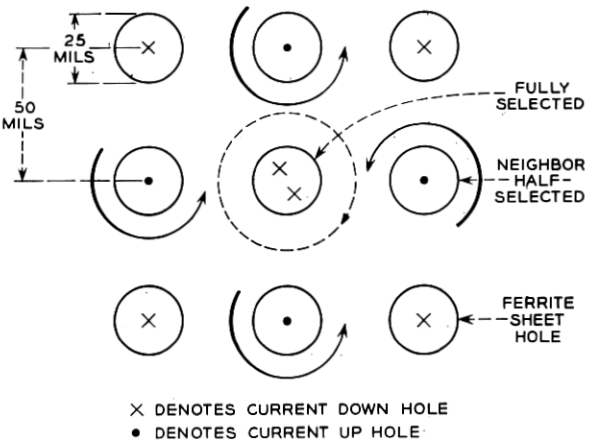

Fig. 3 — Flux locking.

arate X-plane conductors are necessary to guarantee that only 1 bit is switched in a bit plane and that all ferrite sheet holes are fully utilized.

3.3 *Basic Module — Size and Wiring Patterns*

The 8,192 words of a call store are obtained from 2,048-word modules which in turn are constructed from 512-word submodular assemblies. The modules are interconnected with all electrical connections on a plug-in basis, while the submodule assemblies are permanently mounted. Conductor length and possible increased manufacturing (yield) rejection are the major considerations which limit the maximum module size. The number of interconnecting terminals increases for smaller modules, with an accompanying reduction in reliability and an increased cost. A compromise between the yield or wiring length problems of a large module and the reliability or cost constraints of a small module has led to the 2048-word size.

The formation of the ferrite sheet module is dependent upon a number of noise-reducing techniques. An attempt is made to maintain all current carriers on a tight twisted-pair basis outside of a module and within the module, with geometric orthogonality between X, Y, and inhibit conductors. The positive and negative terminals of all conductors are arranged in close proximity. Since the read cannot be completely orthogonal with the X and inhibit, another basic requirement introduced complementary wiring with as much geometric symmetry as possible to realize balance and assist noise cancellation. Noise cancellation tech-

niques take on particular importance for the readout wire because of the large capacitive and magnetic coupling between drive and readout leads. Consequently, special noise cancellation wiring patterns are used.

A single ferrite sheet module is shown in Fig. 4. This unit with the four subassemblies, each containing three columns of sheets, is mounted with all holes in registration. The submodules are first fabricated with separate read conductors, each woven with special wiring patterns. These patterns (shown in Fig. 5) minimize coupling with the Y or inhibit drive lead by reversing the sense direction in a binary fashion. For example, the first two columns of read holes intersect the Y in the positive sense and the next two in a negative sense. For the next set of four holes the pattern is reversed. For the next set of eight holes the first eight-hole pattern is reversed, and so on. This scheme compensates for the variation

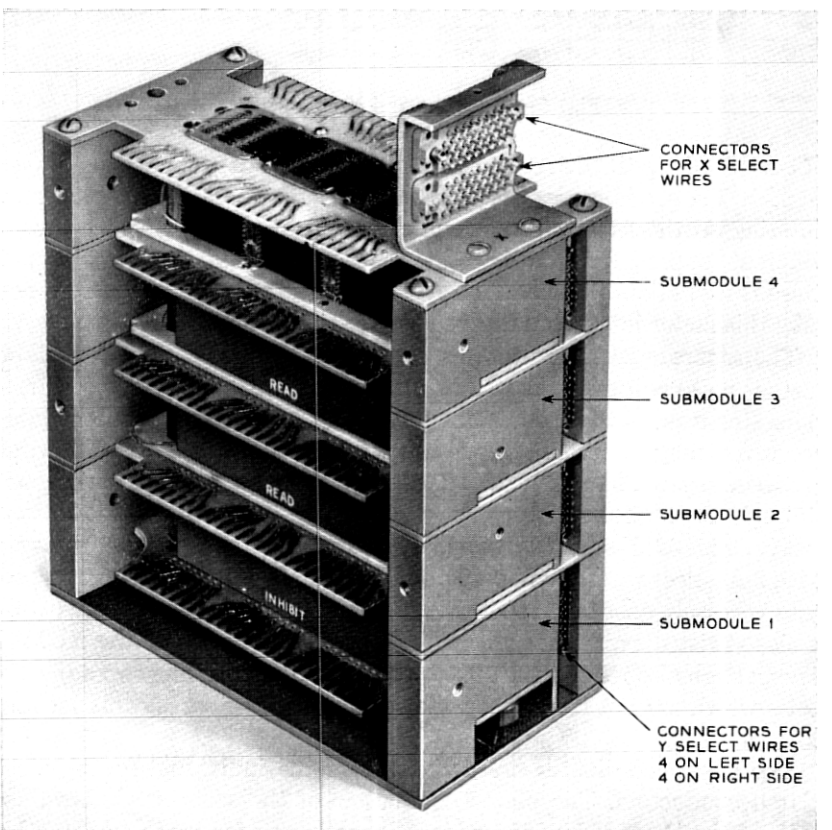

Fig. 4 — Module.

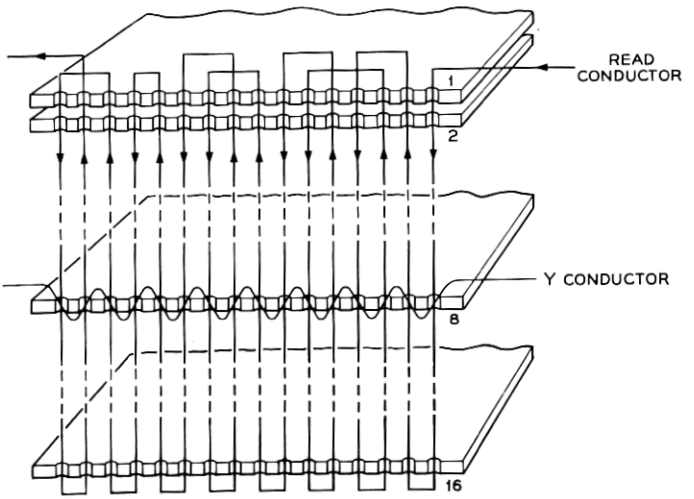

Fig. 5 — Readout and Y-axis wiring.

of current along the drive wire due to distributed capacitance losses (see Fig. 6). The shunt losses due to stray capacitance degrade the current entering on the left to that shown on the right. This difference causes different coupling from the drive to the readout wire and prevents proper noise cancellation. Simple inductive cancellation schemes which do not take this factor into account give less effective noise cancellation.

The separate 24 readout wires for each submodular assembly allow further noise reduction, as well as introducing flexibility of interconnections (for reasons to be described presently). Once the four submodules are wired they are mounted one above the other. The 24 inhibit wires are then inserted like the read wires, except that they pass up and down through all the holes of the four submodules in a simple up-and-down weave. The 32 X-select wires are threaded orthogonally to the inhibit, with 2 X-select wires per X plane, so that each X wire intersects a folded read wire only once on a sheet. Fig. 7 illustrates the X weave wired with a close-twisted pair arrangement both within and outside the module. The pattern also reflects the added requirement of coupling two adjacent holes which are not coupled by the same inhibit, to satisfy flux locking constraints.

The 64 Y coordinates are derived from the individual ferrite sheet plated conductors. The plated conductors of the same level sheets on each of the three stacks are soldered together to form a Y plane, with 16 Y planes per submodule and 64 Y planes per module. Although a

careful screening process on individual sheets is implemented prior to assembly, occasional defective sheets might occasionally appear in a finished module. One additional Y plane is included per submodule to allow a defective sheet to be replaced by a spare. This substitution is employed only in the manufacturing process.

To summarize the makeup of the completed module, there are four Y connectors on one side for entrance and four Y connectors on the other side for exit, each connected to a submodular assembly of 16 coordinates, each coordinate containing 3 sheets. The twenty-four twisted-pair readouts are brought out to four printed wiring boards, one at each submodule. One printed wiring board located at the bottom of a module provides access for 24 twisted-pair inhibits. Two connectors are located at the top of the module where the twisted-pair X-selected wires originate and terminate. Each module contains 64 Y coordinates, 32 X coordinates and 24 bit planes.

3.4 *Memory Organization*

Overcoming the prohibitive delta noise and the large, variable driver loads in an undivided or unduplicated memory, is a difficult goal for a

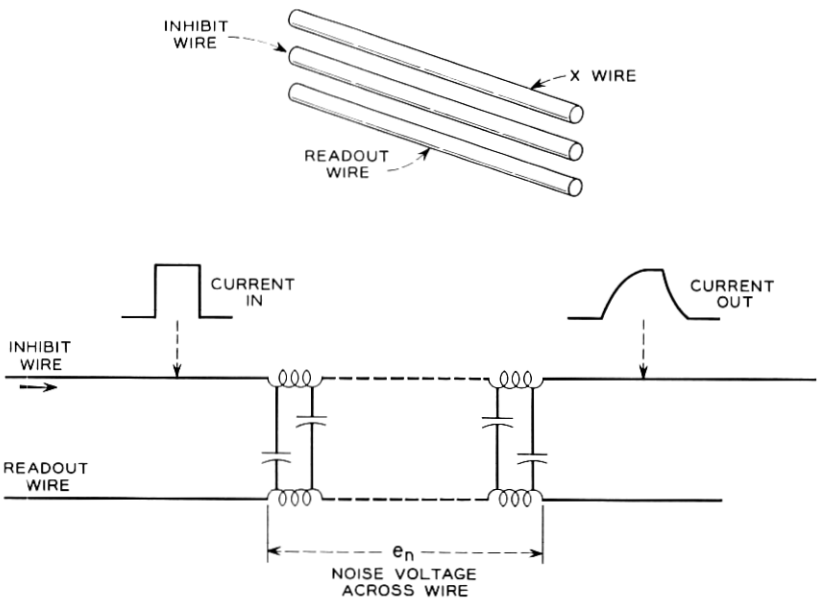

Fig. 6 — Inhibit transmission line.

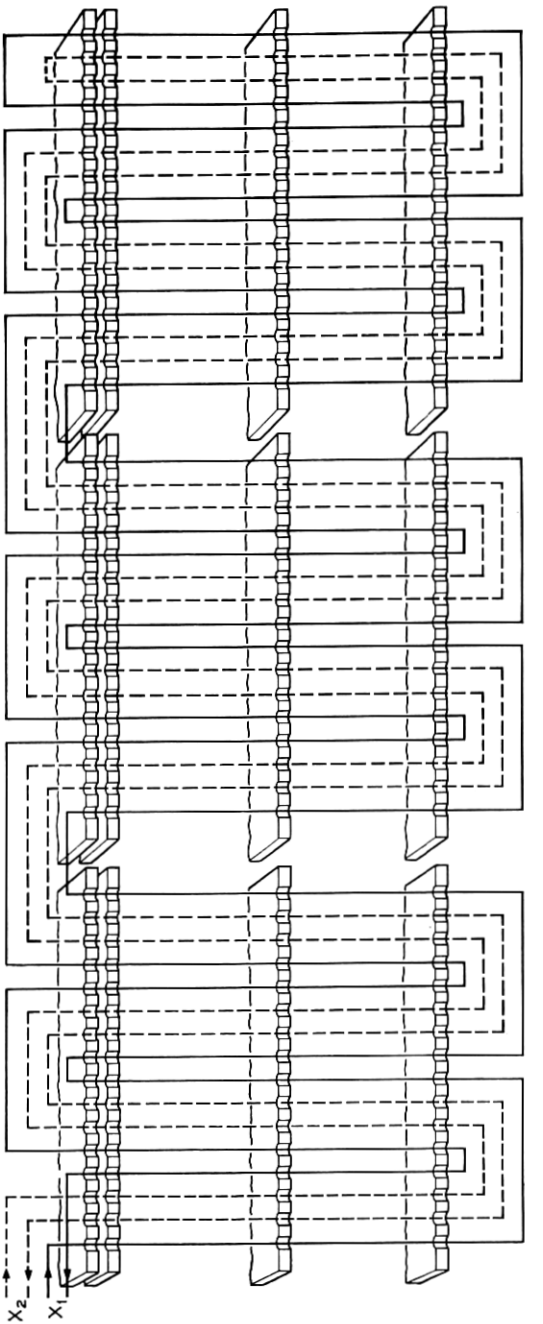

Fig. 7 — X-wiring module cutaway.

large memory designed for a 40-year life without potentiometer adjustments. Circuit schemes are introduced which drive large loads, stabilize currents, reduce delta noise via a post-write disturb, and shape current rise time. A novel scheme of measuring the noise with sample currents and subtracting the predicted noise during the read interval is also included. However, these appliques by themselves are insufficient to overcome the large delta noise of a full 8192-word coincident array with the extended life and reliability requirement of a telephone switching office.

Consequently, in this system the inhibit, read, and Y coordinates are subdivided and duplicated. The duplication is incorporated in such a manner as to minimize delta noise and reduce interactions between the coordinates, and cost reduction techniques are developed by utilizing common controllers as much as possible and placing the minimal hardware in the duplicate sections.

The interaction and delta noise minimization is illustrated by means of a Venn diagram (see Fig. 8). The matrix shown represents one of the 8192-word bit planes containing 64 horizontal Y lines and 128 vertical X lines. The matrix is split into 16 sections, each a 16-by-32 coordinate array with the upper 8 sections coupled to the A-read wire while the lower 8 are coupled to the duplicate B. The sections labeled α are driven by the α inhibit, while the remainder are driven by the duplicate β. The one-half length horizontal line, representing a Y current into the memory, shows the Y duplication, while the full-length vertical line represents an X current into the memory. The horizontal and vertical line segments indicate how the memory should be organized to minimize the coupling

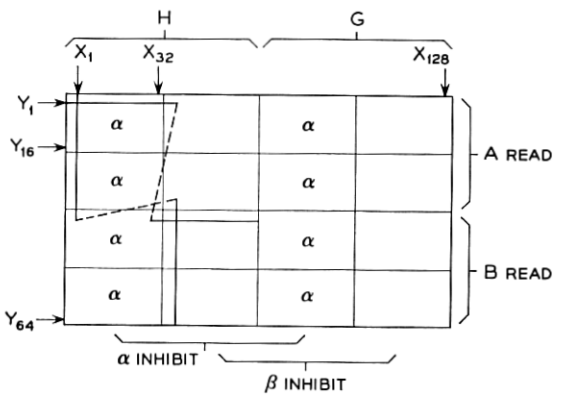

Fig. 8 — Bit plane, Venn diagram; minimum interaction and delta noise.

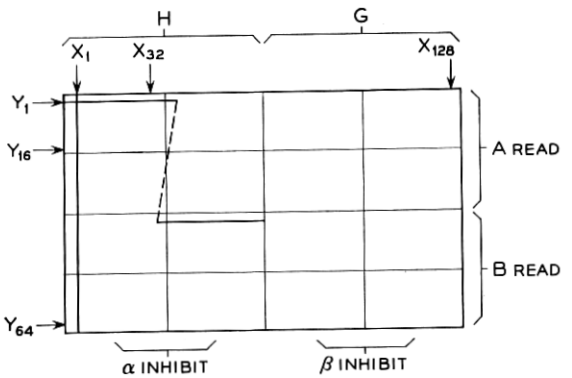

Fig. 9 — Bit plane, Venn diagram; compromise scheme.

of half-drive holes to the read wires and the coupling of inhibit currents to the X and Y wires. Since this organization is highly related to the module construction and fabrication, it is difficult to completely realize the objective; a compromise scheme results (see Fig. 9) which reduces terminal and solder connections.

Fig. 10 is a block diagram of the full 8192 words formed from 4 modules and shows the Y, inhibit, and read duplication. The first submodule read conductors are connected in tandem to the first, second, third and fourth modules. A jumper at the end cross-connects two adjacent read conductors to form a folded read plane. Each bit plane is split into two segments. One segment is derived by interconnecting the first and second submodules of all four modules, while the second segment is derived from the third and fourth submodules. Each segment is terminated by a separate preamplifier with 24 preamplifiers in the upper A half and 24 preamplifiers in the lower B half. The 2 preamplifiers per bit plane are recombined by an exclusive OR gate into a decision-level circuit.

The duplicated 64 Y coordinates are interconnected between modules so that Y currents through submodule 1 of module 0 will travel to submodule 3 of module 1. This type of cross connection reduces the Y-to-read noise by one-half. The Y-access source is an 8-by-8-by-2 three-dimensional matrix with current steering logic to decide if the G or H half is chosen. Through this technique the more expensive selecting switches and current generators are shared by both Y halves. Only the selecting diodes, some transformers, and two switches must be doubled.

The 128 X selections, with 32 X coordinates per module, are not duplicated. However, the noise coupling between the X and read has been cut in half because of the A and B read segments. For this access an

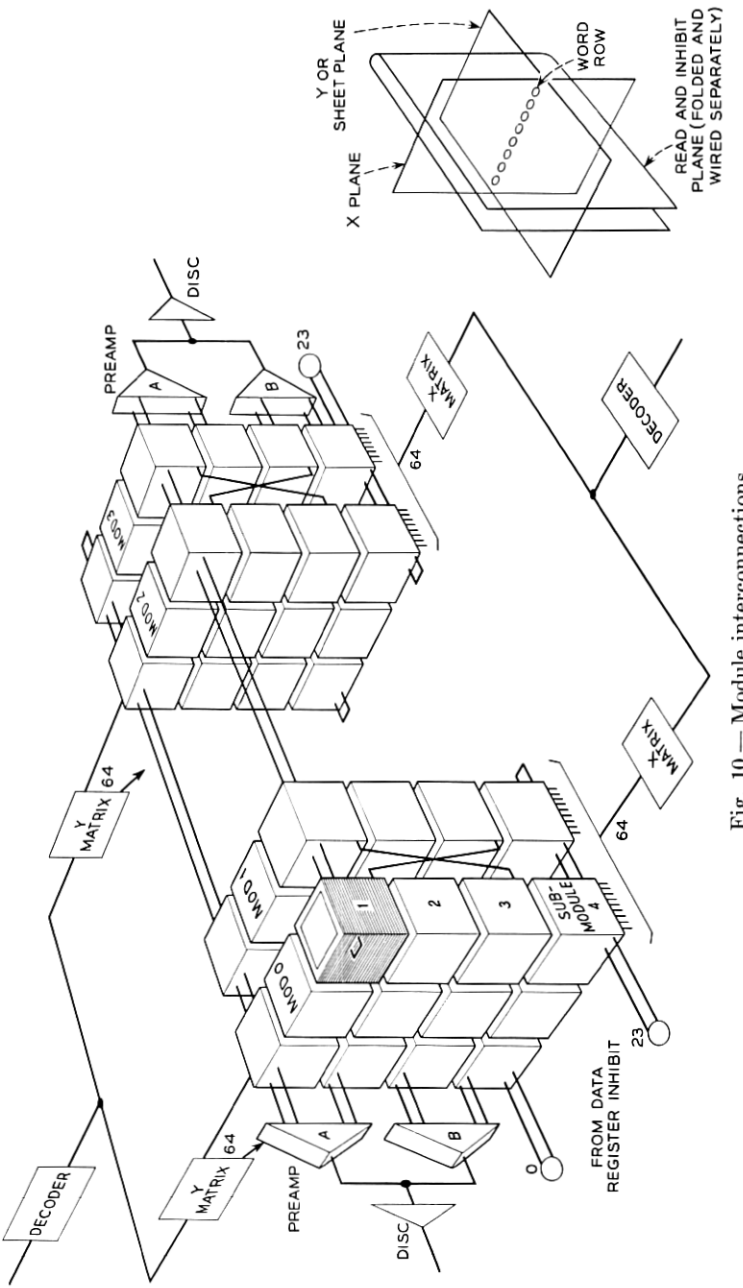

Fig. 10 — Module interconnections.

8-by-8-by-2 matrix, identical to the Y matrix, introduces significant cost reductions.

The 24 separate write back or inhibits also are duplicated because of the large inhibit wire inductance. One set of 24 inhibit drivers is coupled to the first two modules and the second set is coupled to the last two modules. This duplication is orthogonal to the read split to minimize the intersections between read and inhibit.

IV. MEMORY CIRCUITS

4.1 *Readout*

The readout complex is a circuit block which equalizes near- and far-end read signals to the preamplifier output. It contains two 3-stage high-gain transistor feedback preamplifiers with an EXCLUSIVE-OR gate for recombination of the read segments. DC restoration is used to reduce bias drifting caused by long bursts of unidirectional inputs, along with a scheme that measures the noise before sampling and subtracts the undesired noise from the output. The complex also accepts either positive or negative signals and samples or strobes the signal into a bidirectional gated-oscillator decision-level circuit (see Fig. 11).

Transmission line characteristics causing unequal response of read signals from near- and far-end points can create severe degradation of performance. To equalize the read response for both gain and phase, two transformers are used to couple both ends of the read wire, matching the characteristic impedance and balancing the transmission. The secondaries are connected in series to reconstruct the full source amplitude without attenuation.

The EXCLUSIVE-OR gate, dc restoration, and special noise measurement and subtraction functions are combined by a simple resistance-capacitance and bidirectional switch scheme (see Fig. 12). In this scheme the preamplifier capacitor output is shorted to ground by a clamp unless the preamplifier is chosen; if chosen, it is enabled only during the read interval. The small time constant formed by the low preamplifier output impedance and the low resistance in series with the capacitor allows quick discharge for dc restoration. After the clamp is open, the time constant is increased and the network transmits the preamplifier output with little attenuation. By opening the clamp during the early noise peak, the noise is measured and stored across the capacitor. During the subsequent sampling interval, the capacitor voltage subtracts from the input noise voltage, reducing the noise or undesired signal amplitude. The clamp is

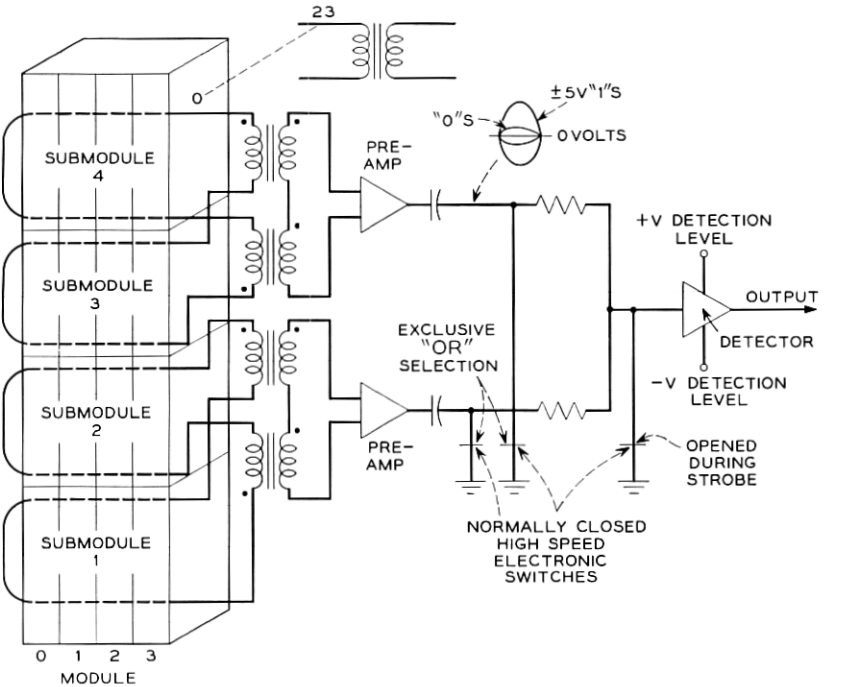

Fig. 11 — Read circuits.

closed shortly after the read sample is taken, to continue the dc restoration.

The bidirectional sampled signal is level-detected by means of a diode bridge arrangement (see Fig. 13). Input currents of either polarity in excess of the bridge currents back bias the diodes and raise the impedance, which changes the detecting amplifier from conditionally stable to unstable. The unstable state causes a severe oscillation, detectable as a "one" output. Use of a gated-oscillator technique with an amplifier normally biased in the class A region along with a current threshold detector significantly improves the sensitivity.

4.2 *Current Drivers*

A single transistor of the type available in No. 1 ESS was not capable of driving the large X or Y load with a 0.5-microsecond rise time. It was necessary to combine transistor circuits so that larger induced voltages could be accommodated. The solution chosen (see Fig. 14) combines 4

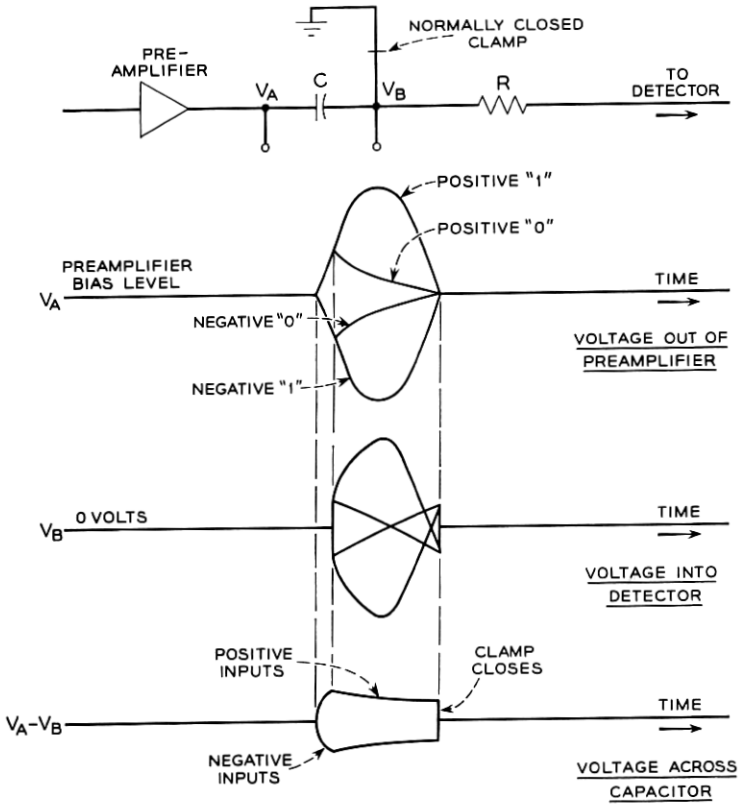

Fig. 12 — DC restoration noise reduction scheme.

separate read current drivers by means of 4 transformers with primaries in parallel and secondaries in series. A similar set of 4 write current drivers uses different windings of the same transformers; the write current drivers are fired after the read currents are turned off. The circuits, each a pulsed-current source of approximately 250 ma, combine to supply a 250-ma, 0.5-microsecond rise-time pulse in the read secondary during read time and in the write secondary during the subsequent write interval. This scheme not only distributes the load voltages but statistically improves stability, since the secondary current is equal to the average source current minus the average shunt transformer losses. The current standard deviation is one-half of a source current driver deviation, because the average of n independent but equal variables has a standard deviation reduced by $\sqrt{n}$.

Repetition rate effects are eliminated because the unbalanced transformer flux of the read interval is recovered by the reverse polarity drive of the subsequent write interval.

One added feature in this scheme is the two-step current rising shape. Rather than stagger the start of the X and Y currents so that the early X noise expires first, both currents are turned on in coincidence with a 125-ma first step and a 125-ma final step. This staircase is useful in three ways. First, the load voltage transients are smaller. Second, the early quarter-drive currents sample the coordinates without fully switching the selected address and the resultant readout noise is stored in the read preamplifier capacitor; during the subsequent full drive when the actual address is gated, the capacitor voltage is subtracted from the second step incoming signal, causing a significant reduction in delta noise. Third, the first step of the current staircase acts as a partial pre-read disturb, removing part of the undesired delta noise and precharging stray capacitance.

The variation of coercive force with temperature necessitates a reduction of drive current as the ambient increases. Currents should track within ± 2 per cent of an optimum value at any given temperature. To

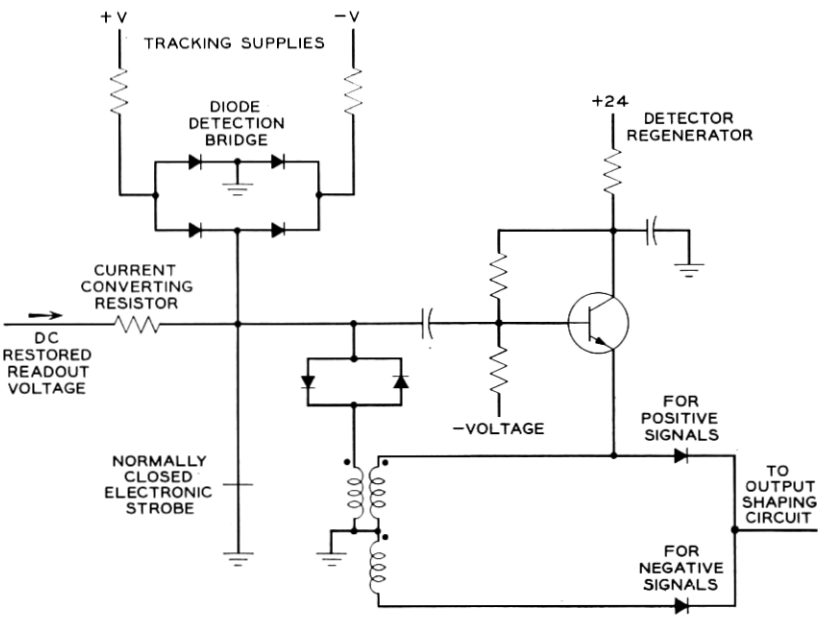

Fig. 13 — Detector.

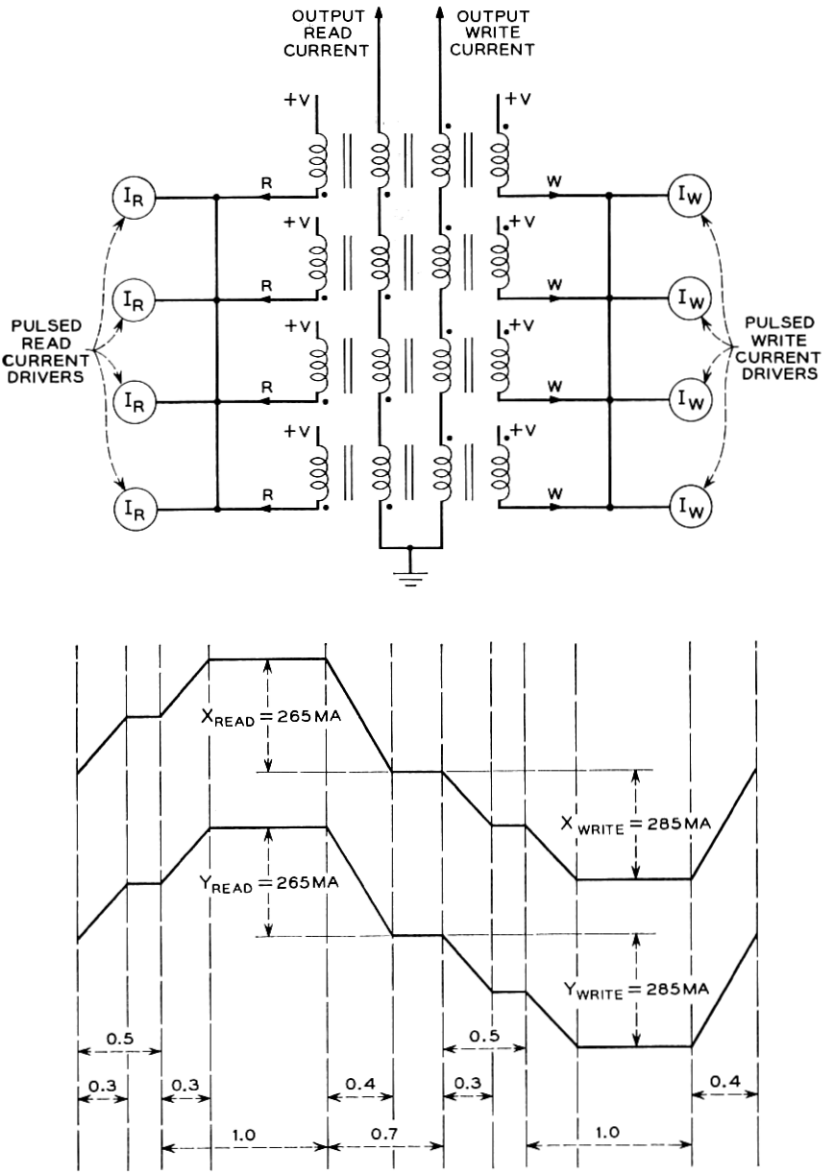

Fig. 14 — Current drivers. All values are μsec except those indicated otherwise.

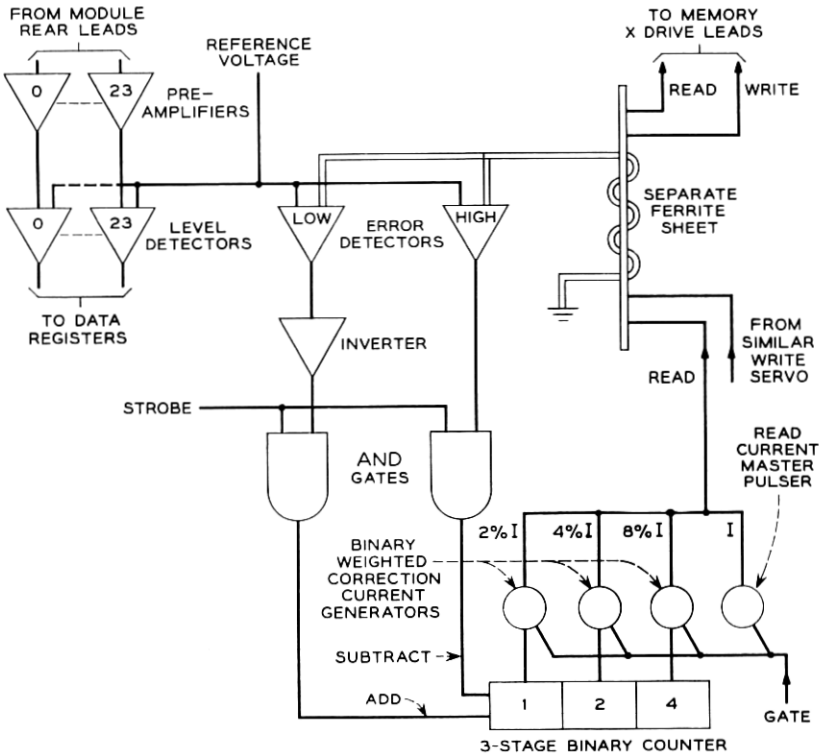

Fig. 15 — Current stabilizing servo loop.

achieve a constant readout over the ambient range of 32°F to 115°F, this optimum current must be varied by 20 per cent. The precise tracking over this large current range is accomplished by means of an electronic analog-to-digital servo loop (see Fig. 15). Two turns of the read and write drive currents pass through 16 holes of a separate sensing sheet. An equivalent 8 turns couple the sum of the 16 switching signals out of this sheet into a high- and low-level detecting circuit. If the signal is lower than a bias voltage, a one-step add command into a 3-stage binary counter is initiated. If the signal is high, a one-step subtract command is initiated. The three counter stages directly control three auxiliary current circuits whose amplitudes are binary weighted at 2, 4, and 8 per cent of the nominal value. This system automatically adjusts itself so that the sensing ferrite sheet peak output signal is constant at the high-low detector bias voltage level. However, since the ferrite sheet coercive force

changes with temperature, the currents are automatically adjusted to maintain constant peak switching voltages. This adjustment corresponds exactly to the required variation of drive current with temperature changes. Another significant feature is the stabilizing nature of the ferrite sheet, which, in addition to the extremely low aging drift, is due to the nonlinearity of the device. The product of the 16-hole switching voltage (V) and the switching time is approximately constant for full drives, but as the current (I) is raised, the voltage increases in the following manner:

$$dV/V = 4dI/I.$$

A 2 per cent variation in input current results in an 8 per cent variation in output signal. In this application the ferrite device amplifies the hard-to-detect small current drift and develops a large voltage variation which is easier to detect.

The drift effect of the high-low detector bias voltage is also reduced by tracking this supply with the readout detector level voltage. A downward voltage drift reduces the servo loop current, which in turn lowers the memory output signal. However, compensation for the decreased output signal is achieved by a simultaneous lowering of the readout detector threshold.

These current driver schemes are used both for X and for Y. Each contains an individual servo loop with independent controls. The X and Y read and write currents are also threaded through another sensing ferrite sheet, with the resulting 500-ma sum of the X plus Y read currents resetting 16 holes and the 500-ma sum of the X plus Y write currents setting the same 16 holes. The amplified voltage output of the 16 holes is used as a timing source for the readout clamp and sampling signals. Because of this arrangement the critical timing signals track the current rise-time variations.

4.3 *Access*

In this system the X and Y access circuits are identical. The 1-out-of-128 coordinate selections for the X (constructed from two sets of 1-out-of-64 selections circuit), is realized by a circuit identical to that which derives the two sets of 1-out-of-64 for the Y. Costs are minimized by employing a 3-dimensional $8 \times 8 \times 2$ diode array as the selecting source; the 1-of-128 selections can be decoded by 18 transistor switches. The positive read and negative write current bidirectional requirements, which normally necessitate a duplicate set of switches, have been satisfied with unidirectional circuits by employing a four-winding transformer-

coupled switch scheme in which a common selection of all the secondary windings determines the direction of current.

Fig. 16 illustrates a 1-out-of-64 access grouping with current drivers of the type described in Section 4.2. One of the eight horizontal and one of the eight vertical dc switches are simultaneously closed by decoding the input binary address. During read time, a closed read ac switch directs the current through the primary read winding of the selected horizontal transformer to the closed horizontal switch. This generates a pulse in the read secondary winding through the selected load, down a column line, through the selected vertical transformer, and back to the read secondary winding of the horizontal transformer. The vertical transformer is chosen by first shorting the primary to ground through the selected vertical switch and then establishing a +24-volt bias on the unselected column lines, so that all diodes in the unselected seven columns are back biased. During the subsequent write interval a closed write ac switch directs the current through the write primary winding of the chosen horizontal transformer. This reverses the current in the secondary loop and recovers the unbalanced flux generated during the read interval. The necessary biases to uniquely select one of the column lines are derived by precharge switches which insert a −24-volt bias on all unselected columns.

The combined group of the 8 horizontally arranged transformers is called an "input marker" and the combined group of the 8 vertically arranged transformers is called an "output marker." The set of 8 horizontal and vertical dc switches is shared by two groups of input markers, output markers and diode matrices. (See Fig. 17.) Each group is uniquely selected by a primary ac switch. By this technique only the passive markers and diode matrices must be duplicated when extending from a 1-out-of-64 to a 1-out-of-128 scheme.

A highly significant byproduct of the access is the precharge feature. The stray and interwinding capacitances of unselected memory coordinates can cause severe current leakages into unselected locations until these capacitances are charged. Leakages, which destroy the fidelity of the current rise-time shape, occur even if an ideal system with ideal switches is used. This system precharges all the capacitances until the unselected diodes are back biased.

4.4 *Inhibit*

The 48 inhibit drivers are simple pulsed-current sources whose amplitudes are determined by a 5-volt reference bias. The voltage is designed

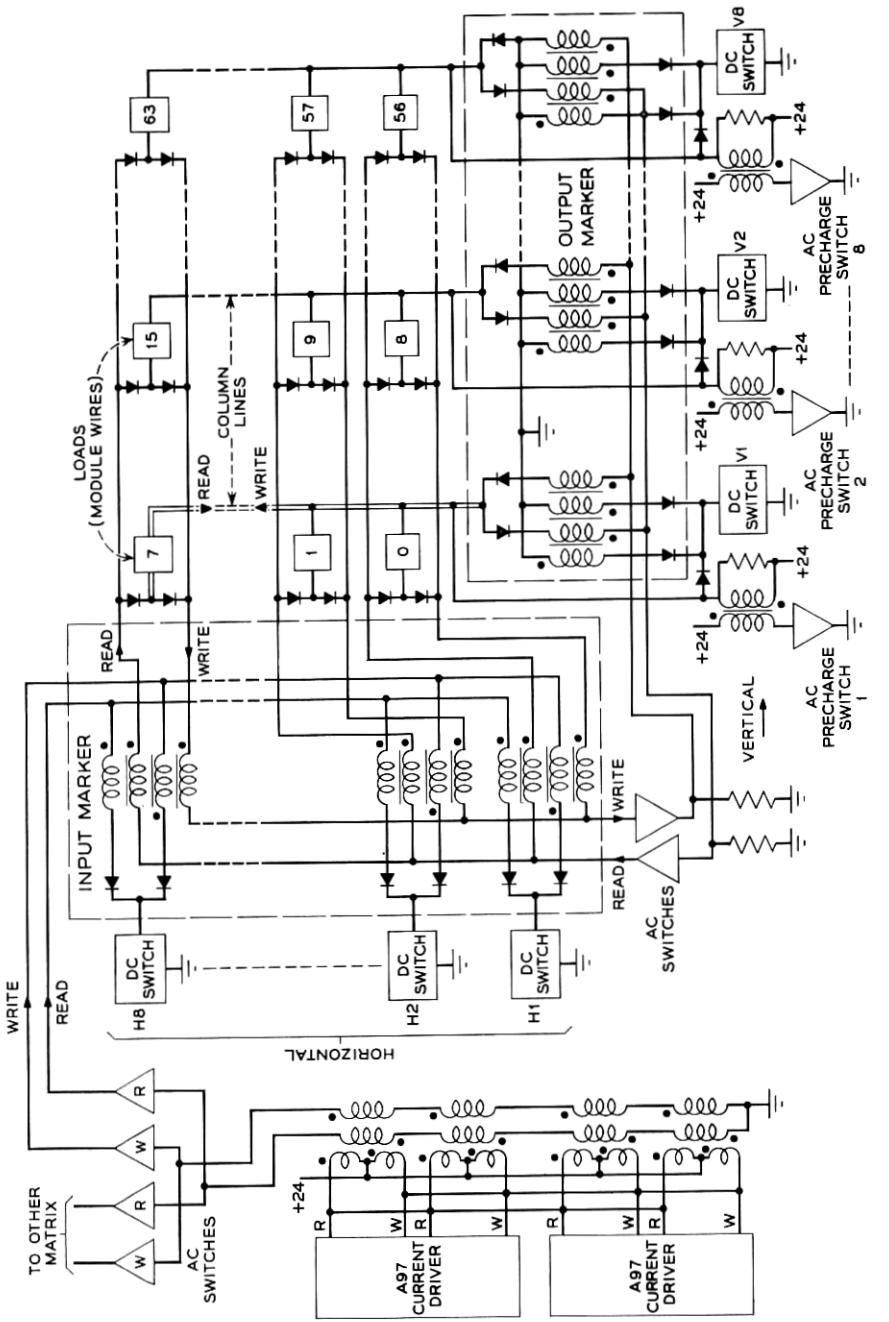

Fig. 16 — 1-out-of-64 selection matrix.

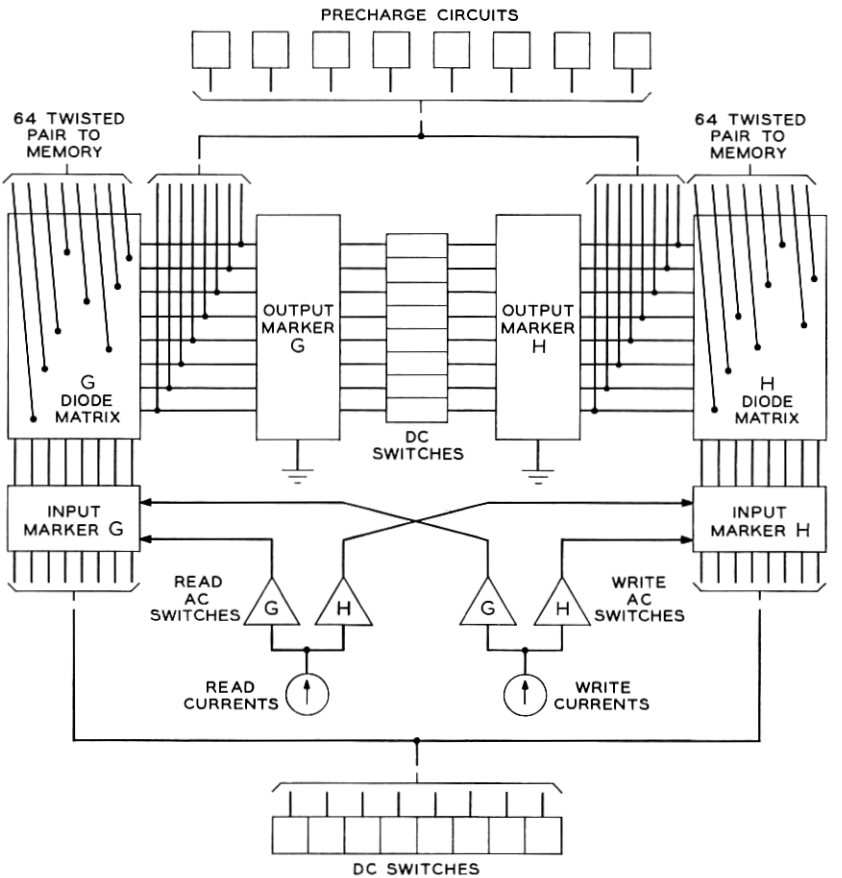

Fig. 17 — Input markers, output markers, and diode matrices.

to vary with temperature to properly compensate the inhibit current with ambient temperature. The major feature of the inhibits is the application of a post-write disturb (see Fig. 18), which reduces delta noise by referencing all holes with a half-read drive.

V. LOGIC AND SEQUENCE CIRCUITS

5.1 *General*

As shown in Fig. 1, the No. 1 ESS call store is a self-contained memory system that can read or write information, as ordered, in any externally

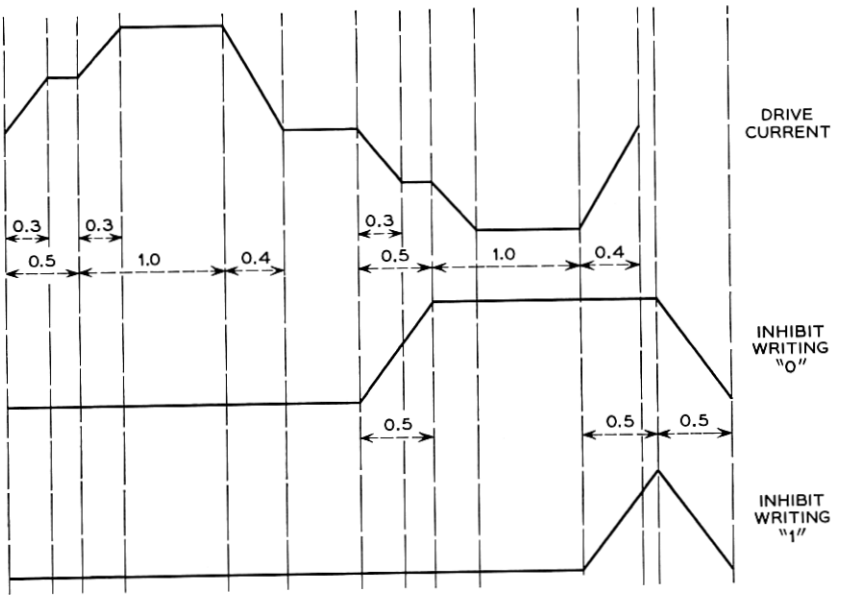

Fig. 18 — Inhibit current with post-write disturb. All values are μsec.

specified address location. It contains logic circuits such as address decoding and data registration, and timing circuits typical of memory systems. However, it also contains a wealth of maintenance and checking circuits not typical of memory systems. Its operation can be considered as an independent subsystem with self-diagnostic facilities. Much of the logic design is concerned with the operation of the call store in the larger system. Of particular interest is the common bus communication which provides duplication of memory and eliminates the need for expensive private buses in central offices with widely varying memory requirements. Other important sections are the automatic maintenance circuits, including fault-recognition and trouble diagnosis, which integrate the call store operation with the system maintenance plan.

5.2 *Common-Bus Communications*

Inputs are transmitted over a duplicated bus shared by all call stores. Each store is preset to receive from one of the buses by an internal flip-flop called the "R_0 flip-flop," which is controlled in each unit by a separate input channel. A call store will consistently receive from the same bus unless a trouble condition arises.

All call stores on the common bus receive and register every order.

An order is processed and the answer returned if the 6-bit input code matches the store name. In effect, the code is part of the information address and from the system point of view the 6-bit code and 12-bit address make up an 18-bit address for the entire office temporary memory file. For convenient bookkeeping, however, the office temporary memory is broken up into 4096 word blocks. The 12-bit address selects one word location within a block and the 6-bit code selects the memory block within the office. Recall that for growth economics the 8192-word capacity call store is divided into two 4096-word blocks called the "G half" and "H half" ("Gee" and "Haw" being a mule driver's terminology for "right" and "left" respectively). The code name of the H half is wired in a store at installation and is called the "fixed name." The G-half code name, called the "variable name," is contained in 6 call store flip-flops which are under system control and can be changed in a 5.5-μsec cycle.

Fig. 19 shows three call stores on a duplicated call store bus. As shown, all three units are set to receive from bus 0. Answers from the H half of each store are sent back on bus 0. G-half answers are returned on bus 1. A read order with a code of 1 will activate CS1 and CS3. Each store sends the answer on a separate bus, where central control match circuits can check for a fault in communication or memory action.

Routing of answers from the G and H halves is controlled by four answer flip-flops in each store. The answer flip-flops can be set in any combination, so that either half may answer on either, neither, or both buses. Answer flip-flops, like the variable-name flip-flops, can be set in a 5.5-μsec cycle by a control mode order from the central control.

5.3 *Bus Receivers and Registers*

All inputs to the call store are routed to register flip-flops, and the essential memory circuits use the semi-dc outputs of these registers.

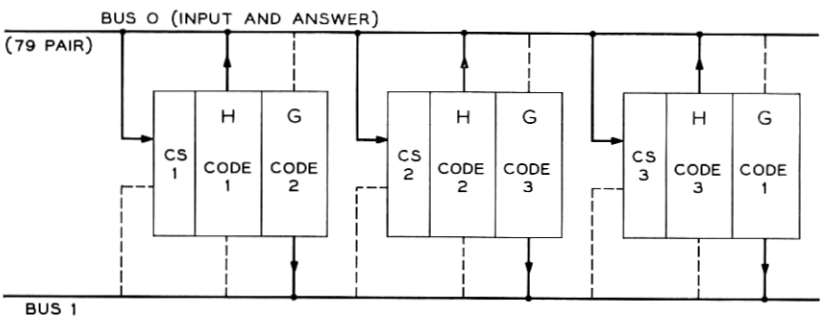

Fig. 19 — Call stores on bus.

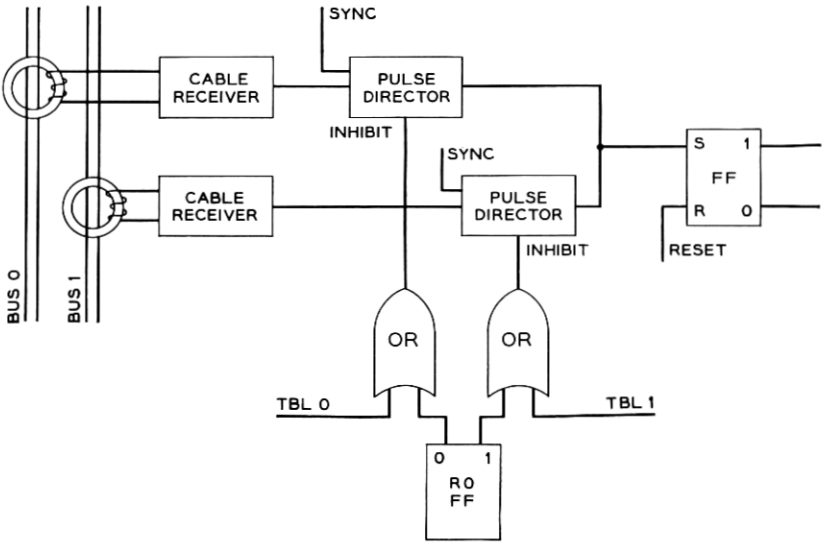

Fig. 20 — Bus input path.

Fig. 20 shows a typical input path. The inputs from the separate buses are transformer coupled to cable receivers and transmitted to "pulse director" circuits. The pulse directors gate the inputs with their associated sync pulse and may inhibit the input. Bus selection is made by inhibiting the unselected bus input at the pulse director. Also shown in the figure are the TBL0 (trouble on bus 0) and TBL1 inhibiting functions. These leads are controlled by a separate communication channel and can be used to shut off inputs from either or both buses.

The outputs of the pulse directors are logically added to set the register flip-flops. All inputs, code, mode, address, order, and data are single-rail, and the register flip-flops are reset by internally generated pulses at the end of each cycle.

The diagram in Fig. 21 gives the complete contents of the input and answer buses along with the nominal timing.

Each wave of information on the input or answer bus is accompanied by a time-coincident sync pulse. The receiving circuits require the coincidence of the sync pulse and the information to protect against false operation on bus noise.

5.4 *Modes*

In the "normal" mode two call stores respond as a regular memory to every order. Under trouble conditions it is necessary to communicate

with a single store in order to determine the location and nature of the trouble. For this purpose, two maintenance modes are used in which the call store responds to a code match with the fixed name only. Thus two maintenance modes are necessary to define the H or G half of a given store. These are designated "H maintenance mode" (HMM) and "G maintenance mode" (GMM). The call store operates as a normal memory in the HMM and GMM; however, only the fixed name is used for selection and the store answers and receives on the same bus.

The fourth and final mode of operation is the control mode. Here the call store does not operate as a memory — no ferrite is switched. In the control mode, the write operation sets flip-flops or initiates conditions in the call store and the read operation sends the state of flip-flops or other test points to the system via the answer bus. For example, setting the 6 variable-name and 4 answer flip-flops is a control mode, write operation. The first 20 bits of the 24 data-input leads carry the set and reset information for the 10 flip-flops. A corresponding control mode read operation returns the state of the variable name and answer flip-flops to the central control on the normal answer bus.

5.5 *Orders*

The read and write orders are received in a redundant code over two bus leads. In the normal and maintenance modes, R,W = 10 is a legitimate read and R,W = 01 a legitimate write. The inputs R,W = 00 or 11 are trouble conditions; however, drive currents have started before the

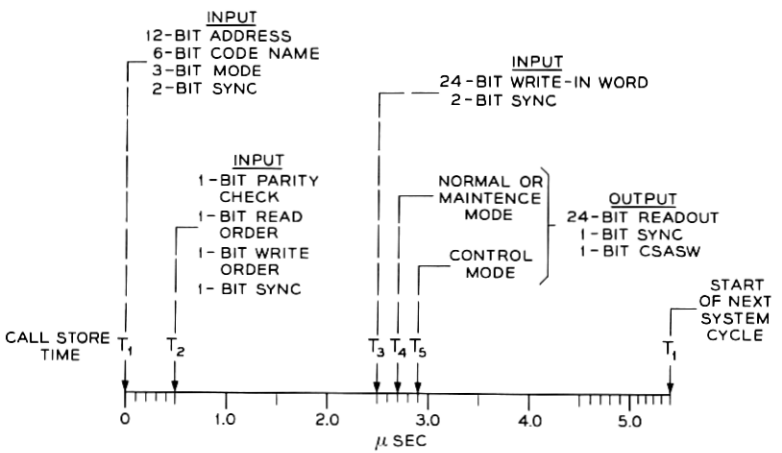

Fig. 21 — Timing of input-output signals.

order is decoded and cannot be interrupted. Illegitimate orders are therefore converted to read orders and no ASW is returned with the answer. A good write order, R,W = 01, is also converted to a read order if the ASW circuits detect any trouble. Thus information is safeguarded by forcing a regenerate sequence if any ASW failure is detected.

In the control mode all four combinations of the read-write order leads are used. Control read and control write operations are used, and the corresponding order bits R,W = 10 and 01 are required. The control functions are further defined by a control address which uses the four least significant address bits. To test the control address circuits themselves, however, it is desirable to have a control order that is independent of address so that all combinations of address inputs can be tested. To this end, the normally invalid order combinations R,W = 00 and 11 are used to read test points associated with the addressing circuits. These special orders check the Y and X portions of the address registers as well as the dc switches in the memory access circuits.

5.6 *Addresses*

In the memory modes, the 12-bit call store address defines one word in the half-store, 4096-word memory block. This block is generally visualized as a square 64 × 64 array in an XY plane. The six least significant bits constitute the Y address. The memory access system described earlier further divides the six Y bits into two groups of three bits each. Each three-bit group is decoded into a one-out-of-eight selection by the dc switches. Selection of the X-drive switches is similarly derived from the six most significant address bits.

In the control mode the address bits select one of the possible control operations in a manner analogous to the selection of a memory location. Since only a few control locations exist, only the four least significant address bits are needed for control addresses. For example, the name and answer flip-flop control address is octal 3. Therefore (see Fig. 19) if we send on bus 0: control mode, code = 3, address = 3, and order = read, the right-hand call store will reply that its variable name is octal 1 and that its answer flip-flops are set to return H-half answers on bus 0 and G-half answers on bus 1.

5.7 *Data Channels*

Call store data are handled by 24 identical channels, one of which is shown in Fig. 22.

During a read order in the normal or maintenance mode the output of

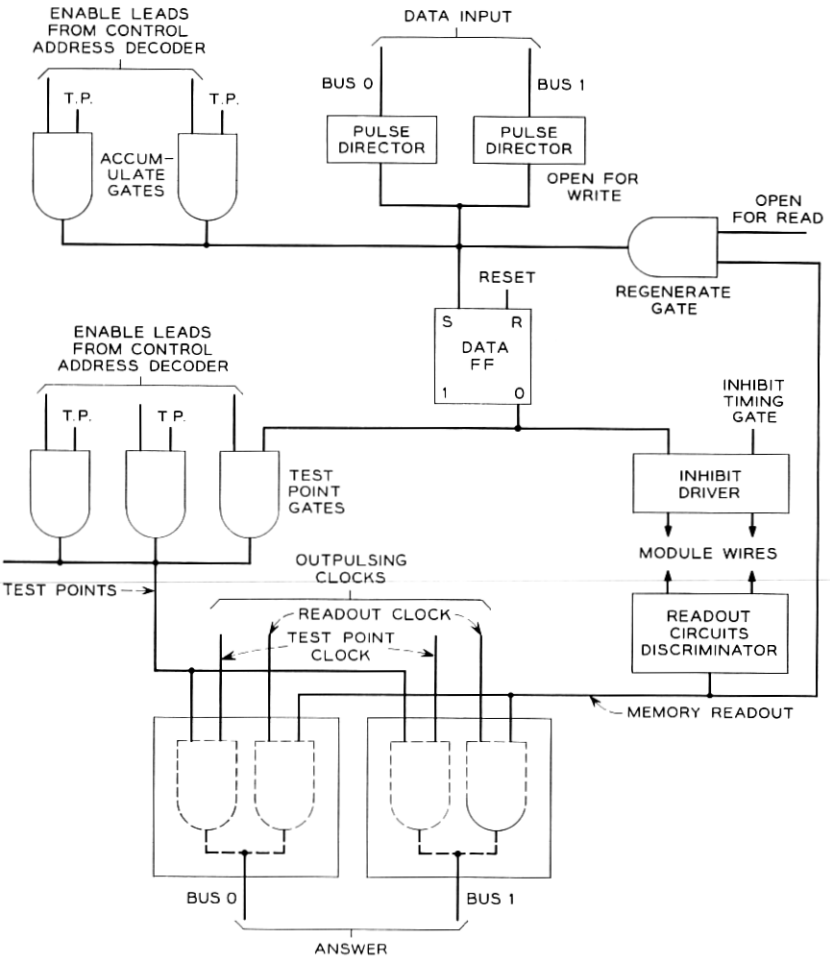

Fig. 22 — Data channel.

the discriminator is gated onto the selected bus by a readout clock pulse. If the mode is normal the four answer flip-flops select the answer bus and either, neither, or both buses could be pulsed. In addition, on a read order the regenerate gate is open and the discriminator output sets the data register. If a 1 is read from memory the data register flip-flop will be set, the associated inhibit generator will not fire, and a 1 will be rewritten in the memory during the write portion of the call store cycle. When a 0

is read out from memory the data flip-flop remains reset, the inhibit generator fires, and a 0 is written in that bit.

For a write order in the GMM, HMM or normal mode the sequence is the same except the regenerate gate is closed, the input data pulse director is enabled, and the data register is set or not set from the bus. On a write order the read part of the call store cycle is used to erase existing information.

Both input data and readout are single rail; the data registers are reset by an internally generated pulse. One of the data register reset pulses is generated at the end of the write-back drive current, 0.5 μsec before the end of the inhibit gate. Therefore all data flip-flops are reset while the inhibit gates are still open, and as a result, all inhibit drivers fire, producing a post-write disturb signal.

In the control mode the data channels are used to transmit test point information to the central control. The flip-flops themselves serve as pulse accumulating registers in two control read cases.

For semi-dc conditions that exist throughout a cycle, or at least exist when the output is gated on the bus, the test point gates are used. Pulses that occur at odd times during the cycle are checked by first giving a control write order to accumulate the pulses in the data register. This enables one of the accumulate gates shown on Fig. 22. The timing pulses, if and when they occur, set the data register flip-flops, whose contents can be read out if the next order is a data register control read.

VI. MAINTENANCE CIRCUITS

6.1 *General*

The maintenance circuits are designed to accommodate a system philosophy of fault recognition and trouble location quite different than those used in most information processing machines. The prime objective is to maintain the continuity of system operation. Thus the first action is to locate the faulty store and remove it from service. Detailed diagnosis which will isolate the fault to a specific plug-in package can then be accomplished on a deferred or low-priority basis. The possibility of 40 or more call stores in an office accents the demand that diagnosis be automatically programmed and as complete as possible.

Flexible switching provides rapid rearrangement of the bus configuration, and the variable-name facility allows the location of memory blocks to be reassigned to retain a duplicate copy of priority information. Because of the complete information duplication and the flexible communication, the system can survive even if half of the stores fail.

The existence of a trouble is generally noted by mismatch between duplicate stores, parity failure, or failure of "all-seems-well" (ASW). Mismatch and parity are clearly over-all checks that include the entire communication link between central control and the stores. Furthermore, they indicate trouble on the bus or in a complete call store rather than detecting failure of some circuit within a store. The ASW circuits do detect specific conditions within a unit, but the system's use of the ASW pulse does not elaborate on the nature of the failure; it merely specifies which store is in trouble.

Table I lists the maintenance facilities in a call store along with their primary functions.

The duplicate bus answer matching as well as the input and answer bus selection were described previously. These insure alternate routing to carry on communication in spite of failures and allow cross checks between channels to weed out faulty links. The maintenance mode orders, which enable the system to choose specific addresses in specific stores, have also been described. The functions of the maintenance mode orders as well as the remaining maintenance facilities are discussed in the following sections.

6.2 *All-Seems-Well (ASW)*

There are six conditions tested by the ASW circuit:

(1) The order combinations R, W = 00 and 11 cause ASW failure. In the normal mode they indicate trouble. In the control mode, these combinations are legitimate but they still cause an ASW failure. However, this failure is intentional and is used to test the all-seems-well circuit.

(2) Parity failure causes ASW failure.

(3) An invalid mode input causes ASW failure.

(4) Simultaneous operation in the control mode and a memory mode causes ASW failure.

TABLE I — CALL STORE MAINTENANCE FACILITIES AND FUNCTIONS

All-seems-well (ASW)	fault recognition in communications
Address parity (over code and address)	
Duplicate bus answer matching	over-all fault recognition
Stored parity (code, address and data)	
Input and answer bus selection	communication diagnosis
Fault flip-flops	logic diagnosis
Control mode orders	
Maintenance mode trouble location	memory circuit diagnosis
Monitor bus	
Scan points and central pulse distributor	store status test

(5) Simultaneous operation in both the G and H halves of the store causes ASW failure.

(6) A permanent code name match causes ASW failure.

The all-seems-well circuit makes all six tests during every call store operation, normal or otherwise. If there are no irregularities this circuit returns an ASW pulse along with the readout onto the answer bus. However, if a trouble is detected the store answer is transmitted without the ASW pulse and the call store is forced into read and regenerate operation regardless of the input order. This restriction on memory writing protects information from being destroyed when the incoming orders are incorrect and is particularly useful with address parity error detection.

6.3 *Fault Flip-Flops*

Five fault flip-flops are included in a call store to detect and register the occurrence of intermittent or transient faults. Either maintenance programs or a maintenance man using teletypewriter control can use the fault flip-flops to locate the general area of intermittent or marginal troubles.

The fault flip-flop indications provided are:

(1) all-seems-well failed,

(2) both the G and H halves were selected simultaneously,

(3) the store tried to operate in the control mode and a memory mode simultaneously,

(4) test point data were sent along with memory readout on the answer bus, and

(5) the code match circuit has a permanent decoder output (PDO).

Item (5) is particularly troublesome. A PDO means that a store will answer an order with any input code and mask the bus with unwanted signals. If PDO is detected, a call store will set both of its own trouble flip-flops, thus taking itself out of the system. This is the only case where the call store tampers with system status or bus selection.

6.4 *Monitor Bus*

The monitor bus is an 8-pair bus common to all call stores, on which test points may be connected through relay contacts to a ferrod scanner. In the call store the monitor bus is used exclusively to test regulated voltages. The outputs of two voltage regulator boards of the same type are connected through current limiting resistors to opposite sides of a bus pair, and the ferrods detect current flow if the output voltages are different and out of tolerance.

6.5 *Address Parity and Stored Parity*

Every memory mode order (normal or maintenance mode) includes a parity bit over the code and address. This parity is checked in the call store. Failure of parity causes failure of ASW and will convert a write order to a read order. Central control is informed of the trouble when it fails to receive the ASW answer pulse and can take corrective action. Since the write order is not executed, information in the incorrectly selected address is not destroyed.

Another parity bit is transmitted to the call store during memory write orders. This parity is over code, address and data. It is stored in memory as the 24th bit and returned to central control when the word is read. This parity is not processed in the call store and is treated as any other data bit. However, central control interprets the parity and checks for errors.

6.6 *Maintenance Mode Trouble Location*

Diagnosis of the memory module and its associated circuits is primarily done by storing and reading information. The faulty package is located by noting at what addresses storage fails and/or in which data channel. For example, a bad diode matrix will cause errors along one X or one Y address. A bad input marker will cause 8 consecutive addresses to fail. Bad output markers cause every 8th address to fail.

To increase the selectivity of this type of diagnosis, associated circuits are packed on the same printed wiring boards, and common operations are grouped to cause recognizable failure patterns. As an example of the latter statement, the 24-bit data register is reset in groups of 12, the inhibit generators are pulsed in groups of 8, and the regenerate gate and input pulse directors are gated in two groups of 8 and 16.

6.7 *Scanner Points and Central Pulse Distribution*

The bus routing R_0 flip-flop, the two error status trouble flip-flops, and the code match indication flip-flop have a very high degree of influence upon call store operation. Therefore the indication of state of these flip-flops is not trusted to the regular bus communication system. Instead the outputs are directly connected to a direct reading ferrod scanner.

The R_0 flip-flop and the two trouble flip-flops are so critical that separate system control of the setting or resetting commands are required.

In these cases the set and reset inputs are directly connected to a central pulse distributor which can alter the flip-flop state.

6.8 *Control Mode Orders*

The control mode operations complete the survey of maintenance features. These are essential for automatic programming diagnosis through the central office facilities. They allow the system to interrogate the inner core of a call store; many circuit failure conditions do not have to be interpreted by evaluating memory readout, but can be directly tested. A test such as the "read Y dc switches" sends back onto the answer bus the binary condition of key circuits in the Y access, which indicates the contents of the Y section of the address register and the Y-access decoding circuits.

6.9 *Control Mode Operations*

(1) Write data register,
(2) read data register,
(3) write name and answer flip-flops,
(4) read name and answer flip-flops,
(5) write — set current correcting servo counter to all 1's,
(6) write — reset servo counter to all 0's,
(7) read servo counter test points,
(8) read fault test point group,
(9) write — accumulate timing pulse group 1 in data register,
(10) write — accumulate timing pulse group 2 in data register,
(11) read Y dc switches,
(12) read X dc switches.

VII. EQUIPMENT

Equipment design of the call store consists of a highly functional layout in which the ferrite sheet memory modules, located behind a shield below the center of the frame (see Fig. 23), are surrounded by the access circuits at the sides and readout and inhibit circuits above and below. This permits the necessary short paths to be maintained for the readout connections while minimizing interference from the access and inhibit circuits. The logic control circuits and cable drivers are located near the top of the frame, below the terminal strips with which they connect. As indicated in the figure, the call store follows the general pattern of equipment design for No. 1 ESS.[7] With only a few exceptions, components are mounted on plug-in circuit packs. External connections

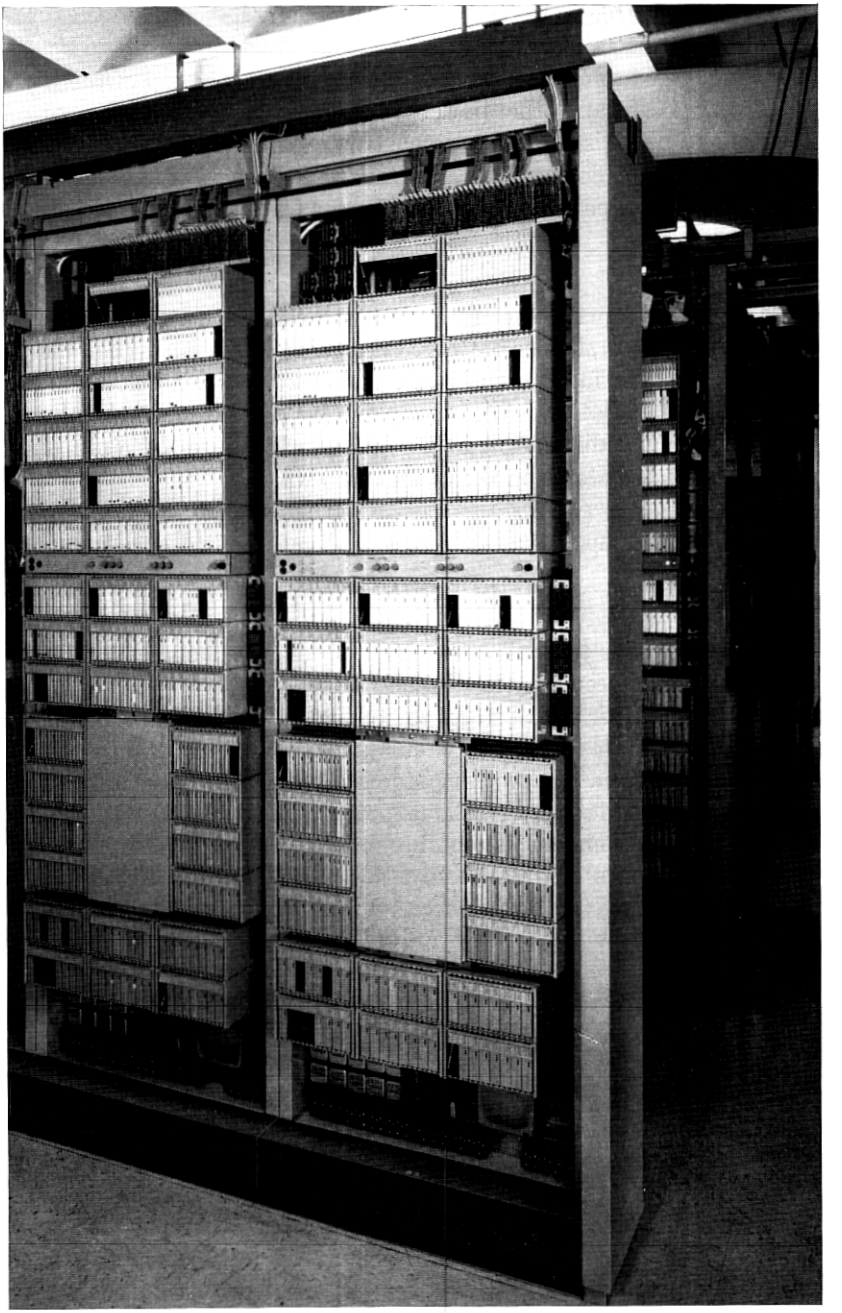

Fig. 23 — Two call stores in a No. 1 ESS installation.

are made with terminal strips and transformers at the top of the frame, while fuses, filters and other power control equipment are at the bottom. The control panel is of standard construction at a convenient height 52 inches above the floor, which is standard for No. 1 ESS. Connectors below the control panel, at the right, are for test purposes.

VIII. POWER

The entire external power supply for the call store comes from +24- and −48-volt central office battery. Emergency limits during commercial ac charging power failure can be as much as 20 per cent below the float voltages. This variation is accommodated by all circuits in the store.

Average power dissipation in a continuously addressed store is 470 watts. Unselected stores on the bus use 360 watts.

IX. OPERATING EXPERIENCE

9.1 *General*

Experience with ten call stores over a combined operating time of 80,000 hours has been very favorable.

The large number of call stores to be installed in the many No. 1 ESS installations dictates complete circuit pack interchangeability without any final adjustments in working stores. To achieve this goal most circuits have been designed without potentiometers and yet maintain tight tolerances. Some packs, notably regulators, delays, current drivers and servo reference circuits, require potentiometers to compensate for semiconductor junction differences and initial parameter differences, but they are set at the factory and will not be adjusted in individual stores.

Temperature effects on the module over the range of ambients from 32°F to 115°F, although quite pronounced, are corrected through the joint action of temperature-sensitive regulators and the servo system to keep the memory output signals well within the margins of the decision circuits. The concurrent change in switching time for the ferrite material with change in temperature is adequately compensated by deriving strobe timing from the switching signal of a standard ferrite sheet.

Although the combined effect of component drift, temperature variations and reasonable circuit pack misalignment does reduce 1 to 0 output signal separation somewhat over the ideal case, the most severe effect is the delta noise generated by the particular pattern of information stored in the memory.

9.2 *Delta Noise Considerations*

9.2.1 *General*

No single information or addressing test pattern suffices to simultaneously tax both the memory and the circuits. Furthermore, it is desirable to facilitate circuit design by separating effects and measuring their relative magnitudes. To achieve this goal, random-access, random-content memories must be exercised by a series of different programs, each generating a different type of worst case. The accumulated results of all these tests are combined to calculate the design margins of the memory. The call store must have extremely good margins because of the intended 40-year life. The huge number of call stores and the vast complex of different program combinations in the many telephone offices throughout the country almost guarantee that any remote combination that is possible will occur. For this reason the call store performance must not be address-sequence dependent or information-content dependent; it must be impervious to any possible normal sequence of events.

9.2.2 *Delta Noise Definition*

The paramount problem in design of coincident-current memories is the delta noise due to accumulation of half-current selected memory locations. Consider first two wires through a single hole in a ferrite sheet (or through a single core). If a half-drive current were passed through one of these wires, it would develop a relatively large signal across the other winding by direct coupling. Now if we consider two windings through a pair of holes, the situation is quite different. The readout winding can be threaded through the two holes so that it couples the drive winding in the opposite sense at each hole. A half-drive current through the pair of holes would induce signals of opposite polarity in the readout wire, and the net signal would be zero. From this it follows that along any memory drive wire there must be an even number of holes (or cores); half of these holes must couple the readout wire with a positive polarity, while the other half couple the readout wire with a negative polarity. In a two-dimensional coincident-current memory both axes must satisfy the above condition. Therefore, it is convenient to think of the holes along a drive winding as forming "canceling pairs." For example, a square array of 1024 holes in a 32 × 32 coincident-current memory plane would have 16 canceling pairs in each dimension.

At this point delta noise will be defined as the summation of the mag-

netic unbalance in canceling pairs due to the half-read drive currents. The large capacitively coupled signals are not as important, because very good cancellation can be achieved by proper wiring techniques and common mode noise rejection techniques. Magnetic unbalance can exist, however, and it is important to consider it from two separate sources.

The output signal from a canceling pair due to a half-drive current is zero if (1) both holes are in the same state (i.e., both 1's or both 0's) and (2) both holes have had the same past history of disturbances. The past history that is important is the polarity of the last half drive, either half read or half write. Condition 1 in the above statement depends only on information contents stored in the memory plane. Delta noise, arising when this condition is violated, will be called pattern noise or ΔP. The past history of disturbances is a function of the sequence of operations and addresses used in the memory and will be called sequence noise or ΔS.

9.2.3 *Hysteresis Model*

The 4-state hysteresis diagram shown in Fig. 24 illustrates sequence and pattern delta noise. This model assumes that a single half read will walk down a 1 hole from state 1W to 1R or a 0 hole from 0W to 0R. Further half-read pulses will not change the conditions, but a single half write will restore a 1 hole to 1W or a 0 hole to 0W. Experimental studies on small groups of cores, single ferrite sheets and the complete ferrite sheet module indicate that this model and its assumptions are very good. The different conditions of canceling pair noise and their relative amplitudes are given in Table II.

Pattern noise which is due to the unbalance of 1R and 0R pair depends on the information content of the memory and very little can be done about it. Asymmetric drive currents with write current larger than read current reduce pattern noise over the symmetrical-drive case, but it cannot be eliminated. The asymmetric drive apparently distorts the *B-H* curve and tends to equalize the slope of walked down 1's and 0's. This effect is limited by partial switching due to the oversize write half drive and inhibit, which can deteriorate storage.

Sequence noise, on the other hand, can be eliminated by providing a uniform "last" operation for all holes. The most popular method of doing this is to use a "post-write disturb" pulse. Generally, post-write disturb is accomplished by firing all inhibit drivers after writing is completed. The inhibit drive is equivalent to a half read; therefore, all holes would be in the 0R or 1R state of Fig. 24. The cure has its cost, how-

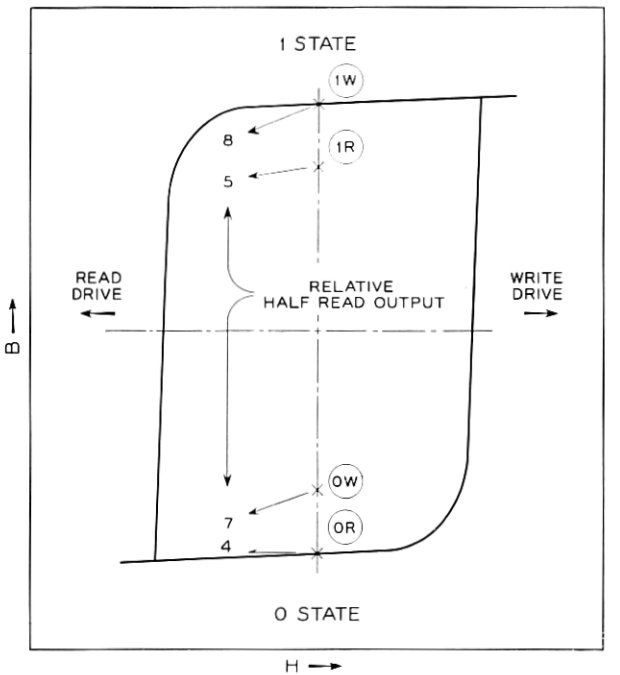

Fig. 24 — Four-state model B-H curve of ferrite sheet.

ever, in cycle time. Inhibit post-write disturb is particularly inefficient, because generally the inhibit winding is very long and has a high inductance. This makes it difficult to produce fast rise and fall on the post-write disturbs. The walk-down phenomenon, on the other hand, is very fast. Unlike hole switching, which for ferrite sheets requires 1 μsec, walk-down from 0W to 0R or 1W to 1R is accomplished during drive current rise time alone.

Sequence noise requires consideration, even though a remedy is at

TABLE II — CANCELING PAIR STATES AND RELATIVE DELTA NOISE AMPLITUDES

State of Holes (Canceling Pairs)	Delta Noise	Relative Amplitude (16 Canceling Pairs)
0R vs 0R	none	1.6
0R vs 1R	ΔP	16
0R vs 0W	ΔS	83
0R vs 1W	$\Delta P + \Delta S$	100

hand, because sequence noise represents energy in the ferrite material, and if this energy is transferred by a post-write disturb or any other disturb, it must be provided for in the readout circuits. In other words, a post-write disturb will generate an output signal equal to the noise condition it corrects, and this signal must be dissipated before the next readout appears.

9.2.4 *Delta Noise Test Patterns*

The basic test pattern for studying delta noise in a two-dimensional coincident-current memory is the pattern which writes all positive readout holes to the one state and the equal number of negative readout holes to the zero state. Fig. 25 shows a 32 × 32 bit plane pattern that satisfies this requirement. It also represents the worst-case delta noise pattern for call stores, because the duplication of readout and Y-axis system reduces the plane of intersection of the X- and Y-access wires with a given readout to a 32-by-32 array.

The figure does not represent the relative location of holes on any physical plane. The X-drive wire, for example, may thread alternately through positive and negative holes, or through any grouping of positive and negative holes. Translation of the address assignments is necessary to produce the four-quadrant picture; any coincident-current memory can be represented in this way.

Ignore for the moment any sequence effect and suppose the pattern of Fig. 25 is continuously repeated. Each read does indeed include the

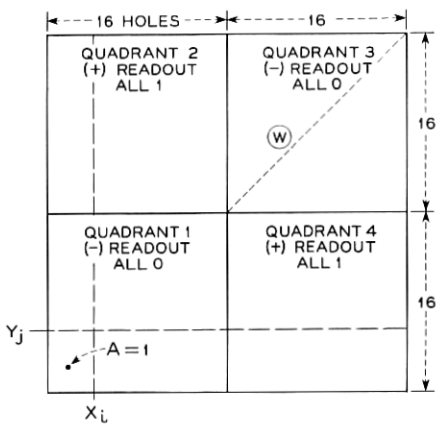

Fig. 25 — Address plane test patterns.

worst case of pattern-dependent delta noise (ΔP), but the noise component is always in the direction to enhance the signal separation by increasing 1's and decreasing 0's. For example, in quadrant 1, the 0's are negative and ΔP is positive; in quadrant 2, both the 1 readout and ΔP are positive.

To measure pattern-dependent delta noise that degrades the 1 to 0 ratio with consistency over every hole in the memory, a double-operation checkerboard pattern can be used as follows. Scan the worst-case delta noise pattern (which is a checkerboard) sequentially with two operations on each hole. First read a hole and write it to the opposite state. Second, read the hole and write it to the original state. On the second read, delta noise will be of a polarity to degrade the signal.

9.2.5 *Sequence Patterns and the "Worst" Worst Case*

Measurement of sequence-dependent delta noise not only adds complications to the testing procedure but also creates some pitfalls that must be avoided. The great opportunity to err comes from the fact that the polarity of the sequence-dependent delta noise can be independent of pattern; therefore it is possible to cancel sequence noise against pattern-dependent noise and obtain measurements that do not reflect the worst case of anything. For the call store the following statements apply:

Pattern-dependent delta noise from a 1,0 canceling pair will have the same polarity as the 1 hole.

Sequence-dependent delta noise from a half-read, half-write canceling pair will have the same polarity as the half-written hole.

To generate the "worst" worst possible delta noise on a test hole A the following operations are necessary:

(1) Write the basic worst-case pattern as shown in Fig. 25.

(2) Write the single test hole A to the opposite polarity. In the figure, A is shown in a quadrant of 0's, so it must be written to 1.

(3) Write a 0 somewhere in the memory. This causes an inhibit current which half reads all holes in the bit plane and neutralizes the effect of writing the 1 in test hole A.

(4) Write 1's along the diagonal W. This makes the "last" operation on every hole in quadrants 2, 3 and 4 a half write. The "last" operation on all holes in quadrant 1 is still the half read due to the previous inhibit pulse of step (3).

(5) Readout test hole A. The readout will be a negative 1. ΔP and ΔS will both be maximum and positive.

The zero "worst" worst case can be generated in a similar fashion.*

9.2.6 *Results*

Testing for "worst" worst case delta noise is extremely difficult, because practical test equipment becomes very complex. However, a partial implementation of this condition has been realized with the "worst" worst case along one axis and the worst case along the other axis. Measurements made on 10 stores over a temperature range of 32–115°F, with currents and circuit parameters perturbed within their expected life variations, have indicated signal-to-noise ratios in the order of 3 to 1.

Using post-write disturb to neutralize sequence noise, the 3-to-1 signal-to-noise ratio or, more accurately, 1-to-0 ratio, is measured with the double-operation worst-case checkerboard described in Section 9.2.4 and the drive currents at the extremes of the servo control (±2 per cent). The measurements are made by changing the discriminator level reference voltage until a 0 is detected as a 1 and until the first 1 is detected as a 0. The nominal value for the discriminator reference is 19 volts. Typical measured signal separations range between 6 volts to 26 volts and 10 volts to 29 volts. The major factors in separation variations are the memory modules themselves and the unclamp and strobe timing differences due to the variability in logic circuit delays.

X. SUMMARY AND CONCLUSIONS

Using ferrite sheets with relatively high Curie temperature, an economical, fast, high-capacity temporary memory unit capable of operating over a 32–115°F temperature range has been achieved.

Many novel circuit features are incorporated to fully exploit the inherent device capabilities.

To achieve the high degree of dependability essential in an electronic switching system, it contains numerous maintenance facilities as well as provisions for rapid reassignment of memory function by means of a flexible intercommunication system.

The experiences with ten stores, in operation for more than 80,000 memory hours during the past year, have proven that the stringent design objectives necessary for reliable and dependable performance have been achieved.

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* $+0$ with $+\Delta P$ and $+\Delta S$ is impossible to generate. -0 with $+\Delta P$ and $+\Delta S$ is the worst practical case.

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