No. 1 ESS Switching Network Frames and Circuits

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The switching network of No. 1 ESS is a space-separated network employing ferreed switches. The switches are organized into a few basic building blocks or frames from which all network configurations are realized. The frames are autonomous in operation and demonstrate the peripheral bus concept employed in No. 1 ESS.

The presence of the high-speed digital processing center in the central office has had a marked effect upon the circuits of the switching network. Path hunting has become a central control task, which has freed the network of its traditional path memory functions.

A combination of electronic and electromechanical devices is used to control the ferreed switches. Control duplication assures reliability.

I. INTRODUCTION

The switching network is a major functional unit in a telephone central office, representing in many cases 50 per cent or more of the equipment in the office. The choice of apparatus and general circuit design is highly influenced by the search for the optimum balance between cost, reliability, and maintainability.

The switching network serves the function of interconnecting the many lines and trunks served by the telephone office. In addition, the network interconnects the lines and trunks with the many service circuits and tone sources, such as signal transmitters, signal receivers, party test circuits, coin supervisory circuit, ringing circuit, etc.

A second function of the network is to match the traffic between a large number of lightly used lines and a much smaller number of heavily used trunks, maintaining a satisfactorily low probability of blocking.

These basic functions are performed in an operating environment that slowly changes over the life of the office. Not only can the number

of lines and trunks served by the office change, but the occupancy or offered traffic per line can change, the call-routing patterns within the office can change, and the types of facilities to be interconnected can change. The network, in order to meet the requirements of an office at any time and to match the requirements of initial offices that cover a broad range of sizes and traffic characteristics, must be capable of very flexible interconnecting patterns. This can be facilitated by the use of a minimum number of basic network building blocks whose sizes are tailored to acceptable growth or change patterns and which are then interconnected in series-parallel arrangements to form the complete office network.

A further requirement of a general-purpose network is that it be compatible with present outside plant and not be too restrictive on the future development of that plant. The ideal in this regard is a network that does not reflect its requirements on the outside plant. One method of achieving this is to have a network that is transparent to a wide range of transmission and service signals, passing a wide frequency band and tolerating large signal amplitudes. Also, the network should present a noise-free interconnecting path.

The new element in network design considerations is the presence of a high-speed digital data processing center containing bulk memories. The presence of this processing center permits network designs that are faster acting, less expensive, more flexible and more easily maintained than former network designs. Certain functions formerly delegated to the network have been transferred to central control. Chief among these are the link busy-idle record and the calls-in-progress record. These changes make path hunting a central control task that can be integrated into normal call processing and can be done in microseconds instead of at a much slower rate as a network task. In addition, access requirements into the network are lessened and crosspoint costs are lowered. The change is also beneficial from the operational standpoint: network paths can be reserved and links can be made busy for call routing and for network diagnostic purposes without network equipment action.

The invention of the ferreed switch during the electronic switching development program made it possible for the switching network to be highly compatible both with existing outside plant and with the digital processing equipment. In addition, since the ferreed switches could be packaged in units of almost any size without undue equipment or electrical circuit restrictions, the sizes of the network building blocks could be determined directly by traffic and office growth considerations.

II. NETWORK FRAMES

With each new switching system, a number of new terms are adopted to fit its internal organization and its new type of switching apparatus.

The two largest functional groups in the No. 1 ESS network are the line link network (LLN) and the trunk link network (TLN). Figs. 1 and 2 show these two link networks and indicate the link wiring pattern. The same two figures show the breakdown of the link networks into frames, concentrators, grids and ferreed switches.*

A connection through the network consists of several path segments; each path segment is controlled by a separate network frame (see Fig. 3). Although a No. 1 ESS office network may have 300 or more network frames, these are of just three basic types.[1] They are the line switching frame, the junctor switching frame and the trunk switching frame. These frames are independent functional units and are highly autonomous in their operation. They receive all operating instructions in coded form over a peripheral bus[2] system directly from central control and return information to it at the completion of their operating cycles.

The interconnection of the frames to form functional groups and the further interconnection of these groups to form complete networks are treated elsewhere in this issue.[3] This article examines the three types of network frames, including descriptions of the network fabric in each frame, path selection within the network fabric, and the processing of frame input information to achieve a desired action.

III. LINE SWITCHING FRAMES

3.1 *Frames*

The line switching frames perform the first two stages of switching in the interconnecting process: connecting lines on their inputs to B links on their outputs. The line switching frames also perform the second of the two basic network functions, namely, traffic concentration.

To cover the range of No. 1 ESS offices, two designs of line switch frame are provided. One concentrates traffic by a ratio of 4-to-1 between input lines and B links and the second concentrates traffic by a ratio of 2-to-1. In any office, however, only one of the two types of frame is used.

The 4-to-1 line switching frame contains 16 line concentrators, each of which interconnects 64 lines to 16 B links through two stages of

* See Ref. 3 for a definition of all terms.

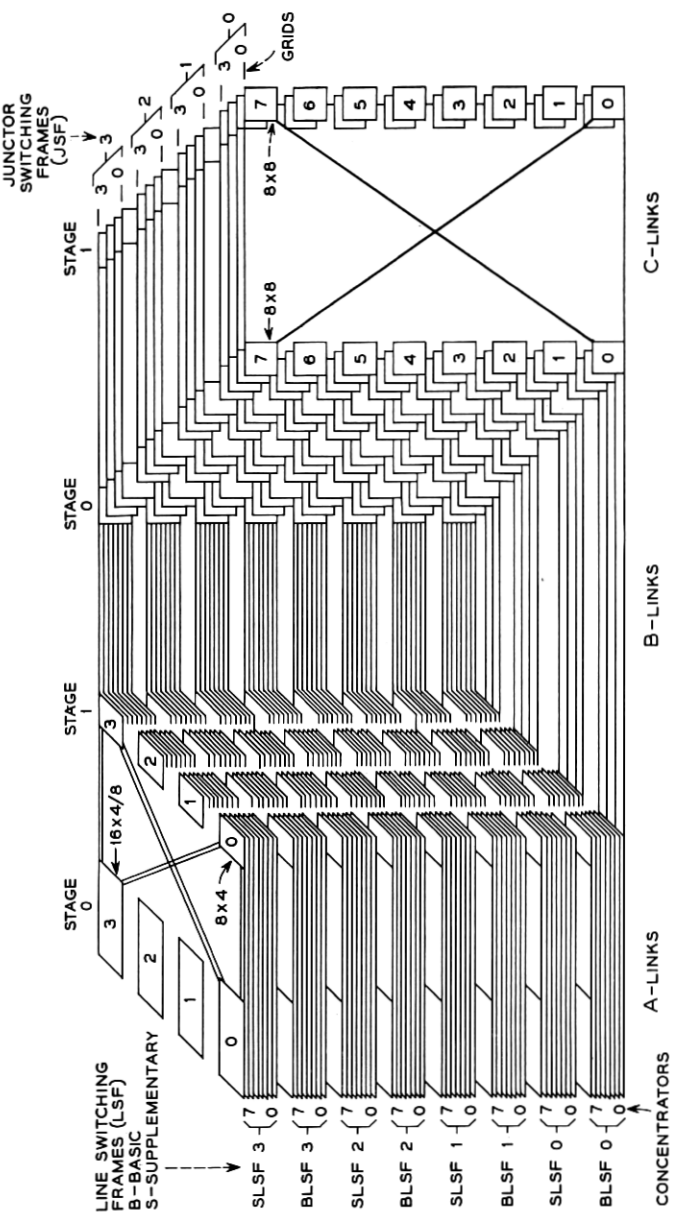

Fig. 1 — Wiring pattern for line link network with 4:1 concentration ratio.

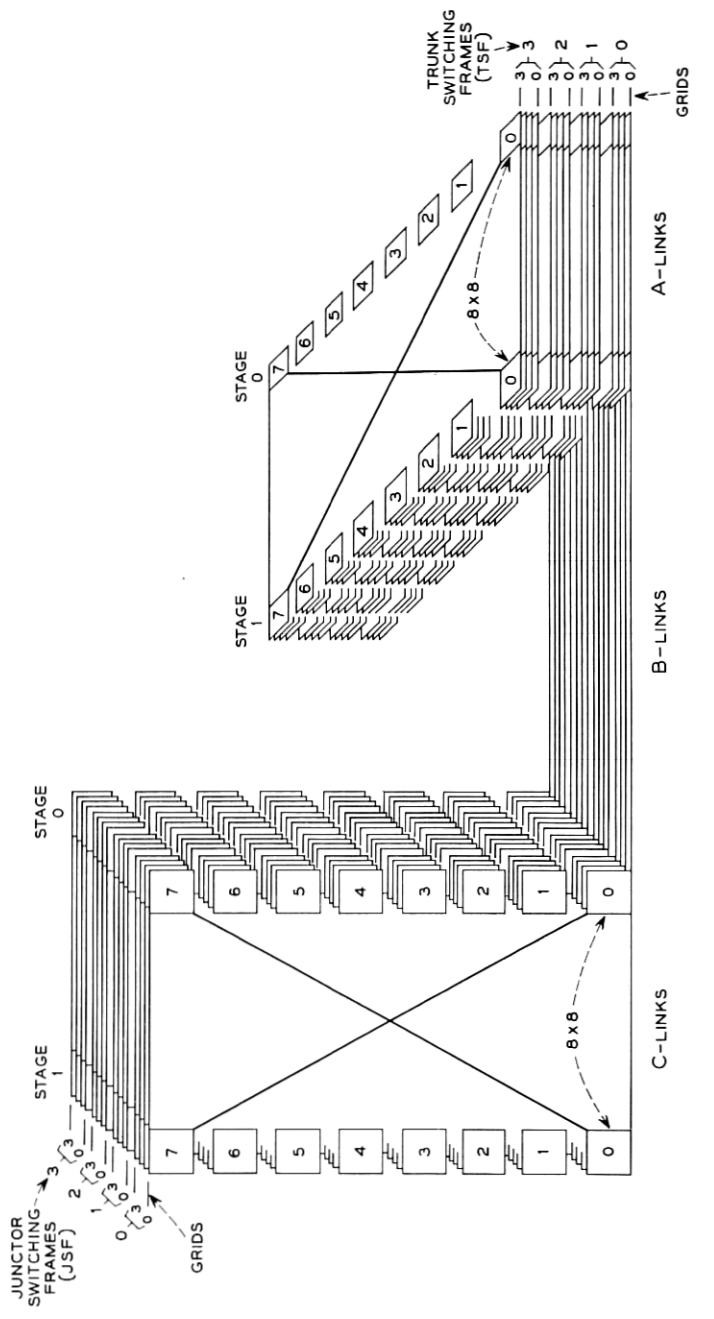

Fig. 2 — Typical wiring pattern for trunk link network with 1:1 concentration ratio.

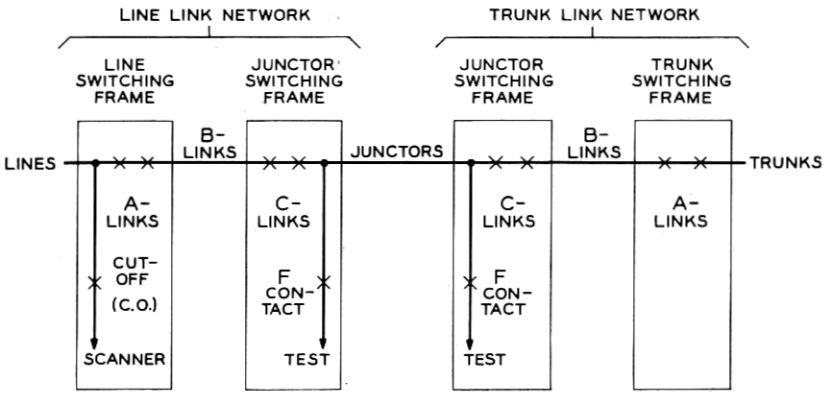

Fig. 3 — Network connections.

switching. The complete frame thus terminates 1,024 lines on its input and 256 B links on its output. For growth purposes, the frame can be separated mechanically into two halves, each containing eight concentrators. The basic half, however, contains all the controlling circuitry needed to control both the basic and supplementary halves. Only one line switch frame in an office would normally operate as a half frame. This half-frame operation provides line growth in steps of 512 lines. The 2-to-1 line switching frame contains 16 line concentrators, each of which interconnects 32 lines to 16 B links through two stages of switching. The frame thus terminates 512 lines on its input and 256 B links on its output. The frame is always supplied as a complete unit.

3.2 *Concentrators and Switches*

The 16 concentrators on a line switching frame are identical. A block diagram of a 4-to-1 concentrator is shown in Fig. 4. The 64 lines are assigned to four input or stage 0 switches, and the 16 output or B links are assigned to four stage 1 switches. The wiring between stages, called "A links," permits each input terminal to have access to each output terminal over a single path defined by a particular A link. Each of the 16 inputs on a stage 0 switch has access to only four of the eight outputs of the switch. The four outputs, however, in every case form a set that is wired one each to the four switches in stage 1. Thus full access of B-link outputs is achieved with a minimum crosspoint count per line.

Each input terminal also connects to a pair of contacts that give the line access to the line scanner for service request indication. These cut-

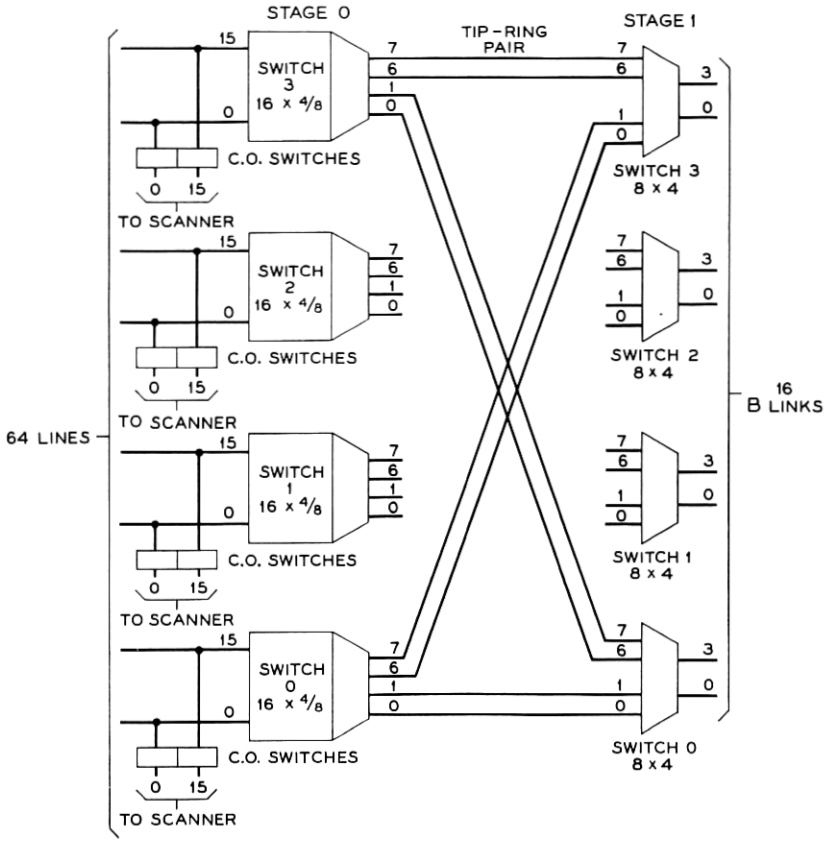

Fig. 4 — Line switching frame: tip-ring block diagram of a 4:1 concentrator.

off ferreed switches, bipolar in operation, are controlled by the line switch frame control equipment.

A block diagram of a 2-to-1 concentrator is shown in Fig. 5. This concentrator differs from the 4-to-1 concentrator only in the stage 0 switch. The 32 input lines are assigned to eight 4 × 4 switches. Full access to the B links is achieved with traffic concentration limited entirely to the stage 1 switches.

IV. TRUNK AND JUNCTOR SWITCHING FRAMES

4.1 *Frames*

The trunk switching frames perform two stages of switching in the interconnecting process, connecting trunks and service circuits on their

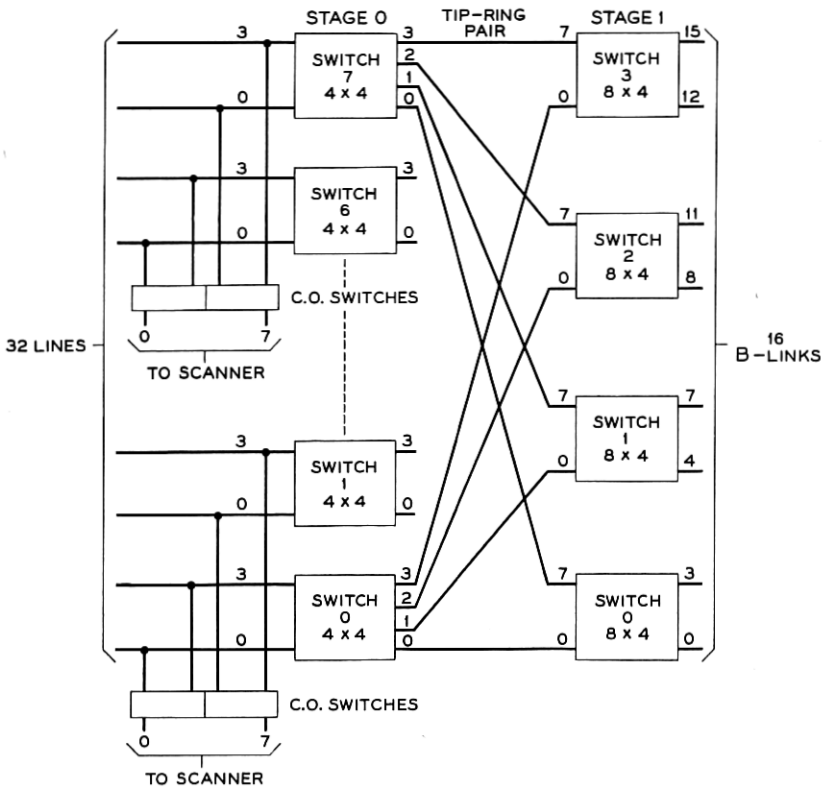

Fig. 5 — Line switching frame: tip-ring block diagram of a 2:1 concentrator.

inputs with B links on outputs. The junctor switching frames perform two stages of switching, interconnecting B links and junctors, the latter being the central link of every network connection. Both these interconnecting links are completely internal to the network connection.

Both types of frames contain four octal grids, each of which interconnects 64 inputs to 64 outputs through two stages of switching. The complete frames are always provided. This provides growth steps of 256 trunks and 256 junctors.

The junctors switching frame, in addition to the above switching grids, contains a pair of contacts per junctor that give the junctor access to a common test vertical. The test vertical ferreed switches, bipolar in operation, are controlled by the junctor switching frame control equipment.

4.2 *Octal Grids and Switches*

An octal grid with test vertical access is shown in Fig. 6. The 64 inputs are assigned to eight input or stage 0 switches, and the 64 outputs are assigned to eight stage 1 switches. The interstage wiring connects each input switch to each of the eight output switches. Each input terminal thus has access to each of the 64 output terminals through a single path defined by a particular link between switches.

V. PATH SELECTION

For path selection purposes, the ferreed switches within each frame are divided into two equal groups, and independent path selection

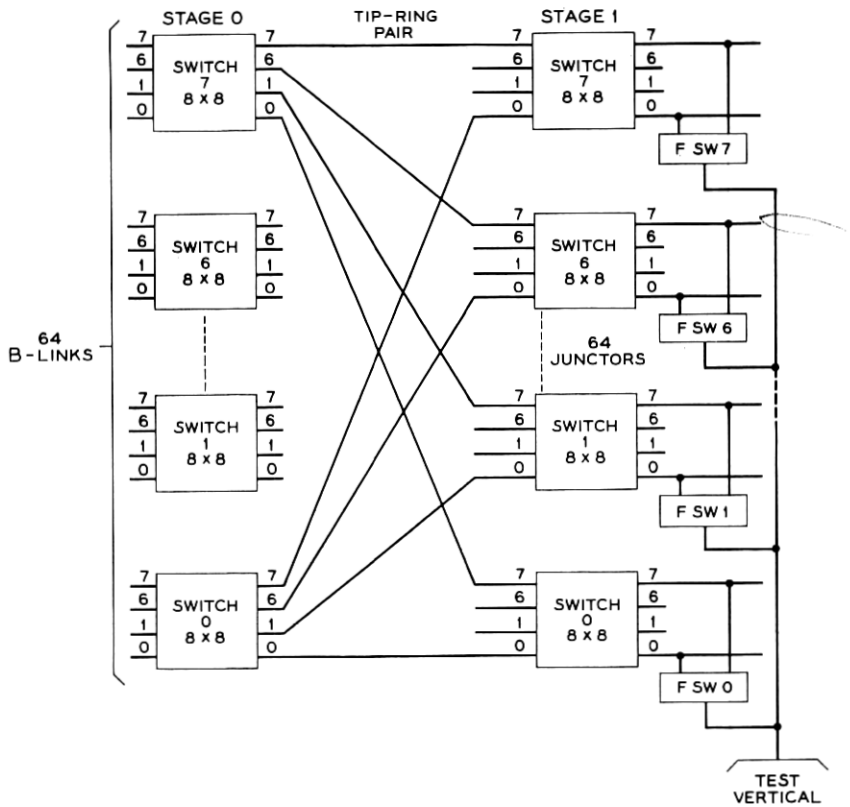

Fig. 6 — Junctor switching frame: tip-ring block diagram of a grid with test vertical access.

facilities are provided for each group. Two simultaneous paths can therefore be established per frame, one per switch group.

The magnetically latched ferreed crosspoints[4,5] are wired into coordinate arrays to form 8 × 8, 8 × 4, 4 × 4 and partial-access 16 × 8 switches.

The control windings are series connected along the rows and columns of the switch. One end of the control windings of all rows and columns is connected to a common multiple within the switch. By pulsing one row and one column via the common multiple, the crosspoint at the intersection is closed. At the same time, any crosspoints previously closed along the pulsed row or column are released. This operating method eliminates the need for specific release operations on the crosspoint. Crosspoints are released as a direct result of the operation of other crosspoints.

In all frames, the control winding interconnection pattern between switches on a frame parallels exactly the interconnection pattern of the tip-ring conductors on the frame.

The closure of a tip-ring transmission path between specific pairs of input and output terminals requires the momentary selective closure and high-current pulsing of the control winding path between these terminals. The pulse path is selected by means of 24-contact wire spring relays. Relay contacts are inserted in the control winding paths of every input, intermediate and output link. Other contacts steer the pulse to general switch groups and control the polarity of the pulse for special purposes. One contact per relay is used for test purposes.

In the junctor and trunk switching frames, the path selecting groups internal to the grid are four groups of eight wire spring relays each. The four relay groups define respectively the input level, the input switch, the output level and the output switch. This is shown in Figs. 7 and 8. The operation of one relay in each group defines a unique pulse path through the grid. Other contacts on these same relays are inserted into the links of the second grid of the selection pair. The function of the relay groups, however, is not always preserved in crossing between grids. This allows the maximum usage of the 24 contacts on each relay.

Within the grid, input switch selection has been made in the intermediate switch links. This performs the added function of disjoining the internal link multiple that results from the control winding multiple within this switch.

In the junctor switching frame, additional contacts are used within the grid to select the bipolar test vertical access ferreed F as shown in Fig. 8. This requires the use of additional contacts on the relay groups

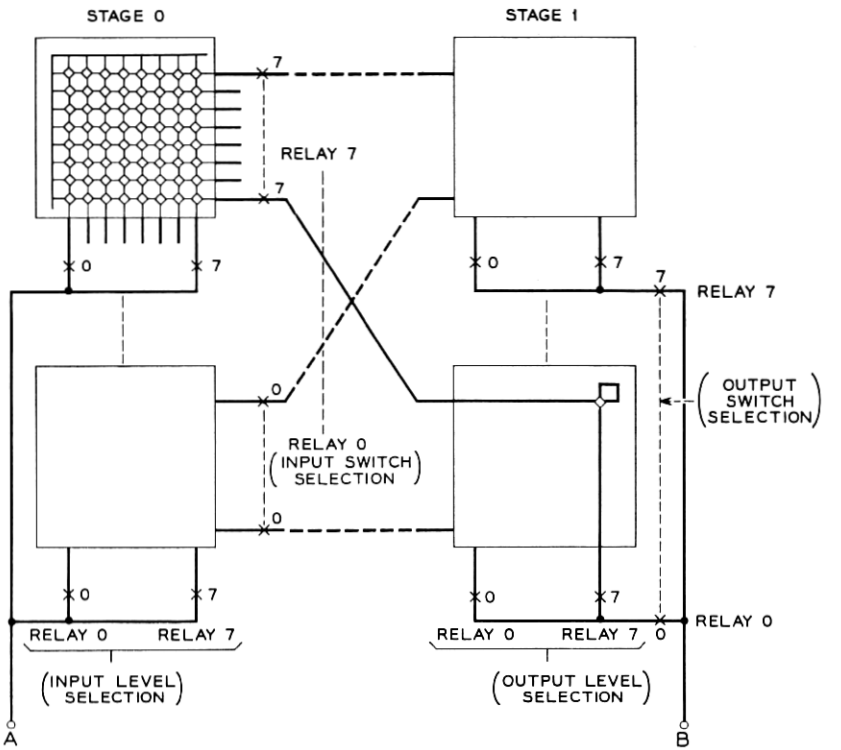

Fig. 7 — Trunk switching frame: path selection within a grid.

that select the output switch and output level. The grid with test vertical access has three possible pulsing points: A, B, and C. By pulsing between terminals A and C with one polarity, the two crosspoints in the grid and the F contact are closed. By reversing the pulse direction between these two points, the two crosspoints in the grid are closed and the F contact is opened. By connecting the pulser between terminals B and C in either of the two polarities, the F contact can be opened or closed without pulsing the transmission crosspoints. Similarly, by pulsing between terminals A and B, the transmission crosspoints can be operated without changing the state of the test vertical access ferreed.

External to the grid, the pulse is steered by means of additional wire spring relay groups as shown in Fig. 9. The first selection group steers the pulse to its normal pair of grids or the grids of the alternative half of the frame. The next relay group, the order group, controls the

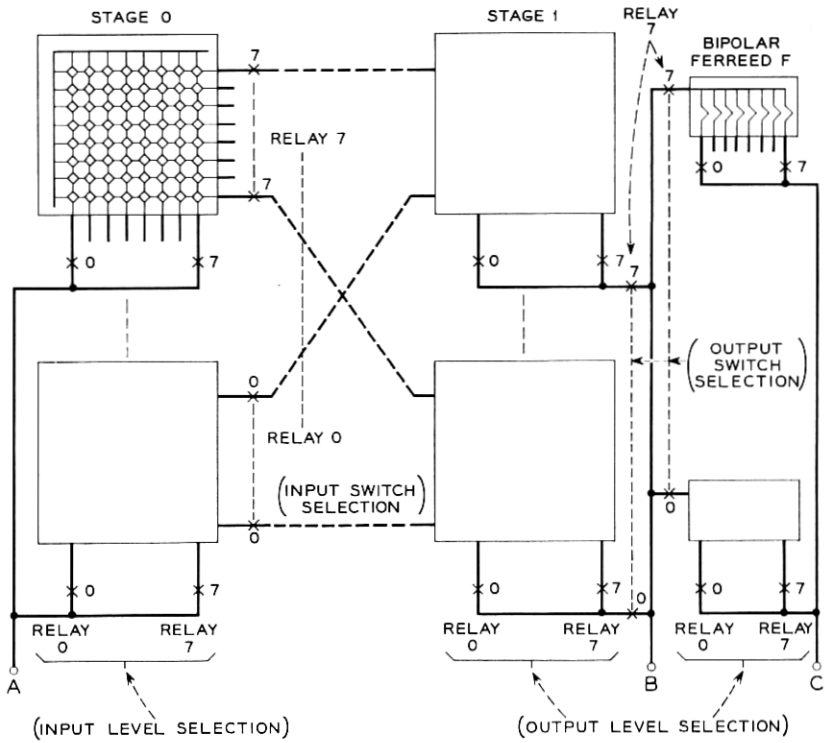

Fig. 8 — Junctor switching frame: path selection in a grid with test vertical access.

grid pulse points and pulse polarity. The third relay group controls the grid selection.

Path selection in the 4:1 concentration ratio line switching frame follows the same general pattern as in the junctor and trunk switching frames. The eight concentrators on the basic frame form one path selection group, and the eight concentrators on the supplementary frame form the second selection group. Within a concentrator, three relay groups perform path selection. These relay groups consist of 16 relays each. As shown in Fig. 10, one group defines the 16 input levels per input switch, the second, the 16 output levels per concentrator, and the third is a make-up group. This group is not too closely defined by equipment layout but essentially chooses input half-switches for a pair of concentrators.

Path selection in the 2:1 concentration ratio line switching frame is similar to the 4:1 concentration ratio line switching frame. Three relay

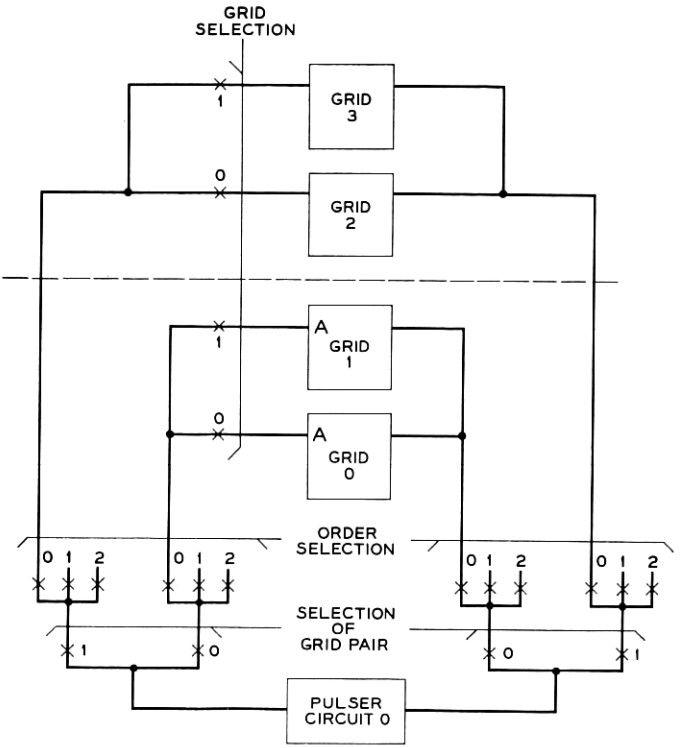

Fig. 9 — Path selection external to grids.

groups of 16 relays each are used for input level, input switch and output level selection as shown in Fig. 11.

In the 4:1 concentration ratio line switching frame selection plan, maximum use has been made of changing the functions of the relay groups among concentrators. In most cases, this has permitted 20 of the 24 contacts per relay to be used for path selection purposes.

External to the concentrator, additional selection groups steer the pulser to the appropriate concentrator. Another group, the order group, is a six-relay group. As can be seen from Figs. 10 and 11, there are three possible pulsing points into a concentrator: A, B, and C. A bipolar ferreed switch (cutoff) is used for the scanner access contact. In a manner similar to the junctor switching frame, the order relays, by controlling the polarity of the pulsing and the point of application, perform the following types of orders:

(a) close stage 0 and stage 1 crosspoints with the cutoff contact either opened or closed,

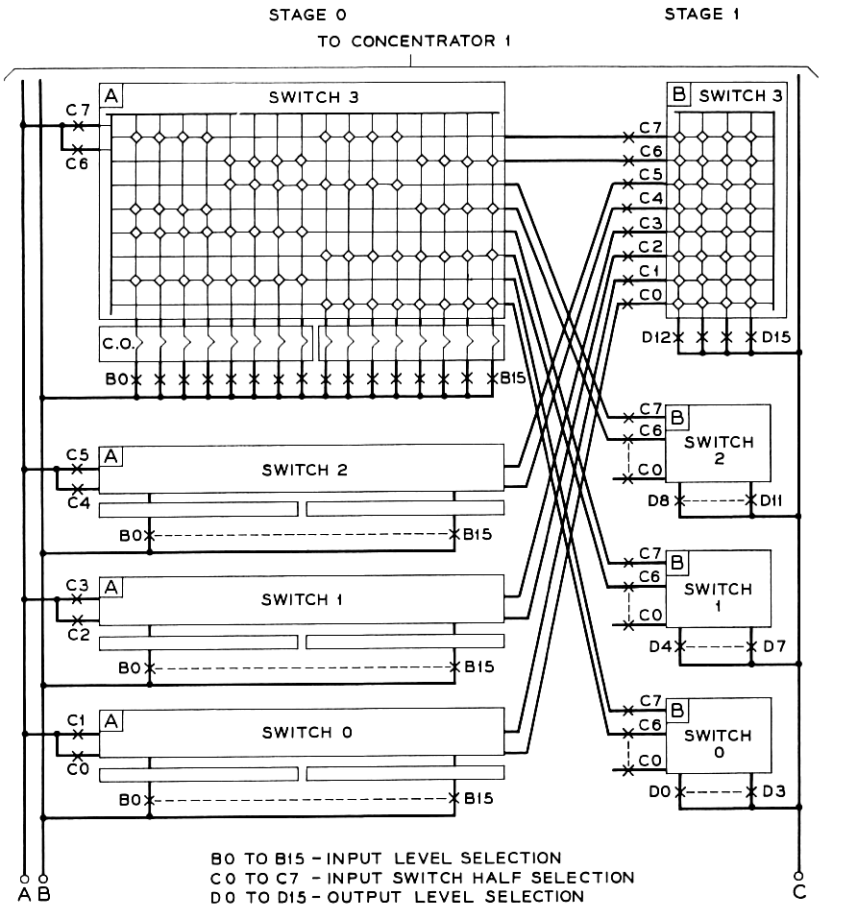

Fig. 10 — Line switching frame: path selection within a 4:1 concentrator.

(b) open stage 0 crosspoint with the cutoff contact either opened or closed, or

(c) open stage 0 and close stage 1 crosspoints with no change in cutoff contacts.

VI. INFORMATION PROCESSING

6.1 *Introduction*

The different types of network frames differ mainly in the internal organization of the network fabric. This results in differences in the

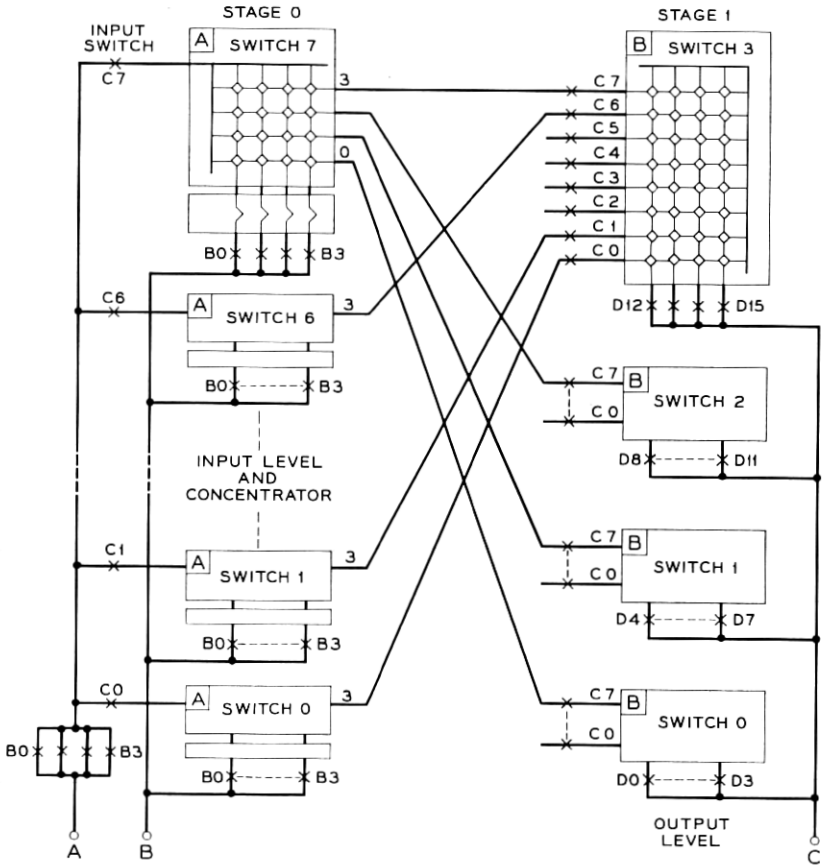

Fig. 11 — Line switching frame: path selection within a 2:1 concentrator.

information processing section of the frame, but these differences are minor. The same type of apparatus and circuit configuration is used in all types of network frames.

Reliability is achieved by means of duplication and redundancy. Duplication is achieved by providing two groups of circuits, each of which is capable of controlling the network fabric. Each of these circuit groups is assigned to control one-half of the frame fabric. Both circuit groups are functionally independent and under normal operating conditions may execute instructions simultaneously. Both circuit groups are normally active.

It is of prime concern that the probability of losing control of any portion of the network fabric be as small as possible. Therefore sufficient

circuit redundancy has been provided in each of the two major circuit groups that either of the two circuits can control all of the frame fabric. This provides standby facilities for controlling any part of the frame fabric.

The functional organization of a network frame is shown in Fig. 12. The cycle time of a network frame is 20 milliseconds. This time is measured from the instant an enable signal and peripheral bus addressing information are received and continues until the time the frame has executed this information and is prepared for a new instruction. With two active circuit groups in each frame, a network frame may establish new connections at a maximum rate of 100 new connections per second.

The high speed of the peripheral bus system in conjunction with the relatively slow-acting network frame requires that the bus information be stored in the network frame for a large portion of the frame operating cycle. The peripheral bus information, which is stored in a buffer register, is translated and checked. The checking circuitry determines if the state of the translator is valid or not. A nonvalid combination of bits on

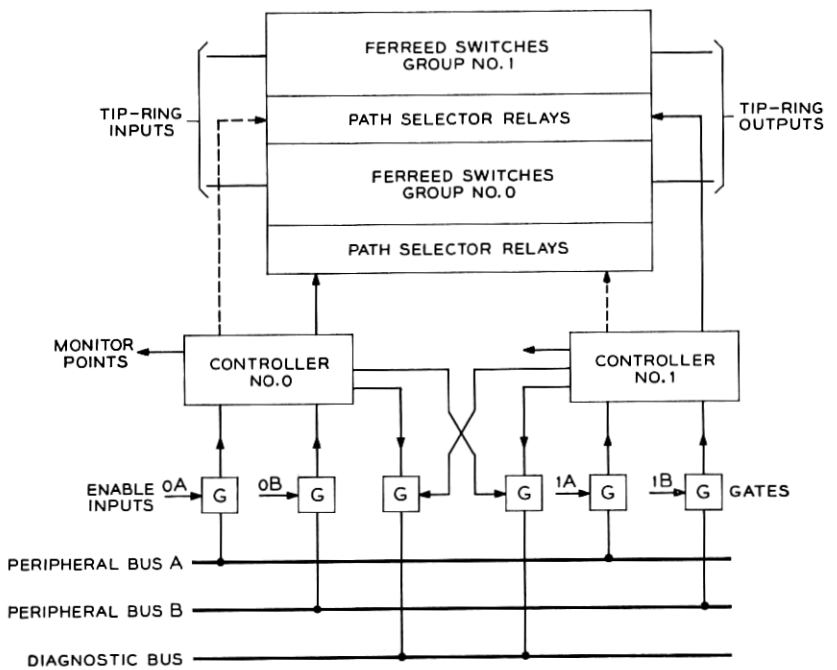

Fig. 12 — Functional organization of a network frame.

the peripheral bus or some malfunctioning of the buffer register or translator will cause the frame circuitry to stop processing the information. These checks will provide some assurance that erroneous action cannot be performed in the frame network fabric.

Each of the two major circuit groups in a frame has three monitor points which connect directly to the central control. These inform the central control about the status of the network control circuit at any time.

6.2 *The Peripheral Bus*

The peripheral bus consists basically of two 38-pair 26-gauge switchboard cables. These two cables are referred to as the 0 and 1 peripheral buses and interconnect the central control and all network frames. Each wire pair of both buses is assigned a bit position number ranging from zero to 37. A bit is said to be present in a position whenever an 80-milliampere, 0.5-microsecond current pulse occurs in that wire pair.

Each network frame expects bits to be present simultaneously in certain combinations on 36 of the bus bit positions. The format of the 36-bit binary word has been selected in such a manner that only a very simple translation has to be performed in the network frames. Bit positions 0 to 29 are used to identify a particular path. In the junctor and trunk switching frames, there are as many as 16,384 possible paths defined by these 30 bits. The grouping of these bits in several one-out-of-four and one-out-of-two subgroups is shown in Table I. Similarly, the line switching frame interprets the peripheral bus bits in several groups of one out of four and one out of two, as shown in Tables II and III. The peripheral bus information does not contain any check bits. The network frame circuitry contains facilities for checking the validity of the bus information. Each type of network frame expects a fixed number of bits to be present and checks that these appear in positions that satisfy the format for that type of frame.

Bits in positions 0 to 29 identify a path in a network frame. Bits in positions 30 to 35 inform the circuitry what kind of action should be performed on the selected path.

This multiple one-out-of-n grouping of the peripheral bus bit positions does require that the central control perform an elaborate translation of its internal binary information. This inconvenience and cost in the central control becomes relatively insignificant when one considers the simplicity of translation and checking that can be employed in each network frame. Bit position 36, referred to as the "reset signal," does

TABLE I—JUNCTOR SWITCHING FRAME: ASSOCIATION BETWEEN PERIPHERAL BUS BIT POSITIONS AND FRAME FUNCTIONS

			Function Selection		Grid Selection		Selection of Path within a Grid											
			1/2	1/4	1/2	1/2	1/2	1/4	1/2	1/4			1/2	1/4			1/2	1/4				
Bit. Pos.	37	36	35	34	33	32	31	30	29	28	27	26	25	24	15	14	13	12	21	20	11	10	9	8	19	18	7	6	5	4	17	16	3	2	1	0
Grid			Order Group (see below for orders)						Group No. 6		Group No. 5		Relay Group No. 4						Relay Group No. 3						Relay Group No. 2						Relay Group No. 1					
0	FCG	reset							grid 0 & 1 or 2 & 3		grid 0 or 1 grid 2 or 3		output switch		output level		output switch		input switch		input switch		input switch		output level		output switch		output level		input level		input level		input level	
1													output level		input switch		output level		input switch		output switch		input switch		output switch		input level		output switch		input level		input level	
2													output switch		input switch		output switch		input switch		output level		input switch		output level		input level		output level		input level		input level	
3													output level		input switch		output switch		input switch		output switch		input switch		output switch		input level		output switch		input level		input level	

Order No.	Designation	Function
0	remove NT, FCG, or verify	releases F contact and removes all connections to the test vertical
1	connect	closes 0 and 1 crosspoints and releases associated F contact
2	connect with FCG	closes stage 0 and 1 crosspoints and operates the associated F contact; connects FCG test circuit to the test vertical
3	test order	changes mode of operation of frame; does not change the state of any crosspoints
4	not used	
5	connect verify (LS)	operates an F contact and connects a resistor across the tip and ring of the test vertical
6	operate NT	operates an F contact and makes the test vertical available to external test circuits
7	connect verify (GS)	operates an F contact and connects a resistor between the ring conductor of the test vertical and ground

TABLE II—4:1 LINE SWITCHING FRAME: ASSOCIATION BETWEEN PERIPHERAL BUS BIT POSITIONS AND FRAME FUNCTIONS

	Line Switching Frame Contact Assignments																					
	1/2		1/4				1/2		1/4				1/4				1/4				1/4			
Bit Pos.	35	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Conc.	Order Group Relays								Gp. 4 Relays				Group 3 Relays								Group 2 Relays								Group 1 Relays							
0	0 not used						basic or supplementary		concentrator selector				input switch half								output level								input level							
1	1 connect* (close 0 and 1, open C.O.)												input switch half								output level								input level							
2	2 FCG (open 0, close 1, no change on C.O.)												input switch half								output level								input level							
3	3 test order												input switch half								output level								input level							
4	4 hi and dry (open 0, open C.O.)												input switch half								input level								output level							
5	5 connect test (close 0, close 1, close C.O.)												input switch half								input level								output level							
6	6 not used												input switch half								input level								output level							
7	7 restore C.O. (open 0, close C.O.)												input switch half								input level								output level							

* For "close 0 and 1, open C.O." read "close crosspoints in stage 0 and stage 1, open scanner cutoff ferreed."

TABLE III — 2:1 LINE SWITCHING FRAME: ASSOCIATION BETWEEN PERIPHERAL BUS BIT POSITIONS AND FRAME FUNCTIONS

	Line Switching Frame Contact Assignments (2:1 Ratio)																															
		1/2		1/4						1/4				1/4				1/4				1/4				1/4							
	Bit Pos.	35	34	33	32	31	30	29	28	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Conc.	Order Group Relays							conc. 0–7 or conc. 8–12		Group 3 Relays								Group 2 Relays								Group 1 Relays							
0 or 8	0 not used																																
1 or 9	1 connect* (close 0 and 1, open C.O.)																																
2 or 10	2 FCG (open 0, close 1 no change on C.O.)																																
3 or 11	3 test order									output level								input switch								input level and conc.							
4 or 12	4 hi and dry (open 0, open C.O.)																																
5 or 13	5 connect, test (close 0, close 1, close C.O.)																																
6 or 14	6 not used																																
7 or 15	7 restore C.O. (open 0, close C.O.)																																

* For "close 0 and 1, open C.O." read "close crosspoints in stages 0 and 1, open scanner cutoff ferreed."

not appear on the peripheral bus with any regularity. The use of this signal is mainly for the purpose of resetting network frames that may have been unsuccessful in executing their instructions, although it may be used for the purpose of generating an early timeout in any frame. Bit 37, also referred to as an "FCG" (false cross and ground) signal, is used only by the junctor switching frame. This signal appears at regular intervals on the peripheral bus. The signal is present at a different time than information bits 0 to 35. A certain time relationship does exist between this signal and the information bits. In the junctor switching frame, this signal is used as a time reference signal or clock.

Since the combination of bits present on either of the peripheral buses will appear in all network frames, all associated cable receivers will respond in all frames. This by itself will not cause any action in any of the frames. A further selection must be made as to which frame should respond. This selection of frame is accomplished by special signals called "enable signals." Each circuit has, in addition to its peripheral bus connections, connections to the central control via the central

pulse distributor[6] for this purpose. Since the network frame circuitry and the peripheral bus are both duplicated, four such enable signals per frame are possible, any one of which may be used to select one of the four possible access patterns. The presence of an enable signal indicates directly which of the four possible combinations of bus and circuit shall be used. The network circuitry will return to central control an opposite-polarity enable verify over the same pair of wires which carried the enable signal. The presence of this signal acknowledges the receipt of the enable and indicates that the frame circuitry has responded properly.

6.3 *Buffer Register*

The central control is capable of transmitting information data on the peripheral bus at a rate of one complete instruction every 11 microseconds. Each network frame requires 20 milliseconds to complete an instruction. Therefore it is necessary that the network frames record the bus information for the length of time necessary to execute the instruction. The bus information is stored in buffer register flip-flops. The flip-flop circuit, illustrated in Fig. 13, is set when transistor Q_2 is on. The output of this circuit is capable of sinking 100 ma. There is one set of registers associated with each of the two groups of controlling circuitry. Each of the two sets of registers in a frame has one such bistable circuit per bit position. Each flip-flop may be set from either of the two buses over separate connections. Two of the three primary windings provide for the separate bus connections. A positive register

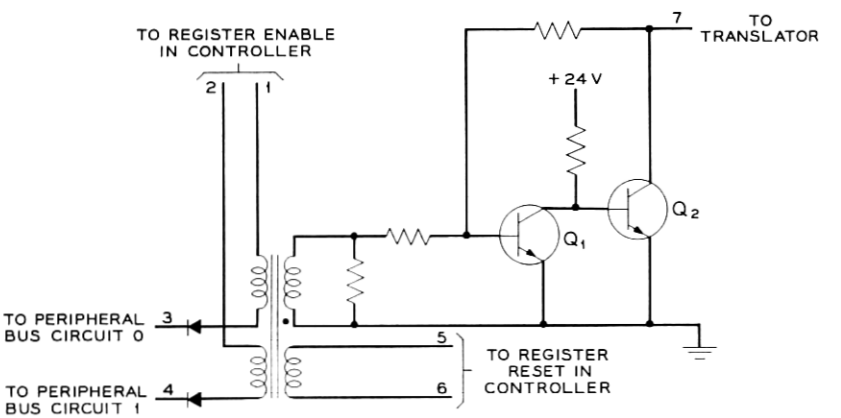

Fig. 13 — Buffer register flip-flop.

enable pulse generated by the network circuitry will appear either on terminal 1 or on terminal 2 and will provide the set current for each register flip-flop. The presence of an address bit, a negative pulse on either terminal 3 or 4, will terminate one of the two primary windings. A third winding provides means for resetting the flip-flops.

6.4 *Translator*

The principle employed in translating the multiple one-out-of-n peripheral bus information is the same in all types of network frames. The line switching frames translate the bus information into multiple one-out-of-sixteen selections, while both the trunk and the junctor switching frames translate the information into several one-out-of-eight selections. In the line switching frames, pairs of one-out-of-four bus information are translated to one-out-of-sixteen selections. The circuits of the one-out-of-sixteen and one-out-of-eight translators are shown in Figs. 14 and 15. They consist of 311-type reed relays which

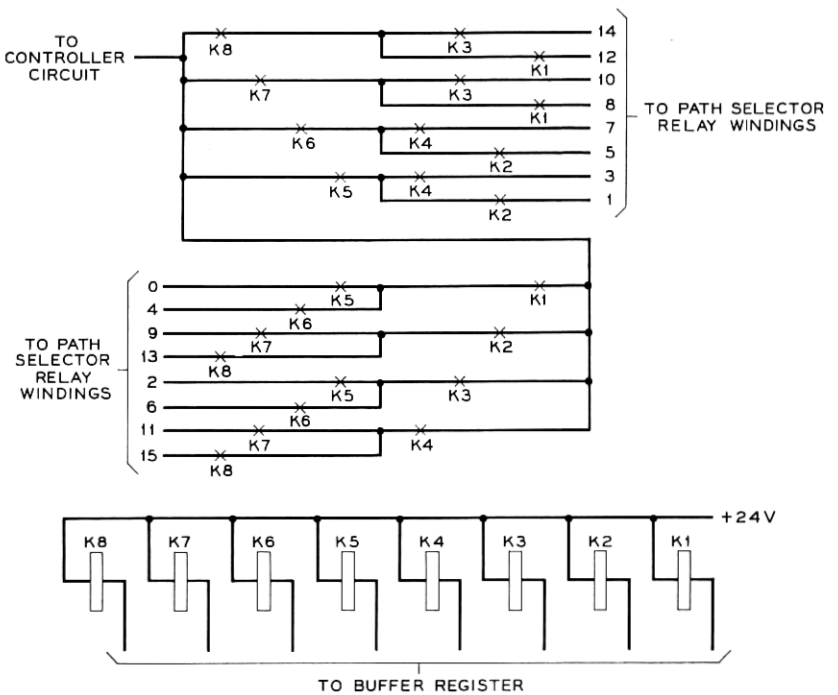

Fig. 14 — 1:16 translator circuit.

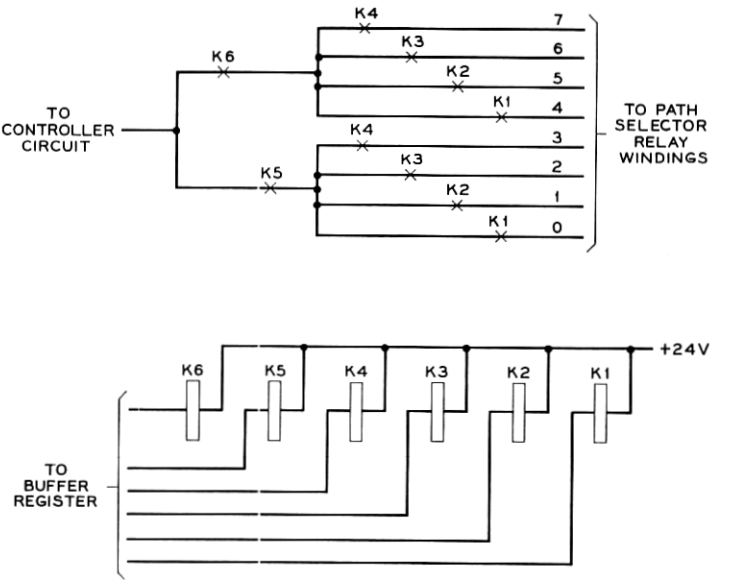

Fig. 15 — 1:18 translator circuit.

are operated directly by the register flip-flops. A fixed wiring pattern of the reed contacts results in the selection of a particular metallic path in each translator group. This metallic path is part of the operate path of a wire spring relay which is used in the ferreed pulse path selection. These relays are grouped and organized to correspond to the several groups of translators. A network frame contains two of each of all functional groups such as registers and translators. Each group of circuits is, under normal operating conditions, strictly associated with the control of one-half of the network fabric in that frame. An alternative access path between the two groups of circuits is provided by redundancy in the translators. Each buffer register circuit operates two reed relays in parallel, and two identical but separate metallic paths are established through each translator group. The selection of either of the two halves of the translator group determines if a circuit is to control its normal half or operate into the alternative path.

The path through a translator establishes continuity between an input terminal and the winding of a wire spring relay. The wire spring relay operate path is completed when cut-through occurs. At the time of cut-through, one path should exist through each translator group.

6.5 *Group Check Circuit*

Each network frame checks the validity of the peripheral bus information. This check is based upon the one-out-of-n grouping of the peripheral bus bit positions and the conversion of these groups into fewer but larger one-out-of-n groups by the translators. Each translator group should, at the time of cut-through, have only one path established between the common cut-through terminal and one of its output terminals. The absence of such a path or the presence of more than one path will cause the group check circuit to respond. Each wire spring relay in a relay group of the pulse path selector has a contact protection network connected across each of its two windings. One side of the output path for one group of relays is common and connects to battery through one winding of a transformer in the group check circuit, as shown in Fig. 16. At the instant of cut-through, a transient current will be present in the group check transformer winding. The waveform of this current is largely controlled by the protection network in shunt with the selected wire spring relay winding. At the same time, a reference current is present in a second winding of the group check transformer. The waveform of this current is controlled by an external *RC* network.

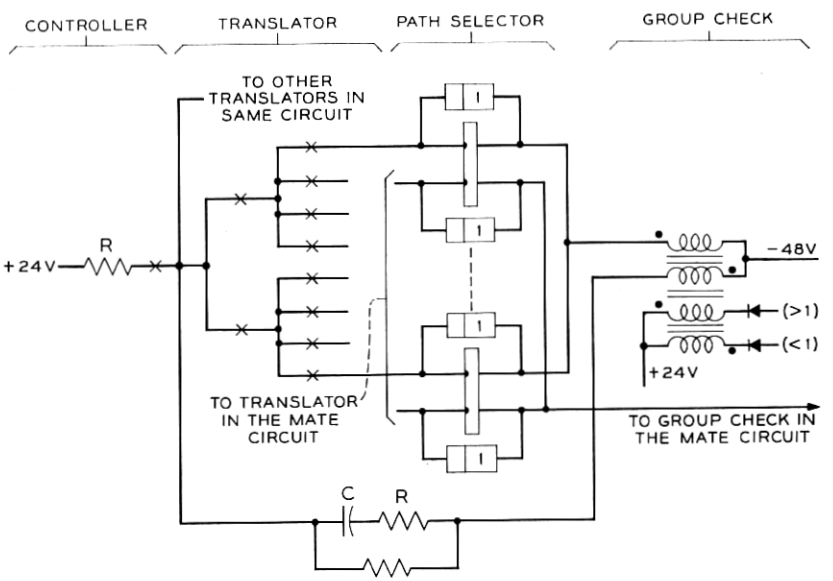

Fig. 16 — Check for single path through a translator by comparing the transient currents at the instant of cut-through.

This external network is designed to give a reference current which closely equals that which is present when one relay operate path exists. The effect of the two nearly equal transient currents is to cancel in the group check transformer and, as a result, no signal appears on either of the two secondary transformer windings. A group check failure signal will be present on both the secondary windings if no, or more than one, relay operate path exists. The polarity of the signals on the secondary windings depends on the type of failure that exists. This is used to detect and report the kind of failure that has occurred. Knowledge of the type of failure is important in diagnosing a frame trouble. One four-winding transformer is associated with each translator group. A group check failure of either kind will cause the wire spring relay voltage cut-through to open. This occurs within a couple of milliseconds and is considerably less than the minimum operate time of any of the wire spring relays.

6.6 *Sequence Control*

The network controller performs all essential timing and sequencing needed for the operation of the switching network circuit. The receipt of an enable signal from the peripheral bus circuit initiates the chain of events leading to the closure of a tip-ring path in the frame. A block diagram of the controller logic is shown in Fig. 17. In the following discussion, all times are measured from the receipt of an enable signal from the central control.

An enable signal may be received from the peripheral bus circuit on either the EN0 or EN1 lead. The corresponding flip-flop will set. The setting of the flip-flop will start the timing circuit, which generates a 2.4-microsecond timing pulse. The timing pulse is gated with the states of the enable flip-flops to enable the address registers to read the information on the peripheral bus (0 or 1) corresponding to the received enable (0 or 1). The trailing edge of the timing pulse is differentiated and gated with the enable flip-flops to return an enable verify signal to the peripheral bus (ENV0 or ENV1) corresponding to the enable (0 or 1) which was received. The differentiated pulse is also used to set the F and VCT flip-flops and reset the S flip-flop. Setting the VCT flip-flop operates the VCT mercury relay, which then cuts through +24 v to the wire spring relay coils through the one-out-of-eight and one-out-of-sixteen translators. The TCV lead activates the group check circuit at this time. The operation of the VCT relay is slowed to insure that the reed relays in the translators have operated before cut-through

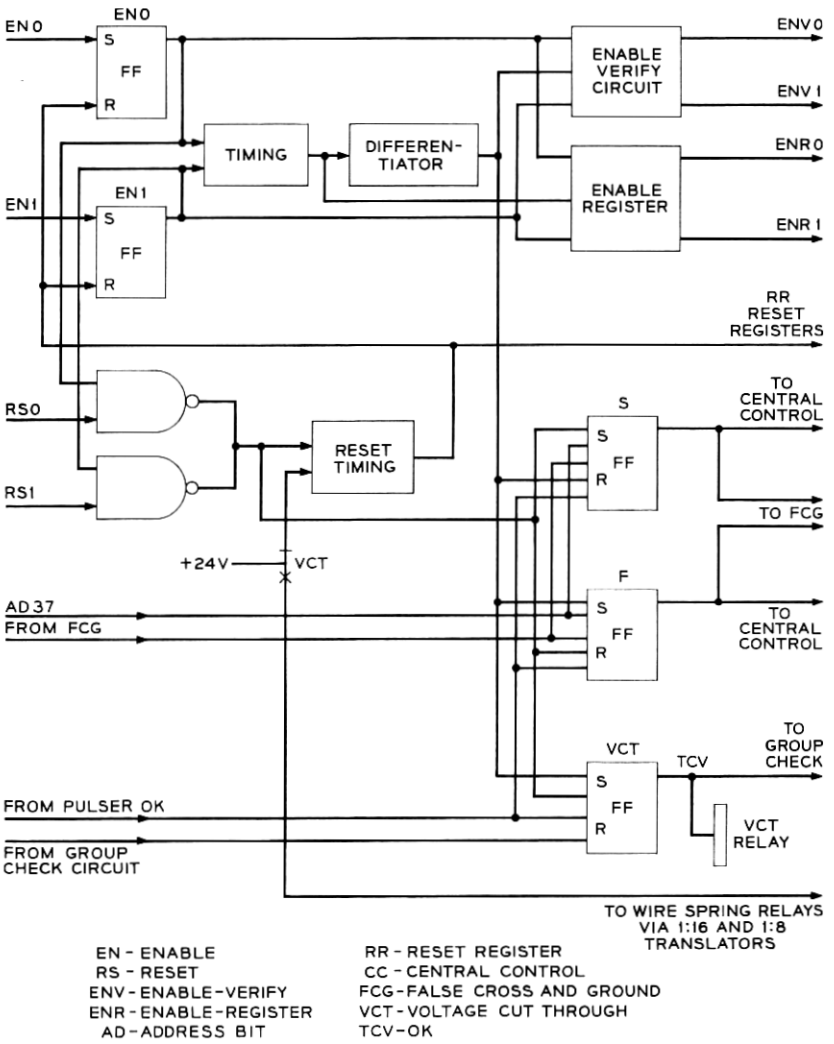

Fig. 17 — Sequence control diagram.

occurs. Under normal conditions, nothing further occurs in the network controller until the ferreed pulser has operated. The signal indicating satisfactory pulser operation starts the resetting of the controller by resetting the S, F and VCT flip-flops. Resetting the VCT flip-flop causes the VCT relay to release, removing power from the wire spring relays.

VCT relay release generates a signal in the reset timing circuit which resets the enable flip-flops and the address registers. The status of the S and F flip-flops is returned to central control. Central control expects that both the S and F flip-flops will be reset in 20 milliseconds. If either or both of these flip-flops are set, it is an indication that the controller has failed to complete a normal cycle.

One such case would be the occurrence of a group check failure. A group check failure causes the VCT flip-flop to be reset. The VCT relay releases, removing power from the wire spring relay. The VCT relay is operated for only 2 milliseconds in the case of a group check failure. This time is insufficient to operate the wire spring relays. The group check failure results in the S and F flip-flops remaining in the reset and set states respectively. When central control detects such a failure, or if it wishes to stop the controller from carrying out a previously transmitted order, it sends a reset signal on the peripheral bus (0 or 1). The reset signal is accepted only from the peripheral bus which corresponds to the previous enable (0 or 1). The external reset signal resets the F and VCT flip-flops and sets the S flip-flop. Resetting the VCT flip-flop initiates the resetting of the enable flip-flop and address register as previously described. The status of the S and F flip-flops indicates to central control that the frame is reset but that the reset was accomplished using the external rather than the internal reset.

The first enable received by a frame operates one of the enable flip-flops and reads information from the appropriate peripheral bus into the address register. Subsequent setting of the other enable flip-flop before the resetting of the first flip-flop will not cause reading of the other peripheral bus, because an EXCLUSIVE-OR circuit, part of the timing circuit, acts to prevent this. Thus the network frame is locked out after receipt of an enable until internally or externally reset.

On junctor switching frames, the S and F flip-flops are also connected to the FCG circuit. This circuit is activated only after a successful network cycle has been completed. The receipt of bit 37 sets both the S and F flip-flops, and interrogates the FCG detector circuit. A successful FCG check will reset both the S and F flip-flops.

6.7 *Ferreed Pulser and Path Check*

The ferreed pulser must be capable of producing a minimum pulse current of 9 amperes in the pulsing path. The 9-ampere minimum must be maintained over all combinations of battery voltage and ferreed load. The pulse width is nominally 300 microseconds at the 2.5-ampere points.

The load impedance varies from 10 ohms pure resistance to 12.5 ohms in series with 1.2 millihenries. Since the available battery voltage varies from 63.7 v to 79.1 v, some step-up in voltage is needed to develop the 9-ampere pulse. The pulser circuit is shown in Fig. 18. A step-up transformer with 4 to 1 secondary-to-primary turns ratio will raise the voltage sufficiently to develop at least 9 amperes into the highest impedance load at the minimum battery voltage. The primary current is obtained by discharging capacitor C_1 through a silicon control rectifier (Q_1) into the primary of the transformer (T_1). The recharging current of the capacitors is limited by a series resistor (R_1) and inductor (L_1).

The wire spring relays used to set up the pulsing path have a variation in their operate time. This makes it desirable to operate the pulser upon the completion of a pulse path rather than on a fixed time basis. To accomplish this, circuitry is included in the pulser which detects the presence of continuity on the pulse path. Two relays (relay 1 and relay 2), whose windings are in series with the battery voltage, transformer secondary and pulsing path, operate when continuity exists through the pulsing path. Relay 1 operates first and removes capacitor C_1 from the battery. The operation of Relay 2, delayed slightly by capacitor C_2, removes a shunt from the gate of the silicon control rectifier and

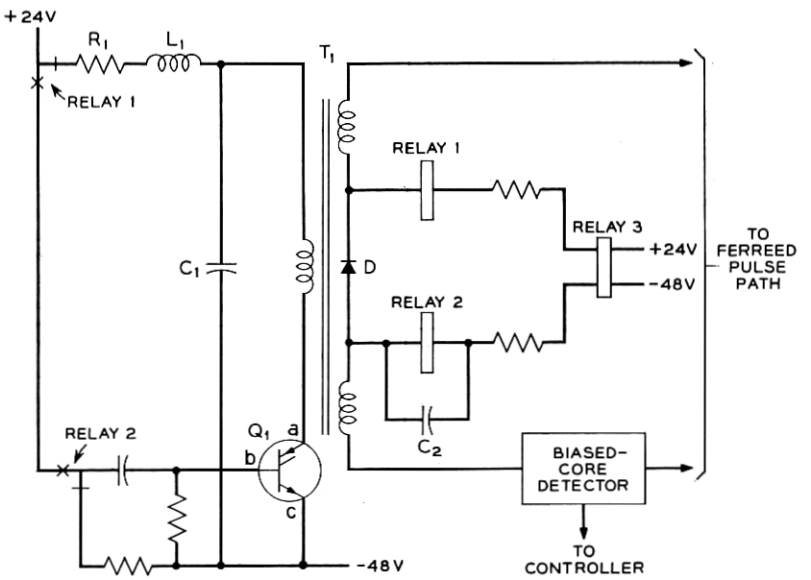

Fig. 18 — Ferreed pulser diagram.

triggers the silicon control rectifier, causing the capacitor to discharge into the transformer primary. The diode (D) in series with the transformer secondary conducts in the forward direction during pulsing and prevents any reversal of current through the load due to overshoot on the trailing edge of the pulse.

The windings of a third relay (relay 3) are also in series with the battery which is connected to the transformer secondary. Under normal conditions, with no short to ground existing in the pulsing path, the current in each winding of the relay will be the same and the relay will not operate. If, however, a short to ground exists somewhere in the pulsing path, the current flow in the winding connected to the −48-v supply will be twice that in the other winding and the relay will operate. The operation of this relay may be detected by the central control.

It is necessary for the pulser circuitry to give an indication to the controlling circuitry that the pulser has fired, so that the wire spring relays and other circuitry can be reset. Also, it is desirable to monitor the amplitude of the pulse to insure that it is of sufficient amplitude to operate the ferreed crosspoints. These two functions are combined in the biased-core detector. This is a square-loop core biased so that the pulser current must exceed 9 amperes to switch the core. A winding on the core goes to the controlling circuitry and signals when the pulser current is greater than 9 amperes.

6.8 *Test Vertical Functions*

Any path through the network fabric involves the use of at least one junctor. The junctor and associated junctor terminals are both physically and functionally the center of the network.

A special connection may be made to any pair of junctor terminals. This is accomplished by means of a test vertical, sometimes called the "ninth vertical." The test vertical and its associated controls are part of the junctor switching circuit. It consists basically of a tip-ring pair which may be connected to any pair of junctor terminals by means of a bipolar switch associated with each junctor terminal. The test vertical and the associated controls are organized in a manner similar to the frame fabric and control circuits. Therefore the junctor switching frame contains two test verticals, one associated with each of the two pairs of grids. One such tip-ring test access serves 128 pairs of junctor terminals. The bipolar test access ferreed switches may be operated or released by separate selected pulse paths, or they may be controlled in some cases by inserting the bipolar switch in the over-all pulsing path

of the junctor switching frame. A test vertical connection may be established or removed independent from or concurrent with the selection of a new network path. The circuitry which controls the state of the test vertical is basically an extension of the frame control circuitry.

The central control uses the test vertical either to perform a test or to establish a test condition on any pair of junctor terminals. The FCG check is a frequent and routine test which is performed on most new network paths. This test checks the newly established path for false crosses or grounds. Access to the path is by means of test verticals. The actual test is conducted by a current-sensing ferrod which is connected to the test vertical as indicated in Fig. 19. An instruction to the junctor switching frame to connect with FCG will establish the desired path through the fabric of the frame and connect the associated pair of junctor terminals to the test vertical. The current-sensing FCG detector circuit is then connected to the vertical. These actions take up most of

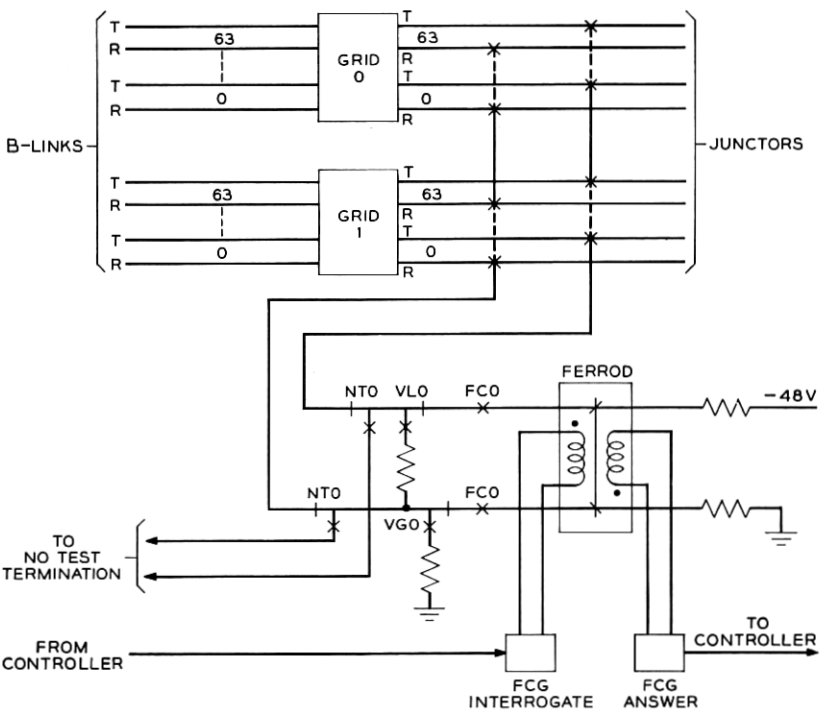

Fig. 19 — Test vertical access for one pair of grids.

the 20-millisecond frame cycle time. Within a millisecond of the end of the cycle, the FCG signal will be present on bus bit position 37. If the indication from the frame control circuitry is that all frame fabric actions have been executed successively, then the presence of this FCG signal will initiate the interrogation of the FCG ferrod. The success or failure of this test will be conveyed to the central control by means of the S and F monitor points of the frame control circuitry.

A "connect verify loop start" or "connect verify ground start" instruction may be performed by the junctor switching frame. These functions connect a resistor across the tip and ring conductors or between only the ring conductor and ground of the test vertical pair. These two test conditions are used by the central control to verify that it has restored the connection between a line terminal and its line scanner ferrod. With a network connection between a junctor terminal and a line terminal, central control can generate a request-for-service condition in any line scanner ferrod. Since the line scanner contains two types of ferrods, two separate test conditions may be established by means of the test vertical.

In addition to the primary functions of the FCG test and both of the restore verify test conditions, these tests also serve as additional aids in the systems network fabric diagnosis.

A fourth function which uses the test vertical is the operate-no-test function. A bridged test connection may be made to any pair of junctor terminals. This type of connection is traditionally referred to as a "no-test connection." This general-purpose type of test connection provides the means for connecting any external transmission testing facilities to any network path.

Each of these four test vertical functions requires a full network cycle. A test vertical may be used for only one of these four test conditions at any time.

A junctor switching frame may execute seven separate instructions; five of these involve the use of the test vertical. Initiation of any of these test vertical functions requires the presence of the peripheral bus bit 37. This FCG signal occurs at a time when all action in the network fabric is completed, and the receipt of bit 37 marks the time in the network cycle when the test vertical becomes connected to either of the two resistive verify terminating resistors or to the external no-test connection. An instruction to the junctor switching circuit to remove NT, FCG, or verify will release the selected bipolar ferreed and disconnect the test vertical from any of its previous test connections.

6.9 *Maintenance Facilities*

A number of test points and special circuits are provided in each network frame to facilitate automatic diagnosis. These test points are connected to strategic points in the circuit. These points may be connected to the central control by means of a diagnostic bus. The central control may request that any network frame be connected to this bus by means of an instruction transmitted to the frame. This diagnostic bus interconnects the central control and all network frames in a manner similar to the peripheral bus. Either of the two circuit groups in any network frame may be connected to the central control in this manner. A special instruction must be transmitted to a network frame requesting that one of its circuit groups be put in a test point access mode. By correlating the states and noting the sequence in the change of states of these test points, it is possible to diagnose malfunctions. Some circuit failures require that the circuit be removed from active control of the frame. This is accomplished by putting that circuit half in a quarantined mode of operation. A circuit half is quarantined by an instruction transmitted by the central control to the remaining active circuit half. Similarly, the circuit half may be restored to its active mode of operation by an instruction to the active circuit group. A quarantined circuit does not have access to any part of the frame network fabric. All control of the network fabric is now performed by the remaining operative circuit half. The quarantined circuit can respond and perform all its timing, sequencing and pulsing functions but will, in this mode of operation, use a dummy pulse path. This allows a circuit to be diagnosed either as an active circuit or while in a quarantined mode of operation. All modes of either circuit half of the network frame are under the control of central control. The monitoring channels that exist between the frames and the central control indicate the states of any circuit half at any time.

Manually operated controls are provided only for the removal of power from either side of the frame. These controls are mechanically interlocked pushbuttons. Manual removal of power will be reported to the central control by means of the identical status-indicating test points which exist in each circuit half.

VII. SUMMARY

Laboratory testing and preliminary system evaluation programs have demonstrated that all initial operating objectives of the switching network have been met very successfully. The result of system testing

programs has also confirmed the accuracy and usefulness of the automatic diagnosis facilities incorporated in the network control circuits.

The several codes of ferreed switches which utilize differentially wound ferreed crosspoints are probably the devices of primary interest in the switching network area. The switches are compatible with both the outside plant and the electronic central processors. The direct control of the ferreed switches by a combination of electronic and electromagnetic devices in duplicated circuitry represents at the present time a reasonable balance between cost and reliability.

The packaging of the network fabric with its associated controls in the same frame and the independent operation of the frames from a common peripheral communication bus present to the traffic engineer an extremely versatile system for building office switching networks. Future growth and changes in traffic patterns are accommodated with a minimum of effort and cost.

VIII. ACKNOWLEDGMENTS

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