No. 1 ESS Scanner, Signal Distributor, and Central Pulse Distributor

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The peripheral units of No. 1 ESS, described in this article, include the scanners and signal distributors. The scanners serve to collect information for the central control, and the signal distributors execute central control orders in the system. The peripheral units receive orders through the communication buses. The central pulse distributor serves to connect peripheral units to the communication buses so that a central control order, which is broadcast over the bus system, enters one particular peripheral unit.

I. INTRODUCTION

The No. 1 electronic switching system (ESS) includes peripheral units which serve as buffers between the central control with its associated stores and the outside world of lines, trunks, automatic message accounting (AMA) centers, and maintenance personnel. The peripheral units include the switching network, scanners, signal distributors, central pulse distributors, AMA recording equipment, teletypewriters and miscellaneous common systems circuits. This article describes the scanners, signal distributors and central pulse distributors. Associated articles describe the network[1] and other peripheral units[2] of No. 1 ESS.

II. FUNCTIONS OF SCANNERS, SIGNAL DISTRIBUTORS, AND CENTRAL PULSE DISTRIBUTORS

2.1 *Scanners*

Every telephone switching system embodies some mechanism for detecting service requests and supervising calls in progress. Input information of this nature is furnished to No. 1 ESS by the operation of scanners which sample or scan lines, trunks and various diagnostic points at discrete intervals of time as directed by the system. It might be said

that the scanners are the sensory organs of the system, since all external stimuli are received through them.

2.2 *Signal Distributors*

In addition to detecting and monitoring changes by means of the scanners, the system must be provided with means to operate and release relays in trunk, service and power control circuits. The signal distributors translate orders received from central control and distribute high-power, long-duration pulses to the various relays in No. 1 ESS. These relays[3] are controlled by polarized signals and are magnetically latched (held operated), thus providing a memory function in the end device.

2.3 *Central Pulse Distributors*

Many control functions in No. 1 ESS must be carried out at electronic speeds or at speeds exceeding the capability of the magnetic latching relays controlled by the signal distributors. Typical functions are outpulsing on trunks, operating miscellaneous flip-flops and the very important function of "enabling" various peripheral units (network controllers, scanners, etc.). Since the many peripheral units receive their orders from central control over a common bus system,[4] a particular peripheral unit must be connected to the bus when it is to receive an order. This is accomplished by sending a preliminary pulse to a particular peripheral unit before the order is transmitted on the bus system. This preliminary pulse, known as the "enable," is provided by the central pulse distributor, which translates a coded address received from the central control and transmits a pulse to the peripheral unit identified by this address.

III. SCANNER DESCRIPTION

3.1 *General*

Several categories of scanners are provided in No. 1 ESS. Primarily, they differ in purpose, location and the type of sensing element associated with the point to be scanned. For convenience and reliability, the scanners are provided in 1024-point modules which are physically located on network, trunk or junctor frames. In addition, one or more master scanners are provided for diagnostic and miscellaneous scanning functions.

3.2 *Ferrods*

The sensing element used in all scanners is the ferrod sensor (hereinafter called a "ferrod"), a current-sensing device operating on electromagnetic principles. It consists of a ferrite rod around which is wound a pair of solenoidal control windings. In addition, a single-turn interrogate winding and a single-turn readout winding are threaded through two holes in the center of the ferrite rod. The control windings are connected in series with the circuit to be sensed or supervised — for instance, a customer line. The ferrod[5] may be visualized as a transformer in which the magnetic coupling between the interrogate and readout windings is determined by the current in the control windings. This current in turn reflects the state of the circuit to be sensed, such as the on-hook or off-hook condition of a line. A diagram of the ferrod is shown in Fig. 1.

The magnetic state of the ferrite rod is sensed by pulsing the interrogate winding with a 0.5-ampere bipolar pulse. The positive half-cycle, of 3 μsec duration, switches the ferrite immediately surrounding the interrogate winding (single turn), provided the control windings (solenoid) are not energized. Ferrite switching induces a voltage in the readout winding. The induced voltage is approximately 200 mv when the control windings are not energized. On the other hand, when the control windings are energized, the ferrite rod is saturated and the coupling between interrogate and readout windings is greatly reduced, with the result that the readout signal is generally less than 20 mv. The negative half-cycle of the interrogate bipolar pulse resets the ferrite in the vicinity of the holes.

3.3 *Ferrod Types*

Three types of ferrods are used in No. 1 ESS. These differ in sensitivity and winding resistance. Their characteristics are shown diagrammatically in Fig. 1 and tabulated in Table I.

3.3.1 *Type 1B Ferrod*

The medium-sensitivity ferrod, type 1B, is used to detect call originations. It supplies ground and battery to the tip and ring of all loop-start lines through the contacts of a normally closed cutoff ferreed in the line switching frame. In the case of coin or PBX lines, the two windings of the ferrod are connected in series and supply battery to the ring conductor through the cutoff ferreed. The 1B ferrod is wound with resistance wire to limit the current in the presence of an accidentally grounded line.

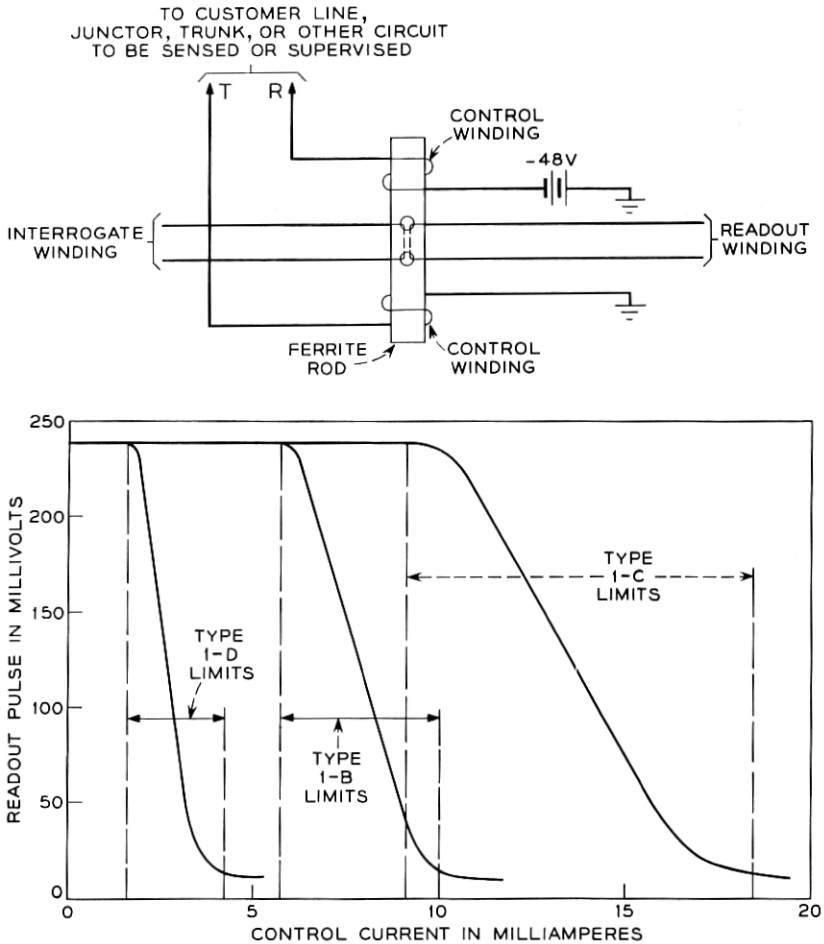

Fig. 1 — Ferrod schematic and typical characteristics.

Incorporated in the ferrod package is a conventional resistor-capacitor contact protection network to protect the cutoff contacts and to suppress electrical interference.

3.3.2 *Types 1C and 1D Ferrod*

The type 1C ferrod is the least sensitive ferrod. It is used in series with the talking battery feed inductors in junctor and trunk circuits to supervise the customer connection. A typical circuit using the 1C ferrod on the

TABLE I — ELECTRICAL SPECIFICATIONS OF THREE FERROD SENSOR CODES

Ferrod Sensor	1B	1C	1D 1E
Number of windings per ferrod	2	2	2
Resistance per winding	660 ± 10%	19 ± 10%	35 ± 10%
Turns per winding	1600	930	1300
Approximate inductance (both windings)	220 mh	70 mh	500 mh
Maximum current	100 ma	100 ma	100 ma
Maximum unbalance between windings	—	1.0 ohms	1.0 ohms
Nonoperate current	5.5 ma	9 ma	1.8 ma
Operate current	10 ma	18 ma	3.9 ma

* The 1E ferrod is electrically identical to the 1D.

local customer side of a trunk circuit is shown in Fig. 2. The type 1D ferrod is the most sensitive ferrod; it is used on the distant office side of trunk circuits.

3.3.3 *Ferrod Sensitivity*

The sensitivity of the various ferrods is controlled by varying the number of turns in the control windings and by adding a magnetic return path for the ferrite rod. The ferrod hole geometry determines the operate threshold and the slope of the output voltage characteristic. The several ferrod types are specified as having a 2:1 ratio of "no output" to "full output" control current, but individual ferrods exhibit a much lower ratio.

3.3.4 *Ferrod Package*

The ferrods are packaged in pairs in a molded ladder similar to that used for wire spring relays. Several ferrod assemblies are shown in Fig. 3.

3.4 *Scanner Operation*

The functional arrangement of the scanner is shown in Fig. 4. The ferrod sensor matrix consists of 64 rows, each containing 16 ferrods. To select a row for interrogation, the addressing equipment of the central control sends an enable pulse via the central pulse distributor. This signal opens the address register, permitting the X and Y signals to be received. One X input and one Y input are then selected and pulsed by the addressing equipment, which will hereafter be referred to only as a "central

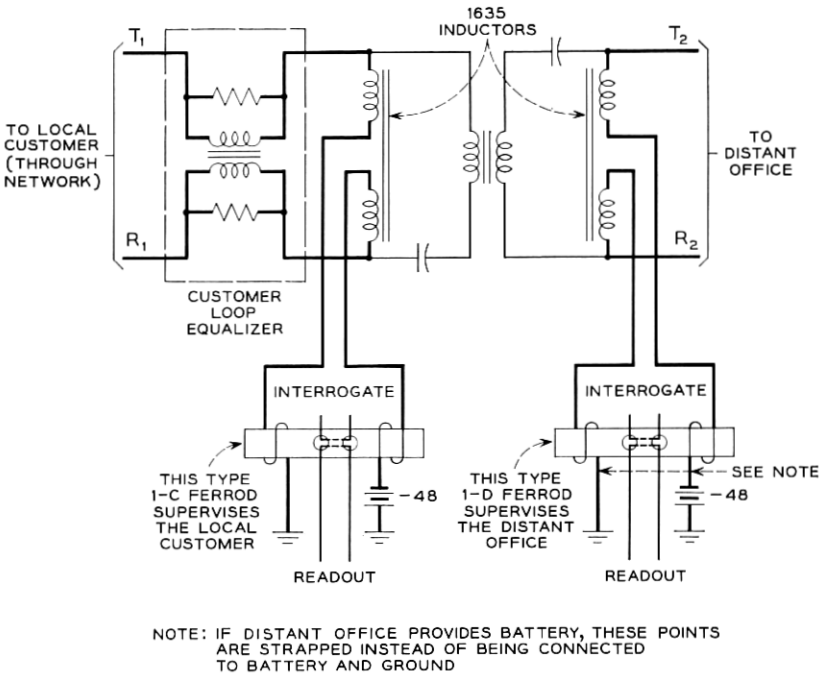

Fig. 2 — Trunk supervision using 1C and 1D ferrods.

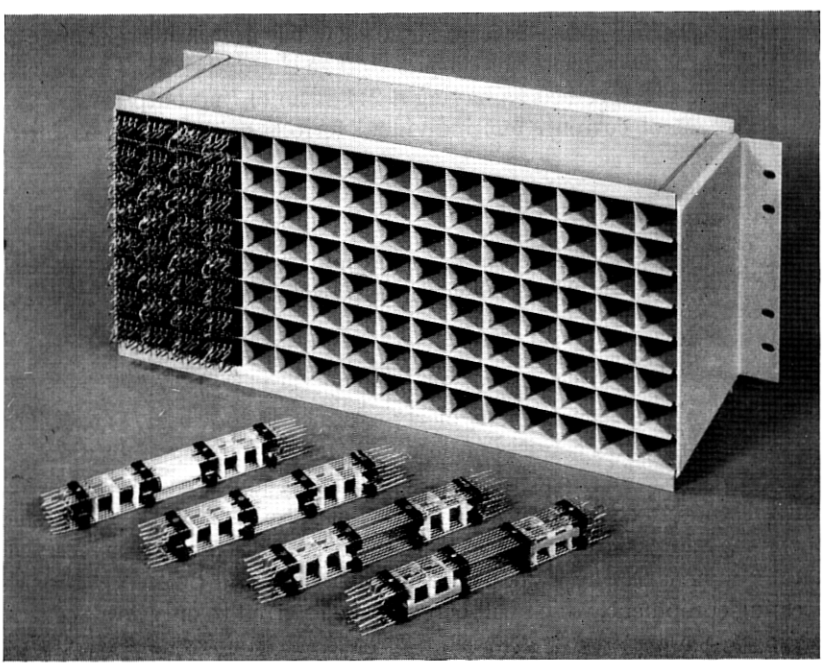

Fig. 3 — Typical ferrods and combined mounting shield.

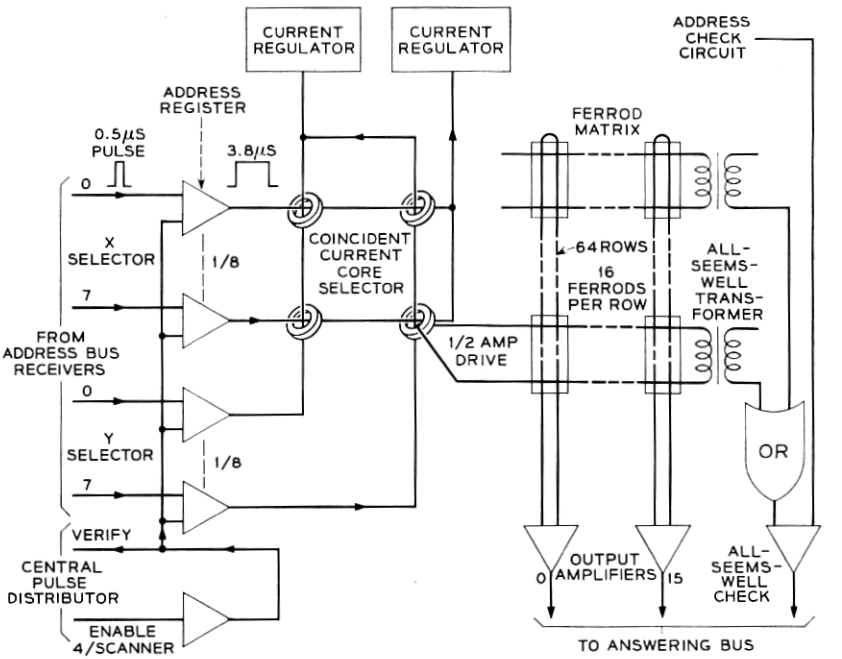

Fig. 4 — Functional diagram of a 1024-point scanner.

control." This in effect selects one of sixty-four cores, the output of which interrogates a row of 16 ferrod sensors. The outputs of all 16 ferrods are detected and transmitted simultaneously back to central control.

3.5 *Scanning Modes and Rates*

The kind of scanner used and the scanning mode, directed or cyclic, depend on the type of information the system desires at any particular time. Each subscriber line is cyclically scanned via a line scanner every 100 msec for originations. When an origination is detected, the subscriber line is connected to a dial pulse receiver. Scanning then occurs, using a master scanner on a directed basis every 10 msec to insure that all of the dial pulses are counted. After all the digits have been received and a connection has been established, the system supervises the call, using either a junctor or a trunk scanner, depending on whether the call is intraoffice or interoffice. Scanning now occurs on a cyclic basis every 100 msec until hangup is detected and the connection is removed. The sequence of events for an intraoffice call is shown in Fig. 5.

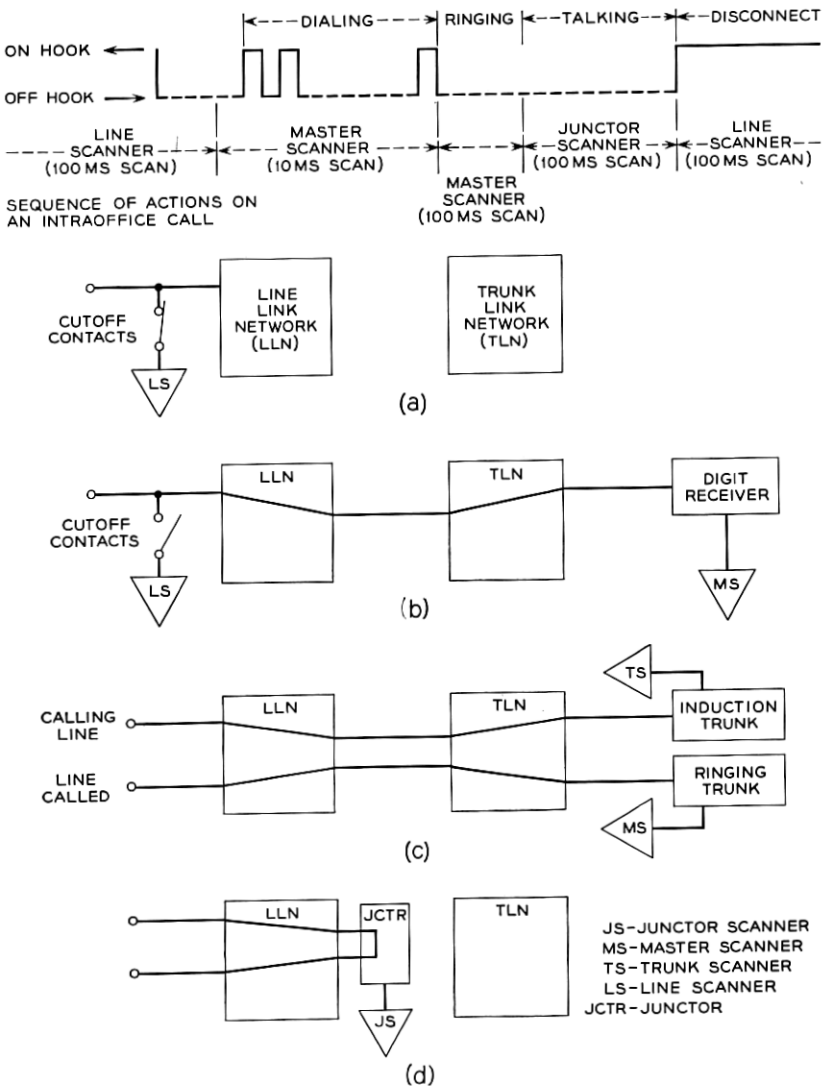

Fig. 5 — Connections for an intraoffice call: (a) line supervision, (b) digit reception, (c) ringing, and (d) talking.

The system uses a basic cycle which is repeated every 100 msec. This cycle is further broken into 5-msec intervals. At the beginning of each interval, the system accomplishes high-priority tasks, such as dial pulse reception and supervisory scanning of junctor and trunk circuits. During each interval, one-half of the digit receivers and one-twentieth of the

junctor and trunk circuits are scanned. Remaining time is used for low-priority work such as line scanning, setting up connections through the network, and maintenance routines.

3.6 *Use of Scanner Information*

There is no intelligence built into a scanner, so all decision making is done by central control. The results of a scan, the states of 16 ferrod sensors, are transmitted simultaneously to central control, where they are stored in flip-flops. These outputs are then compared with the last look information stored in the temporary memory (call store). If there is a change of state, the system, knowing which line (or test point) is involved, concludes that an order was successfully executed or that the next instruction of the stored program must be performed. In either case, the temporary memory is updated.

3.7 *Scanner Organization*

Each scanner consists of two major parts, the ferrod sensor matrix and the access and readout equipment for it. For maximum reliability the access and readout equipment is completely duplicated. Each set of equipment is referred to as a "controller." Ferrods which are assigned on a per-circuit basis are not duplicated.

Being an ESS peripheral unit, each scanner receives and transmits information on the peripheral bus system. This bus system is completely duplicated. Both scanner controllers have the ability to work with either bus. Associated with each scanner are four enable inputs. When the central control selects one of the four enables via the central pulse distributor circuit, it picks a particular controller-bus combination. Each controller-bus combination provides complete access to the unduplicated matrix.

3.8 *Address Register Considerations*

When the central control wishes to scan a particular point, it obtains from the call store the enable information for the particular scanner involved and the X and Y address of the point. This information is in binary form. Since there are many peripheral units (a large central office may contain 100 or more scanners), economic considerations suggest that the central control do as much translation of the binary address as is feasible. The advantage of doing this is obvious. After central control translates the binary word, it sends out addresses in the form of one-out-of-n codes in various numbers of groups, the number of groups and the

value of n being dictated by the size and type of peripheral unit. For a 1024-point scanner there are two address groups each containing eight inputs ($n = 8$).

Addresses (100-ma, 0.5-μsec pulses) are sent to peripheral units as single-rail signals. In practically all cases, these narrow pulses must be stored in order to be useful. Since the input information is sent single-rail, the use of a flip-flop as the storage element would require a reset signal immediately prior to the start of a new cycle or immediately after the execution of an order. The reset signal could, of course, be generated locally or externally. Since the cycle time of a scanner is relatively short (11 μsec), storage elements other than flip-flops become practical. In particular, those types which do not require resetting become extremely attractive. An *LC* type of pulse stretcher which inherently "resets" itself is used by the scanner in its address registers. This type of circuit is also used in numerous other applications in a scanner.

3.9 *Address Register Circuit*

The address register circuit is shown in Fig. 6. It consists of two 2-input AND gates followed by a single pulse stretcher. Each AND gate, one of the primary windings of the transformer, is associated with one of the input buses. The two AND gate inputs consist of an address input and an enable signal. Normally, the enable signal precedes the address to

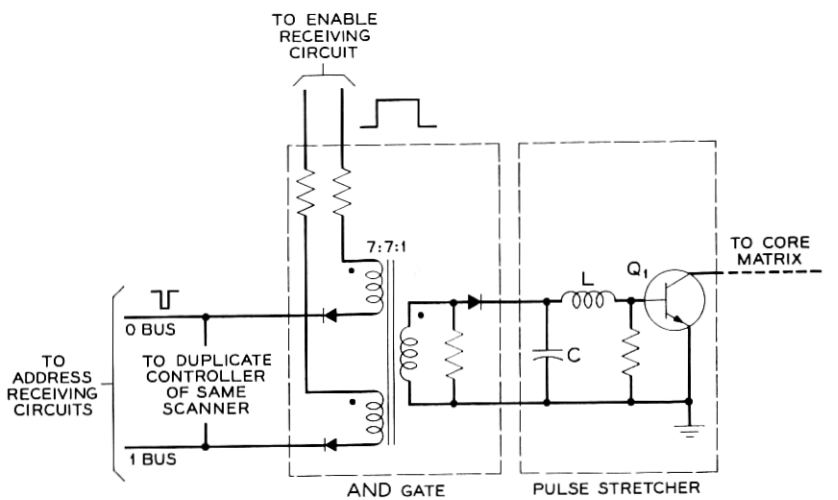

Fig. 6 — Address register circuit.

a controller. To insure sufficient time coincidence of the enable and the address pulses (0.5-μsec pulses), the enable signal is stretched to 2 μsec. Differences in arrival times between the enable and addresses are caused by variations in cable lengths and variations in operate times of transistor circuits.

Battery is connected to one side of the transformer primary by the stretched enable signal. Ground is then applied to the other side of the winding by the address receiving circuit. The resulting current is then transformed to the secondary winding, where it charges capacitor C. The discharge path for the capacitor is through the inductor L and the base-emitter junction of transistor Q_1 to ground. This turns on the transistor for the half-cycle during which the capacitor rings out. A nominal on time of 3.8 μsec is used.

3.10 *Method of Selecting One Row of Ferrod Sensors for Interrogation*

Selection of a particular row out of 64 rows of ferrods in a 1024-point scanner is accomplished using address register circuits previously described and a coincident-current core matrix as shown in Fig. 4. The cores are arranged in an 8-by-8 array. Each core is made of square-loop ferrite and is provided with four windings. Two of these windings are drive inputs and are associated with the X- and Y-address inputs. The third winding is the output, which drives a row of 16 ferrod sensors, while the fourth is the bias winding. When the central control selects one lead in the X group and one in the Y group, it is in effect selecting one row and one column of cores to be driven by 700-ma, 3-μsec pulses. The current pulse to each row and column is a half drive. The core at the intersection of a driven row and column receives full drive, switches, and produces a 0.5-ampere pulse which drives a row of ferrods. Each of the remaining cores in the driven row and column receive only a half drive. These cores do not switch, since half drive is not sufficient to overcome the bias.

The core matrix is duplicated but the ferrod sensor matrix is not. To provide access to the ferrod matrix from either core matrix, the output windings of respective cores in each matrix are connected in series and then to the ferrods. Such an arrangement requires that the standby core matrix present a low impedance to the driving core. This is normally accomplished by maintaining bias current in the standby matrix as well as in the active or driving matrix. The bias current is monitored by a series relay. When current ceases to flow in the bias loop of a matrix, one drive winding of each core in that matrix is switched auto-

matically to the role of a bias winding, using contacts on the released relay. Power is provided to this emergency bias loop from the battery associated with the working controller. The series relay also serves another function. It provides a high impedance in the bias loop, thus preventing unnecessary loading of the drive inputs.

3.11 *Output Circuitry*

It is the function of the output circuitry to convert ferrod outputs (typical amplitudes were given earlier) to signals which are usable by the central control. These signals are then transmitted on both duplicated peripheral reply buses simultaneously. By doing this, synchronous operation of both central controls is possible, since each central control normally receives scanner answers from a different bus.

Scanner output signals consist of either pulses (1's) or no pulses (0's). If the control windings of an interrogated ferrod have less than the nonoperate value of current, the ferrod output is detected and transmitted as a pulse (1). The output of an interrogated ferrod whose control windings have more than the operate value of current is detected and transmitted as a 0.

The output circuitry (see Fig. 7) consists of a 2-input AND-gate amplifier followed by a cable driver. Ferrod outputs provide one input to the AND gate, while a strobe circuit provides the second. Normally, neither of the two transistors in the amplifier is on. If the ferrod output signal has sufficient amplitude to turn on transistor Q_1, its collector current provides base current for transistor Q_2, turning it on. The strobe potential is applied approximately 0.75 μsec after the start of the ferrod output. The resulting current flow from the strobe circuit through the primary winding of transformer T_2 produces an output signal. If the ferrod output signal is insufficient to turn on transistor Q_1, no output signal will be generated when the strobe pulse is applied. However, the strobe input has a fast rise time, so there is an undesirable current path to ground provided by the junction capacitance of the transistor. To prevent this capacitive current from producing a false output, capacitor C is provided as a shunt path around the transformer primary winding.

The readout equipment is duplicated and driven by an unduplicated ferrod matrix. When a controller is ordered to interrogate a row of ferrods, the output amplifiers associated with that controller receive a strobe pulse permitting them to drive both sets of cable drivers.

Signals on the peripheral bus are nominally 0.5 μsec wide. The positive portion of the bipolar ferrod output is approximately 1.5 μsec in duration.

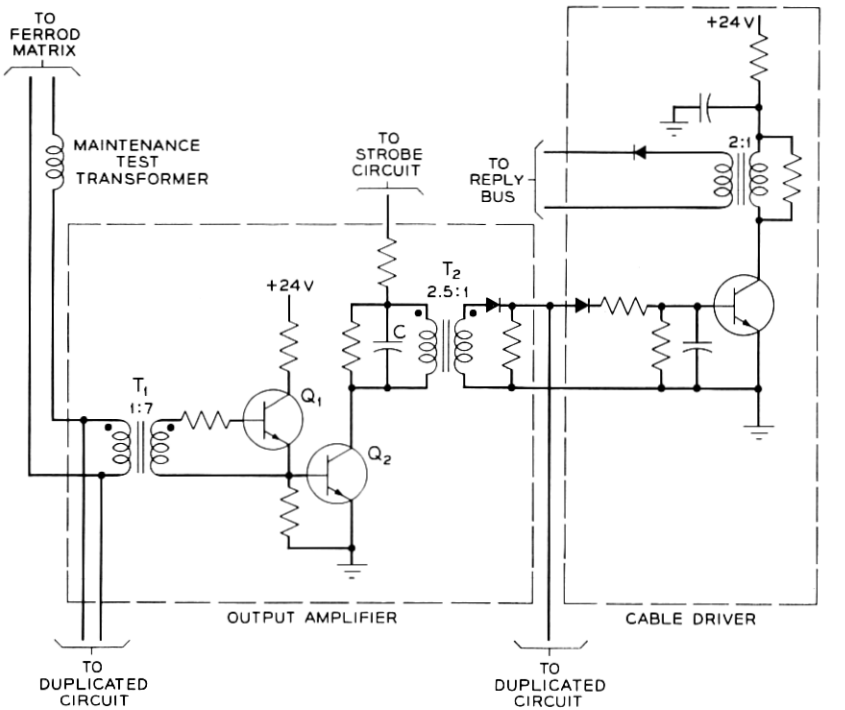

Fig. 7 — Output circuitry.

By sampling this relatively wide pulse with a 0.5-μsec strobe signal, a pulse suitable for bus system use is obtained. There is also a signal-to-noise advantage obtained by strobing. However, the output margins from a ferrod are such that the latter advantage is not an important one in the scanner design.

3.12 *Maintenance Features*

When a controller receives an enable signal over a pair of wires from the central pulse distributor, the signal is stretched to a width of 2 μsec as previously described. At the termination of this stretched enable signal, a new signal is generated by the controller and sent back over the previously enabled pair in such a manner that the enable receiving circuit is not reactivated. Doing this permits central control to verify that the enable signal reached the correct equipment.

During each normal cycle, an all-seems-well scanner (ASW-S) output

is produced and sent with the regular 16 answers to central control. If this pulse does not appear with the scanner replies, the replies are ignored. Central control then repeats the same instruction. If an ASW-S pulse is not produced after several retrials, the particular controller-bus combination used is marked "in trouble" in the call store and another combination is selected merely by using a different enable input to that scanner. When system time permits, the faulty equipment is located, using a stored diagnostic program.

The ASW-S circuitry provides a check on the access part of a controller. In essence, it is a 2-input AND gate. One input indicates that not more than one lead in each address group was selected. The second input indicates that a row of ferrods was interrogated. The absence of either input will manifest itself as an ASW-S output failure.

Normally, scanner outputs are not predictable since they depend upon the state of the ferrods. Therefore, the readout circuitry is routinely checked to determine if it is working properly. This is done using the maintenance test (MT) input which is part of the address bus and is handled like an ordinary address; that is, the enable pulse is first sent, followed by the MT order. In series with each of the 16 readout columns of a ferrod matrix is a secondary of an MT transformer (see Fig. 7), the primaries being in series. By means of these transformers, the MT order generates simulated nonsaturated ferrod outputs. Since the 16 columns receive the test pulse simultaneously, each of the 16 output amplifiers should produce 1's. The ASW-S signal is not produced during this cycle. The absence of an output indicates an open-circuit trouble. Short-circuit troubles in the output amplifiers can be detected by sending an enable and then pulsing only one pair in only one address group. Normally, neither the ASW-S circuit nor any of the 16 output circuits will reply.

A controller can be in any one of several modes, such as normal or power-off. Assigned to each controller are three scan points. When a controller is in a particular mode, it saturates or unsaturates these ferrods so that the unique code assigned to that mode is obtained. By scanning these points, central control can determine the present mode of the controller. These status ferrods are part of the master scanner.

3.13 *Power*

Power for the two controllers of a scanner is provided from an unregulated +24-volt central office battery over separate feeders. The average current requirement for both controllers is approximately 0.5 ampere. In general, ferrod control winding current is provided from the

−48-volt battery. However, there are numerous applications where the +24-volt battery is used instead.

As a maintenance feature, provision has been made to control power remotely by the central control. Out-of-service keys are also mounted on the frame housing the scanner so that power can be removed manually. To insure that power is not removed from both controllers simultaneously, mechanical and electrical safeguards are provided.

3.14 *Equipment Details*[3]

Scanner circuits are built on printed wire boards.[6] This is also true of the coincident-current core matrix. Several circuit packages are shown in Fig. 8. These printed wire boards are plugged into connectors arranged on mounting plates. All connections between circuits are made by wiring from one connector to another.

A master scanner frame is shown in Fig. 9. At the top of this bay are connecting terminal strips and card housings which contain bus and scanner control circuits. The next two mounting plates contain biasing relays, resistors and the control panel. Immediately below these are four ferrod mounting racks. Each rack contains 128 ferrod packages, each package consisting of two ferrod sensors, making a total of 1024 ferrod sensors.

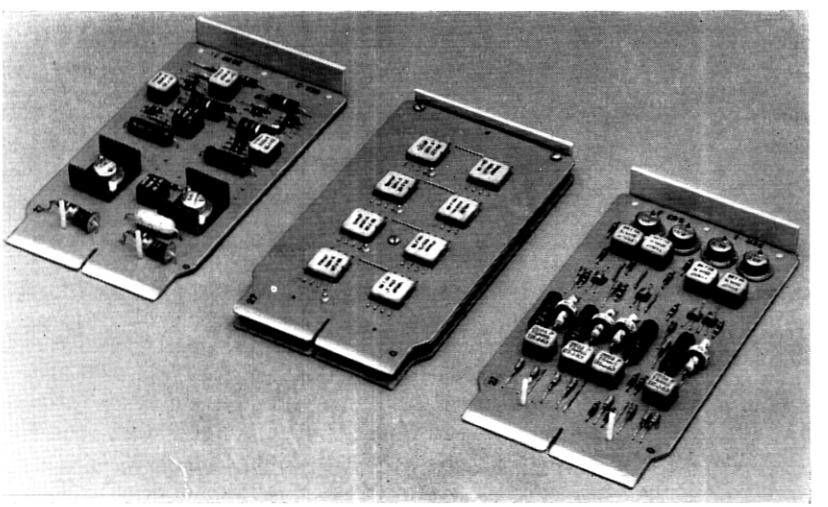

Fig. 8 — Current regulator, 4-by-4 core matrix and address register packages (left to right).

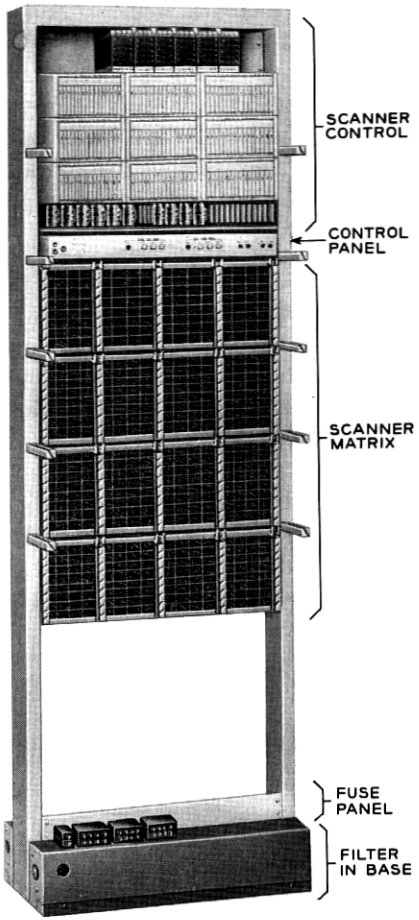

Fig. 9 — Master scanner.

IV. CENTRAL PULSE DISTRIBUTOR AND SIGNAL DISTRIBUTOR DESCRIPTION

4.1 *General*

The central pulse distributors and the signal distributors provide central control with access to many points within the system requiring action signals. Wherever fast access at electronic speeds is required, the central pulse distributor is employed. The signal distributor is used to operate relays in trunk and junctor circuits which do not require access at electronic speeds.

Functionally, both units are large decoders. They are called "peripheral" because they can be located anywhere within the central office and reached from the central control via the peripheral bus. The information is transmitted on the peripheral bus in a coded form. It consists of several groups of 1-out-of-n codes. It is the basic function of both types of distributors to translate this information into 1-out-of-m form, where m is the total number of outputs of the respective distributor.

The decoding and associated functions have to be done in the most economical way which meets the requirements of speed, output level and reliability. The associated functions include receiving and temporarily storing the address information, checking it for errors, and blocking further action while notifying the central control if errors are found.

If errors in the address are not found and the signal indicated by the address is sent out, both distributors in most cases receive a positive indication from the activated point that the decoded signal has been properly received and acted upon. A failure to receive such indication is reported to the central control.

After a failure report, or as a matter of preventive maintenance, the central control may transmit maintenance or diagnostic orders to the respective distributor either to assure that the unit is in proper operational order or to localize a failure.

4.2 *Decoding and Verifying*

The number of outputs required in a distributor is between 512 and 1024. In these sizes, economy can be achieved only if the least expensive devices are provided for each output point. At the present state of the art, there is no electronic device that can economically compete with a contact on a large relay as a decoding element. For this reason the decoding in the signal distributors, where the required access cycle is about 20 msec, is performed by relay contacts.

Where the required access rates exceed the capabilities of relays, electronic devices have been employed. There are several possible arrangements that could provide a decoder capable of operating at electronic speeds in the microsecond range.

In the No. 1 ESS, a diode-transformer gate was chosen as the decoding element in the central pulse distributor (see Fig. 10). One of the reasons is that the transformer provides a balanced output. A pulse from such an output point can be transmitted over twisted pair to remote locations without interference. Also, the pulse provided by an electronic pulser can be shaped so that the least amount of noise is generated in the adjoining cables.

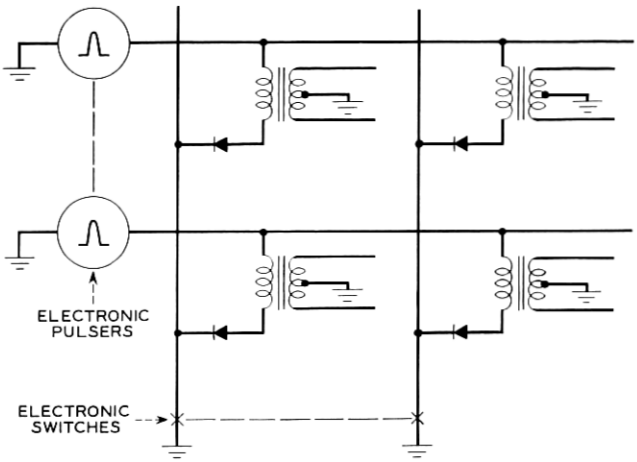

Fig. 10 — Transformer-diode selection matrix.

Another advantage of the transformer-diode arrangement is that bipolar pulses can be easily generated and transmitted by employing a three-winding transformer (see Fig. 11). In many cases, this is done to control the operation and release of a relay over a single pair of wires by using a receiving device that can recognize the two polarities. In the ESS such a device, called a "bipolar flip-flop" (see Fig. 11), is widely employed. This flip-flop assumes one state upon receiving a positive pulse and the other upon receiving a pulse of opposite polarity.

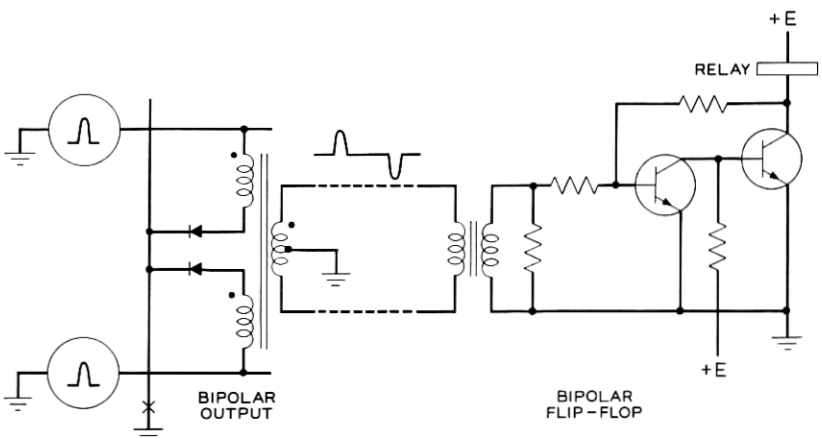

Fig. 11 — Bipolar operation.

The use of a three-winding transformer also provides for the verifying requirement. Whenever the signal transmitted from the central pulse distributor is to enable a peripheral unit for receiving an address from the central control on the peripheral bus, an answer that the enabling has been properly initiated is expected. Such an answer could be transmitted on a separate cable pair. However, the cable pair that transmits the enabling order is vacant at the time the verify answer should come. By employing the third winding on the transmitting transformer, the verify answer can be received over the same cable pair (see Fig. 12).

4.3 *Address Storage*

All the signals on the peripheral bus are in the form of nominal 0.5-μsec pulses. In the signal distributors, the information received from the bus has to be checked for errors before it is acted upon. Some kind of information storage is therefore necessary. The length of storage depends upon the time required to carry out the function of the unit.

In the signal distributor, the information has to be stored until the magnetically latching output relay has definitely operated or released. This time is somewhere between 10 and 20 milliseconds. A bistable transistor circuit (a flip-flop; see Fig. 13a) is employed to perform the storage function in the signal distributor. This flip-flop must have the proper input gating circuitry to permit reception from either of the two buses.

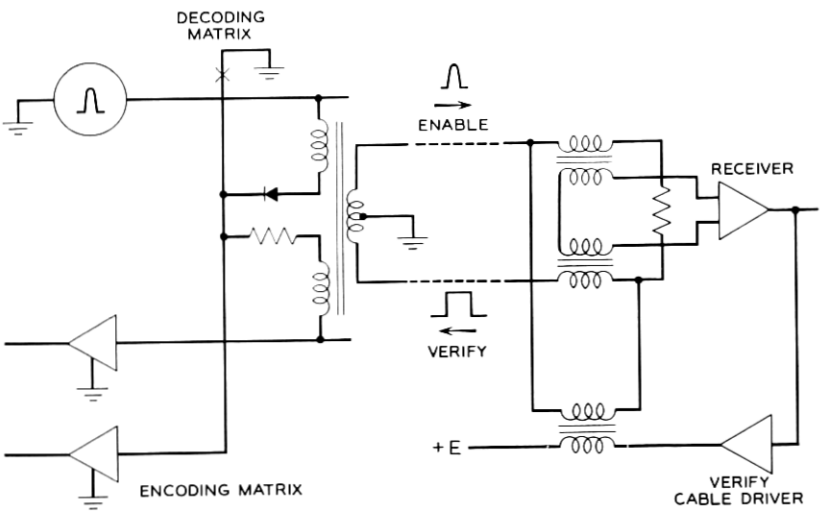

Fig. 12 — Enable-verify operation.

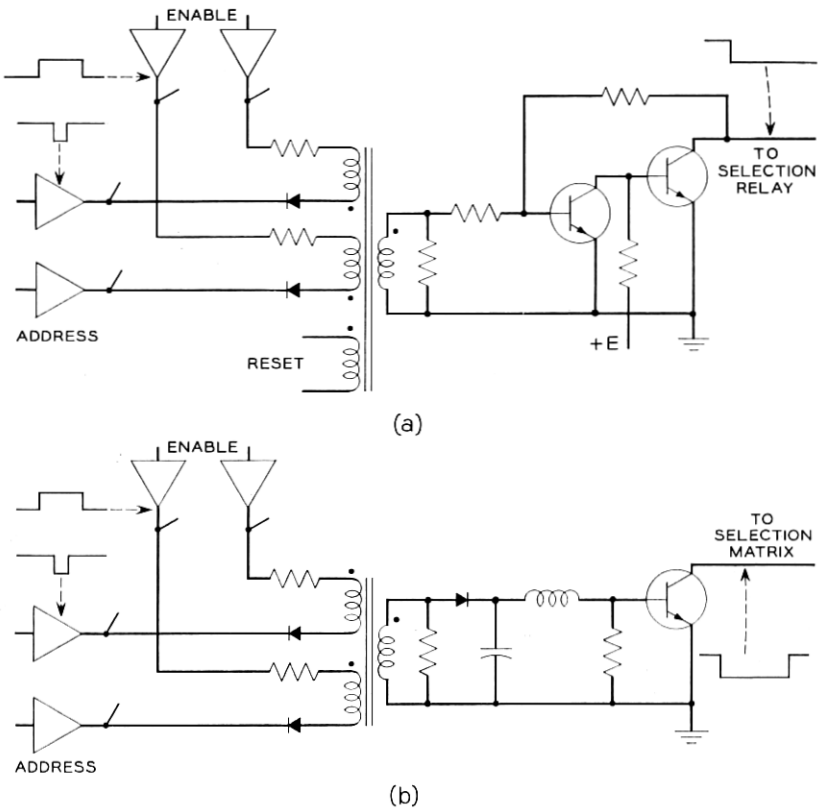

Fig. 13 — Address storage registers.

It also should be capable of operating the primary decoding relays directly, and should use the minimum of components. A special flip-flop has been designed that employs transformer-diode gating for the input signals and has the primary relay as a collector load without buffer stages.

The primary relays operate the multicontact wire spring relays that actually establish a path within the decoding matrix to the output relay.

In the central pulse distributor, the address need only be stored for about 2.5 μsec to perform the error checks and produce a nominal 0.5-μsec output pulse. A device simpler than a flip-flop can be employed. A storage circuit that simply stretches and amplifies the input pulse is used (see Fig. 13b). The input gating is quite similar to that in the signal distributor storage circuit. The stretching is accomplished by a diode-capacitor-inductor combination, which provides a rather exact timing

virtually independent of variations in the input pulse and supply voltage. The transistor acts as an on-off switch and amplifier. The transistor in the register cell controls the decoding matrix.

4.4 *Error Check*

The address information received by the distributors from the central control may contain errors. Errors may be caused by noise in the transmission path. There may be translation errors in the central control, or a faulty component in the sending or receiving circuitry may cause an error. Finally, errors may be purposely introduced in the address to check the error checking circuitry.

The error checking circuitry must find the errors before the action indicated by the address is carried out. The address is transmitted in groups of 1-out-of-n codes. For instance, the address to the central pulse distributors is in the form of 1-out-of-8, 1-out-of-8, and 1-out-of-16 code, a total of 32 pairs. A 1024-point signal distributor receives its address in a 1-out-of-8, 1-out-of-8, 1-out-of-4, 1-out-of-2, and 1-out-of-2 code.

For an address to be correct, each group should contain one and only one active signal. A signal completely missing in a group would constitute an error, as would two or more signals within a group.

In the signal distributor, the check for errors can be performed by employing the proper combinations of spare contacts on the selection relays, as shown in Fig. 14.

The final selection relays have only make contacts. If a signal is missing within any group and no relay within that group operates, a path cannot be established through the selection matrix. If more than one relay within a group operates, a double path will be established and a wrong output point activated. To prevent this, the contacts of the relays are arranged in a combinational network that will provide a path whenever more than one relay operates.

The presence of such a path within any group will prevent the application of the final output current and notify the central control about the nature of the error.

The central pulse distributor has been designed to find an error in the address within less than a microsecond, and electronic circuits have to be employed. The error check is performed at the outputs of the register cells in the three groups.

It is a simple matter to check that at least one register cell within a group has been activated. An OR gate is provided with as many inputs as there are cells in that group and one input connected to each cell. The output of the OR gate indicates that there is at least one activated cell

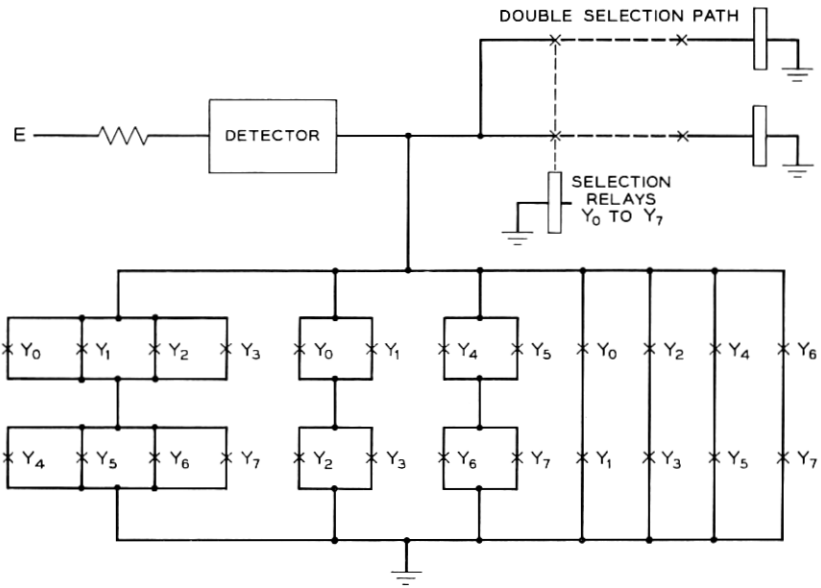

Fig. 14 — Error checking circuits for more than one signal in SD.

in that group. To ascertain that there is no more than one cell activated within that group, a rather elaborate arrangement of logic gates is necessary. For a 1-out-of-n group with $n = 16$, such an arrangement becomes prohibitive. In the central pulse distributor, therefore, a digital-to-analog conversion method is used (see Fig. 15). Let each addressed cell within a group control a unit of current $-i$. Let these currents be added in a low-impedance discriminating circuit of sufficient accuracy to distinguish between one and two units of current. Then the outputs from the discriminating circuits properly combined with the outputs of the OR gates will indicate that there is an error in the address, block the final action, and notify the central control about the type and location of the error.

4.5 *Final Outputs*

If no errors in the address are indicated, the distributors proceed in producing the final output. In the central pulse distributor, the three groups of register cells have already prepared a path in the three stages of selection matrix (see Fig. 16). A properly shaped pulse is now applied at the apex of the matrix and finds its way to the selected output. As

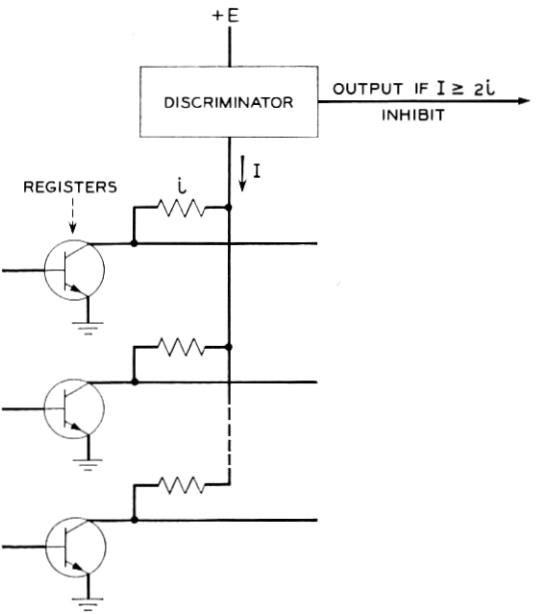

Fig. 15 — Error checking circuits for more than one error in CPD.

it proceeds through the final selection stage, a measurement of the pulse amplitude is made. If the amplitude is within the proper limits, an all-seems-well (ASW) signal is sent to the central control, indicating that the final action has been successfully completed. Absence of the ASW signal indicates either a missing or excessive output pulse. This causes the central control to initiate a trouble localizing or maintenance routine.

The final output element in the signal distributor is a magnetic latching relay. The pulses from the signal distributor have to be long enough and of the proper polarity either to operate or release the relay. The relay then will maintain this state until the next signal. There is no holding current required, which constitutes an appreciable power saving. The latching feature is obtained by making the armature of a mildly remanent material. The duration of the release current, however, must be sufficiently controlled to prevent a reversal of the field during release. A spare contact on the relay is used to verify the operation of the relay. It cuts in and out a shunt resistor, and the change in current is monitored at the apex (see Fig. 17) of the selection matrix. The proper change is interpreted as a successful operation and terminates the pulse to the relay.

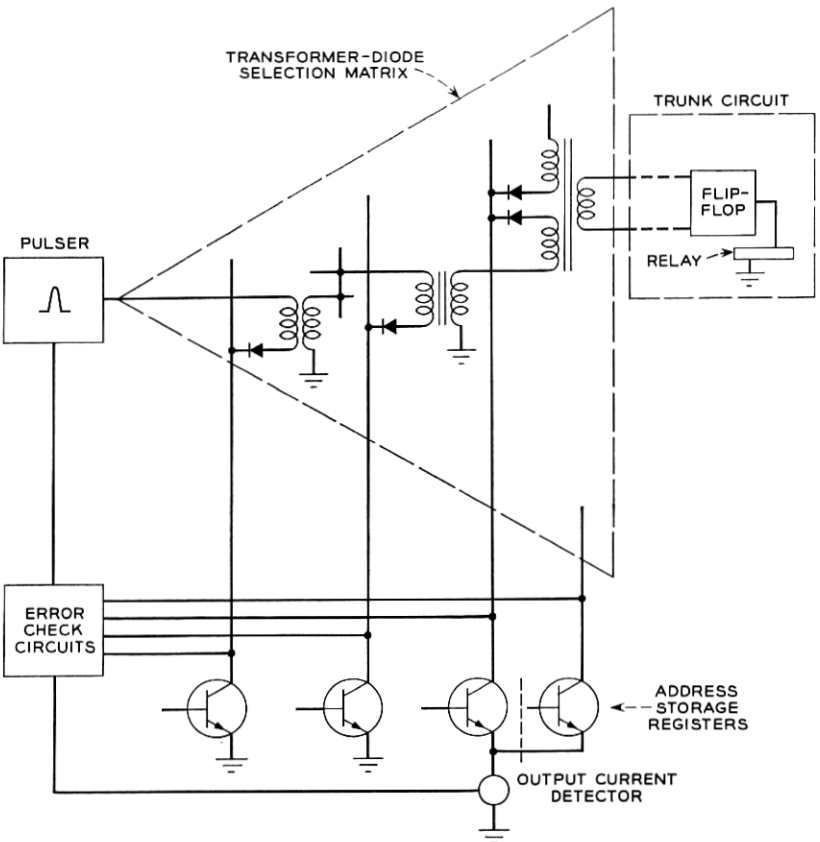

Fig. 16 — Selection in the CPD.

4.6 *Duplication*

The design of the distributors must provide sufficient reliability. A situation where failure of a component would disable the whole system cannot be tolerated.

To insure such reliability, duplication is employed. The central pulse distributors are always provided in pairs. The outputs are either connected together in such a way that either unit can send a signal to the remote point, or, when more than one output is needed for a function, the outputs are equally distributed between the two units. In the signal distributors, the control circuits are duplicated in such a way that either one of them can control all the outputs.

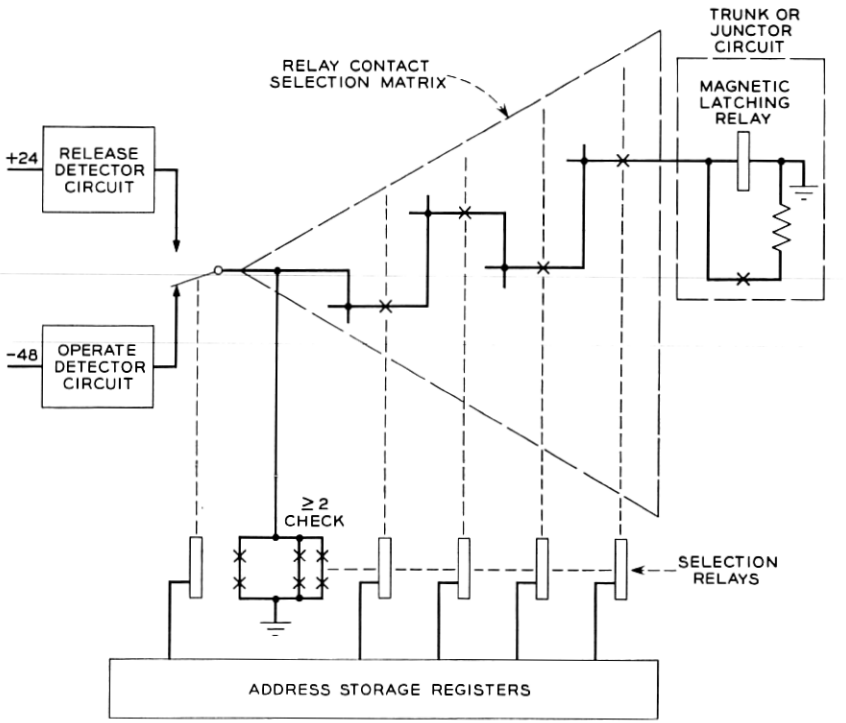

Fig. 17 — Selection and verification in the SD.

4.7 *Equipment Arrangement*

The signal distributors are incorporated in junctor and trunk frames with the magnetic latching relays located in the individual trunk and junctor units. The duplicated control equipment, comprising electronic packages, mercury-wetted contact relays, and wire spring relays, occupies one half of an ESS rack and is shown in Fig. 18.

The central pulse distributors are in their own frames, which also include peripheral bus signal repeaters. A typical central pulse distributor is shown in Fig. 19.

Equipment design details are described in associated articles.[3,6]

4.8 *Conclusion*

The basic principle of No. 1 ESS has been to minimize the varieties of subsystems, while providing the necessary functions in the most econom-

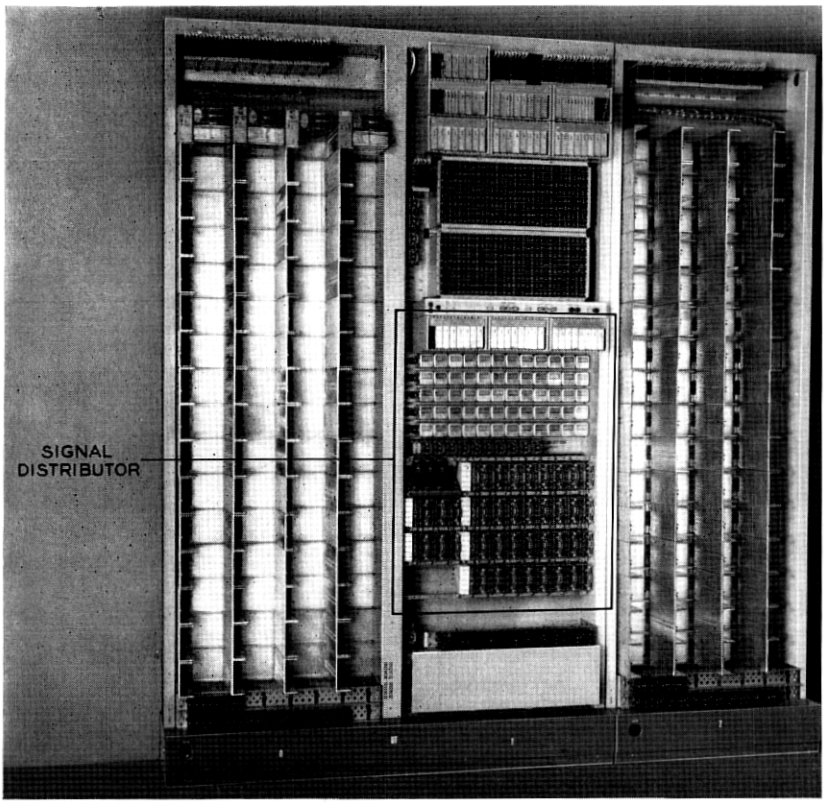

Fig. 18 — Signal distributor in trunk frame.

ical manner. The division of the action subsystems into two categories — signal and pulse distributors — which was dictated at the time of development by the existing state of the art, does indeed provide the necessary functions in the most economical manner.

V. ACKNOWLEDGMENTS

The design and development of the peripheral units described above required the efforts of many people outside the electronic switching area. Particular thanks are expressed to J. A. Baldwin, who collaborated in the ferrod conception, and to H. J. Wirth and R. F. Glore, who contributed the mechanical design of the ferrod. Thanks are expressed to F. P. Balacek, T. G. Grau and A. K. Spiegler for their development of the magnetic latching relay. Within the electronic switching area of Bell

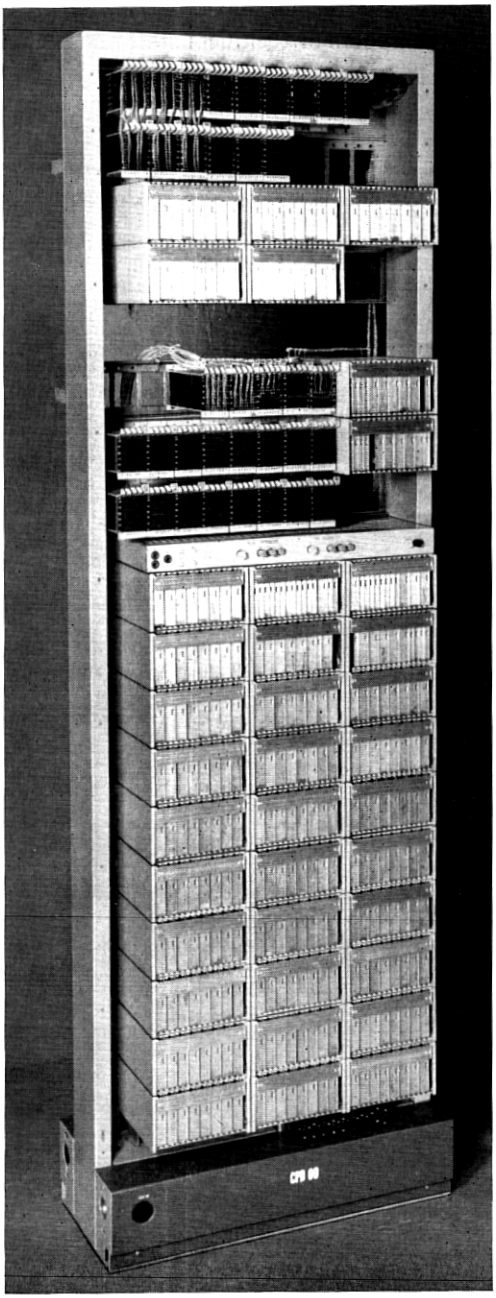

Fig. 19 — Central pulse distributor.

Laboratories, the fine equipment engineering and the unstinting cooperation of many other members of technical staff and technical aides made these developments possible.

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