An Insertion Loss, Phase and Delay Measuring Set for Characterizing Transistors and Two-Port Networks Between 0.25 and 4.2 gc

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A new insertion loss, phase and delay measurement tool has been developed for characterizing gigacycle bandwidth transistors and general two-port networks on a small signal basis over a frequency range from 0.25 to 4.2 gc. Maximum inaccuracies are 0.1 db, 0.6 degree (over a 40-db loss range), and 0.5 nanosecond (over a 20-db loss range). Above 2.0 gc, the errors may double.

The particular parameters selected for measurement are closely related to the scattering coefficients of the device under test, evaluated with respect to a 50-ohm impedance level. When measuring transistors, measurement data are corrected for the residuals of jig and bias fixtures. Transformation from the measured parameters to other sets (e.g., h, y, or z matrices) is routine.

In order to minimize "instrument zero-line" and eliminate errors from circuit drift, a rapid sampling technique sequentially compares the unknown with a high-frequency reference. Measurement accuracy is held substantially independent of test signal frequency by heterodyning the measurement information to a fixed IF, where detection is performed by "IF substitution", using adjustable standards of loss, phase, and delay. Substantial use of automatic control circuitry contributes to an easy and facile interface between machine and operator.

This paper discusses the operation and design of the test set and its use as a tool in characterizing transistors.

I. INTRODUCTION

A new measuring instrument has been developed for making insertion loss, phase, and envelope delay measurements between 0.25 and

4.2 gc. The development was stimulated by measurement requirements growing out of recent advances in gigacycle transistor technology and semiconductor amplification for high bit rate PCM systems. The new instrument extends to 4.2 gc many of the operational features embodied in lower frequency instruments previously reported.[1,2,3]

This new test set is intended for characterizing transistors and general two-port networks, either passive or active, in a coaxial mode between 50-ohm terminations. By use of appropriate transducers, measurement may be extended to noncoaxially terminated unknowns. Of particular interest is the measurement of transistors using a special jig designed to provide a smooth electrical transition between the coaxial geometry of the test set ports and the pig tail lead geometry of the transistor. Waveguide networks are measured with the help of well-matched coax-to-waveguide transducers.

Since the need for reliable transistor characterization over the UHF band was an especially strong stimulus to the development of the measurement set, Section II deals with the transistor measurement problem and how it was solved. This section discusses the merits of the selected plan of measurement, the design of the required jigs and fixtures, the abstraction of transistor parameters from the measurement data, and examples of the results obtained.

Section III deals with the performance of the test set and the basic principles of measurement which are employed.

Sections IV and V describe the measurement circuit in progressively finer detail, starting from a block diagram description. Design questions are discussed, together with approaches used in solution. The goals which motivated the design are summarized.

Among the prime goals was measurement of transistors under "small-signal" excitation. The instrument design was to promote a congenial interface between operator and machine, the aim being to simpify the measurement procedure. This serves both to speed up measurements and reduce operator error.

Validation of accuracy and estimates of the residual inaccuracy are covered in Section VI.

Equipment design features of particular interest are noted in Section VII.

II. TRANSISTOR CHARACTERIZATION

Transistor characterization with the new test set makes use of the following basic data:

(*i*) Insertion loss and phase of the transistor between nominal 50-

ohm generator and load terminations for both the forward and reverse direction of transmission.

(*ii*) Insertion loss and phase which result when first the input terminals and then the output terminals of the transistor are bridged across the transmission path formed by connecting the 50-ohm generator directly to the 50-ohm load. During these bridging measurements, the terminal pair *not* connected to the bridging plane is terminated with 50 ohms.

These four measurement parameters lead naturally to an "exterior" characterization of the transistor in terms of its scattering (s) parameters. Data under (*i*) produce directly s_{21}^{-1} and s_{12}^{-1}; measurements under (*ii*) relate to s_{11} and s_{22} through elementary bilinear transformations. The scattering parameters can be routinely transformed to any of the other usual 2 terminal-pair descriptions (h's, y's, or z's) or, with more work, interior descriptions (e.g., equivalent circuits) may be deduced from the measurement data.

At high frequencies, this method of measurement has several advantages over techniques which attempt to measure directly the h, y, or z parameters. The direct measurement of these parameters calls for the projection of ac shorts and opens to the ports of the transistor through the arms of an intervening jig. It is difficult to reflect these singular values of impedance to the transistor terminals because of the impedance distortions introduced by the parasite residuals of the jig paths and dc biasing arrangements. Moreover, the necessity for using resonant lines to achieve the shorts or opens makes for a high degree of frequency sensitivity and may cause the transistor to oscillate. All of these difficulties are overcome by measuring the transistor between resistive impedances of moderate (and realizable) magnitude. At an impedance level of 50 ohms, stray reactances that would ordinarily make the realization of very large or very small impedances impracticable up to 4000 mc can be compensated so that they produce only modest reflections.

In the previously reported work on transistor measurements up to 250 mc,[1] much effort was expended to develop very low reflection jigs and biasing apparatus. In the case of UHF measurements, where development problems are more severe, it has proved fruitful to pursue an alternative course. Only a modest effort was expended on the design of jigs and biasing fixtures, but these devices were carefully characterized in a series of intensive measurements, and an analytic program was worked out to correct the transistor measurement data for impedance and transmission defects of the measurement hardware.

This approach was attractive for a number of reasons. First, the difficulties of developing jigs and bias fixtures having reflection coefficients under 0.02 up to 3000 mc appeared extremely formidable when compared with the labor of characterizing this hardware and accounting analytically for its defects. Secondly, there is little advantage to be gained in synthesizing a totally reflection-free environment since, even under ideal conditions, the computational work in transforming the measurement data to other characterization sets is sufficiently laborious to warrant the use of a digital computer. It is straightforward to include in the computer program the compensation for the transmission and impedance defects of all auxiliary test devices. And finally, since the measurement set views the transistor through the comparatively long path contributed by the biasing fixtures and jigs, corrections for path length must be introduced even in the absence of reflection. The "transformer" effect of the jig paths during the bridging measurements, for example, alters the apparent impedance of the transistor as sensed by the test set, and must be accounted for.

2.1 *Transistor Jig and Bias Fixture*

The jig for mounting the transistor under test was designed to adapt between the coaxial measurement ports of the test set and the pig tail lead geometry of "TO-18" encapsulated transistors. The objective was to bring a 50-ohm measurement plane right up to the base of the transistor header. In view of the plan to account analytically for hardware defects, a modest reflection target of 0.1 was set up for purity of the nominal 50-ohm termination looking toward source or load from the base plane of the header over the frequency range from 0.25 to 3.0 gc. The transistor lead wires were not to be bent during insertion into the jig, and the jig was designed to allow the metal case of the transistor to be firmly grounded.

The basic principle in achieving a smooth transition consists of forming 50-ohm coax lines around the transistor lead wires inserted into the jig. Fig. 1 shows the actual jig worked out using this principle. Each of the two cylindrical holes in the top of the jig forms a 50-ohm transmission line with one of the terminal wires of the transistor. The lead wires penetrate a brief distance before plugging into a short metal cylinder which functions as the inner conductor segment of a larger bore, 50-ohm line. The cylinder is drilled with a long hole for storing up to $\frac{1}{2}$ inch of lead wire. Discontinuity capacitance caused by the diameter difference between the two sections of 50-ohm line has been compensated by an appropriate setback of the step in the inner conduc-

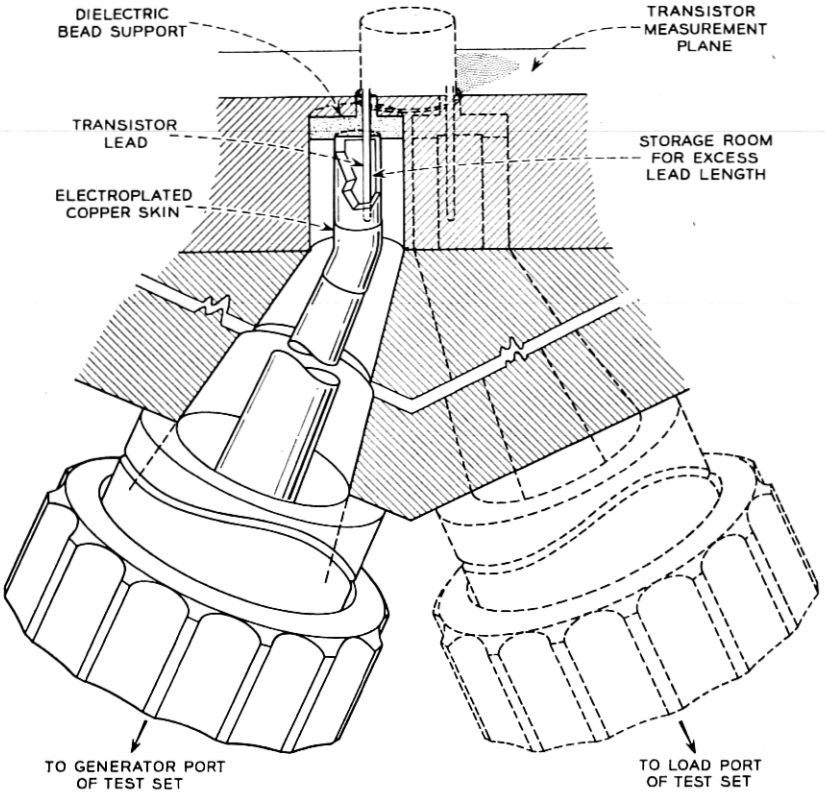


Fig. 1 — Transistor test jig for UHF measurements.

tors.[4] Conically tapered inner and outer conductors below the head piece of the jig slowly bring up the coaxial diameters to match those of a "Dezifix B" fitting. The tapered inner conductor is joined to the short segment of hollow inner conductor by means of a thin electroplated copper skin.

Dc biasing currents and voltage must be introduced to the transistor through the two coaxial paths of the jig. This is accomplished with the aid of biasing fixtures connected to the Dezifix ports. Each biasing fixture consists of a section of 50-ohm transmission line having an inner conductor interrupted with a series capacitor. Dc activating signals are fed in through a high-impedance tap connected to the segment of inner conductor adjacent to the jig. The construction of the bias fixture is suggested in Fig. 2.

Characterization measurements reported in Section 2.4 indicate a

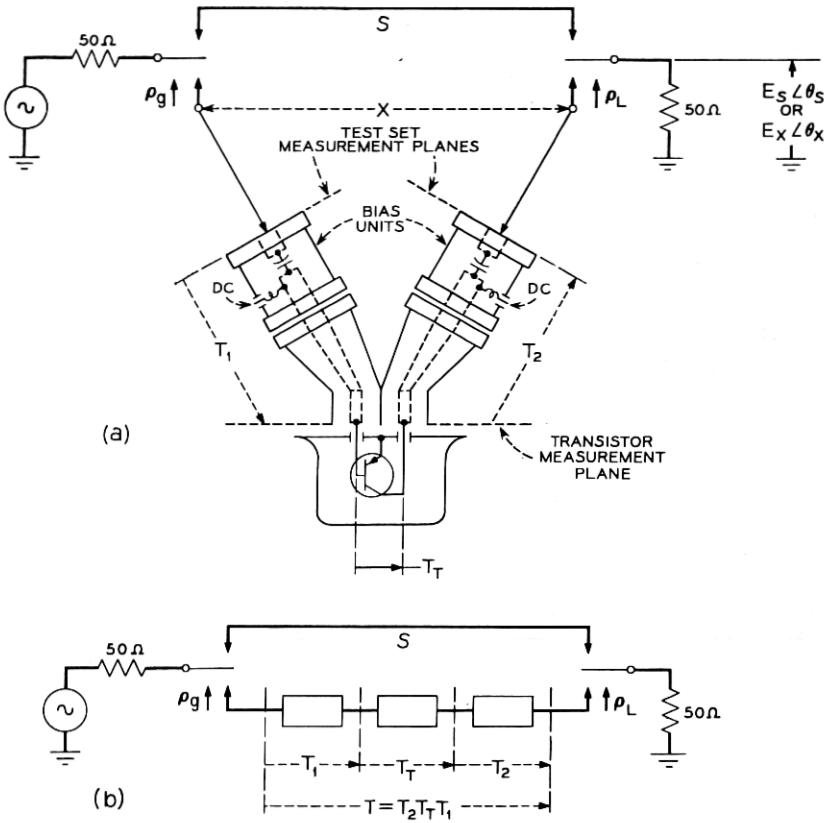


Fig. 2 — (a) Insertion loss, 20 $\log_{10} E_s/E_x$, and insertion phase, $\measuredangle \theta_s - \measuredangle \theta_x$ yield information for computation of scattering parameters S_{21} and S_{12} of transistor; (b) analytical model.

net reflection of less than 0.12 for the path between the small bore (transistor) port of the jig and the output port of the biasing fixture. This applies up to 2.5 gc.

The photo in Fig. 3 shows the jig-bias fixture assembly. Clamping plates for grounding the low-potential transistor lead are visible in the photo.

2.2 *Transistor Measurement*

It was noted previously that a minimum of two transmission measurements and two bridging measurements completely characterize the unknown being tested. For the most precise work it is actually necessary

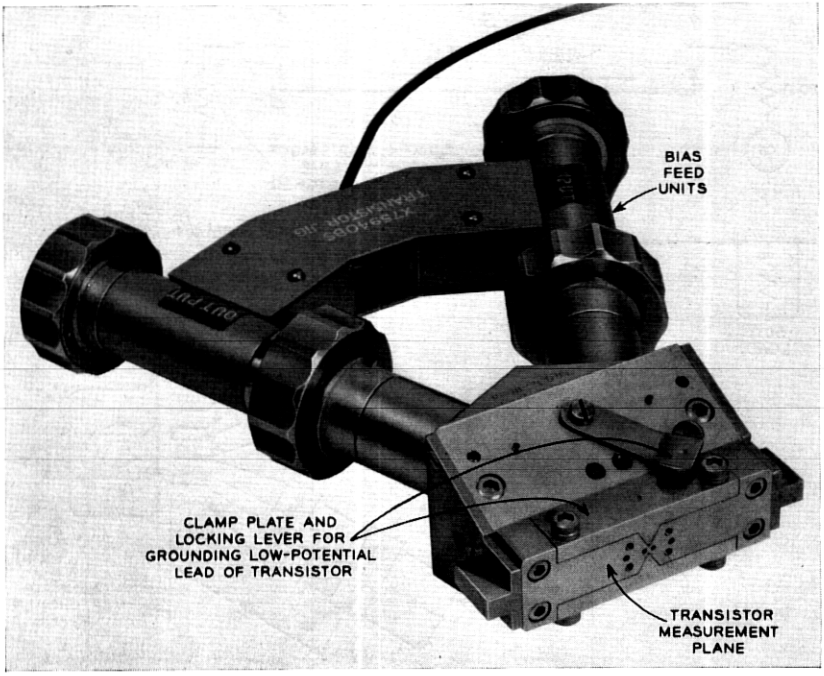


Fig. 3 — Jig and bias unit showing clamp mechanism for joining low potential lead of transistor to measurement plane.

to make additional "calibrating" measurements in order to take account of the electrical length of the jig and to compensate for the small but significant reflections presented at the coaxial test ports of the measuring set. The following procedure is required.

(*i*) The insertion loss and phase in both directions of transmission is measured, as suggested in Fig. 2. The measured losses and phases apply to the tandem connection of transistor, jig, and bias units. To obtain the transistor's loss and phase, the contributions of the jig and bias units must subsequently be subtracted out.

Next, the bridging measurements are made; the details are shown in Fig. 4. Several consecutive steps are involved, as noted below.

(*ii*) The input impedance of the transistor, as viewed through the input bias unit and jig path is connected to one of the ports of a coaxial "trombone". The other port of the trombone bridges the nominal 50-ohm transmission path in the test set. By "play-

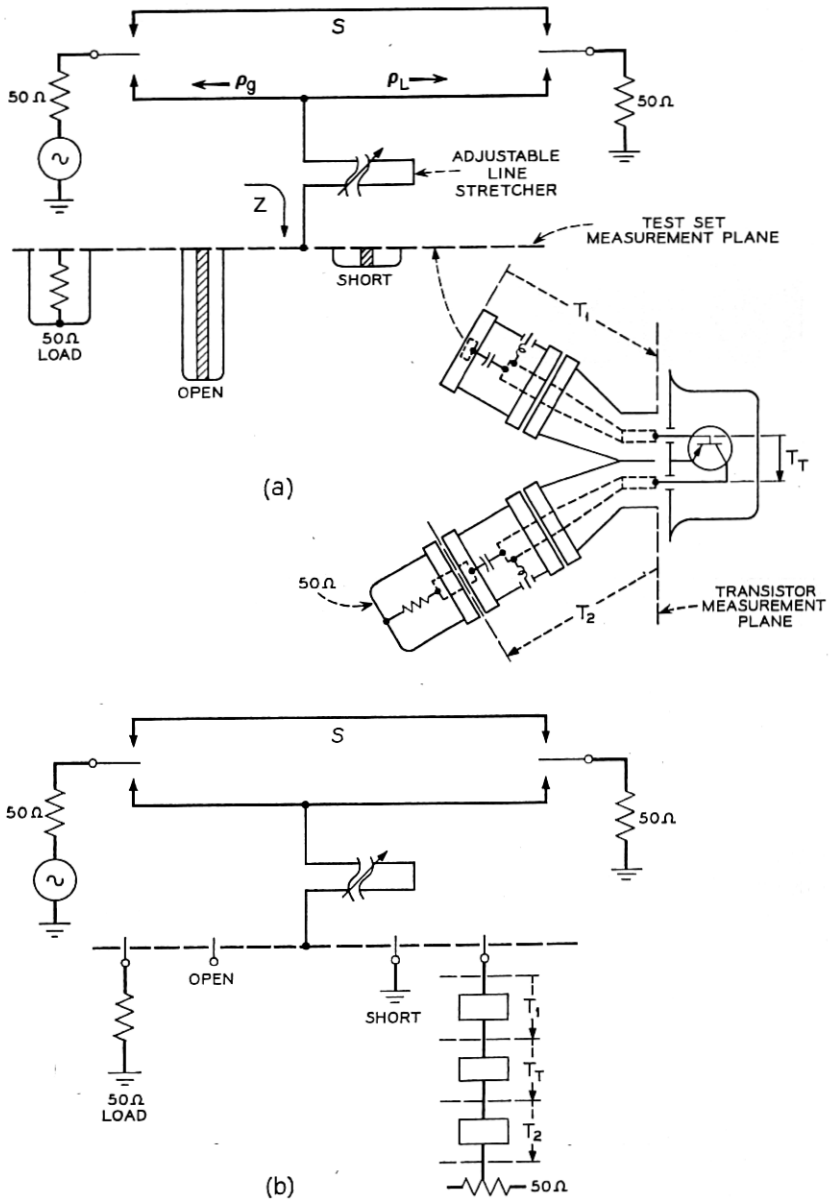


Fig. 4 — (a) Bridging loss and phase measurements to determine S_{11} and S_{22} of transistor; (b) analytical model.

ing" the trombone, a point is quickly found at which the indicated insertion loss is maximum. The loss and phase at this point are recorded; the line is now left undisturbed during the subsequent step (*iii*).

The purpose of the adjustable line is to overcome potentially adverse effects due to the transformation of the transistor input impedance by the electrical length of the input bias unit and jig path. With the physical lengths actually involved, quarter-wave inversion of small impedances to high may occur at frequencies as low as 300 mc. High impedances, if directly connected to the bridging junction in the 50-ohm transmission path, produce only small insertion losses and, as a result, accuracy suffers. The interposition of the adjustable line circumvents this difficulty since a length may always be found which reinverts high impedances back to low.

(*iii*) A known interrelation exists[1] between the impedance, Z, connected to the test set measurement plane at the accessible port of the line stretcher (Fig. 4), and the insertion ratio, $e^{-\theta}$, which this connection produces:

$$e^{-\theta} = \frac{A + BZ}{1 + CZ}. \tag{1}$$

The A, B, and C are constants which depend only on the line stretcher and the test set network behind it. At each frequency of measurement, the three constants may be evaluated by measuring loss and phase for three known values of Z. By combining the three calibrating measurements with the initial measurement on the unknown, the impedance of the unknown may be evaluated. As may be seen in Fig. 4, the calibrating measurements are made by observing the loss and phase caused by connecting in succession a coaxial short, a coaxial open, and a matched termination to the test measurement plane.

(*iv*) Steps (*ii*) and (*iii*) are repeated with the jig turned around to present the output impedance of the transistor to the test set.

To avoid inaccuracies, the standard reflections must be known with exactness, and they must be attached to the test set in precisely the plane occupied by the unknown in step (*i*). The required coincidence between all measurement planes has been assured through the use of the connector type (Dezifix B) in which electrical and physical junction planes are identical.

The 50-ohm standard exhibits a reflection smaller than 0.01 up to

4000 mc. The short-circuit standard is realized with a simple shorting plate and the open circuit is a 90° long section of shorted 50-ohm line of precisely controlled length and transverse dimensions. During the calibrating measurement with the open circuit, the test signal frequency is set to the appropriate nominal with an accuracy of at least 0.1 per cent.

2.3 *Reduction of Measurement Data to Transistor Parameters*

All of the measurements in Section 2.2 are made with respect to terminal planes remote from the transistor. Hence, in order to obtain the contribution of the transistor parameters, it is necessary to subtract out the contribution of the path through the jig and bias fixtures.

If, as indicated in Figs. 2 and 4, the circuit properties of the jig paths and the transistor are expressed individually in terms of their transmission, or "cascade wave" matrices,[5] then the over-all matrix, T, between the ports of the aggregate unknown is

$$T = T_2 \, T_T \, T_1 , \tag{2}$$

where the matrices T_2, T_T, and T_1 refer, respectively, to the output jig path, transistor, and input jig path.

T is defined from the measurements outlined in Section 2.2. T_1 and T_2 are known from the characterization work discussed in Section 2.4. Hence, T_T is completely defined in terms of known matrices, and may be deduced from (2) by the elementary inversion

$$T_T = T_2^{-1} \, T \, T_1^{-1}. \tag{3}$$

T_T may be converted to any of the other characterization sets, e.g., s, h, y, or z parameters.

The actual processing of data involves the following operations, all of which are run on a digital computer.

(*i*) Using relationships developed in previous work,[1] the scattering coefficients, s_{11} and s_{22}, of the aggregate unknown are computed from the bridging measurement data of steps (*ii*), (*iii*), and (*iv*) in Section 2.2. The impedance reference for the S matrix is 50 ohms.

(*ii*) From the transmission data for the aggregate unknown in step (*i*) of Section 2.2, it is possible to compute directly s_{21} and s_{12}.[1] The program includes a necessary correction for the residue of mistermination caused by the fact that the test set reflection coefficients, ρ_G and ρ_L, are not zero. These reflections have

been measured at a large number of frequencies in the 0.25 – 4.2-gc range, and are known.

(*iii*) The complete scattering set,

$$\begin{bmatrix} s_{11} & s_{12} \\ s_{21} & s_{22} \end{bmatrix}$$

obtained from (*i*) and (*ii*) above is transformed to the corresponding matrix, T.

(*iv*) T is inserted into (3) together with the known characterizations T_2 and T_1 and the coefficients of the wave matrix of the transistor, T_T, are computed.

(*v*) T_T from step (*iv*) is transformed to other matrix sets.

A typical end result of this process of measurement and data reduction is illustrated in Fig. 5. The figure shows examples of two of the frequency characteristics of a UHF transistor derived from the measurement and data assimilation routines just outlined.

2.4 *Characterization of Jig and Bias Units*

Serious errors occur in the value of the deduced transistor parameters if the values taken for the matrices T_1 and T_2 do not faithfully represent the actual networks. Hence, considerable care was exercised in the measurement program for obtaining their characterizations.

Since T_1 and T_2 represent networks having very small losses, they were conveniently characterized by a variant of the "Weissfloch" technique. This procedure is based on the well-known transformer law

$$\rho_{in} = s_{11} + \frac{s_{12}^2}{1 - s_{22}\rho_L} \cdot \rho_L \tag{4}$$

relating the reflection looking into a passive two port to its scattering parameters and load side reflection. For example, to determine T_1 at one of the assigned frequencies, reflection coefficient measurements were made at the large bore port on the bias unit with known reflection standards inserted into the small bore port of the jig. Three such measurements, using three different small bore standards, are sufficient to define T_1. The sign indeterminancy in s_{12} is resolved on the basis of consistency with the electrical length as estimated from the physical dimensions of the actual model.

An example of a small bore reflection standard used in these measurements is shown in Fig. 6. The standard consists of a Teflon filled 50-ohm

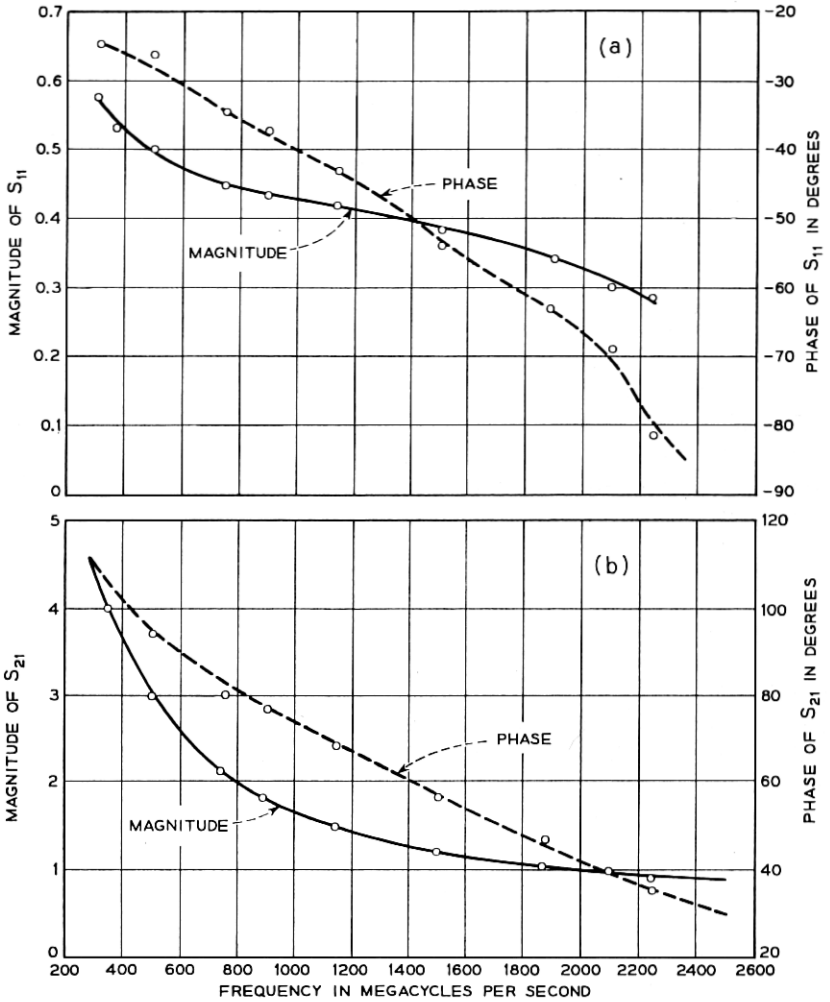


Fig. 5 — Scattering parameters for an L2254 transistor with respect to 50-ohm impedance; grounded emitter, $I_E = +5$ milliamperes, $V_{CE} = -5$ Volts; (a) magnitude and angle of S_{11}, (b) magnitude and angle of S_{21}.

coax line of very small, but also very carefully controlled interior dimensions, shorted at the far end.

The physical parameters were in sufficient control to define the angle of the reflection coefficient standards with an accuracy of about one degree up to 3000 mc. The round trip ohmic loss, and its variation with frequency, were included in the evaluation of the precise reflection magnitudes.

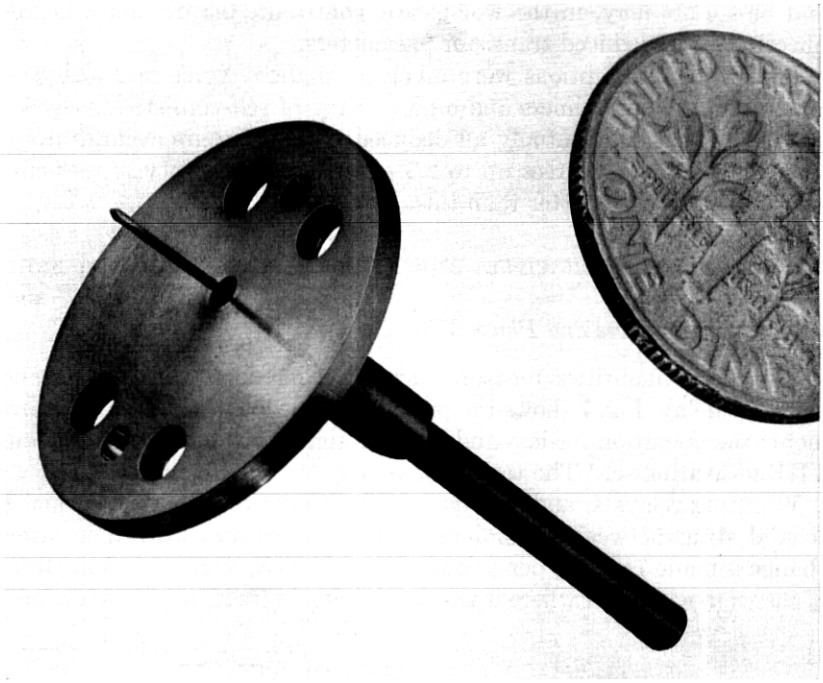


Fig. 6 — Example of one of the 0.054″ bore coaxial reflection standards used in characterization of transistor jig and bias fixture.

A very precise slotted line was used for measuring the values of ρ_{in} in (4). The line was initially checked for accuracy using the "sliding null" technique.[6]

2.5 *Accuracy of Transistor Characterization*

The two chief sources of transistor characterization error are the residual inaccuracies in the characterization of the jig and bias fixture paths and test set errors in measuring loss and phase. The error contributions from both of these sources depend heavily on the characteristics of the transistor, hence a categorical "error statement", in the usual sense, is not possible. Nonetheless, studies have been made which show that loss and phase measurement errors of 0.1 db and 0.6 degree (the maximum expected) may, in the worst conceivable case, produce errors of 0.8 db or 4 degrees in the determination of the s parameters of a transistor having the characteristics displayed in Fig. 5. The error from the estimated defect in the characterization of the jigs

and bias units may, in the worst case, contribute 0.5 db and 3 degree uncertainty in deduced transistor parameters.

Pessimistic assumptions were involved in these worst case analyses. Based on data smoothness and on a number of self-consistency checks, it appears that substantially all deduced parameters are accurate to at least 0.5 db and 3 degrees up to 2.5 gc, with the majority of measurements considerably better than this.

III. MEASUREMENT PRINCIPLES AND PERFORMANCE OF THE TEST SET

3.1 *Principle of Loss and Phase Measurement*

The basic quantities measured are insertion loss, phase shift, and envelope delay. Fig. 7 shows the principle of the loss and phase measurement; the operation for loss and phase is similar to that of the previous VHF measuring set.[1] The technique is that of "IF substitution".

Vibrating relays s_1 and s_2 sequentially interpose the unknown and a coaxial strap between a nominal 50-ohm source and load. The interchange is made $7\frac{1}{2}$ times per second. The signal (E_s or E_x) emerging from s_2 passes to a receiver where it is shifted down in frequency to a constant

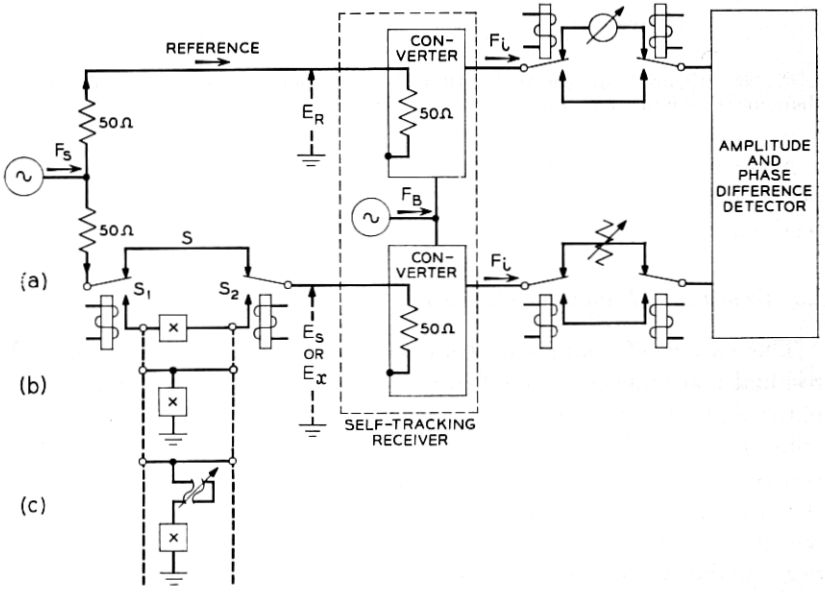


Fig. 7 — (a) Basic insertion loss and phase measuring arrangement embodying rapid comparison and frequency translation to fixed IF, (b) impedance measurement by bridging, (c) inversion of high impedances by adjustable transformer.

IF. A second pair of relays inserted in tandem with the output of the receiver switches an adjustable loss standard in synchronism with s_1 and s_2. The operator adjusts the loss standard so that the detector, which is capable of recognizing when the two sequentially applied inputs are of equal amplitude, delivers a null indication to a loss display meter. At the null point, the attenuator loss equals that of the unknown since the receiver is highly linear.

The difference of phase angle between E_s and E_x is the insertion phase of the unknown. This is measured in a manner exactly analogous to loss, using, this time, an adjustable phase shifter as the null-balanced standard.

3.2 *Principle of Delay Measurement*

Delay is measured by observing the phase shift experienced by a modulation envelope in its transit through the unknown.[7] The basic arrangement, which is illustrated in Fig. 8, employs a relatively simple AM modulator to generate the delay test signal. It is not necessary for the modulation envelope to be low in harmonic content. As in the previous case of loss and phase measurement, a pair of RF comparison switches sequentially completes measurement paths through the unknown and the standard at a $7\frac{1}{2}$-cps rate. The envelope delay data is contained in the phase difference between the fundamental components of the modulation envelopes borne by the signals E_s and E_x appearing sequentially at the input to the self-tracking receiver.

By conversion in the receiver, the modulation envelopes are super-

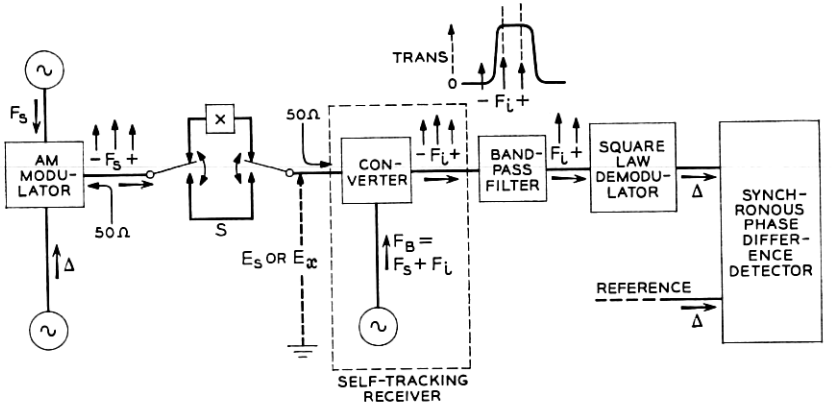


Fig. 8 — Principle of delay measurement showing reduction of three-tone envelope spectrum to twin-tone before demodulation.

imposed on the intermediate frequency, F_i, which is held rigidly constant by automatic frequency control of the beating oscillator. The tight control of the IF makes it possible to depart, at this point, from the usually employed arrangements which pass the IF output from the receiver directly to an envelope demodulator. Instead, advantage is taken of the constancy of the IF to eliminate all but two tones of the modulation spectrum, preliminary to detection. A steep-sided bandpass filter, interposed between the receiver and the demodulator, strips away all tones except the IF carrier and the upper modulation sideband. Since only two input tones are applied to the demodulator, the phase of the beat frequency product is totally independent of the amplitudes of the beating signals. In the conventional arrangement in which a stripping filter is absent, the phase of the baseband signal depends on the relative amplitudes and phases of all of the tones present in the RF spectrum. Hence, significant delay errors may result when the unknown exhibits loss and phase distortion across the frequency interval spanned by the array of side tones.

Of almost equal importance is the reduction in the size of delay measuring "aperture" accompanying the use of the stripping filter. Reducing the width of the modulation spectrum by a factor of two before demodulation serves to improve the ability to resolve finer-grained envelope delay detail by about the same factor.

The delay information is contained in the phase difference, $\theta_s - \theta_x$, between the sequentially appearing signals out of the demodulator. This phase difference is detected in the manner previously described in Section 3.1.

The unknown's envelope delay, τ, is closely given by

$$\tau = \frac{\theta_s - \theta_x}{\Delta} \text{ seconds,}$$

where the angle difference in the numerator and the modulation envelope rate in the denominator are both expressed in radians. By following through the frequency transpositions in Fig. 8, it is clear that the frequency at which τ applies may reasonably be taken to be the mean between the RF carrier and the adjacent lower side band. Δ is equal to (2π) $(5.55)10^6$ radians per second in the present set, hence, an increment of 0.5 nanosecond in the unknown's delay gives rise to one degree of envelope phase shift.

3.3 *Measurement Accuracy and Ranges*

Signal Source: 0.25 to 4.2 gc in four bands; ± 1 per cent scale calibration accuracy. The sources may be set to specific frequencies with a

tolerance of about 5 parts in 10^4 using high accuracy commercial counters for frequency measurement. Band changes are made automatically.

Insertion Loss Range: 50-db loss to 10-db gain. (Gains exceeding 10 db may be measured by preceding the unknown with a loss pad.) Accuracy: ±0.1 db from 10-db gain to 40-db loss; ±0.3 db from 40-db to 50-db loss. The accuracies just cited apply up to 2.0 gc. Above 2.0 gc the errors may increase by a factor of two.

Insertion Phase Range: 360 degrees. Accuracy: ±0.6 degree between 10-db gain and 40-db loss up to 2.0 gc; ±1.0 degree between 40-db and 50-db loss. Above 2.0 gc the errors may increase by a factor of two.

Delay Measurement (Limited to measurement on linear networks between 10-db gain and 20-db loss) Range: 180 nanoseconds. Accuracy: ±0.5 nanosecond up to 4 gc. Aperture width: 5.55 mc.

Source and Load Terminations for Coaxial Unknowns: Nominal 50 ohms; reflection coefficient magnitudes of source and load decay from 0.01 at 1.0 gc to 0.1 at 4.2 gc. Errors due to the residue of misermination have been treated in earlier work,[1,11] and are summarized in Section 6.1.

Source Power Applied to Unknown: Excitation level is automatically varied in accordance with unknown's loss so as to keep the input power at the lowest possible level consistent with satisfying signal-to-noise ratio requirements at the loss and phase detectors in the test set.

Down to losses of 19.9 db, the available source power is kept below −40 dbm. The power increases to −30 dbm for losses between 20 db and 29.9 db, to −20 dbm between 30 db and 39.9 db and to −10 dbm between 40 db and 50 db.

IV. OVER-ALL CIRCUIT DESIGN

4.1 *Objectives*

Experience has amply established that the development of components and devices for new communication systems entails a large volume of measurement. In view of this, it would be most unwise to achieve a high degree of measurement accuracy at the expense of awkward and laborious measurement procedures. Hence, in the present case, the aim has been to design for a facile interface between operator and machine without undue sacrifice of measurement accuracy.

A number of features were introduced to minimize the amount of operator labor required to make measurements. Automatic control circuitry has been liberally employed to tune oscillators, to set levels

and operating points of detectors, and to stabilize and render insensitive to test signal frequency the deflection sensitivity on the display meters. A considerable circuit complexity results from this high degree of automatic operation, but this is not obvious to the operator who benefits from the simplified measuring procedure. Where feasible, machine logic and mechanism have been substituted for operator decision and motor activity.

One of the most vital objectives was to provide a measuring facility with the capability to comprehensively characterize either passive or active linear two-ports. This was accomplished by the inclusion of bridging loss in addition to the insertion loss measurement features.

Transistors were to be characterized under light excitation conditions, in order to permit study of small signal parameter variation with shift of dc operating point. In the majority of measurements, less than 0.1 microwatt of power is absorbed by the transistor.

Measurement range, accuracy, and resolution were to be essentially independent of test signal frequency.

Solid-state design was to be used in all possible instances.

4.2 *Over-all Circuit Operation — Loss Measurement*

To achieve accuracy substantially independent of test signal frequency over the 4 octave range between 0.25 and 4.2 gc, it is necessary to heterodyne the measurement information to a fixed intermediate frequency where detection may be performed with the aid of precisely calibrated loss and phase shift standards. In addition, to minimize "instrument zero-line" and to eliminate error from drifts of phase shift and level within the set, it is desirable to sequentially compare the unknown with a high-frequency reference.[1] The rapid comparison and heterodyne design aspects of the test set were noted in the previous discussion of Figs. 7 and 8. A more complete development of these features is now presented in Fig. 9.

Referring to Fig. 9, loss may be measured with the instrument set up either in the basic phase or delay modes. Assuming selection of the phase mode, the AM modulator preceding the vibrating RF comparison switches is heavily dc biased for small transmission loss. Mode switches S_3, S_4, S_5, S_6, and S_7, program the instrument for phase or delay measurements. These switches are shown in the operating position for phase measurements.

A self-tracking double-conversion receiver translates the measurement information to a first IF of 60 mc, followed by a second conversion to 1.11 mc. Insertion loss is then detected with the aid of a differential

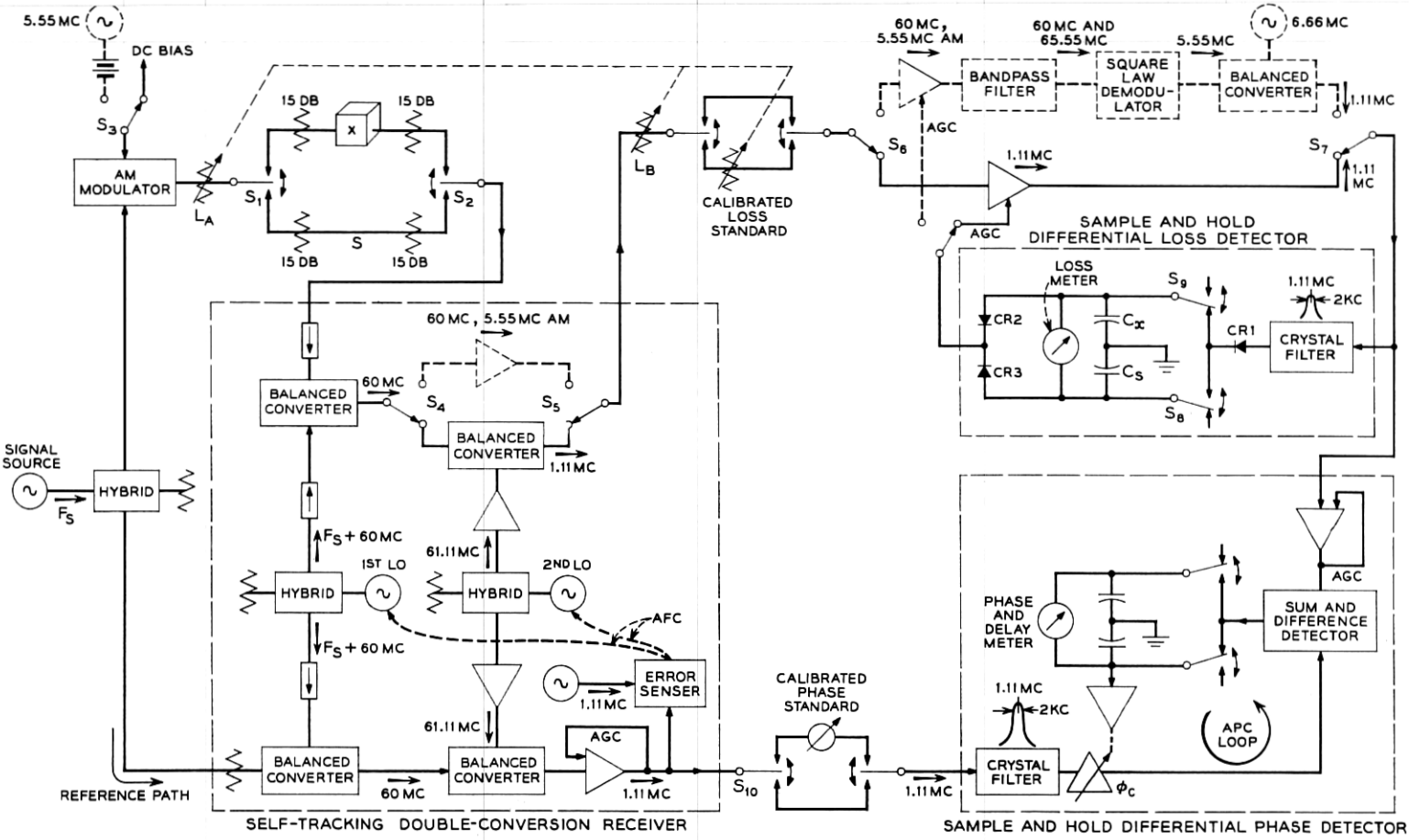


Fig. 9 — Block diagram of test set showing rapid comparison, IF substitution technique of measurement.

"sample and hold" detector involving the rectifier CR_1, the vibrating switches S_8 and S_9 and the storage capacitors C_x and C_s. The relays within the detector and those around the calibrated loss standard vibrate in phase synchronism with the $7\frac{1}{2}$-cycle rate of the RF comparison relays, S_1 and S_2. A null on the loss meter indicates when the attenuation standard, at 1.11 mc, has been adjusted for loss equality with the unknown. The measuring procedure is that of "IF substitution" and yields answers which are valid, for small losses, within the degree of linearity of the tracking receiver and for large losses, within limitations of noise performance.

Approximately equal detection sensitivity for various values of unknown loss is attained automatically by ganging common path attenuation, L_A and L_B, to the loss standard in such a way that the level of signals applied to the loss detector, at the null balance point, is maintained approximately constant.

In measuring at the higher losses, a greater portion of the common-path attenuation is assigned to the attenuator section located at intermediate frequency. Although this does have the somewhat undesirable effect of increasing the signal drive on transistors when measuring at high loss, it prevents the input level to the first converter from dropping dangerously close to noise. The way in which the pattern of attenuation is worked out assures sufficient signal for an S/N ratio of at least 25 db at the detection point during 50-db loss measurements. Error due to noise, under these conditions, is less than 0.05 db.[8]

The operation of the attenuators L_A and L_B does not completely insure constant level operation at the loss detector because of the residual frequency characteristic of the converters and the natural droop in loss of the test set cables with increasing frequency. These effects are prevented from altering the detection sensitivity by the presence of an over-all AGC circuit preceding the input to the loss detector.

A significant feature of this AGC circuit is the use of the steering diodes CR_2 and CR_3 across the storage capacitors for the purpose of rendering the AGC responsive only to the larger of the two stored signals. The resultant AGC action maintains the larger signal stiffly at some standardized level. This arrangement provides both for a constant deflection factor at the loss meter and a symmetrical calibration.

When making gain measurements, the loss standard is inserted in series with the unknown, by transposing it from the S to the X Channel. Necessary changes in common attenuation ganging are made at the same time.

4.3 *Over-all Circuit Operation — Phase Measurement*

Phase measurement, like the loss measurement, is performed by the technique of IF substitution. The essential IF measurement apparatus, as seen in Fig. 9, consists of the calibrated phase standard, the switches to introduce it sequentially in synchronism with the other comparison relays of the test set, and a "sum and difference" phase discriminator feeding the sample and hold circuitry. The capacitors in the sample and hold circuit store the output voltages obtained from the discriminator during the successive dwell periods of the comparison relays. When the two stored voltages are equal, as indicated by a null on the phase meter, the phase shift through the calibrated standard equals the insertion phase of the device under test, since the phase of the common path circuitry makes no contribution whatsoever to the phase meter indication.

The null balancing procedure using the phase standard assures only that the phase difference between the two inputs to the phase detector is the same for both dwell states of the comparison relays. Unless some special circuit provision is made, the absolute phase difference between the detector inputs could, at the null point, range over wide limits because of frequency sensitive asymmetry between the two transmission paths energized from the test signal source. Moreover, the two halves of the receiver, though nominally similar, fail to track perfectly with respect to conversion phase. Hence, in order to fix the operating point and make the provision of a calibrated meter possible, an APC loop was necessary to regulate the value of the common path phase shifter, φ_c, (see Fig. 9) so as to maintain the inputs to the detector in a state of phase quadrature during the period of S path closure. The ninety degree phase difference represents center of range on the transducer characteristic of a sum and difference type of detector.

In addition to operating point control, which is an absolute necessity for the viability of the scale calibration, it is most desirable to maintain constant scale factor. To achieve this, the signal amplitudes applied to the phase detector must be held at fixed values, independent of either the test signal frequency or the dwell state of the comparison relays. This poses no particular problem in the reference path since the operation of the comparison relays around the phase standard does not result in level shifts. An elementary AGC in the receiver is sufficient to remove any reference level variation traceable to frequency characteristic of converters or frequency dependence of signal source amplitudes.

On the other hand, the other input to the phase detector may fluctuate in amplitude at the 7½-cycle comparison rate, depending upon the loss standard setting. It is clear that the AGC circuit introduced in the phase detector to wipe out this cyclic level difference must not introduce spurious phase changes in the course of leveling. By the use of a system of gain control, which is relatively free of reactance shifts with control voltage, the level to phase conversion has been held to 0.1 degree for 10-db input level changes.

4.4 *Over-all Circuit Operation — Delay Measurement*

The elements in dashed outline in Fig. 9 are automatically switched in when the operator selects the delay mode of measurement. The operation closely follows the simplified description given previously in Section 3.2.

A balanced converter, excited from a 6.66-mc local oscillator source, is introduced beyond the square-law demodulator to translate the 5.55-mc envelope signal to the 1.11-mc IF. There is no question of frequency incoherence between the IF signal emanating from this converter and the signal of the same *nominal* frequency emitted at the reference path output of the receiver (Fig. 9), since the 6.66-mc local oscillator tone is formed by modulating the 1.11-mc reference in the receiver with the 5.55 mc producing the AM modulation envelope.

Delay detection is performed with the same measurement apparatus used for phase.

During delay measurement the loss standard is shifted to the 60-mc IF. This prevents any delay error from residual level-to-phase conversion in the square-law detector, since the initial operation of loss balancing equalizes the levels at the input to the detector during the two dwell states of the comparison relays. This would, of course, be only an illusory advantage if the delay through the loss standard varied with the loss setting.

In the course of delay measurements, the over-all AGC for control of loss meter scale factor is transferred to a 60-mc amplifier preceding the square-law demodulator.

4.5 *Principal Features of the Measurement System*

The measurement circuit combines features of rapid comparison and null balancing of standards with heterodyne detection. The advantages inherent in such measurement arrangements have been noted previously.[1]

Briefly, the comparison of s with x is so rapid that the measurement results are unaffected by slow wanders of source level, drifts of conversion gain or phase in the receiver, or by drifts of operating point and sensitivity in the loss and phase detector. This arrangement also obviates error from residual dependence of source level or receiver characteristics on frequency, since the source, receiver, and detector are common to the channels being compared. To prevent errors in the comparison of the unknown with the standard, the transmission paths through the comparison switches must be well matched to the nominal termination level, and the crosstalk from the open to the transmitting path must be small.

It is most desirable that the two paths through the switches transmit equally. This is not mandatory from an accuracy viewpoint, since, by paying the penalty of added labor and inconvenience, an initial "zero run" may be taken to acquire the asymmetry data on the comparison switches. Small "zero-line" residues prove to be inescapable.

The heterodyne technique has several conspicuous advantages. First of all, locating the loss and phase standards at the intermediate frequency avoids the problem of developing broadband standards.

Thermal noise power is reduced before detection by 2-kc wide crystal filters, thereby reducing measurement error due to system noise.

Loss of the device under test may be made up by single frequency gain at the IF.

And finally, the heterodyne system introduces the advantages of selective detection. It provides immunity from errors due to harmonics and stray signals in the output of the unknown.

While the attributes just listed are basic, certain other design features are quite important from the standpoint of conserving operator effort and expediting measurement. In particular, the self-tracking property of the receiver not only relieves the operator of the burden of adjusting local oscillators, but also permits the use of a narrow (2-kc wide) final IF by virtue of the tuning precision inherent in the automatic control.

The provision of calibrated loss, phase and delay scales in combination with slow scan of the signal frequency is useful in network adjustments, e.g., tuning for maximum or minimum responses or estimating limits of response variation over given frequency bands.

V. SUBSYSTEMS OF THE MEASUREMENT SET

The "front end" apparatus in Fig. 9 must span the 0.25- to 4.2-gc range of measurement frequency. This includes the signal and first local oscillator sources and such transmission components as the microwave

converters, hybrids, isolators, and AM modulators. None of this apparatus can be designed to cover the full frequency range without considerable sacrifice in important performance attributes. Hence, the test signal range has been subdivided into 4 bands of octave width, with separate front end apparatus provided for by each band. This represents no complication from the standpoint of the operator, since a system of remotely operated coaxial relays automatically switches the front end apparatus when passing from one band to another.

The test set circuits beyond the output of the first converters (Fig. 9) are common to all four bands.

Four signal sources cover the 0.25- to 4.2-gc range. Butterfly-type oscillators are used below 1.0 gc; klystron sources are used between 1.0 and 4.2 gc. Source oscillators with sliding contact mechanisms for changing frequency were avoided in order to guard against the occurrence of transient level or frequency "hits" on the AFC circuitry in the receiver.

The RF and IF comparison switching, sampling, and storage in this set, while unusually extensive in terms of numbers of relays required, is quite conventional and follows the design principles elucidated in previous work.[1] With the exception of the two comparison relays operating at the test signal frequency, all of the $7\frac{1}{2}$-cycle relays use mercury wetted contacts in order to realize the advantages of low contact resistance, transmission symmetry in the two dwell states and long life. Many of the relays are compound, i.e., complexes of several relays are formed for the purpose of achieving low crosstalk by shorting the nominally open transmission path. Both coaxial and noncoaxial contact designs are employed according to need.

The RF comparison at the $7\frac{1}{2}$-cycle rate is performed with a pair of solenoid-operated coaxial relays. These relays have dry contacts, but the contact pressure is very great and a wiping action occurs during the "make" phase. Leakage through the nominally "open" path is 44 db down on transmission through the closed path at 4.2 gc. Since switching is done at both input and output, error from this cause is less than 0.1 db at 40-db loss level.

With the exception of the signal and first local oscillators, all of the circuitry is solid state.

5.1 *Remote Tuning of Signal Sources*

Good practice in high-loss measurements calls for tight shielding of the signal sources in order to prevent any leakage of source power to susceptible low-level points in the test circuit. Hence, in the present

instance, all four test signal sources are housed in an RF tight cabinet together with associated leveling, control, and coaxial relay band-change circuitry.

The sources are remotely tuned by the use of the tachometer stabilized 60-cycle servo loop shown in Fig. 10. The tach feedback is adjusted to dynamically damp the loop rather heavily in order to limit the maximum rate of test signal frequency change to 100 mc per second. This represents the maximum rate of change of source frequency which the AFC circuitry in the receiver was designed to follow. The dead zone

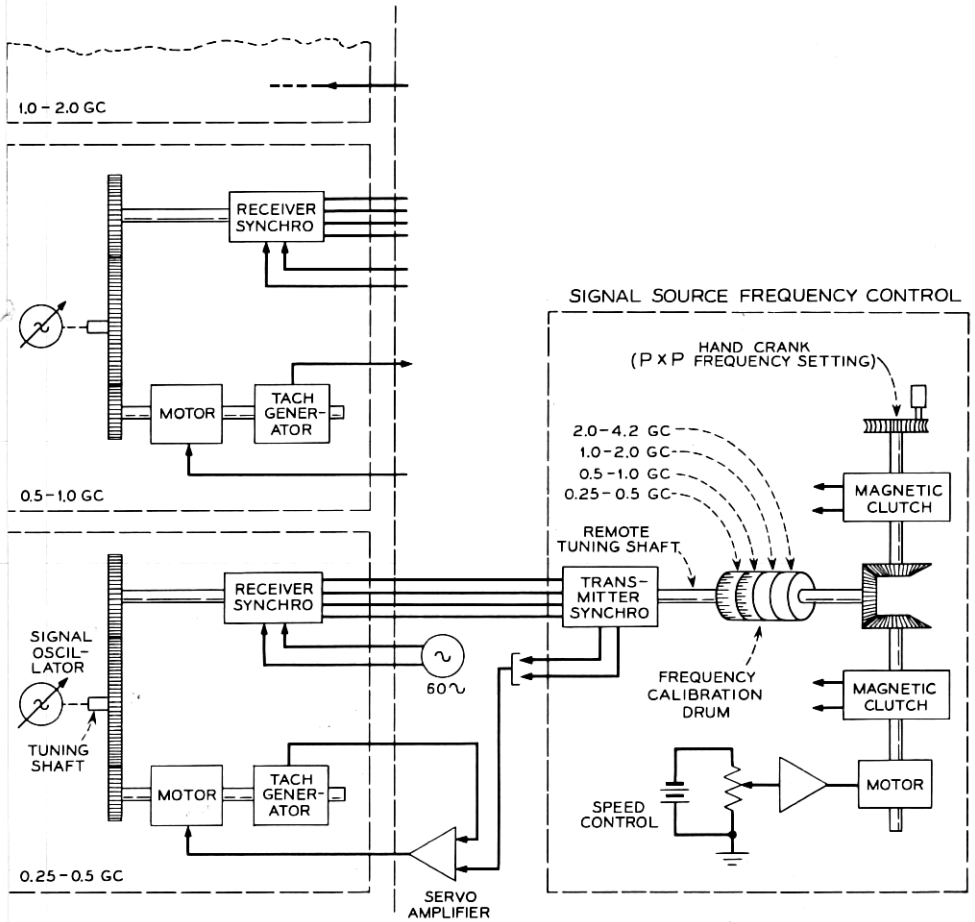


Fig. 10 — Remote tuning of test signal sources.

around the servo null is sufficiently narrow to permit remote frequency settability to about 5 parts in 10^4.

The transmit synchro is automatically switched to the appropriate receiver synchro when changing between bands. The servo amplifier is also shared among all four bands.

Either motor scan or point-by-point tuning is possible. As seen from Fig. 10, the mechanism for accomplishing this consists of an arrangement of electric clutches and differential to permit the operator to turn the frequency calibration drum dial either by hand or by an adjustable speed motor.

5.2 *Self-Tracking Receiver*

The receiver must faithfully transpose measurement data to 1.11 mc in the case of phase measurement and to 60 mc in the case of delay measurement. In Fig. 11, showing a block diagram of the receiver, the following aspects of design must be considered.

(*i*) The linear dynamic range, i.e., the range for applied signals bounded by receiver compression at one end and receiver noise at the other.

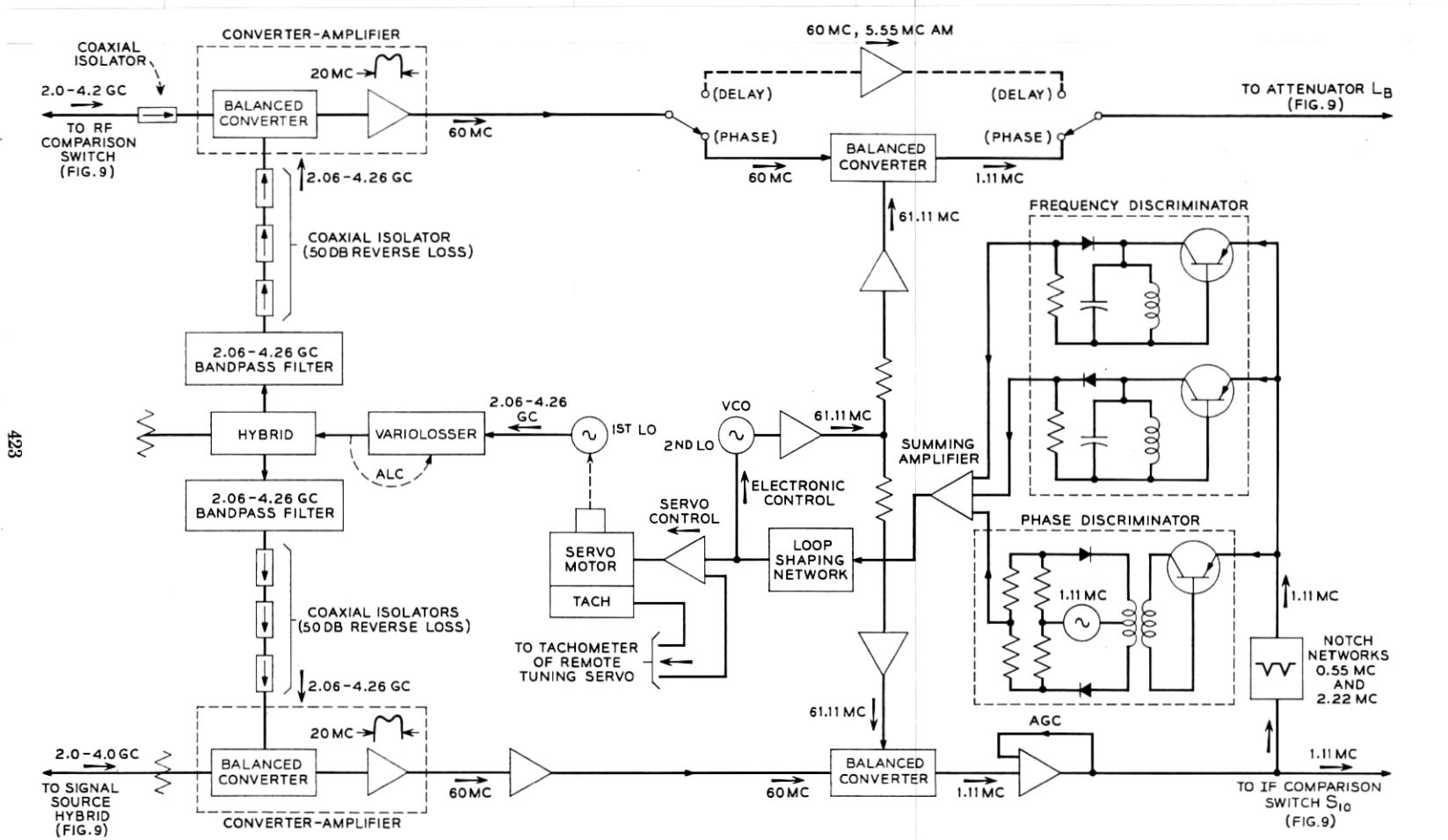
(*ii*) Suppression of crosstalk and pick up between the two similar halves of the receiver.

(*iii*) Execution of an AFC circuit capable of holding the second IF centered within the nominal 2-kc receiver bandwidth in the presence of signal frequency scan up to rates of 100 mc/second.

5.21 *Conversion to First IF*

To be compatible with accuracy objectives, the first converter must have a linear dynamic range of at least 40 db over which errors due either to compression or to noise must be smaller than 0.03 db. It was possible to meet this requirement using coaxial, balanced mixers covering octave bandwidths. The particular mixers employed have about 8-db conversion loss and 10-db noise figure. An integrally mounted 60-mc preamplifier of 20-mc bandwidth provides 25 db of gain.

Referring now to Fig. 11, potentially harmful leakage paths may be identified starting from the test signal frequency input to the first converter in one path and terminating in the local oscillator port of the converter in the other path. Test signal which is transmitted over these leakage paths beats with the local oscillator tones to produce traces of spurious 60 mc. In order to avoid the generation of such signals, which may produce errors when measuring at the highest loss levels, the


CONVERTER-AMPLIFIER
COAXIAL ISOLATOR
2.0-4.2 GC
TO RF COMPARISON SWITCH (FIG. 9)
20 MC
BALANCED CONVERTER
60 MC
2.06-4.26 GC
COAXIAL ISOLATOR (50 DB REVERSE LOSS)
2.06-4.26 GC BANDPASS FILTER
HYBRID
VARIOLOSSER
ALC
2.06-4.26 GC
IST LO
2.06-4.26 GC BANDPASS FILTER
COAXIAL ISOLATORS (50 DB REVERSE LOSS)
2.06-4.26 GC
20 MC
BALANCED CONVERTER
60 MC
2.0-4.0 GC
TO SIGNAL SOURCE HYBRID (FIG. 9)
CONVERTER-AMPLIFIER
60 MC, 5.55 MC AM
(DELAY)
(DELAY)
(PHASE)
(PHASE)
BALANCED CONVERTER
60 MC
1.11 MC
TO ATTENUATOR L_B (FIG. 9)
61.11 MC
FREQUENCY DISCRIMINATOR
VCO
2ND LO
61.11 MC
SUMMING AMPLIFIER
ELECTRONIC CONTROL
SERVO CONTROL
SERVO MOTOR
TACH
LOOP SHAPING NETWORK
TO TACHOMETER OF REMOTE TUNING SERVO
PHASE DISCRIMINATOR
1.11 MC
1.11 MC
NOTCH NETWORKS 0.55 MC AND 2.22 MC
61.11 MC
AGC
BALANCED CONVERTER
60 MC
1.11 MC
1.11 MC
TO IF COMPARISON SWITCH S_{10} (FIG. 9)

coupling between signal frequency and local oscillator terminals of the converters should be small, the transmission paths from the LO source to the converters must exhibit a high ratio of forward to reverse transmission and the conversion efficiency for local and signal oscillator tone applied to a common input of either converter must be low.

All of these factors have been controlled such that errors from signal frequency crosstalk between the two halves of the receiver are held to less than 0.2 db even when measuring at 50-db loss levels.

The isolators in Fig. 11 present high reverse loss over only the octave for which they are optimized. Consequently, in the case of the two bands above 1.0 gc, it is necessary to introduce bandpass filters in the local oscillator paths for the purpose of suppressing interpath transmission of higher order modulation products emitted at the local oscillator ports of the converters.

The unilateralization of the LO paths for the two bands below 1.0 gc is provided by transistorized buffer amplifiers having a 40-db ratio of reverse loss to forward gain. Each amplifier design covers an octave. The high reverse loss is obtained by cascading two grounded-emitter stages. Measurements show that this is the preferred connection to obtain maximum reverse loss in the 0.25- to 1.0-gc region.

5.22 *Conversion To Second IF*

Since the second converter is fed directly from the output of the first, it must meet similar requirements on dynamic range. These requirements, which are noted in Section 5.21, are met without difficulty by the use of ring modulators. Unwanted transmission of 60-mc power between the two converters is prevented by transistor buffer amplifiers inserted in the second local oscillator transmission paths. Direct path loss between the LO ports of the second converters is greater than 100 db for 60-mc signals and sufficient at other frequencies to block the transmission of any disturbing tones created by higher-order modulation.

5.23 *Automatic Frequency Control of Local Oscillators*

The heterodyne technique of phase and delay measurement calls for a first IF to serve as a subcarrier for the AM modulation envelope and a second IF of considerably lower frequency for operation of the null balance standards. In view of the decision to narrow the receiver bandwidth to 2 kc, it would be quite impractical to consider manual tuning of the local oscillators. Moreover, such a course would have been in conflict with the objective of simplifying measurement procedure.

Tight control of the IF is advantageous for several reasons. It permits narrow IF bandwidths, thereby enhancing S/N before detection. The absence of IF flutter permits a great reduction in the tolerance imposed on phase tracking between opposing tuned amplifiers in the 60-mc and 1-mc channels of the set. And lastly, it eliminates any measurement errors from the residual frequency sensitivity of the phase standard calibration.

To achieve the desired precision in control of the intermediate frequencies, the system of frequency and phase discriminators shown in Fig. 11 senses the error of the second IF and delivers a corrective voltage that actuates two modes of control. The first of these is an electromechanical servo which achieves a coarse correction by motor-tuning the frequency of the first LO for minimum IF error. This is supplemented by an all electronic frequency control acting around the second local oscillator. With a hold in range of ± 10 mc and a very crisp response rate, the electronic loop eliminates the residue of static and dynamic errors left by the operation of the mechanical loop.

Butterfly oscillators serve as first LO sources up to 1.0 gc. Klystron oscillators are used between 1.0 and 4.2 gc. The second LO is a voltage-controlled oscillator (VCO) of special design.

The combined use of frequency and phase sensitive transducers endows the control circuit with certain useful attributes which are not present when one or the other of the transducers is used alone.[10] Frequency discriminator control, for example, tolerates static frequency error but polarizes the LO's with respect to sideband of operation. Control by sum and difference phase detector eliminates static error but permits stable, closed loop operation with the LO's in either an upper or lower sidetone relation to the signal frequencies. The combination of the two retains the zero-error property of the phase control and the polarizing property of the frequency control. It is extremely important to establish particular LO sideband sense, since the sign of the measured insertion phase shift depends on the sideband polarity.

It has also been demonstrated that the introduction of frequency discriminator control extends the pull-in range of the loop.

Another feature of interest is the use of rate feedback from the remote tuning servos around the RF test signal sources shown in Fig. 10. This is instrumented by inserting the output of the tachometer generator from the remote tuning loop in series with the tachometer attached to the first LO servo motor. Since the tachometer polarities are connected in series opposition, the control effect is to induce the first LO motor to maintain a rate correspondence with the speed of the motor which tunes

the signal oscillator. This is beneficial in reducing the dynamic stress on the AFC circuit during periods of signal frequency scan.

The dynamical attributes of the servo are essentially those of a conventional, second-order regulator circuit employing tachometer stabilization.[9]

The design of the electronic control loop may be investigated in some greater detail with the aid of Fig. 12, which presents a simplified analytic picture of the operation. For purpose of first-order analysis, a simple time delay factor, T, accounts for the loop phase contributed by the "Q" of resonant circuits in the discriminator. In the actual circuit, this approximation is valid for loop frequencies up to about 50 kc. The collapse of the approximation above this frequency is not really significant, since gain crossover occurs at approximately 40 kc.

The asymptote structures in Fig. 12 show the dominant elements of the design. The essential idea, of course, is that the loop gain must be brought to zero before the parasitic corners in the transducer characteristics cause oscillation. At the lower loop frequencies, the magnitude

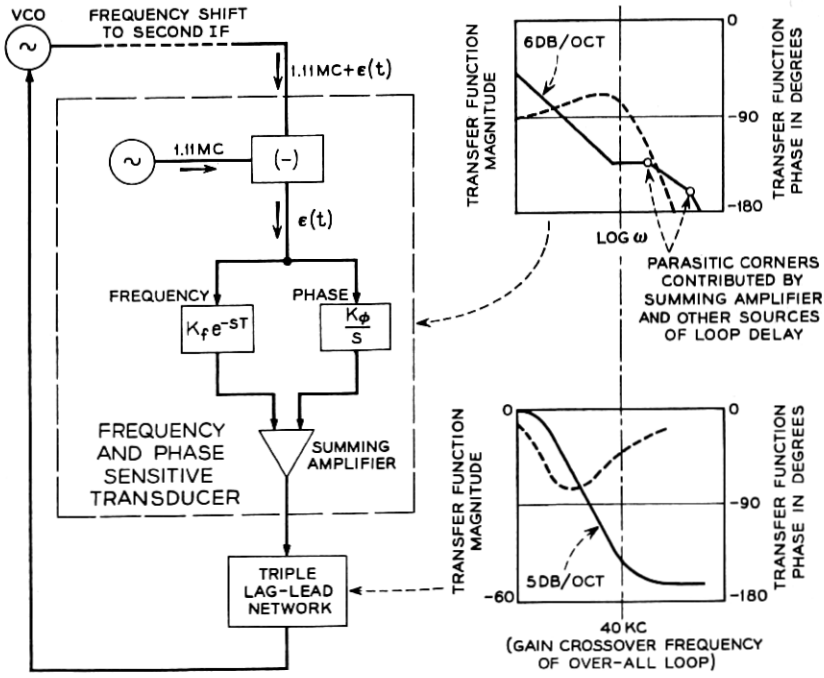


Fig. 12 — Simplified analytic model of AFC circuit.

asymptote of the aggregate frequency and phase sensitive transducer crudely approximates that of a "leading" corner. An upturn of the phase curve in the vicinity of the break may be advantageously used to obtain help on phase margin at gain cross-over. Parasitic corners above the low-frequency break, combined with the assumption of constant time delay in the frequency discriminator response, cause a fairly rapid crossover of the phase.

The loop shaping is done with a cascade of three lag-lead networks whose characteristic combines with that of the error transducer to produce an 11 db per octave over-all gain slope at crossover.

The realized loop gain and phase were measured by the procedure of applying a sinusoidal stress and observing the error residue. A procedure of this sort is necessary since a phase sensitive loop may not be opened without destroying its operation. The results, which are plotted in Fig. 13, show satisfactory agreement with the computed characteristics.

It is of interest to observe that for a given value of the discriminator

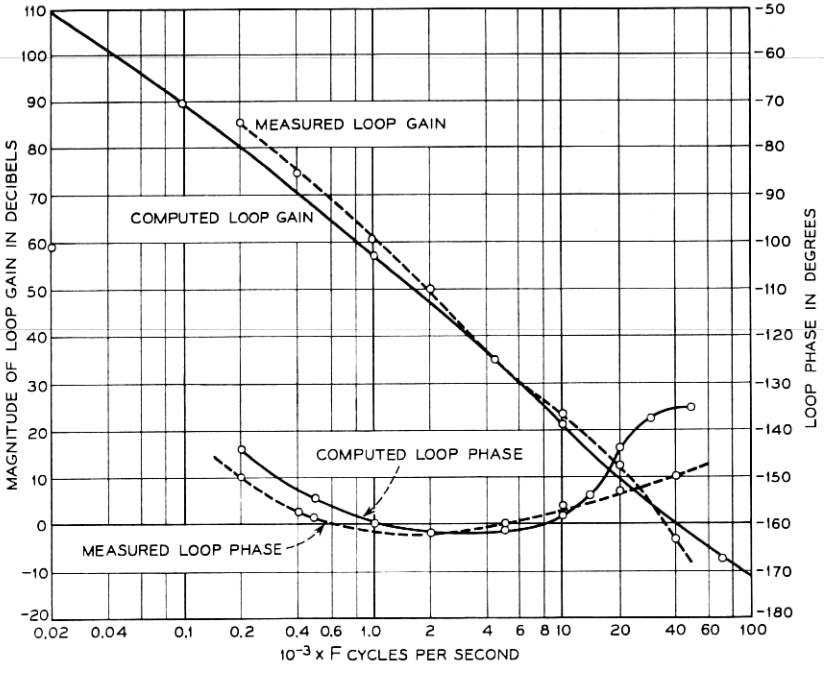


Fig. 13 — Gain and phase characteristic of AFC loop; measured and computed.

delay time, T, increasing the magnitude of the transducer gain, K_f, increases the phase up-lift in the vicinity of the low-frequency corner in the over-all characteristic of the two discriminators. Also, small values of T permit the design of wider band loops. T and K_f are not independently disposable in the actual circuit, since both are related to the network Q's.

The actual transducer parameters used in the loop are:

$$K_f = 0.35\ (10)^{-5} \text{ volt sec/radian}$$
$$T = 2.9\ (10)^{-6} \text{ sec}$$
$$K_\varphi = 4/\pi \text{ volts/radian}$$
$$K_0 = 10^7\pi \text{ rad/volt sec} \quad \text{(VCO sensitivity)}.$$

The VCO is a varactor-tuned oscillator, shown schematically in Fig. 14. The operation is based on negative resistance at the base of the oscillating transistor, Q_1. The impedance presented at the base, which is approximately the product of h_{fe} and the emitter circuit impedance, contains a negative resistance term due to the capacitative emitter load and the phase angle of h_{fe} in the vicinity of 60 mc. Oscillation is supported at a frequency determined partly by the capacitance in the emitter circuit but principally by L_1 in shunt with the capacitance provided by the back-biased varactors. The combination $R_1 - C_3$ limits the oscillation amplitude through self-bias. A predistortion network linearizes the frequency deviation characteristic. This is desirable from the standpoint of maintaining the incremental loop gain of the AFC circuit independent of operating point. Q_2 provides amplification and load buffering for the oscillator.

An automatically executed program for resynching the AFC loop is initiated on test set turn-on or when passing from one test signal band to another.

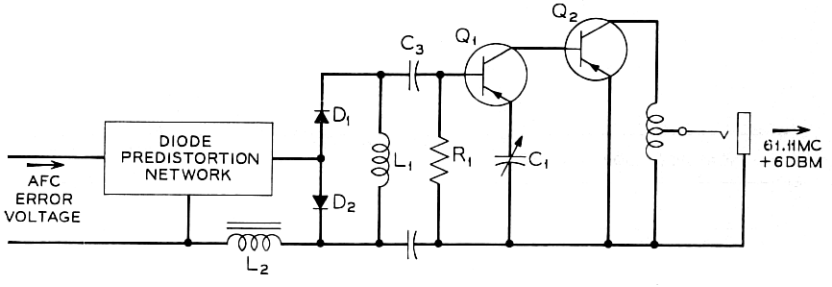


Fig. 14 — 5 mc/volt VCO with 61.11-mc center frequency. Predistortion network linearizes VCO control characteristic.

5.3 *Phase Standard*

The design targets for the phase standard call for a range of 360 degrees, a calibration accuracy of 0.1 degree maintained for long periods, freedom from warmup drift or calibration shift with ambient temperature and an output level independent of the phase shifter setting.

In view of the temperature dependence of critical transistor parameters, it was found desirable to make use of the rapid switching technique shown in Fig. 15. Transmission is alternated between a fixed phase path and the variable phase path at the $7\frac{1}{2}$-cycle repetition rate used universally in the test set. Since the switching rate is sufficiently rapid, drift of the common path amplifier characteristics is eliminated as a source of calibration error. In order to realize the maximum cancellation of drift, the input and output impedances of the fixed phase networks have been designed to approximate those of the opposing variable phase networks. This makes for symmetry of interaction between the amplifiers and the networks. Measurement of the advantage gained from the use of the switching technique shows that potential error due to amplifier drift has been reduced from approximately 0.4° per degree change of ambient to 0.05°.

The prime element of the phase standard is a continuously variable

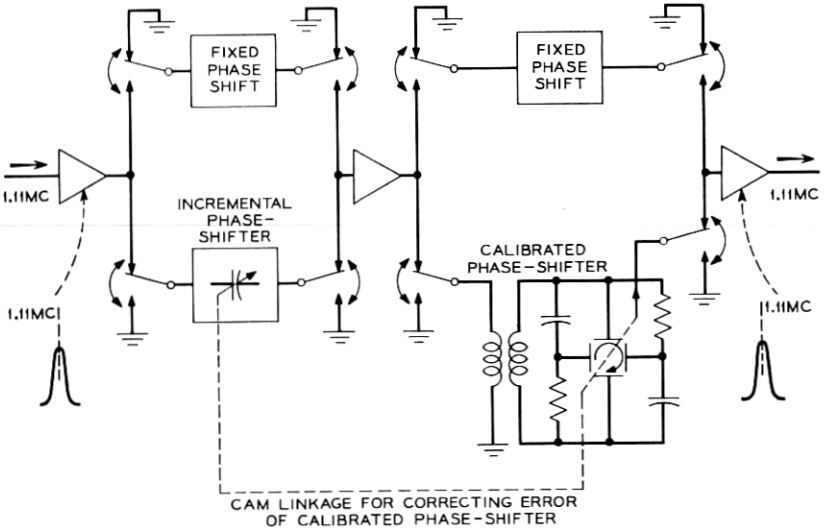


Fig. 15 — Block diagram of phase standard showing use of rapid switching to prevent calibration drift due to shift of amplifier parameters with temperature or age.

four-quadrant sine condenser of high quality and permanence. The linearity error is removed by use of an earlier noted technique.[1] A cam, whose profile is shaped to match the error curve, rotates with the condenser shaft. A follower arm resting on the cam periphery then adjusts an incremental phase shifter to compensate for the non-linearity error.

In addition to phase, the calibrated dials also bear delay scales (in different color than that used for phase); the conversion between delay and phase is on the basis of the equivalence between 0.5 nanosecond of delay and one degree of phase at the 1.11-mc IF. The dials may be slipped for setting up dummy "zeros".

The active circuitry in the common path follows standard design.

5.4 *Loss Standard*

The loss standard operates at 1.11 mc in the phase mode of measurement and at 60 mc in the delay mode. A calibration accuracy of 0.03 db is sought for loss differences up to 30 db. In addition, change of loss setting should not alter the insertion phase of the standard when measuring loss, or the insertion delay when delay is being measured, since phase and delay changes of the standards are indistinguishable from changes of the parameters of the device under test.

A decade attenuator of the dissipative type employing metal-film resistors performs satisfactorily in all respects. The loss standard consists of four such attenuators connected in tandem, spanning a total range of 49.99 db in 0.01-db steps.

Each of the decades is made up of a sequence of π pads mounted around a turret switch. The individual pads are semi-coaxial in design and this endows the loss standard with the bandwidth required for the dual operation at 1.11 mc and 60 mc. At the 1.11-mc level, phase shift is constant to 0.1 degree for any setting of the standard. The envelope delay at 60 mc changes less than 0.2 nanoseconds up to changes of 20 db in loss setting.

5.5 *Loss and Phase Detection*

The essentials of the loss detector operation, as illustrated in Fig. 9, have been discussed previously.

A crucial aspect of the operation of the loss detector relates to the timing of sampling relays, S_8 and S_9, which establish the charging paths to the storage capacitors, C_x and C_s. In connecting C_x and C_s during the sample periods, it is necessary to allow for the physical impossibility of perfectly synchronizing all the relays in the measuring

set with respect to instant of contact transfer and uniformity of dwell time. Moreover, short time transients are initiated at the change of state from x to s and vice versa. For these reasons, S_8 and S_9 are timed so as to delay the start of the sampling intervals until transients set up by the operation of preceding relays have decayed.

The component circuitry involved in the phase detection process, as illustrated in Fig. 16, consists of an AGC circuit to smooth level without accompanying phase change, a sum and difference discriminator with associated sample and hold circuitry at the output, and an APC loop preceding the reference input to the discriminator.

The AGC circuit in Fig. 16 introduces less than 0.1-degree change of phase in 1.11-mc transmission for a 10-db change of input level. Its operation is based on the use of an emitter-coupled transistor pair, Q_1 and Q_2, for gain control. The signal input current, which is applied to the common connection between the emitters, divides between Q_1 and Q_2 in accordance with the AGC error current feeding into the base of Q_2. Since the external emitter circuits of Q_1 and Q_2 share a large dc impedance, changes of dc operating point in Q_2 induce exactly opposite shifts of operating point in Q_1. Hence, the ac impedance (for small signals), seen looking into each of the emitters, shift in opposite directions with the result that the impedance presented to the signal input remains essentially constant over a wide range of gain control. The constancy of the load on the driving source is a prime factor in minimizing the level-to-phase conversion.

The grounded-base operation of Q_1 and Q_2, in so far as ac signal effects are concerned, is an additional aid in suppressing level-to-phase conversion. In this configuration, the parasitic parameters of the transistor shift least with operating point. Thus, by choosing a transistor of high f_α in relation to the operating frequency (1.11 mc), virtually all anomalous effects, including those ascribable to the phase angle of α, are eliminated.

Another aspect of interest arising in the process of phase detection concerns the operation of the APC loop. This loop is unusual with respect to its ability to absorb indefinitely large amounts of stress, without saturating. The operation is as follows: During the period when the S path is closed throughout the test set, signals e_s and e_r appear at the inputs to the phase discriminator in Fig. 16. For an extended interval during this period, the discriminator delivers charging current to capacitor C_2 through sampling relay S_2. Capacitor C_2 charges up to a dc voltage proportional to the deviation of the phase difference between e_s and e_r from ninety degrees. As external conditions change in a way

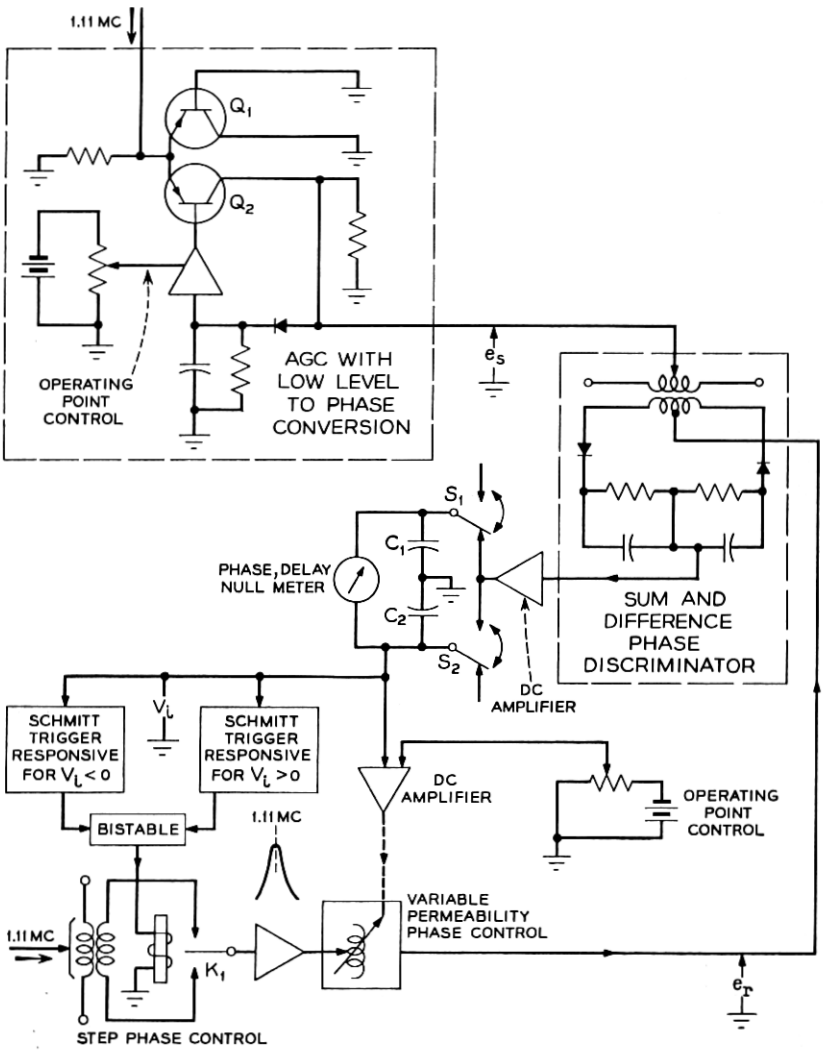


Fig. 16 — Phase detection including AGC circuit with insignificant level-to-phase conversion coefficient and APC circuit to fix operating point at phase discriminator.

which tends to increase the magnitude of this deviation, the APC connection through the voltage-sensitive phase shifters alters the phase of e_r to sustain near-quadrature between the discriminator inputs.

Two kinds of controllable phase networks are present. A continuous control, which makes use of permeability—current sensitivity to alter

inductance values in a cascade of "bridge" type phase shifters can introduce phase changes of up to 200 degrees of either sign. As these limits are approached in the course of introducing corrections, the voltage magnitude across capacitor C_2 increases sufficiently to trip one of the two Schmitt triggers. This occurs when the deviation from quadrature rises to 3 degrees. The particular trigger actuated depends directly on the sense of the loop stress, since this determines whether the departure of the C_2 voltage from null is positive or negative.

The firing of the Schmitt trigger precipitates the operation of relay K_1, which serves to alter the phase of e_r by 180 degrees. This has the effect of subtracting 180 degrees from the initially present stress, thereby removing the cause of loop strain and permitting the voltage across capacitor C_2 to return nearly to zero. This operation can be accomplished repeatedly so that effectively the loop can absorb indefinitely large amounts of stress. It is of interest that the operation of relay K_1 produces the stable effect just described only if another relay is employed to momentarily short the voltage across capacitor C_2 at the instant that relay K_1 changes dwell state. The erasure of "past history" establishes propitious boundary conditions from which the loop executes a stable operating point trajectory to the new state.

Both the step and continuous phase shifters are designed to alter phase, but not level; hence, the operation of the APC loop does not in any way alter the deflection sensitivity on the null meter.

VI. MEASUREMENT ACCURACY

Errors tend to be of two types. The first category includes errors attributable to residual imperfections of the test set. These result from such factors as calibration uncertainty of standards, the presence of low residual crosstalks and pickups, the minor influence of harmonic residues in various parts of the test set and small effects of noise. The error estimates, previously cited in Section 3.3, cover the sources just enumerated and apply equally to the measurement of transistors and coaxial unknowns.

Further errors, however, arise in the measurement of coaxial unknowns which depend upon interaction between the frequency characteristics of the unknown and certain of the attributes of the test set. Included here are errors due to the residual impedance misterminations around the unknown and "aperture" error in delay measurement.

6.1 *Mistermination Errors in Loss, Delay and Phase Measurement*[1,11]

The source and load impedances facing the unknown in this test set have finite return losses which drop to a minimum of 20 db at 4 gc.

When the transmission characteristics of the unknown are measured between these slightly imperfect impedances, the measured data is somewhat different than one would obtain if measurements were made between terminations of infinite return loss. The difference between the actual measurement and those which would be obtained between perfect impedances is the mistermination error.

An estimate has been made for the insertion loss, phase, and delay error due to mistermination. The starting point for such an estimate is the error, ε_f, in measurement of insertion ratio.[1] The magnitude of insertion ratio is the insertion loss expressed as the corresponding numerical ratio, and the angle of insertion ratio is insertion phase. The value of ε_f is given by

$$\varepsilon_f = \frac{\text{measured insertion ratio}}{\text{insertion ratio between 50 } \Omega \text{ impedances}} = \frac{1 - s_{22}\rho_L - s_{11}\rho_G - \rho_G\rho_L(s_{12}s_{21} - s_{11}s_{22})}{1 - \rho_G\rho_L}. \tag{5}$$

The s coefficients are the scattering parameters of the unknown, and ρ_L and ρ_G are the reflection coefficients of source and load in the test set. The impedance reference here is 50 ohms. If the reasonable assumption is made that all of the reflection coefficients are small, i.e., $|s_{11}|, |s_{22}|, |\rho_G|$ and $|\rho_L| < 0.1$, then ε_f may be approximated by

$$\varepsilon_f = 1 - s_{11}\rho_G - s_{22}\rho_L - \rho_G\rho_L(s_{12}s_{21} - s_{11}s_{22} - 1). \tag{6}$$

If further, one deals with the worst case in which the round trip loss through the unknown is 0 db, i.e., $|s_{12}s_{21}| = 1$, then the largest possible error in loss or phase measurement would be closely equal to

$$|s_{11}\rho_G| + |s_{22}\rho_L| + 2|\rho_G\rho_L| \tag{7}$$

in nepers or radians.

Equation (6) is also useful in estimating upper bounds on delay measurement error due to mistermination. When one recalls that the measured envelope delay is equal to the increment of insertion phase shift across the 5.55-mc separation between RF carrier and adjacent sidetone divided by the radian interval between these frequencies, it is then apparent that the error in measuring insertion delay equals the difference of the errors in insertion phase at the two frequencies divided by the radian interval.

If the same assumptions with respect to reflection and transmission magnitude are made which apply to (7), and if the angles of the quantities in (6) are disposed to produce the maximum, oppositely sensed

errors in phase at the two frequencies defining the interval, then the maximum possible error in delay for a network having small loss and only modest reflections would be

$$2\,\frac{|\,s_{11}\rho_G\,| + |\,s_{22}\rho_L\,| + 2\,|\,\rho_G\rho_L\,|}{\Delta}\ \text{seconds}, \tag{8}$$

where it is assumed that $|\,s_{11}\,|$, $|\,s_{22}\,|$, $|\,\rho_G\,|$, and $|\,\rho_L\,|$ are the same at both frequencies. Δ is the radian frequency separation between the RF tones bounding the interval.

For example, consider the application of (7) and (8) at 2.0 gc in the present set where $|\,\rho_G\,|$ and $|\,\rho_L\,|$ are approximately 0.03. Under these circumstances, when measuring an unknown having $|\,s_{11}\,|$ and $|\,s_{22}\,|$ equal to 0.1, (7) and (8) show that the error in loss, phase, and delay measurement could approach 0.06 db, 0.4 degree, and 0.45 nanoseconds. Measured at 4 gc, the network just considered could be erroneously measured by as much as 0.3 db for loss, 2.3 degrees for phase, and 2.2 nanoseconds for delay in view of the increase in test set reflections to a level of 0.1.

The previous equations define absolute upper bounds on measurement error due to mistermination. More realistic error limits, particular to a given situation, may be obtained by applying (5) directly, when the requisite information is available. Advantage may also be taken of constraints imposed on the s parameters by virtue of passivity conditions in order to further bound mistermination errors.[11]

6.2 *Aperture Error in Delay Measurement*

The test set applies an amplitude-modulated wave to the unknown but only the carrier and one of the adjacent side tones ultimately beat together, after downward frequency translation, to form detected signal. The aperture errors are hence characteristic of those encountered in "two-tone" measurement sets, rather than the larger errors produced in a "three-tone" set.[7] The origin of the error is suggested in the Fig. 17. The test set indicates the slope of the secant line connecting the phase ordinates at ω_1 and ω_2. When higher-order curvature exists between ω_1 and ω_2, the slope of the secant line no longer is the same as the slope of the tangent, $\partial\theta/\partial\omega$, drawn at the mean frequency, $(\omega_1 + \omega_2)/2$, where the delay is considered to be evaluated.

If the phase curve of the unknown exhibits only algebraic variation over the frequency range encompassed by the measurements, elementary deductions are then possible with respect to errors in measurement of *delay distortion*, i.e., in measurement of the variation of delay across

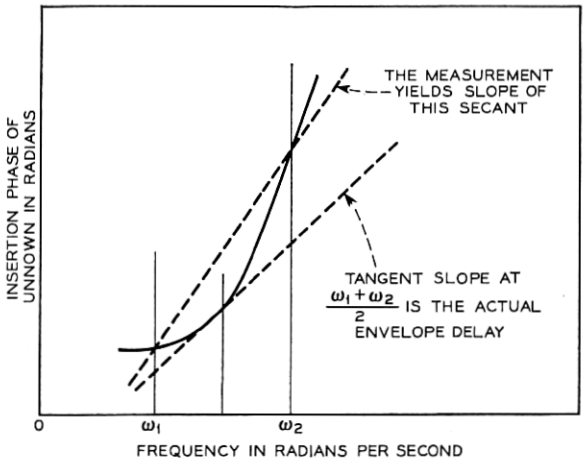


Fig. 17 — "Aperture error" in envelope delay measurement.

the test frequency range. When the phase curve is expressible as the polynominal

$$\Phi = a_0 + a_1\omega + a_2\omega^2 + \cdots a_n\omega^n, \tag{9}$$

it may then be demonstrated that no error results in delay distortion measurement for $n \leqq 3$. Hence, there is no aperture error when measuring a linear or a parabolic delay shape, or an additive combination of these shapes.

On the other hand, quite large errors can result in the measurement of ripples of delay superimposed on algebraic shapes. If the period of the ripple is Q and p is the separation between the two delay measuring tones, then the indicated value of the amplitude of a delay sinuousity having a peak-to-peak value, τ_0, would be erroneously indicated by

$$\tau_0' = \tau_0 \frac{\sin \frac{\pi p}{Q}}{\frac{\pi p}{Q}} \tag{10}$$

The magnitude of the error may be appreciated from the fact that the indicated value of τ_0 is in error by 7 per cent when the ratio of Q to p equals 5.

6.3 *Accuracy Validation*

Broadband standards of loss, phase, and delay, operable between 0.25 and 4.2 gc and having sufficient accuracy for use as a checking

standard, are not available. Hence, indirect techniques of validation had to be resorted to.

As a first step, the insertion loss and phase of each of two coaxial pads was measured at a large number of frequencies. The sum of these measurements was then compared with the over-all measurement of loss and phase through the tandem connection of the two pads. Study of the equation for ε_f in Section 6.1, as applied to the accuracy validation problem, shows that this comparison yields a valid measure of test set error, provided that the test set and pad reflections are sufficiently small. For the frequency range up to 2 gc, over which the test set terminations are <0.03, the use of pad standards with reflections of 0.03 would permit accuracy determinations, by the method just outlined, to a tolerance of 0.04 db and 0.25 degrees. Such pads are available, and when the "bootstrap" experiment was made using a pair of nominal 20-db units, it was found that the sum of individual measurement agreed with the over-all measurement to within 0.1 db and 0.3 degree up to 2 gc. The agreement proved to be about the same for a pair of 10-db pads.

Because of the increased reflection from both the test set and the pads above 2 gc, less favorable results were obtained in this region. The disagreement between arithmetic sum and measured sum cycled with test frequency, and this strongly suggested that the cause lay with reflection coefficient interactions. This was confirmed by building up to a given value of tandem loss using different combinations of pad values. The results varied with specific pad combinations even though the electrical lengths of all the pads were about equal.

In similar tests to evaluate the delay measurement performance, it was possible to correctly sum 2 cables of 20 nanosecond length to within 0.4 nanoseconds up to 4 gc.

VII. EQUIPMENT DESIGN

The test set apparatus is distributed among four bays. One of these bays provides a tightly shielded compartment for the test frequency signal sources. The remaining three bays are united to form a three-cabinet console. This arrangement is shown in Fig. 18.

The layout has been executed with operator convenience foremost in mind. Just above table level in the right-hand bay of the console are the programming knobs for selecting between loss or gain, and between phase or delay modes of measurement. An extensive array of coaxial switching automatically sets up the test set circuitry for measurement in any of the desired modes, on command from the programming knobs. Also occupying convenient locations in the right-hand bay are the

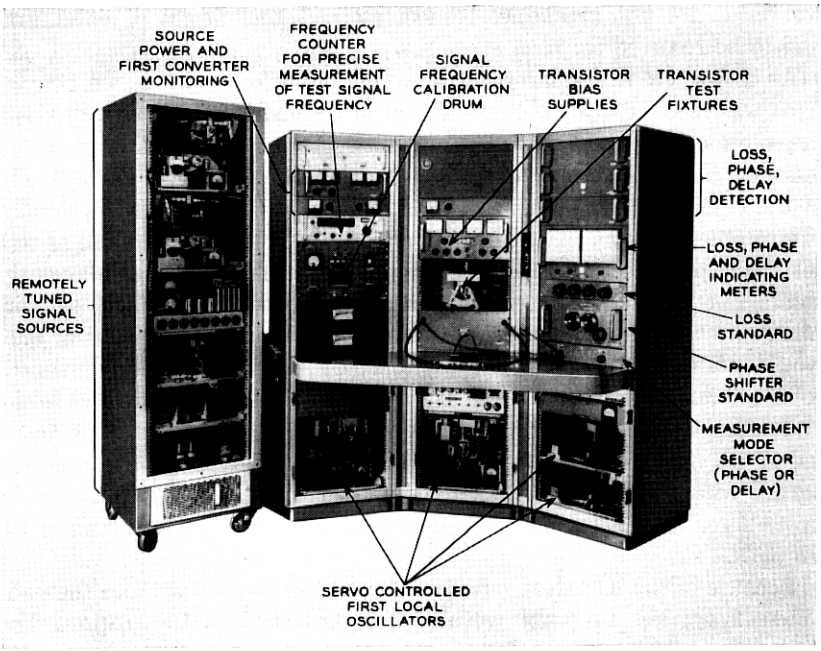


Fig. 18 — 0.25 to 4.2-gc transmission, phase and delay measuring set shown with front covers removed.

calibrated measurement standards and the associated null meters. The various scales on the meters are edge lit to unambiguously indicate the particular scale in use. Automatic ranging circuitry transfers operation to the more coarsely calibrated scales whenever the prevailing loss, gain, phase, or delay unbalances exceed the end limits of the most sensitive scales.

The left-hand bay contains the controls for selecting test signal frequency. The point-by-point and motor scan controls are visible in Fig. 18, just below, and to the left and right of the drum dial which bears the frequency calibrations for all four test signal bands. Monitor meters for indicating the power output of the sources and the dc currents flowing in the converter crystals are also provided in the left-hand bay. These are of no interest to the operator, but do play an important role in preventive maintenance. Each of the chassis modules is mounted on slides, thus making in-situ maintenance feasible.

Resting on the table, and emerging from the center bay, are the flexible cables for connection of coaxially terminated unknowns. Each of these cables is terminated in a 15-db impedance buffering pad. The

center bay also houses the built-in transistor measurement facilities. The jig and associated coaxial trombone mount on a retractable slide which the operator pulls out when making transistor measurements. Connections are made to the input and output test set cables through Type N-Dezifix B coaxial adapters.

VIII. ACKNOWLEDGMENTS

Mr. F. R. Dennis provided the test signal sources and remote tuning servo, as well as the first LO system and associated electro-mechanical servo control. He was also responsible for the original design of the control circuit for automatically switching operation of the set from one band to another.

Mr. W. G. Hammett was responsible for all the design effort involved in adapting the test set to the measurement of transistor characteristics. This included the design and characterization of all of the specially required coaxial apparatus as well as the analytic procedures for reducing measurement data to transistor parameters and estimating the errors involved. Mr. Hammett furnished the design for the VCO frequency control loop and related capture circuitry, phase standard, APC loop for the automatic regulation of the operating point at the phase detector, and the loss and phase detection circuitry.

Mr. O. Kummer contributed the over-all front-end design and specification of test set level patterns to achieve objectives of linearity, crosstalk, and S/N. This work included the provision of the converters and associated isolation circuitry. Mr. Kummer designed the RF comparison switching complex, the loss standard, all of the special circuitry involved in the measurement of envelope delay and the programming features for automatic set up of the instrument in either phase or delay measurement modes. Mr. Kummer was also responsible for over-all accuracy validation.

Mr. R. A. Berner made contributions to many areas of the set through fabrication and test of brassboard models and by supervising many of the details of construction.

As supervisor of the group which developed the measuring instrument, the author held the over-all project responsibility. The author's superior, Mr. S. Doba, Jr., contributed suggestions and comments which often led to improvements in the design.

REFERENCES

1. Leed, D. and Kummer, O., A Loss and Phase Set for Measuring Transistor Parameters and Two Port Networks between 5 and 250 mc, B.S.T.J., *40*, May, 1961, pp. 841–884.

2. Alsberg, D. A., Precise Sweep Frequency Method of Vector Impedance Measurement, Proc IRE, *39,* November, 1951, pp. 1393–1400.
3. Alsberg, D. A. and Leed, D., A Precise Direct Reading Phase and Transmission Measurement System for Video Frequencies, B.S.T.J., *28,* April, 1949, pp. 221–238.
4. Meinke, H. H. and Scheuber, A., Die Berechnung der Ubertrogungseigenschaften Zylin der Symmetriche Bauelemente Koaxialer Leitung aus dem Verhalten von Ebenen Elektrostatischen Feldern, Arch. Elektr. Ubertragung, Band 6, pp. 221–227, June, 1952.
5. Montgomery, C. G., Dicke, R. H., Purcell, E. M., *Principles of Microwave Circuits,* McGraw-Hill Book Company, Inc., New York, 1948, pp. 150–151.
6. Oliner, A. A., Calibration of Slotted Section for Precision Microwave Measurements, Review of Scientific Instruments, *25,* January, 1954, pp. 13–20.
7. Magnusson, R., Sensitive Group Delay Meters, Ericsson Technics, No. 1, 1957, pp. 110–141.
8. Goldman, S., *Frequency Analysis, Modulation and Noise,* McGraw-Hill Book Company, Inc., New York, 1948, p. 246, Eq. 114.
9. Toro, V. and Parker, S. R., *Principles of Control Systems Engineering,* McGraw-Hill Book Company, Inc., New York, 1960, pp. 132–139.
10. Leed, D., Automatic Frequency Control Circuit, U.S. Patent No. 2,610,297, December 14, 1948.
11. Youla, D. C. and Paterno, P. M., Realizable Limits of Error for Dissipationless Attenuators in Mismatched Systems, IEEE Trans., Microwave Theory and Techniques, *MTT-12,* May, 1964, pp. 289–299.