

The Charge-Control Concept in the Form of Equivalent Circuits, Representing a Link Between the Classic Large Signal Diode and Transistor Models

By DANKWART KOEHLER

(Manuscript received November 2, 1966)

It is shown in this paper that the charge-control concept can be conceived as a special form of the Linvill model for semiconductors. Instead of mathematical tools, charge-control models become equivalent circuits amenable to ordinary network analysis techniques. In the simplest form, the charge-control equivalent circuit for the junction transistor is fully equivalent to the Linvill and the Beaufoy-Sparkes model. For all practical purposes, it is also equivalent to the Ebers-Moll model.

The charge-control junction transistor equivalent circuit combines those features of the other models that are important for electrical engineering applications. It also permits the conversion between the three basic types of models. Because of its close relationship to the physical processes governing a device, it can readily be extended to higher-order phenomena. This is usually done by expressing a Linvill-type lumped model in terms of charge parameters. The charge-control equivalent circuit can be useful for modeling a variety of semiconductor devices.

I. INTRODUCTION

Three basic approaches are generally used to obtain descriptive large-signal models for transistors and diodes, the Ebers-Moll model,¹ the Linvill model² and the charge-control concept³ after Beaufoy and Sparkes.

The *Ebers-Moll* transistor model^{1,4} is based on the idea of superimposing a "normal" and an "inverse" transistor. Semiconductor junctions are represented by means of diodes and capacitors, whereas the properties of the transistor base are represented by frequency-dependent current sources. The Ebers-Moll transistor model is the

most popular of all transistor models since it lends itself most readily to simple "rule-of-thumb calculations." The current relations are described in the frequency domain, whereas the junction voltages are described as functions of current in the time domain, or, as in the original paper, only at dc. The model simulates only the effect which minority carrier storage exercises on the relations among the various device currents, but not the effect on current-voltage relations. Since the diode is a one-port device, no diode model of the Ebers-Moll type exists that could simulate carrier storage.*

The *Linvill* model^{2,5-13} is almost a direct representation of the continuity and diffusion equations for semiconductor materials. It uses physical rather than circuit parameters and is superior to any other model when it comes to incorporating second-order physical effects or symbolizing new structures.

The *charge-control* concept^{3,14-33} stands about halfway between physics and circuit considerations. It has proven in the past to be very useful for studying storage effects in diodes and transistors, but appeared to be entirely a mathematical tool. Certain equivalent circuits have been presented^{14,15} to illustrate charge control, but, as Linvill phrased it, "they have little more meaning than a symbolic model useful for the purposes of visualizing only."

Hamilton, Lindholm and Narud compared the three models for the transistor in a well-written tutorial paper.^{9,10} They discussed the approximations used in deriving each model from the same physical background. [See also Ref. 34] In contrast to this parallel treatment of the three models, the following study dwells on the interrelations and conversions between the various models. This is illustrated symbolically in Fig. 1.

We may call the Linvill model a physical model, the Beaufoy-Sparkes charge-control model a mathematical model, and the Ebers-Moll model an electrical model. The link between the three models is accomplished through a modified approach to charge-control theory: instead of deriving, from device physics by means of integration, mathematical charge-control expressions, the charge-control concept can be treated entirely as an equivalent circuit tool.²⁷ The transistor model, for example, is in such a form readily comparable with, and convertible into the Linvill and the Ebers-Moll model, provided all of these models are at the same level of approximation. In its simplest form, the charge-

* Diode models that simulate storage and use neither the charge control nor the Linvill concept are usually extensions of small-signal models towards incorporating certain nonlinear properties.

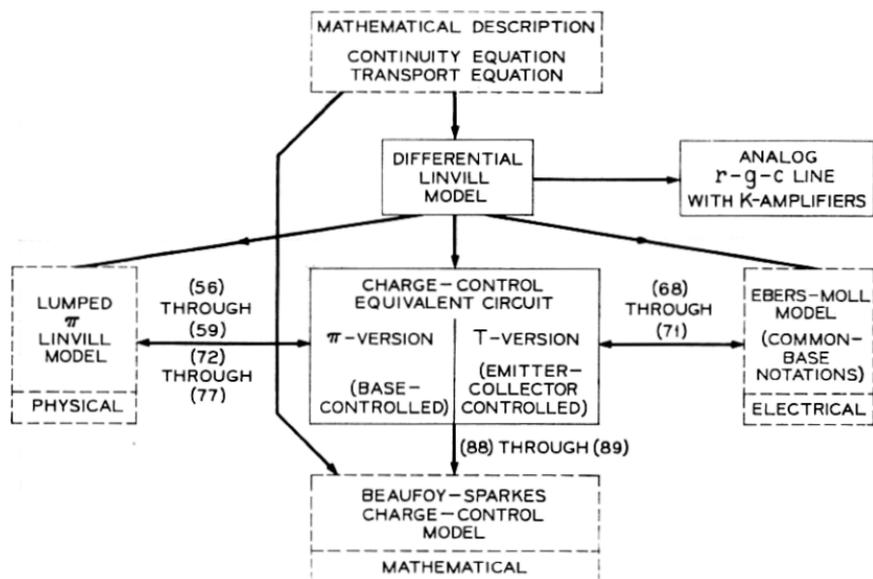


Fig. 1—Principle of derivation of transistor models and their interrelations (heavy lines indicate main aspect of this paper; numbers refer to conversion equations in the text).

control equivalent circuit model is fully equivalent with the standard form of the Beaufoy-Sparkes charge-control model. But equivalency is usually lost, as extensions to higher-order approximations are made in each model.

In this paper, we shall review the derivation of the above-mentioned types of models for diodes and transistors. This will be done with the help of a differential transmission line model. The equivalent circuit type charge-control concept will then be derived for diodes and transistors. This will be followed by a discussion of higher-order approximations, the inclusion of drift fields, and possible applications to other semiconductor devices.

II. DIODE MODELS

2.1 *Mathematical Description*

As a starting point for our discussion it is assumed that the reader is familiar with the continuity and transport equations, describing current flow and carrier density in a semiconductor material. Continuity equations

$$-\text{div } j_p(t) = e \frac{\partial p(t)}{\partial t} + e \frac{p(t) - p_0}{\tau_p} \quad (1a)$$

$$+\text{div } j_n(t) = e \frac{\partial n(t)}{\partial t} + e \frac{n(t) - n_0}{\tau_n}. \quad (1b)$$

Transport equations

$$j_p(t) = e\mu_p E p(t) - eD_p \text{grad } p(t) \quad (2a)$$

$$j_n(t) = e\mu_n E n(t) + eD_n \text{grad } n(t). \quad (2b)$$

j_p and j_n are the hole and electron current densities, respectively. p and n are the hole and electron carrier densities with p_0 and n_0 being their equilibrium values at a given temperature. E is the electric field intensity. D_p and D_n are the hole and electron diffusion constants, and μ_p and μ_n are the respective carrier mobilities. $e = +|e|$ is the value of the electronic charge.

2.1.1 *p-n Junction*

A p-n junction is described in a first-order approximation by the transport equation (2). The well-justified assumption is made that both j_p and j_n are numerically small compared with the mutually opposing diffusion and drift currents. With the help of the Einstein relations

$$D_p = \frac{kT}{e} \mu_p \quad (3a)$$

$$D_n = \frac{kT}{e} \mu_n \quad (3b)$$

and the appropriate boundary conditions one obtains the Boltzmann equations that express carrier densities as functions of the applied junction voltage v_{ext} :

$$p_n(0, t) = p_{n0} \exp \left[\frac{e}{kT} v_{\text{ext}}(t) \right] \quad (4a)$$

$$n_p(0, t) = n_{p0} \exp \left[\frac{e}{kT} v_{\text{ext}}(t) \right]. \quad (4b)$$

Here, $p_n(0, t)$ and $n_p(0, t)$ are the carrier densities on both sides of the junctions; p_{n0} and n_{p0} are the densities for $v_{\text{ext}} = 0$ or, in other words, at points away from the junction, previously called p_0 and n_0 in (1). The definitions of these notations are illustrated in Fig. 2.

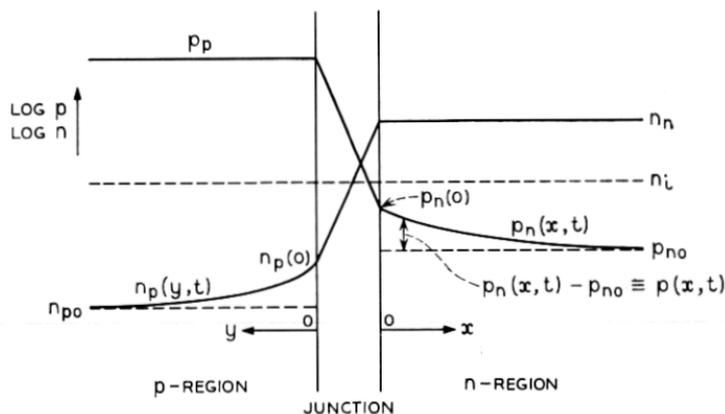


Fig. 2—Carrier density distributions in the vicinity of a p-n junction and explanation of notations used.

In terms of excess carrier densities, (4) transform into the following expressions

$$p_{\text{excess}}(t) = p_n(0,t) - p_{n0} = p_{n0} \left[\exp \left\{ \frac{e}{kT} v_{\text{ext}}(t) \right\} - 1 \right] \quad (5a)$$

$$n_{\text{excess}}(t) = n_p(0,t) - n_{p0} = n_{p0} \left[\exp \left\{ \frac{e}{kT} v_{\text{ext}}(t) \right\} - 1 \right]. \quad (5b)$$

Together with the reasonable approximation that the hole and electron currents pass through the junction unchanged,* (5) uniquely characterizes the junction.

2.1.2 *p* and *n* Regions

The following assumptions are implied in the analysis presented for a p-n diode:

- (i) The p-region is so heavily doped that the electron current can be neglected and appreciable carrier injection occurs only in the n-region.
- (ii) The problem is reduced to one-dimensional variations along the *x* axis.
- (iii) Drift fields are neglected. (Their inclusion will be briefly discussed later in Section 7.3.4.)
- (iv) Space charge neutrality is assumed.

* This is not quite true for silicon diodes at low forward currents and in the reverse direction where recombination in the space charge layer cannot be neglected. With respect to some of the diode properties, especially the current-versus-voltage relationship, the discrepancy can be accounted for by changing the exponent to $e v_{\text{ext}}/2kT$.¹¹

With these assumptions the continuity and transport equations reduce to

$$-\frac{\partial j_p(x,t)}{\partial x} = e \frac{\partial p_n(x,t)}{\partial t} + e \frac{p_n(x,t) - p_{n0}}{\tau_p} \quad (6)$$

$$j_p(x,t) = -eD_p \frac{\partial p_n(x,t)}{\partial x}. \quad (7)$$

We shall now express (6) and (7) in terms of the excess carrier densities $p_{n_{\text{excess}}}$ which we shall denote for simplicity as p , i.e.,

$$p(x,t) = p_{n_{\text{excess}}}(x,t) \equiv p_n(x,t) - p_{n0}.$$

Multiplying by the cross section A we obtain

$$-\frac{\partial i_p(x,t)}{\partial x} = eA \frac{\partial p(x,t)}{\partial t} + eA \frac{p(x,t)}{\tau_p} \quad (8)$$

$$i_p(x,t) = -eAD_p \frac{\partial p(x,t)}{\partial x}. \quad (9)$$

These are the two equations describing the n-region.

2.2 Differential Diode equivalent circuits

Equations (8) and (9) become transmission line equations if i_p and p are taken as currents and voltages, respectively. (Mathematically, one may think of p as an analog voltage representing carrier density.) Fig. 3 illustrates the resulting r - g - c transmission line.

The currents in the network branches are true currents but the voltages associated with the nodes are analog voltages. As a reminder, we have labeled the nodes with encircled "p's". The series and shunt elements are accordingly analog resistors, conductors and capacitors per unit length.

If the diode is forward biased, the junction injects carriers into the n-region. They diffuse across the n-region gradually recombining until, at $x \rightarrow \infty$, all hole current is converted into electron current. Fig. 4 shows the carrier distribution across the n-region which is equal to the voltage distribution along the infinitely long r - g - c line. It can be derived easily from (8) and (9) that, under steady-state conditions, the shape of the charge distribution is proportional to

$$\exp(-x/L_p),$$

where

$$L_p = \sqrt{D_p \tau_p}. \quad (10)$$

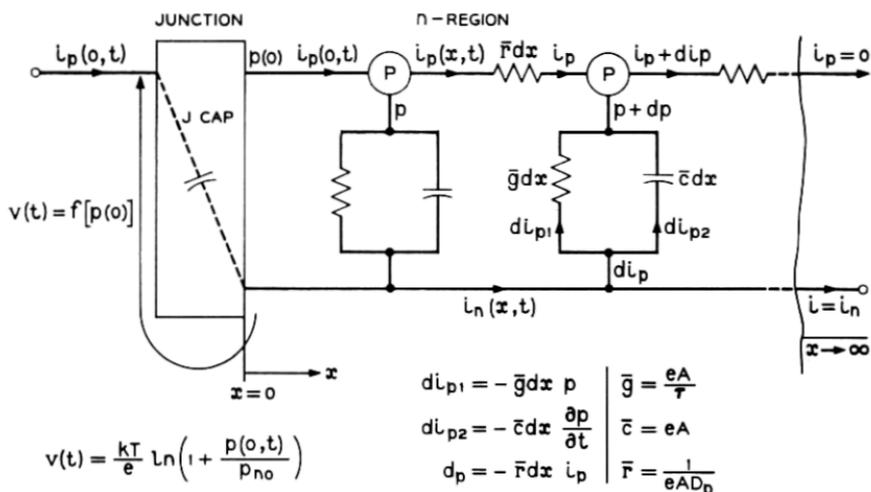


Fig. 3—Analog differential transmission line representation of diode model. (The bars indicate dimension per unit length.)

L_p is called the diffusion length. τ_p is the hole recombination time constant, or hole "lifetime".

Since the analog voltage distribution on the capacitors of the $r-g-c$ transmission line is identical with the physical charge density distribution, and since many engineers have a much better feel for the charging and discharging processes of such a line than for the physical process, the $r-g-c$ line representation may be quite helpful as an illustration of the carrier injection process. In early semiconductor work, such $r-g-c$ transmission lines were frequently used.^{26,35,36,37} No attempt was made, however, to attribute the physical meaning of carrier density to the network nodes; the junctions were represented by so-called K -amplifiers. These amplifiers transform the internal voltage at $x = 0$

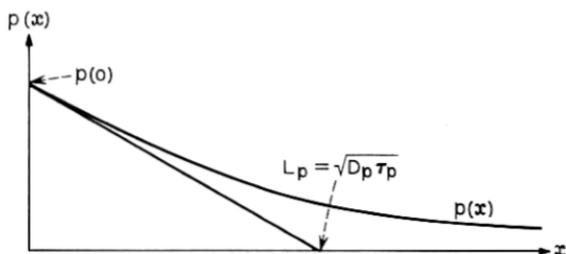


Fig. 4—Excess carrier distribution in diode n-region.

to the external voltage with the appropriate exponential relationship, while not transforming current at all.

Linvill^{2,5,6,7} has introduced new symbols for the network elements which relate current to carrier density. These new notations avoid possible confusion between analog and physical circuit parameters, especially voltages, and hence enable us to combine current/carrier-density with current/voltage networks. Fig. 5 shows such a Linvill model in differential form. Again we have added bars over the letters as it was done with the \bar{r} , \bar{g} , and \bar{c} in Fig. 3 to denote their dimensions as being "units per length".

The symbols in the models are defined as follows:

$$di_{p1}(x,t) = -\bar{H}_c dx p(x,t) \quad (11a)$$

$$di_{p2}(x,t) = -\bar{S} dx \frac{\partial p(x,t)}{\partial t} \quad (11b)$$

$$dp(x,t) = -\overline{(1/H_d)} dx i_p(x,t), \quad (11c)$$

where

$$\bar{H}_c = \text{combinance per length} = eA/\tau_p \quad (12a)$$

$$\bar{S} = \text{storance per length} = eA \quad (12b)$$

$$\overline{(1/H_d)} = \frac{1}{\text{diffusance}} \text{ per length} = 1/eAD_p. \quad (12c)$$

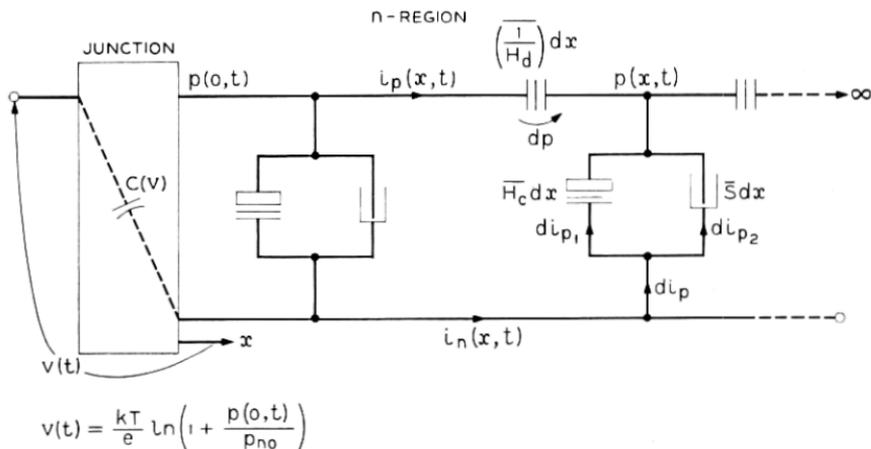


Fig. 5—Differential Linvill diode model. Note that, in consistency with common transmission line notations, the reciprocal of diffusance must be used.

This model can be extended to include majority carriers, drift fields etc. The reader is referred to the literature.^{2,5-13}

2.3 Integrated Diode Models

2.3.1 Mathematical Integration

In order to arrive at an expression for the external diode current from the continuity equation (8) we can integrate this expression with respect to x . Choosing $x = 0$ and $x = \infty$ as the limits of integration, we obtain

$$-\int_0^{\infty} \frac{\partial i_p(x,t)}{\partial x} dx = \int_0^{\infty} eA \frac{\partial p(x,t)}{\partial t} dx + \frac{1}{\tau_p} \int_0^{\infty} eAp(x,t) dx. \quad (13)$$

The third integral represents the total charge in the bulk material. With the appropriate boundary conditions $i_p(0) = i$, $i_n(0) = 0$, $i_p(\infty) = 0$, $i_n(\infty) = i$, the well-known charge-control equation³ can readily be obtained as

$$i(t) = \frac{dq(t)}{dt} + \frac{q(t)}{\tau_p}. \quad (14)$$

To obtain (14) from (13) the assumption must be made that A and τ_p are constant. Note that no approximations or restrictions to specific charge distributions are implied in (14). (They must be made, however, when relating the current to the junction voltage.)

2.3.2 Lumped Linvill Diode Model

The crudest approximation to the distributed Linvill model of Fig. 5 is to replace the "line" by just one storage and one combinance^{2,7} as shown in Fig. 6. These two elements are obtained by summing, i.e.,

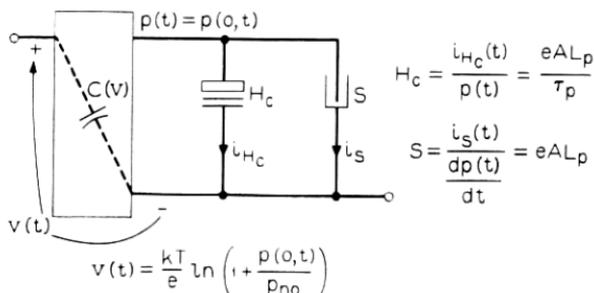


Fig. 6—Lumped Linvill diode model showing single-pole approximation for minority carrier storage. Chosen values: $\Delta x = L_p$, $p(t) = p(0,t)$.

integrating, all differential storances and combinances from $x = 0$ to some value Δx . The value of Δx is usually chosen to equal the diffusion length L_p . This may seem arbitrary,¹² but has no effect on the terminal properties of the first-order model, as long as $p(t)$ is chosen such as to maintain the same amount of total charge.

The values of the circuit elements follow from (11), (12), and (5a) as

$$H_c = \overline{H}_c \Delta x = \overline{H}_c L_p = \frac{eAL_p}{\tau_p} \quad (15a)$$

$$S = \overline{S} \Delta x = \overline{S} L_p = eAL_p \quad (15b)$$

$$v(t) = \frac{1}{\lambda} \ln \left(1 + \frac{p(0,t)}{p_{n0}} \right), \quad (15c)$$

where λ is an abbreviated notation, used hereafter for

$$\lambda = \frac{e}{kT}. \quad (16)$$

The meaning of such lumping with respect to the carrier distribution is illustrated in Figs. 7 and 8. The solid lines in Fig. 7 present the actual carrier distribution in a switching example in which a current pulse is assumed. As required by the transport equation, the slope at $x = 0$ is, at any time, proportional to the current. Under steady-state conditions, an exponential distribution is obtained. To assume such exponential distributions at any instant of time (dashed lines in Fig. 7) represents a simplifying assumption. The corresponding

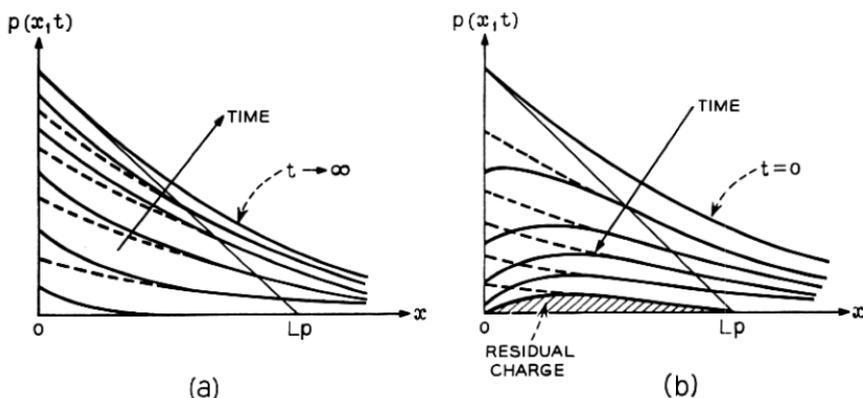


Fig. 7—Illustration of the (a) charging and (b) discharging process in the neutral bulk material. The applied signals are assumed to be forward and reverse current pulses. The solid lines represent the actual shape for current pulse drive; the dashed lines represent exponential model approximations.

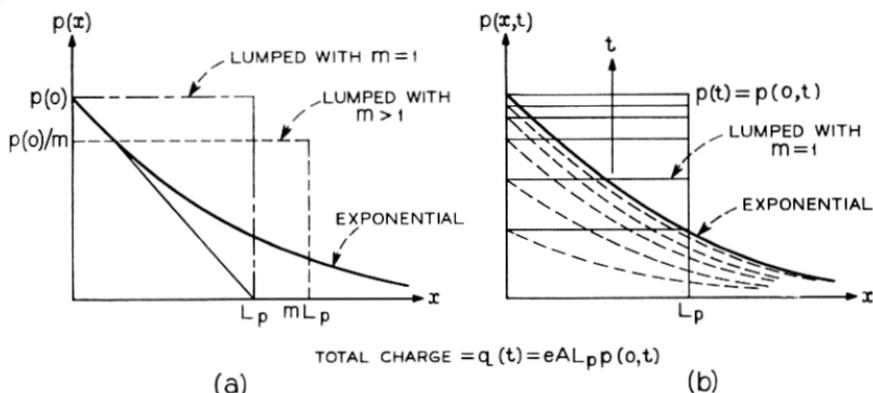


Fig. 8—Exponential and corresponding lumped distribution of excess minority carriers in the bulk material of a diode. (a) Illustration of the choice of lumping length. (b) Time variation for $m = 1$; $m = 1$ is generally preferred in the Linvill model, and is irrelevant in charge models or circuit applications of the Linvill model.

errors are negligible in all those applications where the switching times are large compared with the carrier redistribution times (= diffusion times τ_a and τ_b in Fig. 12).

In the lumped Linvill model, it is assumed that the carrier density is, at any instant of time, constant from $x = 0$ to $x = L_p$, and that it is 0 for all $x > L_p$. Any information on the distribution of the charge, especially of the slope at $x = 0$, as expressed in the transport equation, has been lost since all series elements (diffusances) are neglected. The only parameter of importance left is the total number of minority carriers and hence, the total charge. The approximation used is therefore equivalent to the dashed line exponential distribution in Fig. 7.

As mentioned above and illustrated in Fig. 8(a), the length Δx over which p is nonzero, is most conveniently chosen to equal L_p . But it is permissible to choose $\Delta x \neq L_p$ if the constant value $p(x)$ is recognized to be different from $p(0,t)$; for $\Delta x = mL_p$, we must choose $p(t) = p(0,t)/m$ such as to yield the same total charge

$$q = eAL_p p(0,t). \quad (17)$$

Fig. 8(b) shows, for $m = 1$, the time variation of the carrier distributions for the lumped model (solid lines) and the exponential distribution (dashed lines).

As the external voltage $v(t)$ varies, the carrier density $p(0,t)$ changes accordingly. The relation between $v(t)$ and $p(0,t)$ has been given above in (15c). We shall see below that the approximation made in the lumping process, as discussed above, effects only $v(t)$ but not the current. Little

or no error is made whenever, and as long as the external driving source impedance is large.

Since, in this and any other lumped Linvill model, all circuit parameters are functions of total charges in the various sections of the semiconductor we can transform the model of Fig. 6 into a charge-controlled model, in which all carrier densities are replaced by charges. This will be shown in Section 2.4.1.

2.4 Charge-Control Diode Model

Without invoking any of the approximations introduced in Section 2.3.2 and illustrated in Figs. 7 and 8, the diode is completely described by (14) and (5a). These two equations are the basis for the classic charge-control theory after Beaufoy-Sparkes as applied to diodes. Throughout the charge-control literature, only the current appears as a function of the total charge but not the voltage. If we want to relate the junction voltage to the charge rather than to $p_n(0,t)$ as it was done in (5a), we must make some approximation: The simplest possible approximation is the assumption that $p(0,t)$ is proportional to $q(t)$. This is, for example, satisfied if the shape $f(x)$ of the carrier distribution never changes, i.e., if the carriers redistribute themselves instantaneously. $p(x,t)$ is then of the form

$$p(x,t) = f(x)g(t).$$

The shape of $f(x)$ does not matter as long as the integral $\int f(x) dx$ yields the proper proportionality constant. Examples of this are the exponential distribution or the lumped distribution (with any arbitrary value of m) in Fig. 8(a). This shows the equivalency between the postulate of instantaneous carrier redistribution in classic charge-control theory and carrier density lumping in the first order Linvill model.

If we now want to establish an equivalent charge-control circuit we must first represent (14) by corresponding circuit symbols. This is done in the n-region part of Fig. 9. S is the store originally introduced by Beaufoy and Sparkes.^{11,12} To account for directionality, we have added a vertical bar to the store symbol in the manner of the standard diode symbol. The properties of S , as defined in this paper, are:

- (i) charge stored = $q(t)$
 (ii) current in direction indicated by arrow \overrightarrow{S}

$$i = \frac{dq(t)}{dt}$$

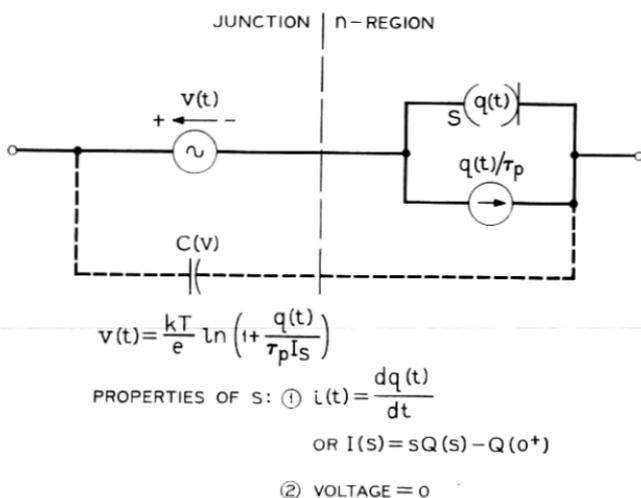


Fig. 9—Complete first-order charge-control equivalent circuit (this circuit is a charge representation of Fig. 6).

(iii) voltage across store = 0.

S is often interpreted as an infinite capacitor for which $i = dq/dt = d(Cv)/dt = \text{finite}$, but $C \rightarrow \infty$ and $v \rightarrow 0$.

It follows from (15c) and (17) that the junction voltage is of the form

$$v(t) = \frac{1}{\lambda} \ln [1 + Kq(t)],$$

where K is a proportionality factor. If we denote the steady-state reverse current (flowing through the diode when $v(t)$ is very large and negative) by I_s we can evaluate the constant: For $v \rightarrow -\infty$ we obtain

$$K \cdot Q = -1$$

and from Fig. 9

$$-I_s = Q/\tau_p.$$

Hence,

$$K = \frac{1}{I_s \tau_p}$$

and thus,

$$v(t) = \frac{1}{\lambda} \ln \left[1 + \frac{q(t)}{I_s \tau_p} \right]. \quad (18)$$

Under steady-state conditions where $Q/\tau_p = I$, this equation becomes the well-known diode equation.

For the possibilities of incorporating the junction capacitances see the discussion in Section 7.3.2.

2.4.1 Derivation of the Charge-Control Model from the Lumped Linvill Model

It represents not merely an additional proof of equivalency but also a good preparation for the derivation of more complex models, if we show²⁷ that we can derive the charge-control model from the Linvill model. A somewhat related modification of the Linvill model was more recently proposed by Beddoes.¹² To this end we calculate the currents through the elements H_c and S in Fig. 6:

$$i_{H_c}(t) = H_c p(0, t) \quad (19a)$$

$$i_s(t) = S \frac{dp(0, t)}{dt}. \quad (19b)$$

Substitution of the values for H_c , S , and $p(0, t)$ from (15a), (15b), and (17) yields

$$i_{H_c}(t) = \frac{eAL_p}{\tau_p} p(0, t) = \frac{q(t)}{\tau_p} \quad (20a)$$

$$i_s(t) = eAL_p \frac{dp(0, t)}{dt} = \frac{dq(t)}{dt}. \quad (20b)$$

This result shows that the current source in the charge-control model of Fig. 9 represents the current i_{H_c} through the combination, and that the store S represents the current i_s through the storage.

To find the expression for the junction, we can express $p(0, t)$ in terms of $q(t)$ by means of (17). p_{n0} can again be obtained from the case, where $V \rightarrow -\infty$, and where $p(0, t) = P(0) = -p_{n0}$:

$$I_{H_c}]_{V \rightarrow -\infty} = -I_S = \frac{eAL_p}{\tau_p} P(0) \Big]_{V \rightarrow -\infty} = -\frac{eAL_p}{\tau_p} p_{n0}.$$

Thus, we find

$$\frac{p(0, t)}{p_{n0}} = \frac{q(t)}{eAL_p} \Big/ \frac{I_S \tau_p}{eAL_p} = \frac{q(t)}{I_S \tau_p}. \quad (21)$$

With this we can make the transition from (15c) to (18).

2.4.2 Evaluation of the Charge-Control Model

The charge-control model is completely equivalent with the lumped Linvill model in Fig. 6; in fact, it may be considered a circuit oriented

form of the Linvill model. In almost all instances^{7,11} where the Linvill model is being used for circuit applications the conversion of carrier density into charge must be made anyhow. The charge-control equivalent circuit in Fig. 9 uses current and voltage sources plus one lesser known circuit element described by the simple relations

$$v(t) = 0 \quad (22a)$$

$$i(t) = \frac{dq(t)}{dt} \quad (22b)$$

or, in Laplace notation

$$I(s) = sQ(s) - Q(0^+). \quad (22c)$$

Ordinary circuit analysis techniques can be used in working with the model. No restriction exists with respect to the external waveforms. Q appears as an additional circuit parameter with additional complexity comparable to that of an additional branch current. From a topological viewpoint it is a branch current. This is the price to be paid for inclusion of the first-order dynamic storage properties.

Junction and n-region are clearly separated in the model. Thus, little difficulty should arise in adding junction capacitors (dashed in Fig. 9), series path resistors, and leakage resistors, provided, physical knowledge of such effects exist.

2.4.3 Charge-Control Model for Short-Base Diodes

Diodes with extremely short bases do not show the exponential minority carrier distribution represented in Fig. 4, but rather a practically linear fall-off (like in a transistor base except that the collector is now a nonrectifying contact). With reference to Figs. 3 or 5, this means that the distributed "transmission line" is so short that the effect of the series diffusances H_d dominates over that of the shunt combinances H_e . The metallic contact behaves like a short circuit at the end of the line.

The analogy with the r - g - c line of Fig. 3 may help the reader visualize the difference between the long base and the short base diode: The first-order approximation for the infinitely long line with respect to currents and input voltage is the parallel connection of the *shunt* resistor and the shunt capacitor; the first-order approximation for a very short line is the parallel connection of the *series* resistor and the shunt capacitor. In terms of the Linvill model, the short base diode model is obtained by replacing H_e in Fig. 6 by $H_d = eAD_p/L$ and

L_p by L . (Note that H_d increases as L becomes small.) In the charge control model, of Fig. 9, the term τ_p , which represents the recombination time constant for the long base diode, now becomes the diffusion time constant. The new value τ'_p can be derived most easily from the Linvill model as follows:

$$\tau'_p = \frac{Q}{i_{H_d}} = \frac{Q}{p(0)H_d/W} = \frac{\frac{1}{2}p(0)eAW}{p(0)eAD_p/W} = \frac{W^2}{2D_p}. \quad (23)$$

Apart from this numerical change, the model in Fig. 9 for the normal diode is equally valid for the short base diode.

2.4.4 Piecewise Linear Charge-Control Diode Model

For many practical purposes the logarithmic voltage source relation can be approximated by a switch as illustrated in Fig. 10. The switch opens when q becomes negative and closes when q is able to charge up to $q > 0$. A threshold voltage V_{th} is connected in series with the forward path. If desired, the slope of the logarithmic curve

$$\frac{dV}{dI} = \frac{dV}{d(q/\tau)} = \frac{\tau}{\lambda q} = \frac{\tau}{\lambda q_{\text{average}}} = \frac{1}{\lambda I_{av}} \approx \frac{2}{\lambda I_{\text{Max}}} \quad (24)$$

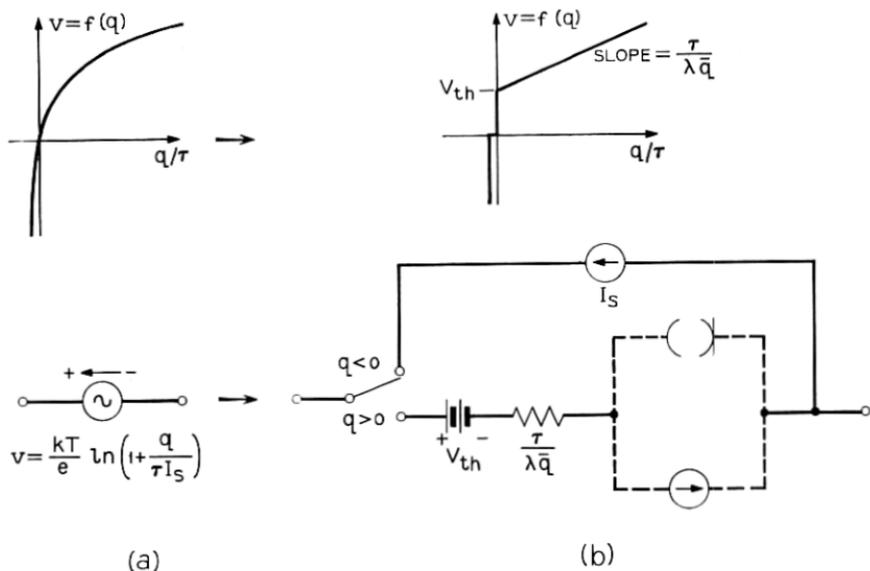


Fig. 10—Piecewise linear approximation for the semiconductor junction. (a) Theoretical logarithmic curve. (b) Approximated curve (the dashed lines indicate the completion of the diode model).

can be added as a resistor, where I_{av} is an average current, which may, in long hand calculations, be assumed to be $\frac{1}{2}I_{max}$. The saturation current I_s must now be represented by an external current source.

2.4.5 Application of the Model

The above discussion of diode models serves two purposes: First, they form a basic understanding for deriving transistor models. Secondly, the diode models can be very useful in simulating dynamic effects due to carrier storage in diodes.

With the piecewise linear junction approximation of Fig. 10 applied to the charge-control model in Fig. 9, storage time equations can be derived easily using Laplace transform concepts. The model has proven to be very useful in the analysis of step-recovery diode circuits. In the piecewise linear form, it can be handled without a computer, whereas, for the more complex models with various parasitics added, computers soon become mandatory.

Switching times for *step-recovery diodes* are derived in Appendix A.1 as an example of the use of the charge-control model. The equations obtained have been found by many authors to agree well with actual measurements. The normalized storage time for recovery from an infinite ON-pulse according to (97) is plotted in curve *a* of Fig. 11 as a function of the reverse-to-forward current ratio according to the relation

$$T = \tau \ln \left(1 + \frac{I_F}{I_R} \right). \quad (25)$$

When applying this result to an *ordinary diode* with homogeneous doping profile, one must be aware of the implied approximations: (i) The single-section approximation in the model does not affect any mutual relationships between currents and charges, but represents approximations with respect to the junction voltage. As the amount of stored charge is reduced considerably in the diode, the junction voltage decreases noticeably. (ii) As the carrier density near the junction becomes extremely small, the voltage reverses sign and the diode impedance, at some point, becomes comparable with the external source impedance. The ideal current source assumed in (97) ceases to exist, and instead of the step-recovery, as given by the model, a long tail in the current response results.

From either one of the two differential models in Figs. 3 or 5, we can calculate the time in which the carrier density at $x = 0$, and hence the junction voltage, reaches zero. Such a calculation yields the relation

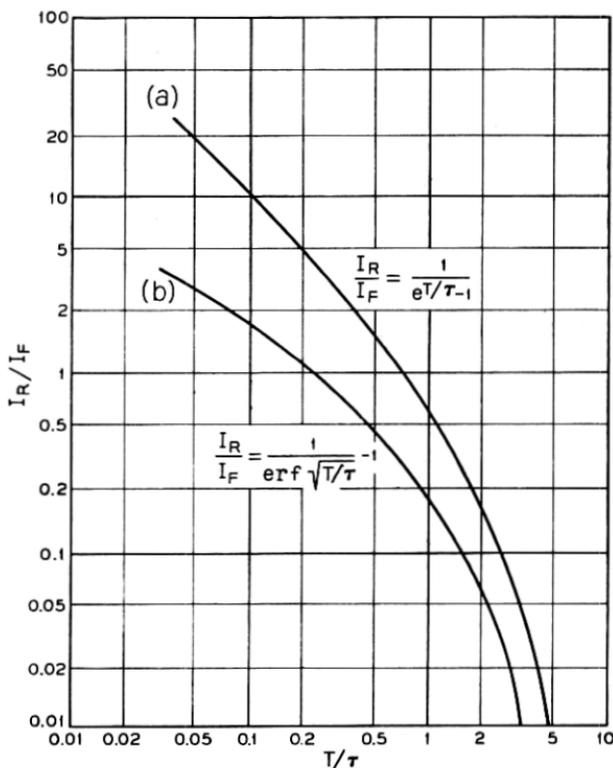


Fig. 11—Comparison of diode storage times as functions of the driving ratios. (a) Single lump model; T = time when charge is fully depleted. (b) Differential model; T = time when excess carrier density at $x = 0$ reaches zero.

originally derived by Lax and Neustadter¹⁵

$$\operatorname{erf} \sqrt{\frac{T}{\tau}} = \frac{1}{1 + \frac{I_R}{I_F}} \quad (26)$$

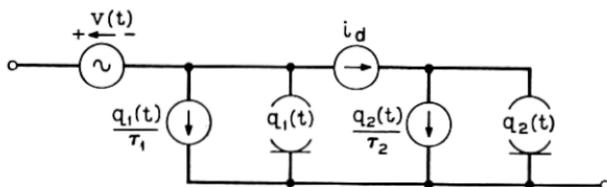
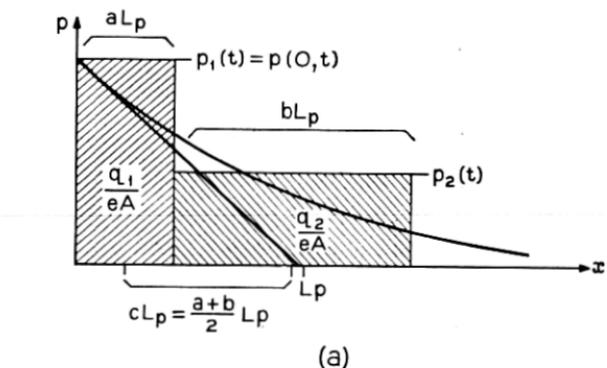
This relationship is illustrated in Fig. 11(b). Since curve (b) represents only the storage phase but not the very long tail of the recovery, the values are much smaller than those in curve (a) in which some sort of "effective total recovery" is represented. The difference is most remarkable at strong relative reverse drives where the carrier distributions on the lines differ most from the steady-state distributions.

If it becomes necessary to incorporate the tail of the recovery into a lumped diode model, the double π -extension described below may prove adequate for most applications.

2.4.6 Higher-Order Approximations

Bearing in mind how the model originated as an approximation to the differential transmission line or as just another form of the lumped Linvill model we can now understand how higher-order approximations are to be obtained.

Fig. 12 shows the example of a π -approximation for a diode. The



$$\text{WHERE } i_d(t) = \frac{q_1(t)}{acL_p^2/D_p} - \frac{q_2(t)}{bcL_p^2/D_p} \equiv \frac{q_1(t)}{\tau_a} - \frac{q_2(t)}{\tau_b}$$

$$v(t) = \frac{kT}{e} \ln \left(1 + \frac{q_1(t)}{\tau_v I_s} \right)$$

$$\tau_v \text{ (FROM DC CONSIDERATIONS)} = \frac{\tau_1 \tau_2}{\tau_1 \left(\frac{1}{a} - 1 \right) + \tau_2}$$

CHARGE CONSERVATION CONSTRAINT ON a, b, c :

$$\frac{cb(1-a)L_p^2}{(a+b-1)D_p\tau_2} = 1$$

WHERE c IS MOST APPROPRIATELY CHOSEN TO BE $c = \frac{a+b}{2}$

(b)

Fig. 12—Higher-order, π -Approximation of diode charge-control model. (a) Charge approximation. (b) Corresponding model.

charge is broken up into two parts q_1 and q_2 . The diffusance between the two stores controls the redistribution of the charge. Such a structure provides a better representation of the junction at the higher frequencies or at higher speeds than the model of Fig. 9, since the junction voltage is now a function of only that part of the total charge which is close to the junction. The model simulates recovery tails. It also permits the simulation of variations in recombination time along the x -axis. Fig. 12 assumes two different recombination times τ_1 and τ_2 . The $i = f(q)$ relation then becomes

$$i = \frac{d(q_1 + q_2)}{dt} + \frac{q_1}{\tau_1} + \frac{q_2}{\tau_2} \quad (27)$$

[which reduces to (14), if one assumes $\tau_1 = \tau_2$].

Three additional time constants τ_a , τ_b , and τ_c , appear in Fig. 12. They depend on the choice of the sections aL_p and bL_p over which the shunt elements are integrated and on the choice of the section cL_p over which the diffusances are integrated. The three degrees of freedom reduce to one, however, if one considers that (i) the total charge must be conserved by the lumped approximation, and (ii) in a multisectional approximation the diffusances are most appropriately lumped over sections cL_p which extend between the centers of the charge sections. The corresponding relations are given in Fig. 12; derivations have been omitted.

III. LARGE-SIGNAL TRANSISTOR MODELS

In complete analogy to the diode models, we shall now compare the various junction transistor models and establish the charge-control model in the form of equivalent circuits. The Ebers-Moll concept, which was found not to be applicable to dynamic diode description, will now enter the "competition".

In order to dwell on the philosophies underlying each concept we shall, at first, limit ourselves to diffusion type junction transistors, neglecting again drift currents and secondary effects such as base-width modulation. All derivations will be carried out for pnp transistors; but, of course, everything will be correspondingly valid for npn transistors.

3.1 *Differential Transistor Model*

The most rigorous of all the equivalent circuits describing a junction transistor, as defined by (5), (8), and (9), is the differential model shown

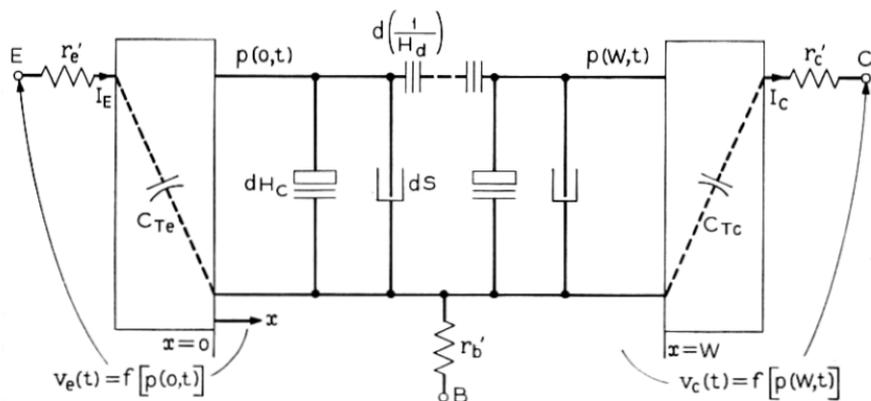


Fig. 13—Differential Linvill model for the transistor with drift fields neglected, *pnp* version shown.

in Fig. 13. Linvill notations comparable to the diode model in Fig. 5 were chosen. (If so wanted, the model could also be drawn with the notations used in Fig. 3 resulting in an *r-g-c* line and two *K*-amplifiers at both ends.)

The base section of the transistor model is only a very short “transmission” line when compared with the “infinitely long” diode n-region of the normal diode. Instead of 100 percent recombination, as found in the diode, the transistor must have as little recombination as possible in order to achieve high gain. Fig. 14(a) shows a steady-state charge distribution under normal forward operation, and Fig. 14(b) shows the distribution for the case where both junctions are emitting, i.e.,

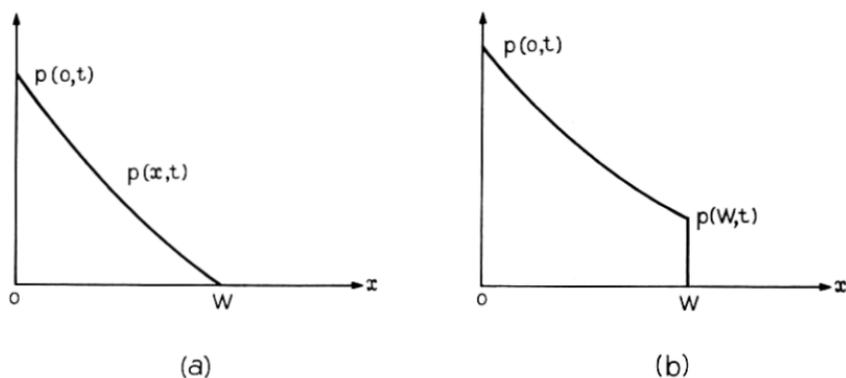


Fig. 14—Excess minority carrier distribution in the transistor base under (a) normal and (b) saturated operation.

in saturation. Under normal operation the collector acts as a "charge short circuit" for the line. For high-gain units, the slope is almost a straight line; at $x = 0$ it is proportional to I_E and at $x = W$ proportional to I_C .

The general case is that of Fig. 14(b) where both junctions are emitting and $p(W) \neq 0$. Any section of the base region can be described analogously to a four-pole using the definitions given in Fig. 15. Note that there are no nonlinearities in the base section.

$$I_E(s) = A_{11}P_1(s) + A_{12}P_2(s) \quad (28a)$$

$$I_C(s) = A_{21}P_1(s) + A_{22}P_2(s). \quad (28b)$$

By using complete analogy to standard transmission line theory, it can be shown that with the use of (10) and (11) one obtains for a homogeneous section Δx

$$I_E(s) = \frac{P_1(s)}{Z} \coth \gamma \Delta x - \frac{P_2(s)}{Z} \operatorname{cosech} \gamma \Delta x \quad (29a)$$

$$I_C(s) = \frac{P_1(s)}{Z} \operatorname{cosech} \gamma \Delta x - \frac{P_2(s)}{Z} \coth \gamma \Delta x, \quad (29b)$$

where

$$Z = \frac{1}{eA} \sqrt{\frac{\tau}{D_p}} \sqrt{\frac{1}{1 + s\tau}} \quad (30)$$

$$\gamma = \sqrt{\frac{1}{D_p\tau}} \sqrt{1 + s\tau}. \quad (31)$$

In the general case, the base is not homogeneous, which means that Z and γ will vary along the line.

The junctions are described by the time relations

$$p_1(0, t) = p_{n0}[\exp \{\lambda v_e(t)\} - 1] \quad (32a)$$

$$p_2(W, t) = p_{n0}[\exp \{\lambda v_c(t)\} - 1]. \quad (32b)$$

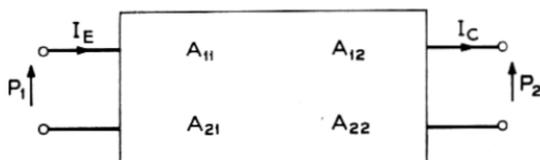


Fig. 15—Symbols and polarity conventions defining the four-pole description of the transistor base.

The four-pole equations describing the transistor base are obtained as

$$I_E(s) = \frac{eAD_p}{W} P_1(s) \left[1 + \frac{A_1 W W_1}{A \tau_1 D_p} (1 + s\tau_1) \right] - \frac{eAD_p}{W} P_2(s) \\ = H_d P_1(s) \left[1 + \frac{H_{e1}}{H_d} \left(1 + s \frac{S_1}{H_{e1}} \right) \right] - H_d P_2(s) \quad (33a)$$

$$I_C(s) = \frac{eAD_p}{W} P_1(s) - \frac{eAD_p}{W} P_2(s) \left[1 + \frac{A_2 W W_2}{A \tau_2 D_p} (1 + s\tau_2) \right] \\ = H_d P_1(s) - H_d P_2(s) \left[1 + \frac{H_{e2}}{H_d} \left(1 + s \frac{S_2}{H_{e2}} \right) \right]. \quad (33b)$$

The junctions are described as

$$p_1(t) = p(0, t) = p_{n0} [\exp \{ \lambda v_e(t) \} - 1] \quad (34a)$$

$$p_2(t) = p(W, t) = p_{n0} [\exp \{ \lambda v_c(t) \} - 1]. \quad (34b)$$

A constraint has to be satisfied: Under equilibrium conditions, the total charge in the base must equal that in the two sections, i.e.,

$$eA_1 W_1 P_1 + eA_2 W_2 P_2 = eA \int_0^W P(x) dx \approx \frac{1}{2} eAW [P(0) + P(W)]. \quad (35)$$

The approximation holds for high-gain units. For this case the base volume sections are equal, i.e., $A_1 W_1 = A_2 W_2 = \frac{1}{2} AW$. For low-gain units (34) must be modified: The terms $p_1(t)$ or $p_2(t)$, or both, must be replaced by $p_1(t)/m_1$ and $p_2(t)/m_2$, respectively, whereby the m 's are constants > 1 , similar to m in Fig. 8.

Equation (33) represents one of several possible approximations to (29) with the additional property of nonsymmetry being added.

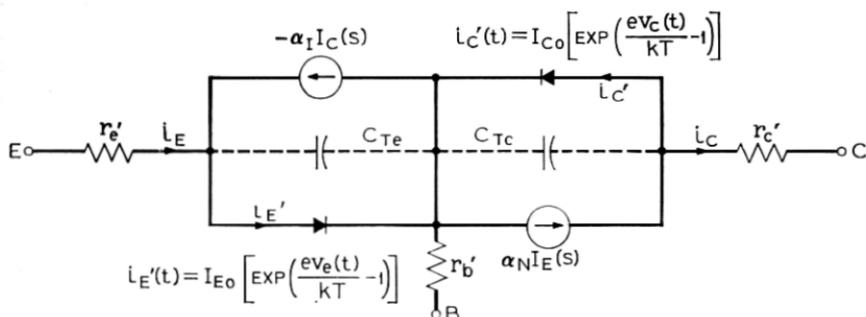
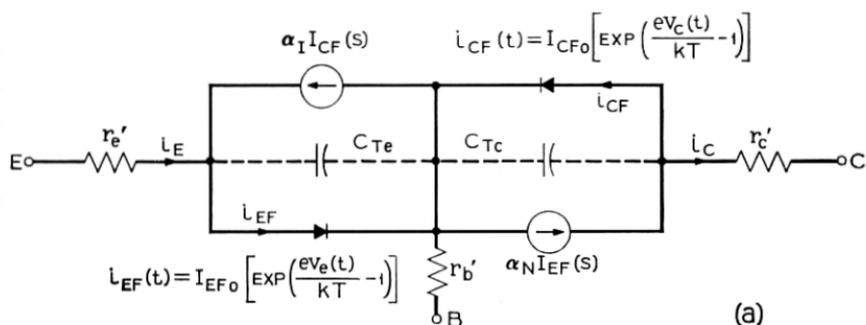
Higher-order approximations of a lumped linear model are obtained by representing the base of width W by more than the two sections W_1 and W_2 .

V. THE EBERS-MOLL TRANSISTOR MODEL

The focal point of the Ebers-Moll model is the two-port description of the base. Such a description has been given in (28) and (29), and is permissible because of the linearity which exists between currents and carrier densities in the base. Nonlinearity exists, however, in the relationship between carrier densities and external voltages according to (32). Since linearity allows the use of the superposition principle,

the total current can be conceived as consisting of the superimposed contributions of the currents injected by the two junctions.

When put into the form of an equivalent circuit, the Ebers-Moll model shows the superposition of a normal transistor (subscript N) and an inverse transistor (subscript I). In Fig. 17(a) the lower diode and current source represent the normal transistor and the upper elements represent the inverse transistor. Each junction is represented by a diode, a fraction of the diode current is collected by the other electrode. The ratios of collected currents to emitted currents are called α_N and α_I for normal and inverse operation, respectively. The general frequency behavior of the α 's can be calculated for a homogeneous base from (29), (30), and (31) as



$$\text{WHERE } \alpha_N(s) = \frac{\alpha_{N0}}{1 + \frac{s}{\omega_{\alpha N}}} \quad \alpha_I(s) = \frac{\alpha_{I0}}{1 + \frac{s}{\omega_{\alpha I}}}$$

Fig. 17—The two forms of the Ebers-Moll transistor model: (a) direct representation of the idea of superimposing a normal and an inverse transistor, (b) collecting current sources as functions of the electrode currents. The junction saturation currents in (b) are identical with the open-electrode diode saturation currents.

$$\alpha(s) = \frac{I_{\text{output}}(s)}{I_{\text{input}}(s)} \Big|_{P_{\text{output}}=0} = \frac{\operatorname{cosech} \gamma \Delta x}{\coth \gamma \Delta x} = \frac{1}{\cosh \gamma \Delta x}$$

$$= \frac{1}{1 + \frac{\gamma^2 \Delta x^2}{2}} = \frac{2D_p \tau}{2D_p \tau + \Delta x^2 + s\tau \Delta x^2} \quad (36)$$

But symmetry does not exist in a practical transistor. The constants in (36) are therefore, different for α_N and for α_I . Equation (36) can be rewritten under this consideration in the well-known form

$$\alpha_N(s) = \frac{\alpha_{N0}}{1 + s/\omega_{\alpha N}} \quad (37a)$$

$$\alpha_I(s) = \frac{\alpha_{I0}}{1 + s/\omega_{\alpha I}} \quad (37b)$$

The relations between the constants in (37) and the physical parameters (corresponding to the constants in (36) modified for the non-symmetrical case) will be derived in Section 5.1.

On account of their nonlinearity, the junction diodes must be described in the time domain. In their original paper, Ebers and Moll defined only a dc relationship between voltages and currents. This would restrict the use of their model to piecewise linear analysis. But the model can be made more general³⁸ by postulating that the $v = f(i)$ relation be valid at all times, as indicated in Fig. 17.

In either case, an important property of the semiconductor junction is lost: Voltages and currents appear as being directly related instead of being related indirectly through current density or charge. This can best be illustrated by an example. If a forward current through a junction is suddenly replaced by a reverse current the voltage actually does not reverse sign until the excess carrier density at the junction is reduced to zero. According to the Ebers-Moll model, voltage and current always change polarity together. As mentioned before, it is for this reason that for a diode, no dynamic model of the Ebers-Moll type exists that would represent charge storage effects. In addition to this shortcoming, the feature of mixed time and frequency domain characterization is undesirable if the model is to be used in its nonlinear form, say on a computer.

The Ebers-Moll model was originally presented in a form, shown in Fig. 17(b), which differs slightly from that in Fig. 17(a). Both versions have been used throughout the literature over the past years and very few authors^{39,40} have clearly pointed out the difference between

them. In Fig. 17(b) the collecting currents are α times as large as the total emitter and collector currents, respectively. A simple calculation shows that the two versions are formally equivalent, if the relations

$$I_{EF}(s) = \frac{I'_E(s)}{1 - \alpha_N(s)\alpha_I(s)} \quad (38a)$$

and

$$I_{CF}(s) = \frac{I'_C(s)}{1 - \alpha_N(s)\alpha_I(s)} \quad (38b)$$

are satisfied. A glance at the equations for the voltage sources in Fig. 17 reveals that the two versions could not be completely equivalent, unless either I_{EF0} and I_{CF0} or I_{E0} and I_{C0} would be considered frequency dependent. Due to the approximative nature of both models, this is normally not done.

From both Fig. 17(a) and (b) the respective four-pole equations, on which the model is based, can readily be derived in terms of electrical parameters:

$$I_E(s) = I_{EF}(s) - \alpha_I(s)I_{CF}(s) = \frac{I'_E(s) - \alpha_I(s)I'_C(s)}{1 - \alpha_N(s)\alpha_I(s)} \quad (39a)$$

$$I_C(s) = \alpha_N(s)I_{EF}(s) - I_{CF}(s) = \frac{\alpha_N(s)I'_E(s) - I'_C(s)}{1 - \alpha_N(s)\alpha_I(s)}. \quad (39b)$$

After substituting the expressions for the junctions one obtains for the *steady-state* case the well-known Ebers-Moll equations

$$I_E = \frac{I_{E0}}{1 - \alpha_{N0}\alpha_{I0}} [\exp(\lambda V_e) - 1] - \frac{\alpha_{I0}I_{C0}}{1 - \alpha_{N0}\alpha_{I0}} [\exp(\lambda V_e) - 1] \quad (40a)$$

$$I_C = \frac{\alpha_{N0}I_{E0}}{1 - \alpha_{N0}\alpha_{I0}} [\exp(\lambda V_e) - 1] - \frac{I_{C0}}{1 - \alpha_{N0}\alpha_{I0}} [\exp(\lambda V_e) - 1]. \quad (40b)$$

5.1 Comparison Between the Ebers-Moll and the Linvill Model

Comparing (40) with (33) and (34) for the steady-state solution leads to the following relations:

$$\frac{eAD_p p_{n0}}{W} = \frac{\alpha_{N0}I_{E0}}{1 - \alpha_{N0}\alpha_{I0}} = \frac{\alpha_{I0}I_{C0}}{1 - \alpha_{N0}\alpha_{I0}}. \quad (41)$$

A corresponding comparison for the ac case would yield the same expression as in (41), except that α_{N0} and α_{I0} would have to be replaced by their frequency dependent forms. Since the left side term of (41)

is frequency independent, no rigorous equality exists between the Linvill model and any of the two versions of the Ebers-Moll model under ac conditions. In the Ebers-Moll model, the junction voltage is a function of the total diode current [being different in the two versions of Fig. 17(a) and (b)]; in the Linvill model it is only a function of the resistive component of the diode current in Fig. 17(a); this component equals the current through the combination which is proportional to the carrier density p . It can be shown that the correct solution in which the junction voltage is a function of the carrier density directly at the junction, lies between these two cases but much closer to the lumped Linvill simulation. The discrepancy, mentioned here, affects only the junction voltages and does not appear in many analyses that use piecewise linearity.

$\alpha_N(s)$ and $\alpha_I(s)$ can be expressed in terms of the physical parameters by comparing (39) and (33) separately for the normal operation ($I_{CF} = 0$) and for the inverse operation ($I_{EF} = 0$). Subsequent conversion of the α 's into β 's yields

$$\beta_N(s) = \frac{\alpha_N(s)}{1 - \alpha_N(s)} = \frac{\beta_{N0}}{1 + \frac{s}{\omega_{\beta N}}} = \frac{A\tau_1 D_p / A_1 W W_1}{1 + s\tau_1} \quad (42)$$

$$\beta_I(s) = \frac{\alpha_I(s)}{1 - \alpha_I(s)} = \frac{\beta_{I0}}{1 + \frac{s}{\omega_{\beta I}}} = \frac{A\tau_2 D_p / A_2 W W_2}{1 + s\tau_2}, \quad (43)$$

where

$$\omega_{\beta N} = \frac{\omega_{\alpha N}}{1 + \beta_{N0}} = \frac{1}{\tau_1} \quad (44)$$

and

$$\omega_{\beta I} = \frac{\omega_{\alpha I}}{1 + \beta_{I0}} = \frac{1}{\tau_2}. \quad (45)$$

By definition we shall call in later sections

$$\tau_1 \equiv \tau_{BN} \quad (46)$$

and

$$\tau_2 \equiv \tau_{BI} \quad (47)$$

5.2 A Better Approximation for the α Frequency Dependence in the Ebers-Moll Model

Pritchard⁴¹ has first suggested that a better approximation for the 3-dB cut-off points of the α 's or β 's are obtained if one inserts a factor

1.22 into the corresponding equations, i.e.,

$$\alpha_N = \frac{1}{\cosh \gamma \Delta x} \approx \frac{1}{1 + \frac{1.22j\omega}{\omega_{\text{cut-off measured}}}}. \quad (48)$$

This can readily be calculated from the fall-off behavior of the cosh expression while assuming $\beta_{N0} \gg 1$.

The same factor 1.22 appears in the corresponding expressions for α_I , β_N and β_I . It is evident from (48) that this problem can be reduced to a matter of defining $\omega_{\alpha N}$. For less ideal transistors the factor is usually between 1 and 1.22.

Higher-order approximations to the hyperbolic function commonly use two pole expressions or delay-producing excess phase terms.

VI. THE CHARGE-CONTROL TRANSISTOR MODEL

In analogy to the diode charge-control model we can establish a charge-control equivalent circuit for the transistor. To that end, we want to express all parameters in terms of the charge in the base.

Three approaches appear feasible: A lumped Linvill model can be labeled in such a way that all elements appear as functions of charges rather than integrated charge densities of the form $p\Delta x$. The two are proportional; the proportionality factors are of the form "electron charge times area". Most of the special circuit components of the Linvill model become current or voltage sources in the charge-control version. This procedure of converting a Linvill model into a charge control model can readily be applied to higher-order Linvill models.

A second approach is to use the Ebers-Moll principle of superposition whereby two charge-control diode models plus the corresponding collecting currents can be joined to form the transistor model. This approach is essentially limited to the first order of approximation. Two seemingly different, but fully equivalent and easily convertible models result.

The third and classic approach to charge-control theory, originated by Beaufoy and Sparkes,³ is basically mathematical. Through integration of the continuity equation the carrier density as a variable is replaced by the total charge in the base. Certain simplifying assumptions have to be made to obtain a relation between currents and charges. In essence, these assumptions are equivalent to the approximations implied in the first-order Linvill and Ebers-Moll models as well as in the first-order charge-control equivalent circuits to be described below.

Some equivalent circuits have been presented in the literature, but they were less rigorous than the circuits described below in the sense that they cannot be used as complete networks. Additional knowledge of the physics of the device is required to use these models. Extension to higher-order models in the Beaufoy-Sparkes approach is accomplished through increased physical and mathematical complexity and not through more complex network topology as in the Linvill model or the charge-control model to be described.

6.1 The π -Version (Base-Controlled Version) of the Charge-Control Equivalent Circuit

In the lumped Linvill π -model of Fig. 16, the base charge distribution is approximated by two levels of carrier density. This is illustrated in Fig. 18. $p_1(t)$ is constant over the length $\Delta x = W_1$, and $p_2(t)$ is constant over the length W_2 , where $W_1 + W_2 = \text{basewidth } W$. The total charge in the two sections follows with (34a) and (34b) as

$$q_1(t) = p_1(t)W_1eA_1 = p_{n0}W_1eA_1[\exp\{\lambda v_c(t)\} - 1] \quad (49)$$

$$q_2(t) = p_2(t)W_2eA_2 = p_{n0}W_2eA_2[\exp\{\lambda v_c(t)\} - 1]. \quad (50)$$

Using the definitions of the elements given in Fig. 16, one can calculate from the Linvill model in Fig. 16 the currents through H_{e1} , H_{e2} , and H_d and obtains

$$i_1(t) = H_{e1}p_1(t) = \frac{eA_1W_1}{\tau_1}p_1(t) = \frac{q_N(t)}{\tau_1} \equiv \frac{q_N(t)}{\tau_{BN}} \quad (51)$$

$$i_5(t) = H_{e2}p_2(t) = \frac{eA_2W_2}{\tau_2}p_2(t) = \frac{q_I(t)}{\tau_2} \equiv \frac{q_I(t)}{\tau_{BI}} \quad (52)$$

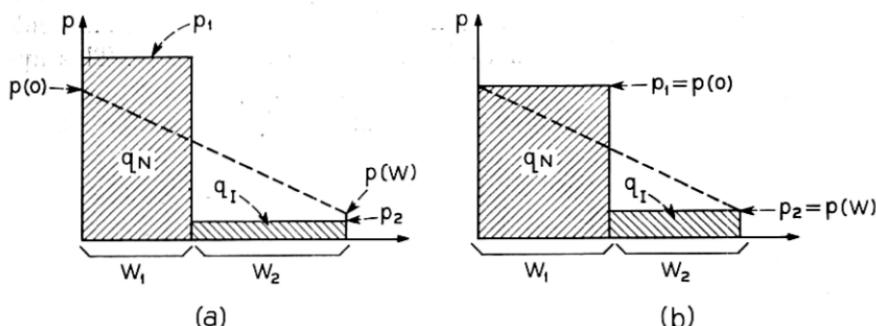


Fig. 18—Excess carrier distribution in the transistor base as used or implied in all first-order transistor models. (a) General case $p_1 \neq p(0)$, $p_2 \neq p(W)$. (b) Commonly used choice $p_1 = p(0)$, $p_2 = p(W)$.

$$i_3(t) = H_d[p_1(t) - p_2(t)]$$

$$= \frac{eAD_p}{W} (p_1(t) - p_2(t)) = \frac{D_p A}{W} \left(\frac{q_N(t)}{W_1 A_1} - \frac{q_I(t)}{W_2 A_2} \right). \quad (53a)$$

Using the more familiar Ebers-Moll notations and the relations found earlier in (42) through (47), i_3 can be expressed as

$$i_3(t) = \frac{\beta_{N0}}{\tau_{BN}} q_N(t) - \frac{\beta_{I0}}{\tau_{BI}} q_I(t). \quad (53b)$$

Thus, the three current sources in the charge-control model are found and related to the Linvill model by means of (51) through (53).

The remaining two branch currents i_2 and i_4 are obtained from Fig. 16 as

$$i_2(t) = eA_1 W_1 \frac{dp_1(t)}{dt} = \frac{dq_N(t)}{dt} \quad (54)$$

$$i_4(t) = eA_2 W_2 \frac{dp_2(t)}{dt} = \frac{dq_I(t)}{dt}. \quad (55)$$

These equations describe two stores S_N and S_I , whose properties have been described in Section 2.4.

The conversion between the two models will be summarized and further discussed in Section 6.4.

The voltage sources for the junctions follow from (34), (51), and (52) as

$$\lambda_{v_e}(t) = \ln \left(1 + \frac{p(0,t)}{p_{n0}} \right) = \ln \left(1 + \frac{q_N(t)}{p_{n0} W_1 e A_1} \right) \quad (56)$$

$$\lambda_{v_c}(t) = \ln \left(1 + \frac{p(W,t)}{p_{n0}} \right) = \ln \left(1 + \frac{q_I(t)}{p_{n0} W_2 e A_2} \right). \quad (57)$$

With the help of (41) through (47) that link the constants used in the Ebers-Moll model to those in the Linvill Model, (56) and (57) can be rewritten as

$$\lambda_{v_e}(t) = \ln \left[1 + \frac{q_N(t)}{\tau_{BN}} \times \frac{1 + \beta_{N0}}{I_{E0}/(1 - \alpha_{N0}\alpha_{I0})} \right] \quad (58)$$

$$\lambda_{v_c}(t) = \ln \left[1 + \frac{q_I(t)}{\tau_{BI}} \times \frac{1 + \beta_{I0}}{I_{C0}/(1 - \alpha_{N0}\alpha_{I0})} \right]. \quad (59)$$

(The reader may prefer to derive the constants directly from the steady-state Ebers-Moll model in (40) by considering the limiting

cases $v_s = 0$ and $v_c = 0$.) With the addition of (58) and (59) the equivalent circuit in Fig. 19(a) is completely defined.

It is customary and useful in charge-control work to define additional parameters τ_{BN} , τ_{CN} , τ_{EI} , τ_{CI} . We define their relationship as follows:

$$\frac{\tau_{BN}}{\beta_{N0}} \equiv \frac{\tau_{EN}}{\alpha_{N0}} \equiv \tau_{CN} \quad (60)$$

$$\frac{\tau_{BI}}{\beta_{I0}} \equiv \frac{\tau_{CI}}{\alpha_{I0}} \equiv \tau_{EI} \quad (61)$$

Since, as usual,

$$\alpha_{N0} = \frac{\beta_{N0}}{1 + \beta_{N0}} \quad (62)$$

and

$$\alpha_{I0} = \frac{\beta_{I0}}{1 + \beta_{I0}}, \quad (63)$$

it also follows that

$$\frac{1}{\tau_{EN}} = \frac{1}{\tau_{BN}} + \frac{1}{\tau_{CN}} \quad (64)$$

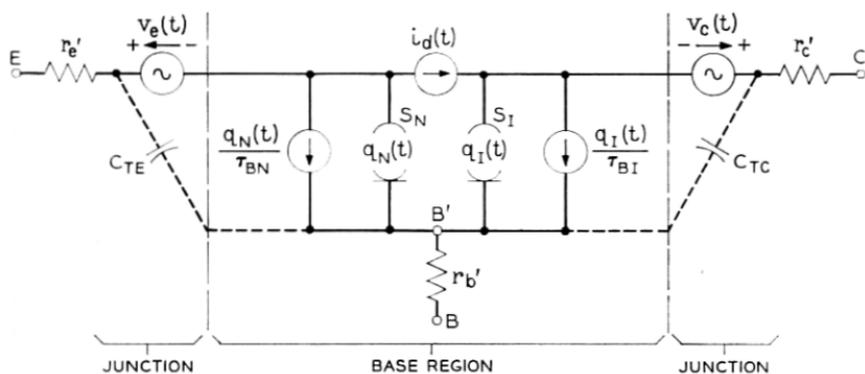
and

$$\frac{1}{\tau_{CI}} = \frac{1}{\tau_{BI}} + \frac{1}{\tau_{EI}} \quad (65)$$

(The classic definition of these time constants after Beaufoy-Sparkes will be discussed in Section 6.5.) The subscripts B , E , and C stand for base, emitter, and collector, respectively. The subscripts N and I on the time constants and on the charges have been chosen to indicate the normal and inverse transistor operation. Many authors^{9,10,11} use F (forward) and R (reverse) instead of N and I . Since F and R are commonly reserved for diode forward and reverse currents, and since such currents can flow in each of the two junctions, the different notations N and I , as proposed by Ebers and Moll, appear more appropriate.

In Appendix B, the notations for the stored charges and the time constants used in this paper are related to those used in a recent book published by the Semiconductor Electronics Education Committee;¹¹ they are also compared with the notations and definitions used by Beaufoy and Sparkes.

The additional time constants do not add any additional degree of freedom. But it is advantageous to use "base" notations when controlling base current, i.e., in common-emitter or common-collector



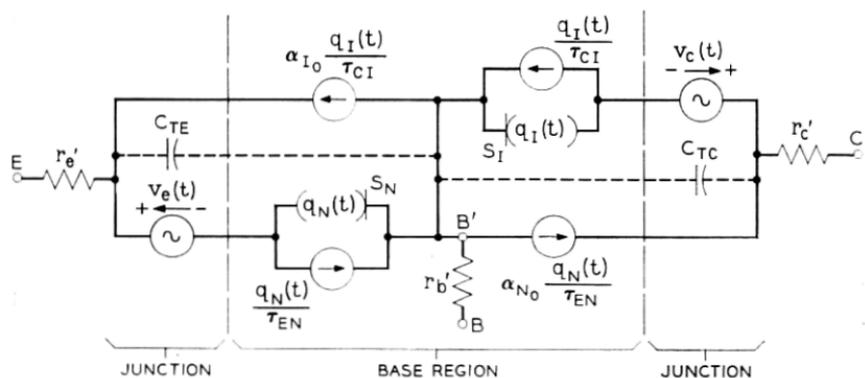
WHERE:

$$i_d(t) = \beta_{N_0} \frac{q_N(t)}{\tau_{BN}} - \beta_{I_0} \frac{q_I(t)}{\tau_{BI}} = \frac{q_N(t)}{\tau_{CN}} - \frac{q_I(t)}{\tau_{EI}}$$

$$v_e(t) = \frac{kT}{e} \ln \left[1 + \frac{q_N(t)(1 + \beta_{N_0})}{\tau_{BN} I_{E0} / (1 - \alpha_{N_0} \alpha_{I_0})} \right]$$

$$v_c(t) = \frac{kT}{e} \ln \left[1 + \frac{q_I(t)(1 + \beta_{I_0})}{\tau_{BI} I_{C0} / (1 - \alpha_{N_0} \alpha_{I_0})} \right]$$

(a)



WHERE:

$$v_e(t) = \frac{kT}{e} \ln \left[1 + \frac{q_N(t)}{\tau_{EN} I_{E0} / (1 - \alpha_{N_0} \alpha_{I_0})} \right]$$

$$v_c(t) = \frac{kT}{e} \ln \left[1 + \frac{q_I(t)}{\tau_{CI} I_{C0} / (1 - \alpha_{N_0} \alpha_{I_0})} \right]$$

(b)

Fig. 19—Charge-control equivalent circuit for transistor in first-order approximation, shown in two equivalent and convertible forms: (a) π -version, Linvill type, (b) T -version, Ebers-Moll type.

connection, and to use "emitter" and "collector" notations when emitter and collector forward currents are injected, such as in common-base connection.

The model obtained in Fig. 19(a) maintains the most valuable property found in the Linvill model, namely the close relationship between the physical processes and the circuit elements. For example, τ_{BN} and τ_{BI} are the recombination times on the emitter and collector side, respectively, and τ_{CN} and τ_{EI} are the diffusion time constants for the charges injected from the two junctions. Junctions and base are represented by individual sections within the equivalent circuit. This separation makes it easy to expand the model and to take other effects into account.

6.2 The *T*-Version (Emitter-Collector Controlled Version) of the Charge-Control Equivalent Circuit

In complete analogy with the derivation of the Ebers-Moll model in Fig. 17(a) we can take two diode charge-control models back to back and add current sources on the collector and emitter side, which are α_{N0} and α_{I0} times the diode currents.

For the simulation of the junctions, we are left with two alternatives: One is to convert the corresponding expressions in the Ebers-Moll model in Fig. 17(a) into charge functions; the other is to use the expressions in the charge-control π -model (which are equivalent to the Linvill model), but replace the β -notations by α -notations according to (60) through (63). The first-mentioned alternative for simulating the voltage sources would amount to simply substituting the diodes from Fig. 17(a) for the voltage sources in Fig. 19(b). The property of charge control would not be simulated. The second procedure is therefore chosen; it yields

$$v_e(t) = \frac{1}{\lambda} \ln \left(1 + \frac{q_N(t)}{\tau_{EN} I_{E0} / (1 - \alpha_{N0} \alpha_{I0})} \right) \quad (66)$$

$$v_c(t) = \frac{1}{\lambda} \ln \left(1 + \frac{q_I(t)}{\tau_{CI} I_{C0} / (1 - \alpha_{N0} \alpha_{I0})} \right). \quad (67)$$

Thus, the equivalent circuit in Fig. 19(b) is obtained.

As far as the current relations in the models are concerned, the main difference between the charge-control *T*-model and the Ebers-Moll model is that the frequency dependence is simulated by a mathematical expression in the Ebers-Moll model, and by an additional network branch in the charge-control model. This is analogous to the option existing in small signal models where one can represent the frequency dependence either with an appropriate RC circuit, holding α_0 frequency

independent, or alternatively, with a frequency dependent α in the collecting current source.

The equivalency of the charge-control model with the Ebers-Moll model exists only for the relations between the currents. It can be shown readily that the following relations must be satisfied to establish equivalency:

$$(i) \quad \tau_{EN} = \frac{1}{\omega_{\alpha N}} \quad (68)$$

$$(ii) \quad \tau_{CI} = \frac{1}{\omega_{\alpha I}} \quad (69)$$

$$(iii) \quad \tau_{BN} = \frac{1}{\omega_{\beta N}} = \frac{1 + \beta_{N0}}{\omega_{\alpha N}} \quad (70)$$

$$(iv) \quad \tau_{BI} = \frac{1}{\omega_{\beta I}} = \frac{1 + \beta_{I0}}{\omega_{\alpha I}} \quad (71)$$

All ω 's must be replaced in these equations by the corresponding $\omega/1.22$ if the ω 's correspond to the measured 3-dB gain fall-off points, and if the better approximation mentioned in Section 5.2 is to be included in the Ebers-Moll model, provided the particular transistor follows the underlying theory well enough.

6.3 Conversion Between the Two Proposed Charge-Control Models

The identity between the two charge-control models, presented in Figs. 19(a) and (b) can best be proven by converting one model into the other.

To convert the π -model into the T -model one first adds a branch current i_d both into and out of the base point B' and splits i_d up into its two components. The resulting circuit diagram is shown in Fig. 20. The two parallel current sources proportional to $q_N(t)$ on the left side can then be combined into one current source. Likewise, the two current sources proportional to $q_I(t)$ on the right side can be combined. If with the help of (60) through (63), one now relabels all current sources in terms of α_N and α_I instead of β_N and β_I and extends the upper current sources beyond the voltage sources, one obtains the model in Fig. 19(b).

6.4 Summary of the Conversion Equations between the Linvill and the Charge-Control Model

6.4.1 Conversion Equations for the First-Order Transistor Model

In (49) through (59), the charge-control π -model was derived from the Linvill model. With the help of the defining equations for the

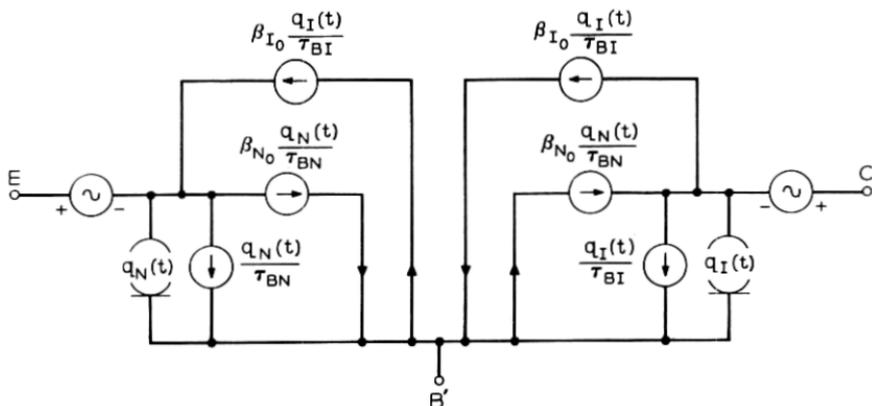


Fig. 20—Intermediate step used in the conversion from the π to the T charge-control model, demonstrating equivalency between these two models.

Linivill model elements, the constants in the charge-control model can be calculated as a function of the Linivill combinances, storances, and diffusances. For the relation between the Linivill π -model of Fig. 16 and the charge-control π -model of Fig. 19(a), such calculations yield

$$\tau_{BN} = \frac{S_1}{H_{e1}} \quad (72)$$

$$\tau_{BI} = \frac{S_2}{H_{e2}} \quad (73)$$

$$\tau_{CN} = \frac{S_1}{H_d} \quad (74)$$

$$\tau_{EI} = \frac{S_2}{H_d} \quad (75)$$

$$I_{E0} = p_{N0} \frac{H_{e1}H_{e2} + (H_{e1} + H_{e2})H_d}{H_{e2} + H_d} \quad (76)$$

$$I_{C0} = p_{N0} \frac{H_{e1}H_{e2} + (H_{e1} + H_{e2})H_d}{H_{e1} + H_d} \quad (77)$$

Note that (72) through (75) reveal that the five parameters in the Linivill model lead to only four parameters in the charge-control model. The one degree of freedom that is lost in the charge-control model is the conversion factor from current to carrier density; conversion of the charge-control model into a Linivill model is only possible, if one of the five Linivill parameters is known. This is tantamount to saying that one needs some information on the geometry of the device

such as the value of one, or in low-gain units, both of the two base volume sections A_1W_1 and A_2W_2 .

6.4.2 Conversion Between the Linvill and the Charge-Control Model for an Arbitrary Number of Base Sections

In higher-order approximations for diodes or transistors, the parameters of the Linvill and the charge-control models, as defined in Fig. 21, are related by the equations

$$\tau_1 = \frac{S_1}{H_{c1}}, \quad \tau_2 = \frac{S_2}{H_{c2}}, \quad \tau_\mu = \frac{S_\mu}{H_{c\mu}} \quad (78)$$

$$\tau_{12a} = \frac{S_1}{H_{d12}}, \quad \tau_{\mu\nu a} = \frac{S_\mu}{H_{d\mu\nu}} \quad (79)$$

$$\tau_{12b} = \frac{S_2}{H_{d12}}, \quad \tau_{\mu\nu b} = \frac{S_\nu}{H_{d\mu\nu}} \quad (80)$$

$$q_{10} = S_1 p_{n0} \quad (81)$$

$$q_{m0} = S_m p_{n0} \quad (82)$$

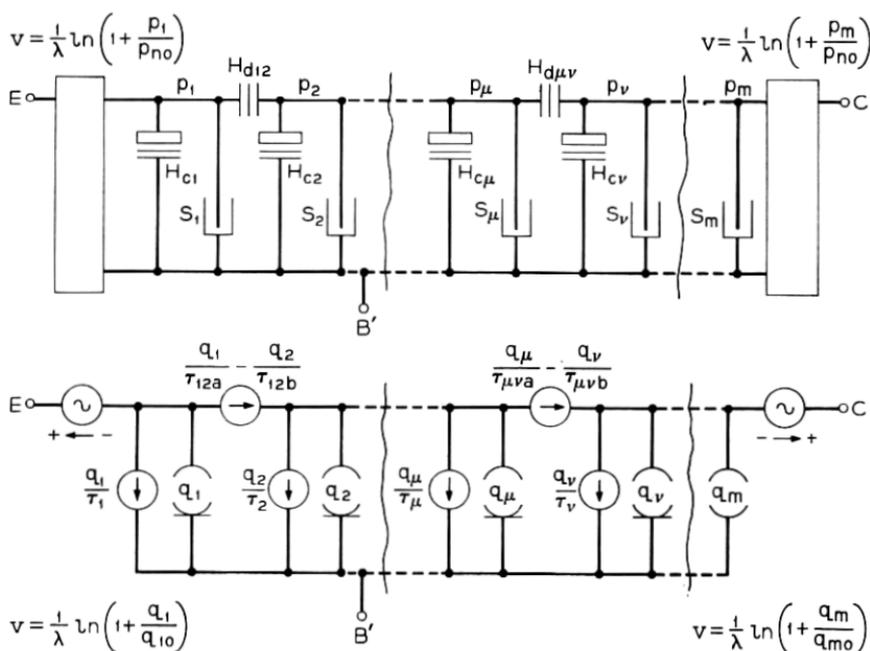


Fig. 21—A Linvill and a charge-control equivalent circuit for a junction and part of a multisectional n -region, with indication of the notations used in converting one model into the other.

6.5 The Transistor in Saturation

In all lumped transistor models (Linville, Ebers-Moll, or charge-control type) the charge in the base is explicitly or implicitly broken up into the charge q_N injected from the emitter under normal operation and the charge q_I injected from the collector under inverse operation, e.g., in saturation. This was illustrated in Fig. 18.

When the transistor is overdriven into saturation with a base current larger than $I_{C \text{ sat}}/\beta_{N0}$, the two stores q_N and q_I do not change by exactly equal amounts, i.e.,

$$\frac{dq_N}{di_{B \text{ excess}}} \neq \frac{dq_I}{di_{B \text{ excess}}}$$

where, by definition,

$$i_{B \text{ excess}} \equiv i_B - \frac{I_{C \text{ sat}}}{\beta_{N0}}. \quad (83)$$

This is illustrated in Fig. 22. It can be calculated from any of the two models of Fig. 19 that, under steady-state conditions, the excess charges in the two stores are related to the excess base current by the expressions

$$\Delta Q_I = Q_I = \frac{\alpha_{N0} \tau_{CI}}{1 - \alpha_{N0} \alpha_{I0}} I_{B \text{ excess}} \quad (84)$$

$$\Delta Q_N = \frac{\tau_{EN}}{1 - \alpha_{N0} \alpha_{I0}} I_{B \text{ excess}}. \quad (85)$$

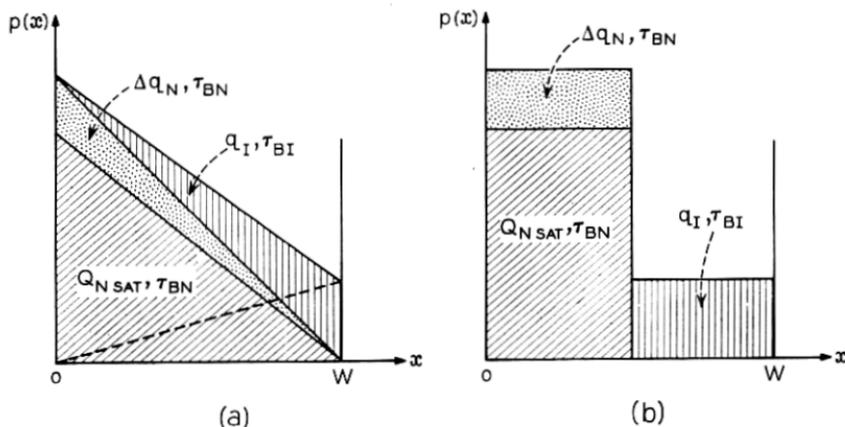


Fig. 22—The transistor in saturation. (a) Actual distribution of excess minority carriers. (b) Lumped approximation. The π and the T models use q_N and q_I with lifetimes τ_{BN} and τ_{BI} ; the Beaufoy-Sparkes model uses $Q_{N \text{ SAT}}$ and $q_{BS} = \Delta q_N + q_I$ with lifetimes τ_{BN} and τ_S , where τ_S is as defined in (88).

From this it follows that

$$\frac{\Delta Q_N}{Q_I} = \frac{\tau_{EN}}{\alpha_{N0}\tau_{CI}} = \frac{\tau_{CN}}{\alpha_{I0}\tau_{EI}} = \frac{\omega_{\alpha I}}{\alpha_{N0}\omega_{\alpha N}} \neq 1. \quad (86)$$

Since $\alpha_{I0} < 1$, the charge-up ratio is somewhat larger than the ratio of the diffusion times of the normal and inverse transistor.

The rate at which the two stores charge and discharge in saturation because of external step disturbances is described by the eigenfunction of the system

$$s^2 + s \left[\frac{1 + \beta_{N0}}{\tau_{BN}} + \frac{1 + \beta_{I0}}{\tau_{BI}} \right] + \frac{1 + \beta_{N0} + \beta_{I0}}{\tau_{BN}\tau_{BI}} = 0. \quad (87)$$

If $\beta_{N0}\tau_{BI}/\tau_{BN} \gg 1$, the two poles are far apart in frequency. Furthermore, the high frequency pole contributes in most nonoscillatory cases little to the overall response. The higher pole or, alternatively, the s^2 term can then be neglected and a single time constant results described by

$$\tau_S = \frac{(1 + \beta_{N0})\tau_{BI} + (1 + \beta_{I0})\tau_{BN}}{1 + \beta_{N0} + \beta_{I0}} = \frac{\tau_{EN} + \tau_{CI}}{1 - \alpha_{N0}\alpha_{I0}}. \quad (88a)$$

Using ω -notation, one obtains the expression given by Ebers and Moll

$$\tau_S = \frac{\omega_{\alpha N} + \omega_{\alpha I}}{\omega_{\alpha N}\omega_{\alpha I}(1 - \alpha_{N0}\alpha_{I0})}. \quad (88b)$$

For large β_N and small β_I , τ_S is approximately equal to

$$\tau_S \approx \tau_{BI} \left(1 + \frac{\tau_{EN}}{\tau_{CI}} \right). \quad (88c)$$

If $\tau_{EN} \ll \tau_{CI}$, i.e., if the carriers diffuse more easily from the emitter to the collector than vice versa, then the recombination rate τ_{BI} on the collector side is mainly responsible for the overall decay of the excess base charge.

6.5.1 Storage Time Calculations

For first-order storage time calculations with the transistor driven into a steady-state saturation condition by means of an excess base current $I_{B \text{ excess}}$, one can simplify the charge-control model to the one shown in Fig. 23. Storage time is the time it takes to deplete the store which is charged to a value of

$$Q_{BS} = Q_I + \Delta Q_N = I_{B \text{ excess}}\tau_S = I_{B \text{ excess}} \frac{\tau_{EN} + \alpha_{N0}\tau_{CI}}{1 - \alpha_{N0}\alpha_{I0}} \quad (89)$$

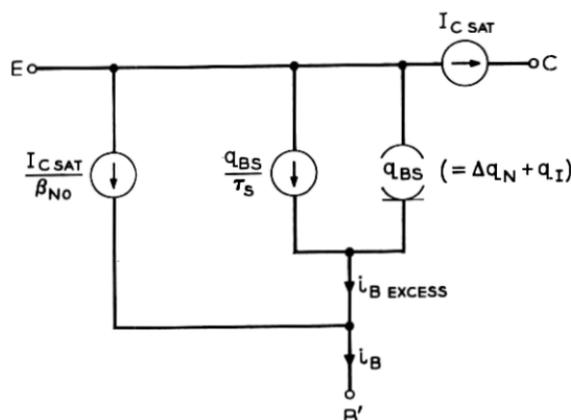


Fig. 23—Single-pole equivalent circuit for saturated transistor after Beaufoy-Sparkes.

while, at the same time, this charge is exposed to an effective recombination time of τ_S as given in (88). In this form the model is identical with the classic Beaufoy-Sparkes model for the saturated transistor.

In the general case one must refer to the complete model.

6.6 The Beaufoy-Sparkes Charge-Control Model

In the classic approach to charge-control theory, the starting point is, like in the diode case, the integration of the continuity equation (8). In comparison with the integration performed for the diode in Section 2.3.1, the upper limit of integration has to be changed to $x = W$. The expression

$$i_p(0, t) - i_p(W, t) = \frac{dq_N(t)}{dt} + \frac{q_N(t)}{\tau_{BN}}$$

obtained from the integration becomes that for the base current under normal, nonsaturated operation:

$$i_B(t) = \frac{dq_N(t)}{dt} + \frac{q_N(t)}{\tau_{BN}}; \quad (90)$$

$q_N(t)$ is the total charge in the base. The next step being made is again the approximative assumption that the carriers redistribute themselves so quickly, that we can always assume steady-state distribution. (See also Section 2.4.) Mathematically, this means that in normal transistor operation both $p(0, t)$ and $i_c(t)$ are proportional to the base charge $q_N(t)$. It can be seen from Fig. 19 that the same assumption

is implied in the two charge-control models presented there, despite the fact that they were derived through entirely different procedures. (Instantaneous redistribution is, however, not implied in models that use more than one π or T section for representing the base.)

The time constants are defined in the classic charge-control theory on the basis of the above-mentioned assumption of instantaneous carrier redistribution, i.e., in steady state

$$\tau_{BN} = \frac{Q_N}{I_{BN}}, \quad \tau_{CN} = \frac{Q_N}{I_{CN}}, \quad \tau_{EN} = \frac{Q_N}{I_{EN}} \quad (91a)$$

and dynamically

$$i_{BN} = \frac{q_N}{\tau_{BN}} + \frac{dq_N}{dt}, \quad i_{CN} = \frac{q_N}{\tau_{CN}}, \quad i_{EN} = i_{BN} + i_{CN}. \quad (91b)$$

The remaining three time constants can be defined likewise for the inverse transistor. Narud, et al⁹ have used such definitions in an equivalent circuit for the charge-to-current relations in the transistor. Beaufoy and Sparkes discussed this possibility in their original paper³ but chose to present two separate charge-control models, one for the normal active operation and one for saturation. In normal operation, the charge q_N called " q_B " is bounded by the value reached at the edge of saturation:

$$q_B \leq Q_{N \text{ sat}}, \quad \text{where} \quad Q_{N \text{ sat}} = \frac{I_{C \text{ sat}}}{\beta_{N0}} \tau_{BN}.$$

In their saturated model, all excess charge which exceeds $Q_{N \text{ SAT}}$ is lumped into one store rather than two; this charge " q_{BS} " has a lifetime $\tau_S = q_{BS}/i_{B \text{ excess}}$ which is identical with τ_S as defined in (88).

By lumping $\Delta q_N \equiv q_N - Q_{N \text{ SAT}}$ and q_I into q_{BS} , the Beaufoy and Sparkes arrangement provides only a minor short cut for calculating storage time, while sacrificing not only some of the physical understanding, but also the possibility of mutual conversion with the other models. No relations have been given that would express the junction voltages in terms of the charges in the stores, and recourse must be taken to the Boltzmann equation to find expressions for the voltages.

Throughout the literature the charge-control concept has been used primarily as a mathematical-physical tool. Extensions to higher-order effects are usually made by improving the simple continuity and transport equations stated in (8) and (9) and then carrying out the corresponding integration for the specific application.

VII. SOME REMARKS ABOUT THE EQUIVALENT CIRCUIT TYPE CHARGE-CONTROL APPROACH

7.1 Use of the Charge-Control Models

It is believed that the first-order approximation to a charge-control model in the form presented for the transistor in Fig. 19, combines the main advantages of the three basic approaches to modeling. The π and the T -models are as easy to handle from an equivalent circuit point of view as the Ebers-Moll model. Instead of frequency dependent α 's and β 's, one additional current branch exists for each side of the transistor. Circuit problems are solved in the usual way by means of loop and node equations. The charges q_N and q_I appear as circuit parameters which can either be calculated, if so desired, or else, eliminated in the algebraic process. The store elements in the circuit are clearly defined by the circuit properties given in (22).

The model provides all the features that have made the charge-control concept attractive in the past: quick estimates of switching times by integrating the base current and equating with the charges needed to fill and deplete the stores. The general base current equations of charge control are directly read from Fig. 19(a) as

$$i_B = \frac{q_N}{\tau_{BN}} + \frac{dq_N}{dt} + \frac{q_I}{\tau_{BI}} + \frac{dq_I}{dt} + \frac{C_{TE} dv_e}{dt} + \frac{C_{TC} dv_c}{dt}. \quad (92)$$

Of course, there is no restriction to step inputs. The chore of calculating responses to a nonstep input is transformed through the model into a circuit problem. In complex cases the help of a computer will be required.

Due to its direct relationship to the Linvill model, the charge-control model lends itself quite readily to extensions based on the physics of the device. This will be discussed in Section 7.3.

7.2 Piecewise Linear Approximation of the Logarithmic Voltage Function

The logarithmic voltage functions for the junctions are of the form

$$v = \frac{1}{\lambda} \ln \left[1 + \frac{q/\tau}{I_0/(1 - \alpha_{N0}\alpha_{I0})} \right]. \quad (93)$$

For most practical cases, this can be approximated by piecewise linear functions, like in the diode case of Fig. 10. Except for small values of q/τ , i.e., q/τ not $\gg I_0/(1 - \alpha_{N0}\alpha_{I0})$, one obtains

$$\frac{dv}{d(q/\tau)} = \frac{\tau}{\lambda q}. \quad (94)$$

Thus, the slope can be represented by a resistor $\tau/\lambda q$, which may, like in Section 2.4.4, be taken as the average value

$$\frac{dv}{d\left(\frac{q}{\tau}\right)} \approx \frac{\tau}{\lambda \bar{q}} \approx \frac{\tau}{\frac{1}{2}\lambda q_{\max}} = \frac{1}{\frac{1}{2}I_{\max}\lambda}, \quad (95)$$

where I_{\max} is the maximum forward junction current.

It can be shown that in models which use the exponential relationship, the expressions of the form $\ln(1+x)$ can be replaced by just $\ln x$ if one simulates the majority carrier currents by special current sources as follows:

$$\frac{1 - \alpha_{I0}}{1 - \alpha_{N0}\alpha_{I0}} I_{C0} \quad (\approx I_{C0}) \quad \text{from internal base to collector}$$

and

$$\frac{1 - \alpha_{N0}}{1 - \alpha_{N0}\alpha_{I0}} I_{E0} \quad (\approx 0) \quad \text{from internal base to emitter.}$$

This transformation is rigorous only at dc. However, in a piecewise linear analysis, as discussed above, the addition of one current source, namely I_{C0} , becomes mandatory if the model is to be valid at very small collector currents.

7.3 Extensions of the Model

7.3.1 Path Impedances, Leakage Resistors

Like in the Linvill model, junctions and base material are clearly separated in the charge-control model. Therefore, it is a straightforward procedure to add series path resistors, series inductances, or leakage resistances to models like the ones in Figs. 9 or 19.

7.3.2 Junction Capacitors

It has been indicated by the dashed lines in Figs. 9 and 19 how the junction capacitances are to be incorporated into the model. They are properties of the junction, but their currents flow as majority carrier currents through the bulk material. Hence, in Fig. 9, for example, they must be connected across the whole n-region. (Connecting directly across the voltage source would have no effect on the external properties.) In Fig. 19 they lead to the internal base point.

7.3.3 Higher Order than π -Transistor Models

Another desirable expansion may be to replace the π structure of Fig. 19(a) by a double π or by some other higher-order approximation

to the original differential "transmission line". This is of special importance, if emphasis is to be placed on charge redistributions in the base. By extending the model in such a way, the restricting assumption of instantaneous carrier redistribution is no longer implied. A qualitative example of an elaborate planar or mesa transistor model is given in Fig. 24.

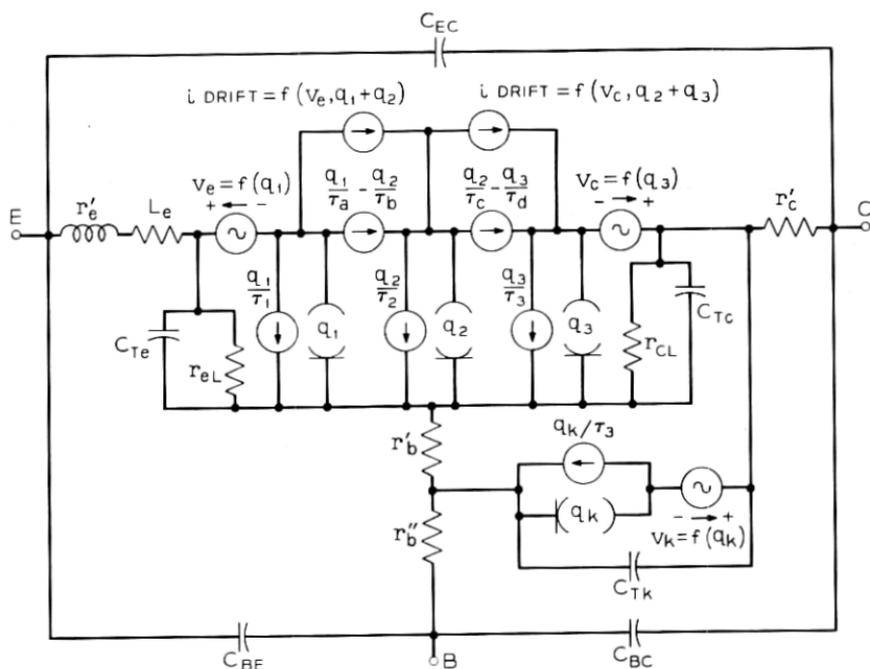


Fig. 24—Example of an elaborate high-frequency planar or mesa transistor equivalent circuit.

7.3.4 Drift Fields

If the charge-control model under consideration is being developed on the basis of physical phenomena such as in the model of Fig. 19(a), the contribution from drift effects may be represented in the same way as has been proposed by Linvill [Ref. 7, Sections 2, 3]. As a direct consequence of the transport equation (2), drift can be represented by a current source added in parallel to the diffusion current source. In terms of the r - g - c transmission line representation, discussed earlier, drift consideration amounts to a resistor in parallel with the series diffusance resistor r . This was used in a recent paper by Bloodworth.²⁶

Alternative methods of representing drift effects in conjunction with

conductivity modulation are presently being investigated; results will be published later.

7.3.5 Base Width Modulation

Base width modulation can be taken into account by replacing the basewidth, especially the collector section W_2 , by an expression $W_2(1 + \Delta)$, where Δ is some function of the junction voltage. Equations (52) and (53) show the dependence of the branch currents on W_2 , from which we can readily derive the required modification of the charge-control model in Fig. 19(a).

7.3.6 Multiple-Layer Devices, Multiple Storage

In accordance with Linvill's proposal, storage in more than one region can be simulated by considering that the minority carrier current on one side of a junction becomes the majority carrier current in the adjacent region. An example is shown in Fig. 25. This figure represents the charge-control model for an npn device. Avalanche

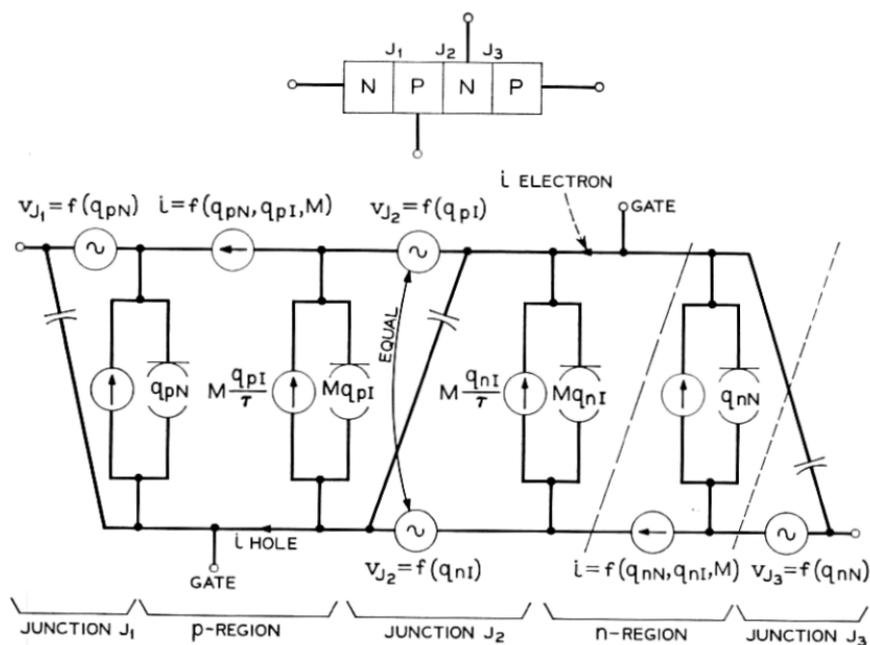


Fig. 25—Charge-control model for npn device. The model for an npn-transistor with storage in the collector can be obtained from this model by omitting the part to the right of the dashed or the dotted line.

multiplication may be considered by adding a multiplication factor M to all hole and electron currents flowing through the junction of interest (usually the center junction J_2), as indicated in Fig. 25. M is a function of the voltage across the junction.

By omitting the last electrode, an npn transistor with charge storage in the collector is obtained.

7.4 Establishment of a Large-Signal Model

The question naturally arises as to how one arrives at a numerical model. There is no clear-cut answer to this question, since the procedure to be taken depends on whether the informations available are predominantly physical or electrical in nature, whether a computer is available or not, etc. The following outline can, therefore, only be considered as a typical example.

(i) Obtain dc measurements which yield information on junction characteristics and electrode resistances. All measurements must be made under widely differing drive and load conditions.

(ii) Add information from device manufacturer to establish first-order dc model. (If necessary, convert to Linvill model.)

(iii) Add dynamic parameters, such as capacitances, as far as they are known and establish first-order dynamic model.

(iv) Use computer to improve numerical parameter values by matching frequency response curves or switching data in the active region with the model.

(v) Use computer to match large-signal nonlinear switching data.

(vi) Check model with switching measurements under different conditions, such as extremely low, extremely high and medium input and output impedance levels for various drive conditions. Improve model basically and numerically as necessary.

For purposes of *device* design, more emphasis is generally placed on the simulation of higher-order effects than in model building for *circuit* design where, especially in the case of integrated circuits, it is necessary to trade accuracy for simplicity.

VIII. CONCLUSIONS

The differential Linvill model stands out among all models as the most perfect one. Whereas the lumped Linvill model is the most suitable model for the device physicist, the circuit engineer usually prefers a more circuit oriented approach. It is felt that the charge-control *equivalent circuit* approach is well suited to combine the main advantages

of the various models: It is as easy to handle as the Ebers-Moll model, yet bears the close relationship to the physical phenomena of the device inherent in the Linvill model. It can also be extended easily to include higher-order physical phenomena.

Despite the difference in basic philosophy underlying the creation of each of the three classic modeling concepts (such as lumping, superposition, and integration), they are equivalent with respect to their current relations and to all dc properties. When compared at the same level of complexity, equivalency with respect to time dependency of the junction voltages exists between the two charge-control models and the Linvill model, but not between these models and the Ebers-Moll model.

In the Ebers-Moll model the effect which storage exercises on voltage cannot be included. The hybrid use of both time and frequency domains in the model may also be felt as a disadvantage in some applications.

At the first-order level of approximation, the charge-control equivalent circuit can be converted into the Ebers-Moll model, the Beaufoy-Sparkes model, and into the Linvill model (in the latter case the base volume is a constant which must also be known). Thus, the charge-control model serves as a bridge between the various models. This can be very useful in establishing a model, since both physical and electrical information can be incorporated easily into the model.

The diode charge-control model has been found very useful for analyzing storage effects in diodes.

Because of the close relationship to the physical phenomena in the device, extensions to larger complexity can readily be accomplished. We may interpret the charge control equivalent circuit as simply a circuit-oriented form of the Linvill model. The basic ideas and procedures that are used in converting diode and transistor linear models into equivalent charge-control models can be applied to many other semiconductor devices.

APPENDIX A

Switching Time Calculations for Ideal Charge-Storage-Step-Recovery Diodes

(Example for use of charge-control model)

A.1 *Equivalent Circuit* (See Fig. 26)

A.2 *Generator Source Current* (See Fig. 27)

A.3 *Diode Model* (See Fig. 28)

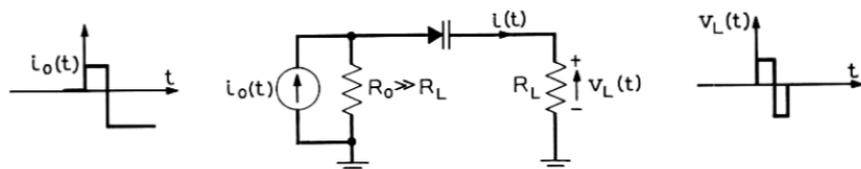


Fig. 26—Equivalent circuit for charge-control model.

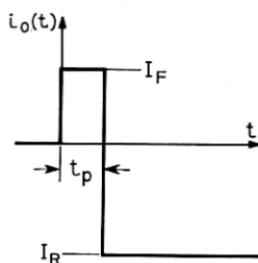


Fig. 27—Generator source current.

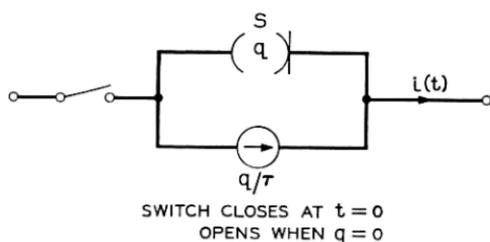


Fig. 28—Diode model.

A.4 Forward Operation

$$I(s) = \frac{Q(s)}{\tau} + sQ(s) = \frac{I_F}{s}$$

From this follows

$$Q(s) = \frac{I_F}{s\left(s + \frac{1}{\tau}\right)}$$

$$q(t) = \tau I_F [1 - \exp(-t/\tau)]$$

$$Q(t_p) = \tau I_F [1 - \exp(-t_p/\tau)]$$

A.5 Reverse Operation

For simplicity of writing, $t = t_p$ will now be referred to as $t = 0$:

APPENDIX B

Comparison of Notations

Table I lists comparisons of the notations used in this article. The first column lists the notations used in this article while column A lists those used by Beaufoy and Sparkes.³ Column B lists the notations used in *Physical Electronics and Circuit Models* by P. E. Gray, et al;¹¹ SEEC Series, 2.

TABLE I—COMPARISON OF NOTATIONS

This paper	A Beaufoy-Sparkes	B SEEC	
q_N	q_B (for $q_N < Q_{NSAT}$ only)	q_F	
q_I		q_R	
$\Delta q_N + q_I$	q_{BS}	$1 / \left(\frac{1}{\tau_{BF}} + \frac{1}{\tau_F} \right)$	
} where $\Delta q_N = q_N - Q_{NSAT}$			T_B
			T_C
τ_{BN}			T_E
τ_{CN}			$1 / \left(\frac{1}{\tau_{BR}} + \frac{1}{\tau_R} \right)$
τ_{EN}			
τ_{BI}			T_S
τ_{CI}			τ_{BF}
τ_{EI}			τ_F
τ_S			τ_{BR}
	τ_R		
	τ_{SL}		

LIST OF SYMBOLS

Lower-case letters are used for time variables, capital letters are used for steady-state values or Laplace transforms of values.

A, A_1, A_2	cross-sectional areas
$A_{11}, A_{12}, A_{21}, A_{22}$	four-pole parameters
a, b, c, K	constants
$c; \bar{c}$	analog capacitance; same per unit length
C_{Te}, C_{Tc}	emitter and collector junction capacitance, respectively
D_p	hole diffusion constant
D_n	electron diffusion constant
e	magnitude of electronic charge
E	electric field intensity
$g; \bar{g}$	analog shunt conductance; same per unit length

$\frac{H_c}{H_c}, H_{c1}, H_{c2}$	lumped combiances
$\frac{H_d}{H_d}$	combance per unit length
$\frac{H_d}{H_d}$	lumped diffusance
$\frac{1}{H_d}$	reciprocal of diffusance, per unit length
i_1, i_2, i_3, i_4, i_5	network branch currents
i_B	base current
$i_{B \text{ excess}}, I_{B \text{ excess}}$	excess base current in saturation
i_C, I_C	collector current
i_E, I_E	emitter current
I_F, I_R	forward and reverse diode switching current, respectively
i_n	electron current
i_p	hole current
I_S	diode saturation current
i'_C, I'_C, i'_E, I'_E	} network branch currents as defined in } Figs. 17(a) and 17(b)
$i_{CF}, I_{CF}, i_{EF}, I_{EF}$	
$I_0, I_{C0}, I_{E0}, I_{CF0}, I_{EF0}$	dc junction saturation currents
$I_{C \text{ sat}}$	collector current in saturation
i_{H_c}, I_{H_d}, i_S	currents through combance, diffusance and storance, respectively
i_{BN}, i_{EN}, i_{CN}	base, emitter, and collector current in normal transistor operation
j_n	electron current density
j_p	hole current density
k	Boltzmann constant
L_p	diffusion length for holes
m, m_1, m_2	constants relating lumped carrier density to carrier density at junction boundary
n	electron density; excess electron density
n_p	excess electron density in p-region
n_p, n_{p0}	values of n and n_p in thermal equilibrium
$p, P(s)$	hole density or excess hole density
p_n	excess hole density in n-region
p_0, p_{n0}	value of p and p_n in thermal equilibrium
q, Q	charge
q_1, q_2, q_m	lumped charges in base region
q_N, Q_N	charge in normal store
q_I, Q_I	charge in inverse store
$\Delta q_N, \Delta Q_N, \Delta q_I, \Delta Q_I, Q_{BS}$	additional charges stored due to saturation
$Q_{N \text{ SAT}}$	limiting value of Q_N , reached at edge of saturation

q_{10}, q_{m0}	total minority carrier charge in equilibrium
r, \bar{r}	analog resistor, same per unit length
r_e	small signal junction resistance
s	Laplace operator
S, S_1, S_2, S_m	stores = storances
\bar{S}	storance per unit length
t, t_x, T	time
T	absolute temperature
v, V	voltage
v_{ext}	externally applied junction voltage (excluding resistive drops)
v_c, v_e	collector and emitter junction voltages
W_1, W_2	lengths denoting sections in neutral region
W	base width
x	neutral region length variable
Z	characteristic impedance
α_N, α_I	normal and inverse ac current gain in common-base connection
α_{N0}, α_{I0}	dc values of α_N and α_I
β_N, β_I	normal and inverse ac current gain in common-emitter connection
β_{N0}, β_{I0}	dc values of β_N and β_I
γ	transmission line propagation constant
λ	short for e/kT
μ_n, μ_p	electron and hole mobility, respectively
τ, τ_p	recombination time constant in p -region
$\tau'_p, \tau_a, \tau_b, \tau_{12}$	diffusion time constants
τ_e	approximative effective recombination time constant for excess charge in saturation
$\tau_1 \equiv \tau_{BN}$	recombination time in base under normal operation
$\tau_2 \equiv \tau_{BI}$	recombination time in base under inverse operation
τ_{CN}, τ_{EI}	normal collector and inverse emitter diffusion time constants, respectively
τ_{EN}, τ_{CI}	normal emitter time constant ($= 1/\omega_{\alpha N}$) and inverse collector time constant ($= 1/\omega_{\alpha I}$), respectively
$\omega_{\alpha N}, \omega_{\alpha I}$	common-base angular cut-off frequencies
$\omega_{\beta N}, \omega_{\beta I}$	common-emitter angular cut-off frequencies

REFERENCES

1. Ebers, J. J. and Moll, T. L., Large Signal Behavior of Junction Transistors, Proc. IRE, *42*, December, 1954, pp. 1761-1772.
2. Linvill, J. G. and Gibbons, J. F., *Transistors and Active Circuits*, McGraw-Hill Book Co., New York, 1961.
3. Beaufoy, R. and Sparkes, J. J., The Junction Transistor as a Charge-Controlled Device, ATE Journal, *B*, October 1957, pp. 310-327.
4. Moll, J. L., Large Signal Transient Response of Junction Transistors, Proc. IRE, *42*, December, 1954, pp. 1773-1783.
5. Linvill, J. G. and Wunderlin, W., Transient Response of Junction Diodes, IEEE Trans. Circuit Theor., *10*, June 1963, pp. 191-197; Technical Report No. 1513-1, August, 1962, Stanford University.
6. Linvill, J. G. and Wunderlin, W., Untersuchung von Schaltvorgaengen in Halbleiterdioden mittels Modellen mit konzentrierten Ersatzelementen, AEU, *17*, 1963, pp. 35-40.
7. Linvill, J. G., *Models of Transistors and Diodes*, McGraw-Hill Book Co., New York, 1963.
8. Hamilton, D. J., Lindholm, F. A., and Narud, J. A., Large Signal Models for Junction Transistors, Engineering Research Laboratories College of Engineering, University of Arizona, Tucson, Arizona.
9. Narud, J. A., Hamilton, D. J., and Lindholm, F. A., Large Signal Models for Junction Transistors, 1963, ISSCC Philadelphia, Digest, pp. 56-57.
10. Hamilton, D. J., Lindholm, F. A., and Narud, J. A., Comparison of Large Signal Models for Junction Transistors, Proc. IEEE, *52*, March, 1964, pp. 239-248.
11. Gray, P. E., et al, *Physical Electronics and Circuit Models of Transistors*, Semiconductor Electronics Education Committee, *2*, John Wiley & Sons, Inc., New York, 1964.
12. Beddoes, M. P., Linvill's Lumped Models and the Simplified Model, Proc. IEEE, *53*, Correspondence May, 1965, pp. 552-554.
13. Melchior, H. and Strutt, M. J. O., Small Signal Equivalent Circuit of Unsymmetrical Diodes at High Current Densities, IEEE Trans. Electron Devices, *ED-12*, February, 1965, pp. 47-55.
14. Boothroyd, A. R., Charge Definition of Transistor Properties, 1962 ISSCC Philadelphia, Digest, pp. 30-31.
15. Lax, B. and Neustadter, S. F., Transient Response of a P-N Junction, J. Appl. Phys. *25*, September, 1954.
16. Sparkes, J. J., A Study of the Charge Control Parameters of Transistors, Proc. IRE, October, 1960, pp. 1696.
17. Ekiss, J. A. and Simmons, C. D., Junction Transistor Transient Response Characterization, Solid-State J., *2*, January, 1961, pp. 17-24.
18. Ekiss, Spiegel, Simmons, and Blank, Characterization of Switching Transistors, Armed Serv. Techn. Inf. Agency, Philco, No. R-113, AD 271/122, 275/510.
19. Ekiss, J. A., Applications of the Charge-Control Theory, IRE Trans. Electron Computers, *EC-11*, June, 1962, pp. 374-381.
20. Bader, C. J., Charge-Step-Derived Transfer Functions for the Junction Transistor, IEEE Trans. Commun. Electron, *66*, May, 1963, pp. 179-185.
21. Schmeltzer, R. A., Transient Characteristic of Alloy Junction Transistors Using a Generalized Charge Storage Model, IRE Trans. Electron Devices, *10*, May, 1963, pp. 164-170.
22. Den Brinker, C. S., Fairbairn, D., and Norris, B. L., An Analysis of the Switching Behavior of Graded Base Transistors, Electron. Eng., August, 1963, pp. 500-505.
23. Singhakowinta, A., Some Effects of Transit Time Through the Collector Depletion Layer of Junction Transistors, IEEE Trans. Circuit Theor., *CT-10*, September, 1963, p. 445.
24. Cho, Y., A Method of Theoretical Analysis of High Speed Junction Diode Logic Circuits, IEEE Trans. Electron Computers, *EC-12*, October, 1963, pp. 492-502.
25. Hegedus, C. L., Charge Model of Fast Transistors and the Measurement of

- Charge Parameters by High Resolution Electronic Integrator. *Solid-State Design*, 5, August, 1964, pp. 23-36.
26. Bloodworth, G. G., The Significance of the Excess Charge Product in Drift Transistors, *Radio Electron. Eng.*, 28, November, 1964, pp. 304-312.
 27. Koehler, D., A New Charge Control Equivalent Circuit for Diodes and Transistors and Its Relation to Other Large Signal Models, 1965 International Solid-State Circuits Conference, Philadelphia, Digest of Technical Papers, pp. 38-39.
 28. Bassett, H. G. and Greenaway, P. E., Electrical Properties of High-Frequency Transistors, *Post Office Elec. Engrs. J57*, April, 1964, pp. 54-59.
 29. Nanavati, R. P., Charge Control Analysis of Transistor Storage Time Dependence on Input "On" Pulse Width, *IRE Trans. Electron Devices*, 10, July, 1963, pp. 290-291.
 30. Thiney, A., Rise and Fall Times of Transistors in Switching Operation Regardless of the Driving Source Impedance, *IEEE Trans. Electron Computers*, EC-12, February, 1963, p. 23.
 31. Simmons, C. D., High-Speed Microenergy Switching, *Solid-State J.*, 1, September-October, 1960, pp. 31-36.
 32. Nanavati, R. P. and Wilfinger, R. J., Predicting Transistor Storage Time for Non-Step, Quasi-Voltage Inputs, *IRE Trans. Electron. Devices*, ED-9, November, 1962, pp. 492-499.
 33. Kuno, H. J., Rise and Fall Time Calculations of Junction Transistors, *IEEE Trans. Electron Devices*, 11, April, 1964, pp. 151-55.
 34. Lindholm, F. A. and Hamilton, D. J., Systematic Modeling of Solid-State Devices and Integrated Circuits, 1965 International Solid-State Circuits Conference, Philadelphia, Digest of Technical Papers, pp. 36-37.
 35. Lo, A. W., et al., *Transistor Electronics*, Prentice-Hall, 1955.
 36. Gärtner, W. W., *Transistors, Principles, Design and Applications*, D. van Nostrand Company, Inc., Princeton, 1960.
 37. Lindmayer, J. and Wrigley, C. Y., *Fundamentals of Semiconductor Devices*, D. Van Nostrand Co., Inc., Princeton, 1965.
 38. Narud, J. A., Seelbach, W. C., and Meyer, C. S., Microminiaturized Logic Circuits: Their Characterization, Analysis, and Impact Upon Computer Design, *IEEE Conv.*, March, 1963.
 39. Searle, S. C., et al., *Elementary Circuit Properties of Transistors*, Semiconductor Electronics Education Committee, 3, John Wiley & Sons, Inc., New York, 1964, Section 2.1.
 40. Lloyd, R. H. F., A Simpler Transistor Model, *Proc. IEEE*, 53, Correspondence, May, 1965, pp. 527-528.
 41. Pritchard, R. L., Frequency Variations of Current Amplification Factor of Junction Transistors, *Proc. IRE*, 40, November, 1952, pp. 1476-1481.
 42. Geller, S. B., Mantek, P. A., and Boyle, D. R., A General Junction Transistor Equivalent Circuit for Use in Large-Signal Switching Analysis, *IRE Trans. Electron Computers*, December, 1961, pp. 670-679.
 43. Beale, J. R. A. and Beer, A. F., The Study of Large Signal High-Frequency Effects in Junction Transistors Using Analog Techniques, *Proc. IRE*, January, 1962, pp. 66-77.