Semipermanent Memory Using Capacitor Charge Storage and IGFET Read-out

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One of the earliest computers used capacitors as its memory.[1] A mechanical means was used for both read-in and read-out operations. Electronic accessing was used in conjunction with vacuum tube or solid-state diodes in relatively modern computers such as the SEAC computer.[2] Capacitor storage is rarely used at present since magnetic memories meet the modern computer requirements much better. The inherent difficulty with capacitor storage was the limited holding time since a nonlinear resistor with small enough leakage currents to allow useful memory holding time was then not readily available. The old capacitor memory was charged through a diode with slow recovery time and with leakage current of 10^{-10} amp at best and required a large capacitor for any appreciable holding time. Furthermore, the read-out was usually destructive.

The capacitor storage merits re-examination in view of the advanced solid-state devices and technology now available. Coupled with an Insulated Gate Field Effect Transistor (IGFET),[3] the read-out can be nondestructive. Integrated circuit techniques may prove superior to the current magnetic memories for some applications where infrequent recycling is permissible. The inherent speed should be much faster than that of magnetic units.

Consider a capacitor C in series with a nonlinear element as shown in Fig. 1. The capacitor may represent the gate capacity of the IGFET plus any external capacitor in parallel with the gate capacitor. When a positive voltage pulse with amplitude V and duration τ is applied at the nonlinear element terminal, it can be shown that the stored charge $Q(\tau)$ and the decay time constant τ_e, defined as the time required to reach $1/e$ value of the initial stored charge Q_o, can be calculated for various nonlinear resistors.

I. POWER-LAW RESISTORS

The I-V characteristics are given by

$$I = KV_n^m, \tag{1}$$

then

$$Q(\tau) = C\left[V - \left(\frac{1}{V^{(m-1)}} + K(m-1)\frac{\tau}{C} \right)^{-1/(m-1)} \right] \tag{2}$$

and

$$\begin{aligned} \tau_s &= \frac{C^m}{(m-1)K} \frac{1}{Q_0^{(m-1)}} (e^{(m-1)} - 1) \\ &= \frac{(e^{(m-1)} - 1)}{(m-1)} \frac{Q_0}{I_0}, \end{aligned} \tag{3}$$

where I_0 is the discharge current at the termination of charging. It is clear from (2) that m $\geqq$ 1 for physically meaningful $Q(\tau)$. For a long holding time, (3) tells us that the nonlinearity of the resistor should be large. These equations would describe the behavior of the storage unit comprising a space-charge-limited-current diode.[4] If traps are present, only a simple modification is needed in the analysis. Structures comprising photosensitive space-charge-limited-current diodes such as CdS diodes should allow optical read-in operations which might be advantageous for certain applications such as a vidicon.

II. TUNNEL SANDWICH DIODES

For this nonlinear element, the circuit in Fig. 1 should be modified to include the shunt capacitance of the tunnel sandwich. Thus, at the instance of pulse application, the voltage divides between the two capacitors. The I-V relationship for Fowler-Nordheim type tunneling is

$$I = KV_x^2 e^{-V_0/V_x}. \tag{4}$$

With the appropriate initial conditions, the stored charge $Q(\tau)$ is given by

$$Q(\tau) = C\left[V - \alpha V_0 / \ln \left(e^{\alpha V_0/V} + \frac{KV_0}{C}\tau \right) \right], \tag{5}$$

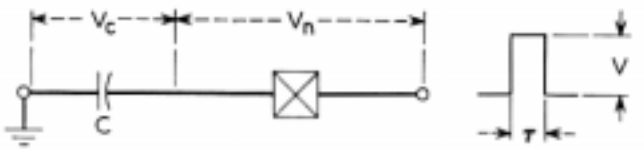

Fig. 1 — A capacitor being charged through a nonlinear resistor.

where α is defined as unity plus the ratio of the shunt capacitance of the tunnel sandwich, C_n to the charging capacitor, namely $\alpha = 1 + (C_n/C)$.

The discharge time constant τ_e can also be shown to be

$$\tau_e = \frac{\frac{\alpha C}{KV_0}\left(e^{(\alpha CV_0/Q_0)(e-1)} - 1\right)}{e^{\alpha CV_0/Q_0}} = \tau_c e^{(\alpha CV_0/Q_0)(e-2)}. \tag{6}$$

It is clear that charging time required for adequately large Q is very short, allowing fast read-in operation. The decay time can be seen to be large for tunneling across well-known insulators such as SiO_2 and Al_2O_3. Therefore, the decay is not controlled by (6) but rather by the dielectric relaxation time of the insulators used for the entire assembly including the IGFET gate material. The dielectric relaxation time of the best inorganic insulators is of the order of one day at room temperatures. However, certain organic insulators are known to have theoretical dielectric relaxation times of many years. Performance of a memory cell incorporating a tunnel sandwich diode is described in more detail elsewhere.[5]

III. SCHOTTKY BARRIER DIODES

For charging through a rectifier, Schottky barrier diodes are preferred over pn junction diodes since Schottky barriers are majority carrier devices and hence fast recovery is achievable.[6] I-V characteristics may be represented by

$$I = I_s(e^{\beta V} - 1). \tag{7}$$

For charging, we may neglect the unity in the bracket in (7), and the stored charge can be shown to be

$$Q(\tau) = C\left[V - \frac{1}{\beta}\ln\left(\frac{\tau}{\tau_c} + e^{-\beta V}\right)^{-1}\right], \tag{8}$$

where

$$\tau_c = \frac{C}{\beta I_s}.$$

For decay, it is easy to show

$$\tau_e = \frac{Q_0}{I_s}(1 - e^{-1}). \tag{9}$$

Fig. 2 shows the stored charge Q computed from (8) as a function of pulse duration for several pulse amplitudes. The characteristic time constant τ_c is not much less than 1 sec for a typical configuration ($C < 10^{10}$ Fd, $I_s > 10^{-12}$ amp). Therefore, it is seen that the stored charge is proportional to the pulse amplitude for sufficiently large V. This suggests that the device may be used as a multi-level storage unit.

The combination of Schottky barrier diodes and the IGFET is shown in Fig. 3. A similar structure has been fabricated and tested. The holding time was of the order of 10 sec when the charging was done by 15 volts pulse in agreement with (9) since the IGFET gate capacitance was about 10^{-12} Fd and I_s of the diode was 10^{-12} amp (measured at 10 volts reverse bias). The maximum pulse amplitude before the breakdown of the gate insulator was about 30 volts, allowing a longer holding time of about 30 seconds. The read-in time was less than 10^{-7} second and the reverse breakdown of the diode was used to turn the IGFET off, which also took less than 10^{-7} second.

A memory featuring nondestructive read-out, access times in the

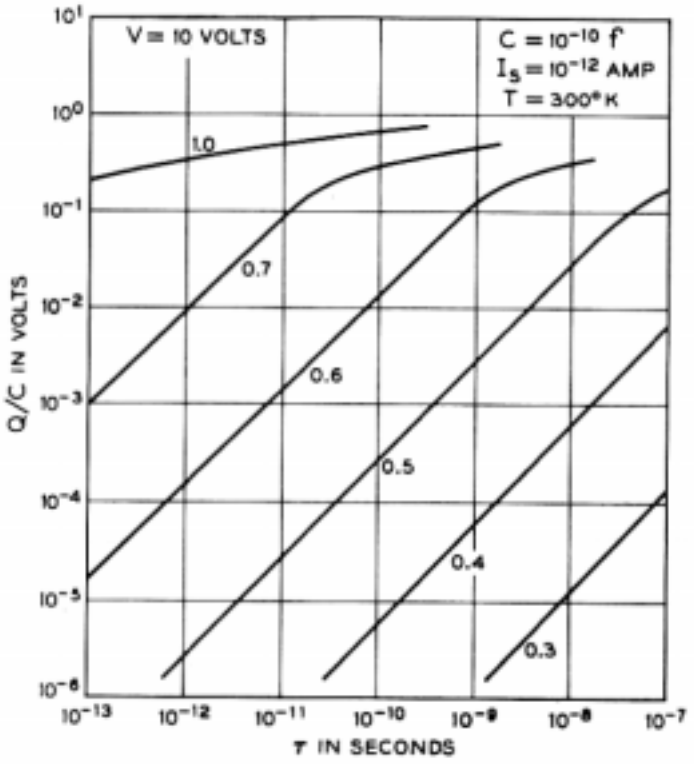

Fig. 2 — Theoretical stored charge/storing capacitance (the floating potential) as a function of time for charging through a Schottky barrier diode.

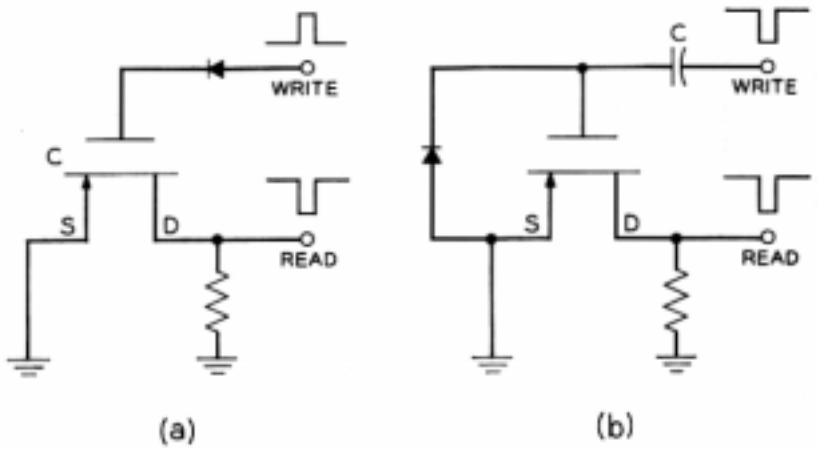

Fig. 3 — Combination of the capacitor storage unit with a p-channel IGFET for read-out. (a) Series connection, read-in should be positive. (b) Parallel connection, read-in should be negative.

submicrosecond range, and holding times of many seconds should find many applications. An integrated structure incorporating Schottky barrier diodes and IGFETs is readily obtainable with modern solid-state technology.

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