Gold Doped Silicon Compandor Diodes For N2 and N3 Carrier Systems

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Companding has proven to be a valuable technique for improving the signal-to-noise ratio of voice transmission at baseband frequencies. A compandor consists of a compressor element which reduces the dynamic range of a transmitted signal in a predetermined manner and an expandor element which restores the signal range at the receiver. Practical Bell System applications to date have used electron tubes, germanium point-contact semiconductor diodes and unpassivated silicon mesa diodes. Each of these variolosser elements had serious shortcomings. Two new diode pairs have been designed which eliminate the problems of impedance range control and linearity, diode noise and electrical stability. The new design utilizes heavy gold doping of a planar oxide-passivated wafer design to produce a bulk controlled device capable of unusually high manufacturing yields.

I. INTRODUCTION

Compandors are a special application for a diode because the diodes are used as variolossers and the electrical parameter which must be controlled is the small signal forward impedance as a function of bias current. Furthermore, control of impedance is required over two orders of magnitude. Other requirements are low noise and good stability. The 484/489A and 484/489B diode pairs, which are electrically identical and differ only in mechanical outline, are silicon "planar" diodes which were designed for use in this application. The new devices were designed to replace two pairs of troublesome unpassivated "mesa" type devices in both the N2 and N3 carrier systems.

A comprehensive diode design was not previously available for this application. Diodes were obtained by selection from available types at low yield. This paper discusses the theoretical and empirical design and the fabrication of the new diodes.

II. CIRCUIT FUNCTION OF COMPANDORS

Noise is an important problem associated with long distance telephone transmission. Elimination or reduction of this undesirable effect is a consideration in the design of all transmission equipment. Noise occurs in transmission from many sources such as thermal noise, external interferences, and crosstalk. The compandor circuit, which was first introduced into the Bell System in the transatlantic radio circuit in 1932,[1] is one of the methods used to reduce noise. While the first compandor circuits used vacuum triodes[1] as the variolosser units, later compandor circuits used semiconductor diodes when they become available.

A compandor[2] is composed of two-parts, compressor and expandor, one at each end of a transmission path. The compressor circuit compresses the dynamic range of the transmitted signal power by taking the square root of the signal (although other functions could be used). If the maximum signal levels are transmitted at the same power with compression as they would be without compression, then the minimum signals will be transmitted at relatively higher power with compression than without. Therefore, a higher signal-to-noise ratio results for the minimum signals on the transmission path if compression is used. At the receiving end of the transmission line the expandor circuit squares (expands) the signal to its original dynamic range.

The N2 and N3 carrier system compandors[3] compress a 60-dB signal range into a 30-dB range for transmission. Therefore, 30-dB higher noise may be potentially tolerated in the transmission path. At the receiving terminal the expandor portion of the compandor expands the signal range to its original value of 60 dB and restores the signal to its original form. Since a compandor is an interchangable plug-in unit and the compressor and the expandor in the same unit do not work together, it is necessary that all compressor circuits track closely with all expandor circuits.

The core of the compressor and expandor circuits is a pair of variolosser diodes. The stringent requirements on the compandor circuits are reflected in stringent requirements on the variolosser diodes. This paper reports the development of two diode pairs which meet the unique requirements of these circuits.

III. THE DIODES

3.1 *General Description*

The first semiconductor diodes used as the compandor variolossers were selected from available types. While the New York-London long

wave radiotelephone circuit (1932) used vacuum triodes,[1] the N1 carrier system used germanium point-contact diodes;[4] the P1 and O carrier systems used silicon alloy diodes;[5] and the N2 carrier system originally used diffused silicon, mesa diodes.[3] Several problems arose with the use of these state-of-the-art-diodes although careful selection and circuit adjustment could correct most of them. The major problems of high device cost, high noise, and periodic supply shortages arose directly from a lack of understanding of the physical mechanism controlling the forward impedance characteristic.

It was possible, by designing a new diode, to overcome all of the problems and at a much lower cost. The new design uses silicon planar techniques coupled with controlled gold doping and heat treatment to produce the desired diode characteristics.

The following parameters are used to characterize the diodes for the compandor applications:

(*i*) The small-signal forward impedance,* Z_f, at a specified mid-range dc dias current.

(*ii*) The ratio, R_1, of the small-signal forward impedance at a specified lower current to the impedance at the above mid-range current.

(*iii*) The ratio, R_2, of the impedance at the mid-range current to the impedance at a specified higher current.

(*iv*) The impedance difference between the diodes of a pair measured separately at the idling current.

(*v*) Noise generated by the diode over the current and frequency ranges of interest.

Table I shows the limits for these parameters for both the mesa and the planar type diodes.

3.2 *Design Theory*

The primary parameter to be controlled was the small-signal forward impedance, Z_f. The theoretical forward impedance of the semiconductor diode may be obtained by differentiation of the current-voltage equation. For semiconductor diodes the relationship is:

$$I_F = I_s(\exp qV/nkT - 1), \tag{1}$$

where

I_s = saturation current,

*For simplicity the expression 'small-signal forward impedance' will often be shortened to 'forward impedance' or 'impedance' in this paper.

q = electronic charge,
V = applied voltage,
n = experimentally determined constant commonly between 1 and 2,
k = Boltzmann's constant,
T = absolute temperature.

Therefore,

$$Z_f \equiv \frac{\partial V}{\partial I_F} = \frac{nkT}{qI_s} \exp - qV/nkT.$$

For forward bias, V, greater than a few nkT/q ($kT/q = 0.026$ volts

TABLE I — SALIENT CHARACTERISTICS

Parameter	Planar compressor and expandor	Mesa compressor and expandor	Units
Z_f, Forward impedance, at 50 μA dc bias			
For single diode of pair	900 ± 35	1045 ± 125	ohm
For diode pair in series	1800 ± 70	2070 ± 70*	ohm
R_1, Impedance ratio = $\frac{Z_f \text{ at } 10\ \mu\text{A dc}}{Z_f \text{ at } 50\ \mu\text{A dc}}$			
For single diode of pair	5.0 ± 0.2	4.9 ± 0.4	—
For diode pair in series	5.0 ± 0.2	4.9 ± 0.2*	—
R_2, Impedance ratio = $\frac{Z_f \text{ at } 50\ \mu\text{A dc}}{Z_f \text{ at } 300\ \mu\text{A dc}}$			
For single diode of pair	6.0 ± 0.2	6.2 ± 0.5	—
For diode pair in series	6.0 ± 0.2	6.15 ± 0.2*	—
Parameter	**Compressor only**	**Compressor only**	**Units**
ΔZ_f = Difference in impedance of diodes of pair measured separately:			
At 2 μA dc bias	2000 max	2000 max	ohms
At 10 μA dc bias	500 max	500 max	ohms
v_n = Noise voltage of single diode or pair at 2.5μA dc bias. Bandwidth 200–3500Hz. Parallel resistance 17,000 ohm.	20 max	— —	μVrms

* Computer selected.

at room temperature) one has $\exp qV/nkT \gg 1$ and to a good approximation*

$$Z_f = \frac{nkT}{q}\frac{1}{I_F}. \tag{2}$$

It is this Z_f-I_F functional relation which is used in the design of the N2 and N3 compandor circuits.

There are five sources of current in a forward biased p-n junction; diffusion, bulk recombination, surface recombination, channel and tunneling currents. The total diode current is given by

$$\begin{aligned} I_F &= I_D \text{ (diffusion)} + I_{BR} \text{ (bulk recombination)} \\ &\quad + I_{SR} \text{ (surface recombination)} + I_{CL} \text{ (channel)} \\ &\quad + I_T \text{ (tunneling)}. \end{aligned} \tag{3}$$

The diffusion current[6] at small bias is given by

$$I_D = I_d(\exp qV/nkT - 1), \tag{4}$$

where

$$I_d = qA[p_n(D_p/\tau_p)^{\frac{1}{2}} + n_p(D_n/\tau_n)^{\frac{1}{2}}]$$

and

τ_p = lifetime of holes on n side of junction,
τ_n = lifetime of electrons on p side of junction,
p_n = hole concentration in n-region,
n_p = electron concentration in p-region,
D_p = diffusion constant for holes,
D_n = diffusion constant for electrons,
A = area.

At high forward bias (injection) the current will be given by

$$I_D = I_d(\exp qV/2kT - 1) \tag{5}$$

and in the intermediate range the current equation will be similar to (1).

The bulk recombination current[7,8] for bias voltages, V, greater than several kT/q is given by

$$I_{BR} = I_{r0} \exp qV/2kT, \tag{6}$$

where

$$I_{r0} = \frac{\pi}{2}\left(\frac{kT}{qE}\right)\frac{qn_i}{\tau_0}A,$$

n_i = intrinsic carrier concentration,

* The error is less than 1 percent for voltages greater than 0.2 volts and less than 0.1 percent for voltages greater than 0.3 volts.

E = electric field at junction,

and τ_0 = lifetime.

The exact voltage dependence of (6) depends in a complicated way on the physical parameters of the junction, but in a given range may be described by

$$I_{BR} = I_{br} \exp qV/n_{br}kT, \tag{7}$$

where $n_{br} \leqq 2$ and accounts for the voltage dependence of I_{r_0}, while I_{br} is the voltage independent factor.

Surface recombination current may be described by a similar equation;[8]

$$I_{SR} = I_{sr} \exp qV/n_{sr}kT, \tag{8}$$

where $n_{sr} > 1$.

Channel current[8] at $V > kT/q$ may be described by

$$I_{CL} = I_{cl} \exp qV/n_{cl}kT, \tag{9}$$

where $n_{cl} = 1$ up to 4 or 5 or more for poorly stabilized surfaces.

By considering the five currents in parallel one may calculate a small-signal impedance for each current, and the forward impedance of the diode may be expressed as five impedances in parallel.

$$\frac{1}{Z_f} = \frac{1}{\frac{kT}{qI_D}} + \frac{1}{\frac{n_{br}kT}{qI_{BR}}} + \frac{1}{\frac{n_{sr}kT}{qI_{SR}}} + \frac{1}{\frac{n_{cl}kT}{qI_{CL}}} + \frac{1}{Z_T} \tag{9}$$

or

$$\frac{1}{Z_f} = \frac{q}{kT}\left(I_D + \frac{I_{BR}}{n_{br}} + \frac{I_{SR}}{n_{sr}} + \frac{I_{CL}}{n_{cl}} + \frac{kT}{qZ_T}\right). \tag{10}$$

Diffusion current cannot be made dominant over recombination current in silicon except at high current densities where the value of the multiplier, n, may be modified by carrier injection. In both mesa and planar diodes the diffusion current was reduced by using heavily doped starting material (approximately 0.005 ohm-cm p-type silicon). The use of such low resistivity material had the further advantage of reducing the series resistance of the bulk silicon to about 0.04 ohms. At all currents of interest the 0.04 ohms made a negligible contribution to the diode impedance.

The bulk recombination current was greatly enhanced by introducing trapping centers by heavily gold doping the diodes. The effect on the diode parameters of various gold doping levels was investigated by

varying temperature and time of gold diffusion and subsequent heat treatments. These effects are discussed in detail in Section 3.4.3.

From the previous equations and measurements on existing diodes the relative values of the five currents and their contributions to the total impedance may be compared. As an example, values are calculated for a bias of 0.4 volts and diode parameters which approximate those of the actual diodes.

The diffusion current is calculated from (4) as

$$I_D = 10^{-9}A = 0.001\mu A,$$

where the following values are assumed:

$\tau_n = \tau_p = 10^{-10}$ sec (Ref. 9)
$N_n = N_p = 2 \times 10^{19}$ cm^{-1} (0.005 ohm-cm)
$\mu_p = 30$ cm^2/volt sec (Ref. 10)
$\mu_n = 75$ cm^2/volt sec (Ref. 10).

The bulk recombination current is calculated from (6) by using the approximation

$$E = (\psi_0 - V)/W,$$

where ψ_0 is the built-in voltage and W is the space-charge width. The bulk recombination current is

$$I_{BR} = 30\mu A \gg I_D = 0.001\mu A.$$

Estimates of surface recombination and channel currents were made from measurements on planar type diodes. These estimated values were much smaller (by several orders of magnitude) than the bulk recombination current. Likewise, the observed magnitude of the forward tunneling current is negligible since doping levels are relatively light and the junction is graded.

Hence, bulk recombination current is dominant and the junction impedance becomes

$$Z_f = \frac{nkT}{q}\frac{1}{I_F} \cong \frac{n_{br}kT}{q}\frac{1}{I_{BR}}. \tag{11}$$

By way of contrast the impedance of the mesa diode was primarily dependent on surface damage introduced during mechanical formation of the active diode wafer. High surface recombination (mechanically damaged) wafer edges were created when the diffused slices were diamond sawed into wafers. A portion of this damage was then removed

by chemical etching to set the diode multiplication factor, n, and hence forward impedance to the nominal value.

3.3 *Mesa Diode Deficiencies*

System and manufacturing experience pointed out three major shortcomings of the unpassivated mesa design. The first of these shortcomings was lack of good control of the nominal impedance value and range. Manufacturing problems were experienced until the planar redesign efforts delineated the physical mechanisms controlling forward impedance. Even with this understanding manufacturing control could not be improved sufficiently to obtain narrow distributions of impedance; a computer selection of individual diode pairs was necessary for reasonable yields.

A second electrical characteristic which could not be controlled in the manufacturing operation was the noise voltage produced by the device in the 200-3500 Hz band. The N2 and N3 systems require that the noise voltage be less than 20 microvolts for the compressor pair and 40 microvolts for the expandor pair when operating at a direct current of 2.5 microamperes. This characteristic was checked on a nonparametric basis at the equipment assembly location; and, quite frequently, shipments of diode pairs would be found which exhibited excessively high noise.

Finally, the short-term stability objectives of the systems could never be achieved with the unpassivated device.

As shown in this paper, the redesigned device readily meets all noise and stability objectives and permits manufacture of diodes at very high yields without the need for computer matching.

3.4 *Planar Diode Design*

3.4.1 *Structural Features*

While the primary compandor diode design effort was directed toward understanding and controlling the physical variables associated with the active semiconductor chip, the encapsulating structure was also changed to provide an assembly more suited to printed circuit board mounting. As shown in Fig. 1, each diode pair of the mesa type was composed of two metal package diodes molded in epoxy and glued together with an epoxy cement. This arrangement is costly and results in a double ended structure whose leads must be trimmed and formed for mounting. The redesign diode structures are simply two TO-18 en-

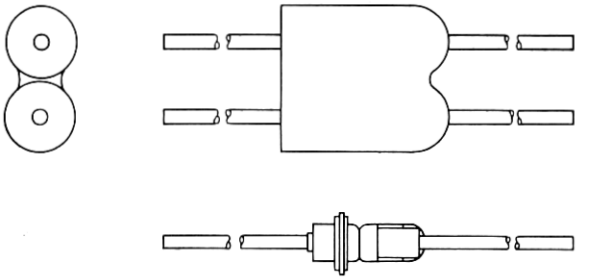

Fig. 1 — Outline of mesa diode pairs and package outline.

capsulations which are snap fitted into an acytal copolymer plastic block. The lead arrangement shown in Fig. 2(a) was used for immediate production and field replacements; the straight-through lead arrangement shown in Fig. 2(b) is being used in new equipment which incorporates modified circuit boards. The latter structure requires neither lead trimming nor forming for insertion. Code and date markings are molded into the plastic carrier which eliminates the need for coding individual finished devices. The plastic carriers are bullet-shaped to identify polarity and are color coded to provide positive differentiation of compressor and expandor pairs in the equipment assembly areas. The leads of the device are solder coated to facilitate wave soldering to printed circuit boards.

The essential features of both mesa and planar type wafers are depicted in Fig. 3. Fig 3(a) shows the mesa structure used in the earlier diode. In this case, a p-n junction is formed approximately

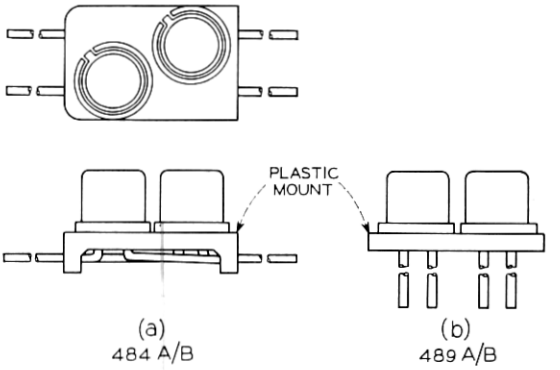

Fig. 2 — Outlines of 484A/B and 489A/B diode pairs.

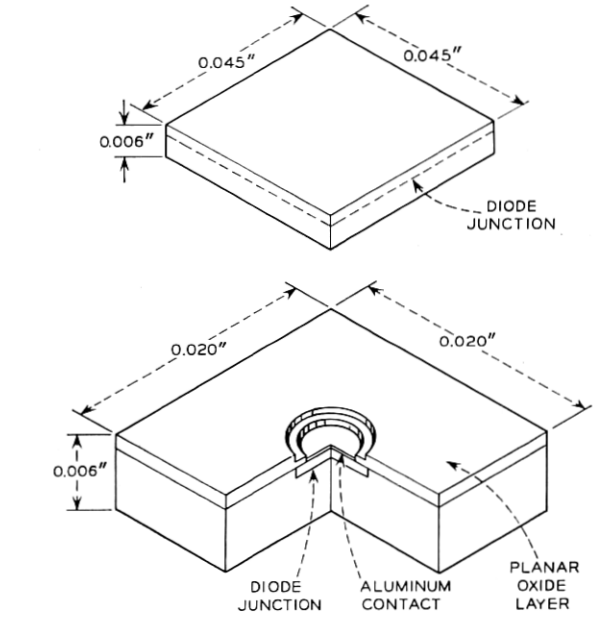

Fig. 3 — (a) Mesa structure of component diodes. (b) Planar structure of component diodes.

0.0002 inch below both faces of a one-inch diameter silicon wafer by gaseous diffusion producing a p-n-p structure. One of the p-n junctions is then removed from the wafer by mechanical lapping. The lapped slices are next plated with nickel and gold to form ohmic contacts. The wafers are then cut into 0.045-inch square chips by a diamond sawing operation to produce the final chip. This chip is subsequently eutectic-bonded to the package mounting stud, etched to remove a controlled amount of sawing damage (thus adjusting the impedance to the nominal value), and finally spring contacted during final encapsulation to complete the device. A cut-away view of this structure is shown in Fig. 4.

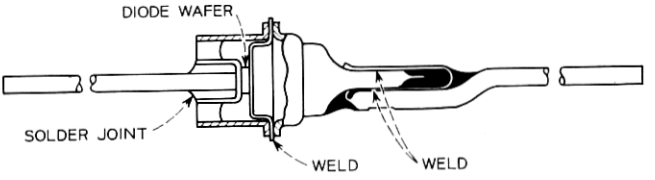

Fig. 4 — Cut-away view of mesa diode package.

Fig. 3(b) depicts the mechanical features of the planar wafer. In this case, a p-n junction is formed in the p-type silicon by diffusing phosphorus through a 0.008-inch hole cut into the protective layer of silicon dioxide. Since the starting crystal is very heavily doped with boron (approximately 2×10^{19} atoms/cc), it is difficult to overdope this material and produce a deep junction; in this device, the junction lies 0.0003 inch below the initial surface of the silicon. As explained elsewhere, the silicon is also very heavily gold doped by a high temperature diffusion to control the recombination-generation current and thus the diode multiplication factor which in turn controls diode impedance. An aluminum contact is evaporated and alloyed selectively into the hole in the oxide to complete wafer fabrication. The planar wafer is next eutectic-bonded to a gold-plated TO-18 header and a thermocompression wire bond is made between the metal button and the header lead. Final closure of the device is accomplished by resistance welding a Kovar can to the gold-plated Kovar header. A barium oxide impregnated porous nickel cylinder is brazed to the top of the can and serves as a moisture getter. A cut-away view of the individual planar device is shown in Fig. 5.

3.4.2 *Fabrication Process*

Many of the basic processes used to fabricate these diodes are common to other planar silicon devices and have been presented elsewhere.[11, 12] This section, then, will deal mainly with those processes which determine the forward impedance, noise and stability aspects of the device. A basic flow chart of the major assembly operations is presented in Fig. 6. In this chart, the header assembly operations, getter fabrication, activation and assembly operations and the semiconductor crystal growing operations are not shown.

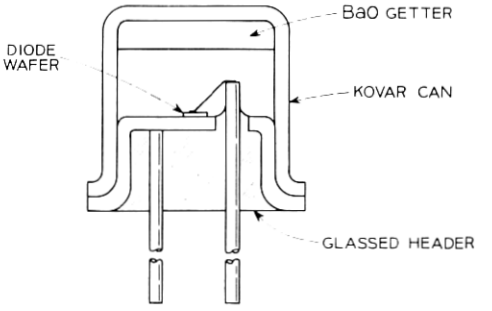

Fig. 5 — Cross-section view of planar component diode.

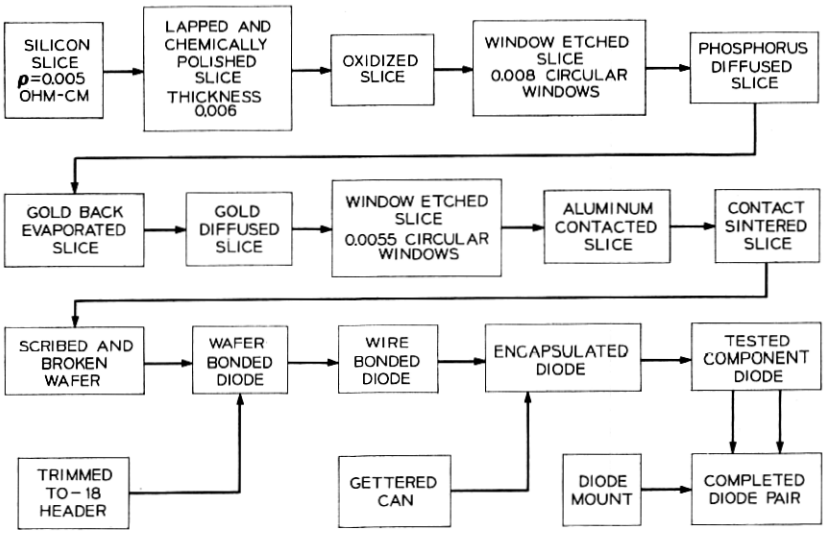

Fig. 6 — Flow chart for fabrication of planar diodes. Only fundamental operations are shown.

The first fundamental design choice involves the selection of resistivity type and doping level. The choice of p-type silicon allows use of a junction diffusant (phosphorus) which can be easily cleaned off of the surface of the wafer contact area. The choice of very heavily doped starting material is also of paramount importance in producing a stable device. It has been demonstrated[13] that alkali ions, a universal source of contamination, can electrolize through a protective silicon dioxide layer at high temperature under reverse bias and invert the conductivity type of the p-type material surrounding the junction. This inverted area can cause high channel currents to flow and also drastically increase the capacitance of a device when operated under reverse bias.

When operated in the forward direction, a "channeled" device will exhibit a multiplication factor of typically 2–4 and occasionally up to 10. Obviously, such changes would drastically shift the impedance levels of the device. However, with starting material doped to a level of 2×10^{19} atoms/cm^3, it is estimated from the curves of Ref. 14 that 10^{13} surface charges/cm^2 would be necessary to invert the material. Contamination levels of this magnitude are not encountered if minimal care is exercised in the oxide growing, diffusion and contact evap-

oration steps. Hence, as discussed in Section 3.2, the choice of heavily doped starting material essentially eliminates the contribution of channel recombination-generation current to the total diode current when compared to the bulk recombination-generation current. Also, as calculated in Section 3.2, the diffusion current contribution to the total diode current for this (or any practical) starting resistivity is also negligible compared to the bulk recombination-generation current.

The next pair of design choices, heavy gold doping and planar oxide-passivated technology, combine to produce a very large bulk controlled recombination-generation current and a negligibly small surface current contribution. As indicated in Fig. 6, the polished slice is first oxide passivated and then is selectivly etched to open 0.008-inch circular holes in the oxide using photolithographic techniques. Kodak Thin Film Resist (KTFR) is used as the emulsion in the photo-shaping operation. After junction diffusion, the junction assumes the shape shown in Fig. 3(b). The junction diffuses laterally as well as vertically. Lateral diffusion under the oxide layer provides a p-n junction which terminates at the semiconductor surface at a low surface charge location (under the passivating oxide). The low surface charge results in low surface recombination current. Thus, the resultant low resistivity, planar, oxide-protected, heavily-gold-doped combination results in a device which is completely bulk controlled and capable of being predictably controlled in manufacture.

The gold doping level must next be selected to provide the desired value of diode multiplication factor and hence forward impedance. Since many mesa devices are currently in field service, and since both the N2 and N3 were designed to accommodate this device, it was desirable to attempt to set the impedance level at a value of 1035 ohms at 50 microamperes or a multiplication factor of approximately 2. Since values of the multiplication factor at room temperature from gold doping as high as 1.85 had been reported in the literature,[8] this approach appeared to offer promise of successfully achieving the desired objective. As shown in Fig. 7, the impedance level of the device is a very strong function of the gold diffusion temperature. As can be seen from this combined plot of impedance and maximum solid solubility[15] of gold in silicon as a function of temperature, the impedance level is directly related to only the bulk properties of the device as calculated in Section 3.2 and discussed previously in this section. The impedance values presented in this plot were achieved with other impedance controlling variables held constant. In particular, the time and tempera-

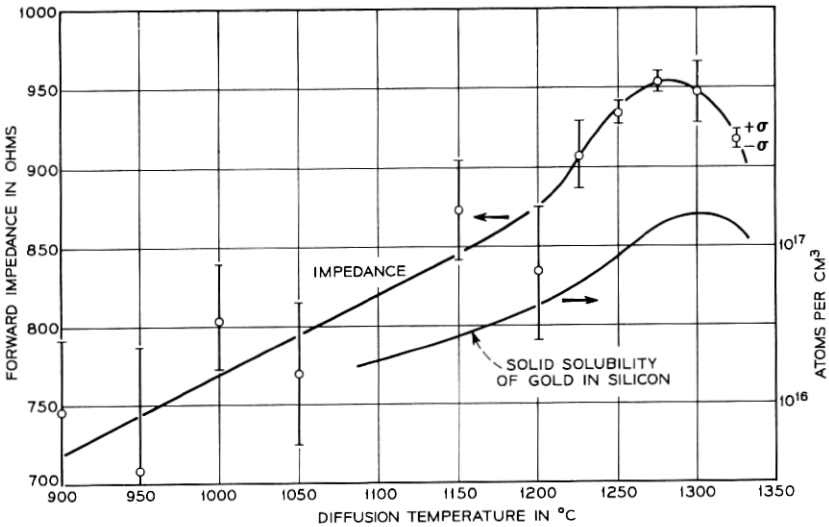

Fig. 7 — Forward impedance at 50μA bias current as a function of gold diffusion temperature. Diffusion time 10 minutes. Contact sinter time 3 minutes. Solid solubility after Trumbore.

ture used for contact sintering to provide contact adherence were held at 3 minutes and 625°C, respectively. Fig. 16 presents the variation of impedance level with contact sintering time at 625°C. It can be seen that maximum impedance results when the contact is not sintered. Heat treatment of the gold-loaded slice (even without metal contacts present) results in lowered impedance probably through an oxide-gettering or precipitation mechanism. With minimum contact sintering, average values of impedance as high as 990 ohms at a forward current of 50 microamperes have been achieved for a gold diffusion temperature of 1300°C. The corresponding multiplication factor for these experimental conditions is 1.91. For good mechanical adherence of the contact it was desirable to sinter the contact at about 625°C for 9.5 minutes (a standard process); hence, the impedance level of the redesigned device was set at 900 ± 35 ohms for a gold diffusion temperature of 1300°C. This shift in impedance nominal from the mesa component diode nominal value of 1045 ± 125 ohms necessitated a change of a few resistor values in the compandors.

As discussed in Section 3.3, noise in the low audio frequency range was a serious problem with the mesa diode. While a detailed study of the physical noise mechanisms in silicon was not undertaken in this

development, design information was obtained which clearly indicates methods of controlling this important parameter. Control of the $1/f$ low-frequency noise results as a by-product of heavy gold doping for impedance control. As illustrated in Fig. 10, the noise voltage of the device in the 200-3500 Hz band when biased in the forward direction at 2.5 microamperes is independent of the gold level up to about 1200°C then drops sharply and begins to level out beyond 1300°C. Since the mesa device saw no high temperature gold diffusion, no beneficial effect of the gold was realized.

As seen from Fig. 10, at the specified diffusion temperature of 1300°C the bulk of the planar component diodes are approaching the test set lower limit of 2.4 microvolts and no devices are approaching the compressor or expandor limits of 20 and 40 microvolts, respectively. This parameter is now easily controlled in manufacture; hence, both compressor as well as expandor limits have been set at 20 microvolts.

After oxidation, diffusion and contacting, the slices are simply diamond scribed, cracked apart, eutectic (gold-silicon) wafer bonded and thermocompression wire bonded to the T0-18 header. Finally, the metal can containing an activated moisture getter is resistance welded to the assembled header. The excellent device stability which will be presented in a later section is attributable to the use of very low resistivity semiconductor material, to extremely high gold doping and to the use of oxide passivation techniques.

The design factors discussed in this section combine to produce a device with a very narrow range of impedance, a low noise voltage, extremely stable electrical characteristics and which can be produced with good manufacturing control.

3.4.3 *Design Variables*

The diffusion of gold into silicon is a complex process involving interstitial-substitutional equilibrium.[16] In addition, both diffusion constant and solid solubility are partially dependent on the concentration of other impurities such as boron and phosphorus.[17, 18] Because complete data were not available on the entire ranges of interest of diffusion temperature or boron and phosphorus concentration, and because data were not available on the effect of annealing which would necessarily occur during the contact sintering, the effects of gold diffusion temperature and time and contact sintering time were determined empirically. A matrix experiment was performed where one parameter was varied, and then another etc., holding the other parameters constant.

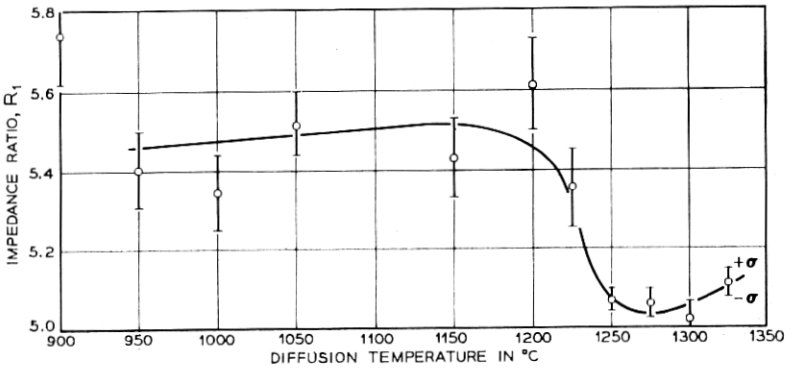

Fig. 8 — Impedance ratio, $R_1 = Z(10\mu A)/Z(50\mu A)$, as a function of gold diffusion temperature. Diffusion time 10 minutes. Contact sinter time 3 minutes.

Selected results of the experiments are shown in Figs. 7 through 16. Each point represents the average of about 40 diodes. Unless indicated otherwise, the gold diffusion temperature was 1300°C, the gold diffusion time was 10 minutes, and the sintering time was 3 minutes.

The effect of gold diffusion temperature on $Z(50\mu A)$, R_1, R_2, noise voltage, capacitance and forward voltage is shown in Figs. 7 through 12. Below about 1200°C the gold diffusion has little effect, but at higher temperatures the diode parameters depend mainly on the gold solubility. Above 1200°C the spread of measurements was also much smaller, which indicates that the bulk rather than the surface prop-

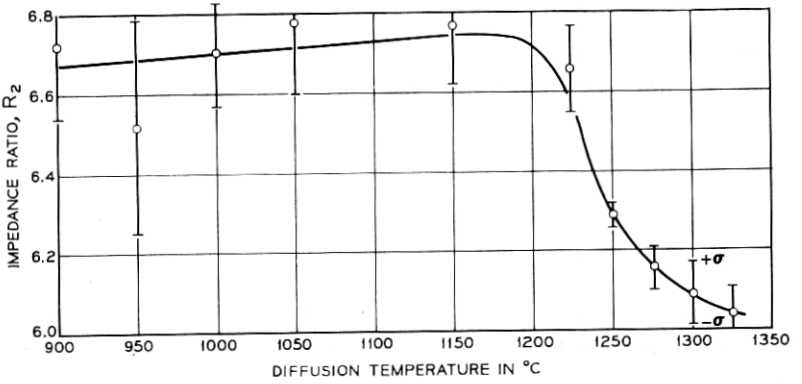

Fig. 9 — Impedance ratio, $R_2 = Z(50\mu A)/Z(300\mu A)$, as a function of gold diffusion temperature. Diffusion time 10 minutes. Contact sinter time 3 minutes.

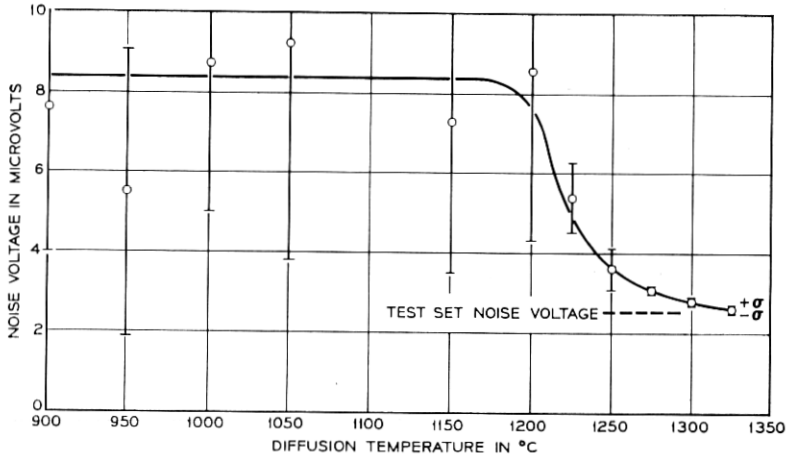

Fig. 10 — Noise voltage (200-3500 Hz) at 2.5μA forward bias current as a function of gold diffusion temperature. Diffusion time 10 minutes. Contact sinter time 3 minutes.

erties were dominant. This information resulted in the choice of a high gold diffusion temperature of 1300°C.

The effect of gold diffusion time on $Z(50\mu A)$, forward voltage and noise voltage is shown in Figs. 13 through 15. At times greater than 10 minutes the forward voltage and noise did not change with time. However, the diode impedance and hence the multiplier, n, did change which means that an equilibrium condition was not reached. Since

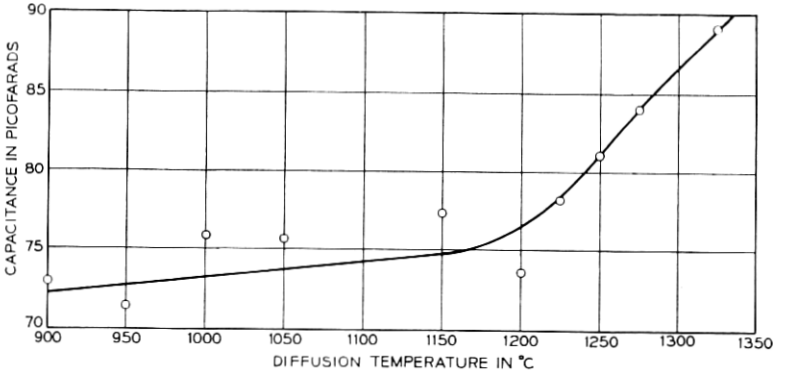

Fig. 11 — Capacitance at 1 MHz and zero bias as a function of gold diffusion temperature. Diffusion time 10 minutes. Contact sinter time 3 minutes.

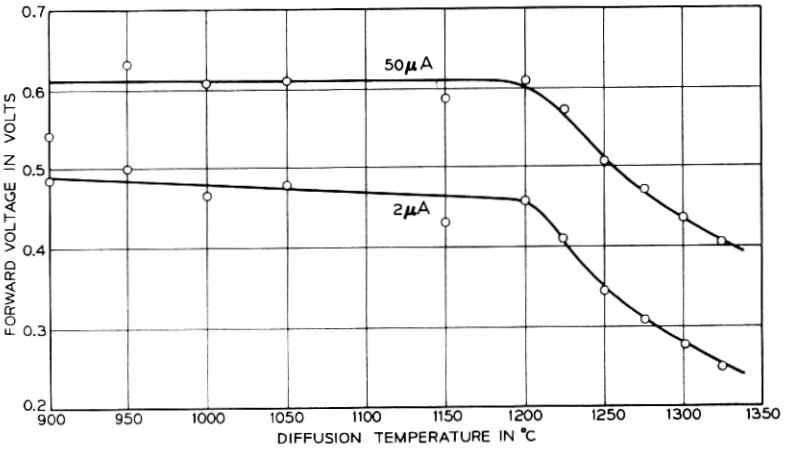

Fig. 12 — Forward voltage at 2μA and 50μA bias currents as a function of gold diffusion temperature. Diffusion time 10 minutes. Contact sinter time 3 minutes.

gold is known to precipitate or collect in phosphorus doped silicon dioxide[19] and at dislocations, as well as to form a complex with phosphorus, equilibrium would not be expected only on the basis that solid solubility had been reached. Ten minutes was chosen for the diffusion time.

The importance of contact sintering time can be seen in Fig. 16 which shows forward impedance, $Z(50\mu A)$, as a function of sintering time. A sintering time of 9.5 minutes was chosen because it corresponds to a standard transistor process which results in good contact adher-

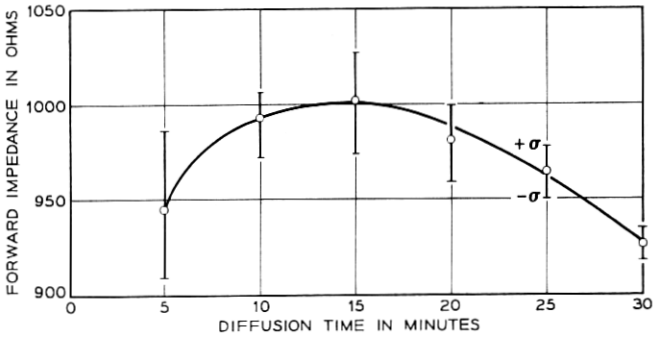

Fig. 13 — Forward impedance at 50μA bias current as a function of gold diffusion time. Diffusion temperature 1300°C. Contact sinter time 3 minutes.

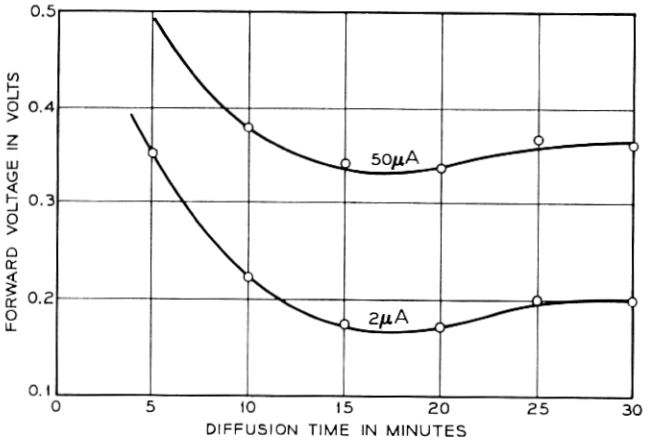

Fig. 14 — Forward voltage at 2μA and 50μA bias current as a function of gold diffusion time. Diffusion temperature 1300°C. Contact sinter time 3 minutes.

ence and because the slope of impedance versus sinter time is low at that time.

Studies were carried out in which the diffusion depth was varied from 0.3 to 0.8 mils while holding the gold diffusion to the standard conditions. There was no effect on diode parameters.

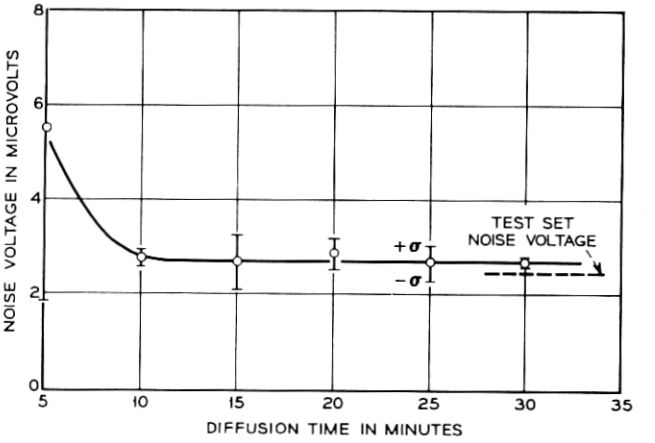

Fig. 15 — Noise voltage (200–3500 Hz) at 2.5μA bias current as a function of gold diffusion time. Diffusion temperature 1300°C. Contact sinter time 10 minutes.

3.4.4 *Electrical Characteristics*

The salient electrical characteristics of the planar diodes namely: forward impedance, impedance ratios and impedance differences are summarized in Table I. The impedance of a typical unit is shown in Fig. 17 in the range of 1μA to 10mA bias. Impedance measurements are made at a frequency of 1000 Hz. In the frequency range of interest, the capacitance has negligible effect on the impedance. In the worst case, at the highest frequency of interest (3500 Hz), and at a forward current bias of 10μA, the capacitive reactance is more than two orders of magnitude greater than the resistive component. Therefore, the difference between the total magnitude of impedance and the resistive component is less than 0.01 percent. The dependence of forward impedance with temperature is shown in Fig. 18 for $Z(50\mu A)$. The temperature coefficient of 0.85 ohms/°C is less than would be predicted directly from (2) and implies a temperature dependence of the multiplier, n, which has been noted elsewhere.[8]

Although no requirements are placed on forward voltage, a plot of forward voltage versus forward current for a typical component diode is shown in Fig. 19 for completeness. It is, of course, the linearity of this semilogarithmic plot which results in the excellent impedance control of the new diodes with current.

The stability requirement placed on the diodes is that the impedance value, $Z(50\mu A)$, should not drift with time; in particular it should not drift in the first few minutes of application of bias. The short term drift, as has been noted, was a problem with the mesa diodes. No short term drift has been detected in the planar diodes by a test system

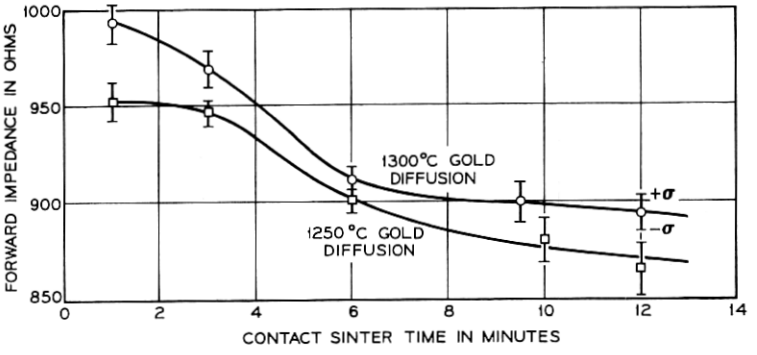

Fig. 16 — Small signal forward impedance at 50μA bias as a function of contact sinter time. Nominal sintering temperature was 625°C.

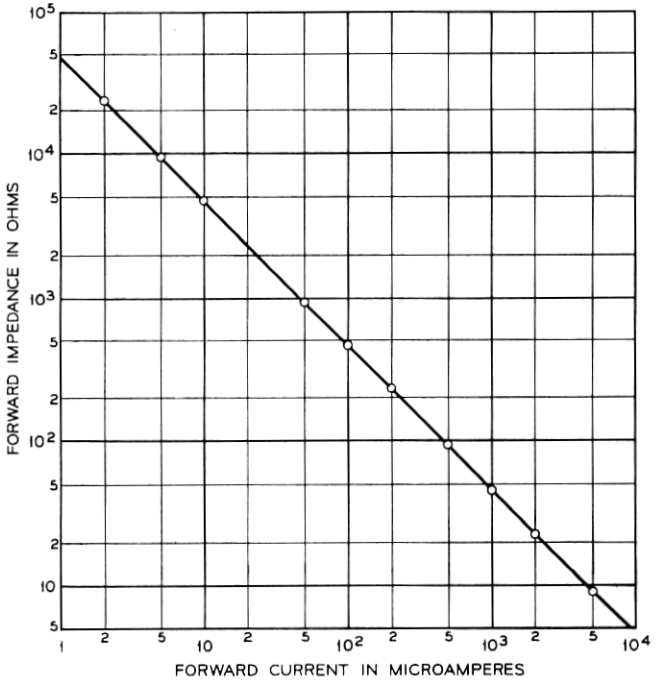

Fig. 17 — Typical forward impedance versus bias current at 25°C for component diode.

capable of detecting a drift of 1 ohm (0.1 percent change). Likewise, no long term drift has been detected either. In one life study a sample of 24 component diodes showed a drift of less than 0.5 percent (which was test set limit) after 4000 hours of greatly accelerated switched power aging (I_0 = 50 mA, V_R (peak) = 5V) at an ambient of 150°C. Another important characteristic is the noise generated by the diodes in the frequency range 200 Hz to 3500 Hz (C message weighting). The noise appears as a hissing sound to the listener when no voice signal is present. Measurements are made with 17,000 ohms in parallel with the diode or diode pair which is what appears in the actual circuit. Since the diode impedance at 2.5 μA is comparable to 17,000 ohms, and the noise voltages add as the square root of the sum of the squares, the measured noise voltage of two diodes in series is actually less than the noise voltage of either diode singly. The circuit requirement was less than 20 μV rms for a compressor pair and 40 μV rms for an expandor pair. Therefore, by requiring a single diode to have less than

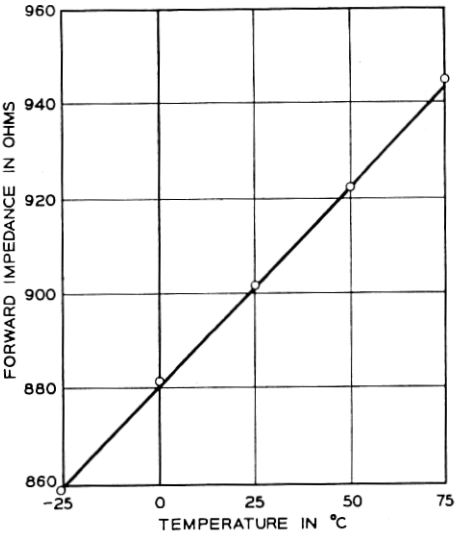

Fig. 18 — Typical forward impedance at 50μA bias current as a function of temperature.

20-μV rms noise, the pairs are guaranteed to meet the 20-μV rms limit. Most diodes had noise voltages less than or comparable to the test set limit of 2.4 μV rms. A check of 862 diodes produced during the development showed only 1 device to fail the noise limit.

Measurements made on noisy mesa diodes and other diodes produced

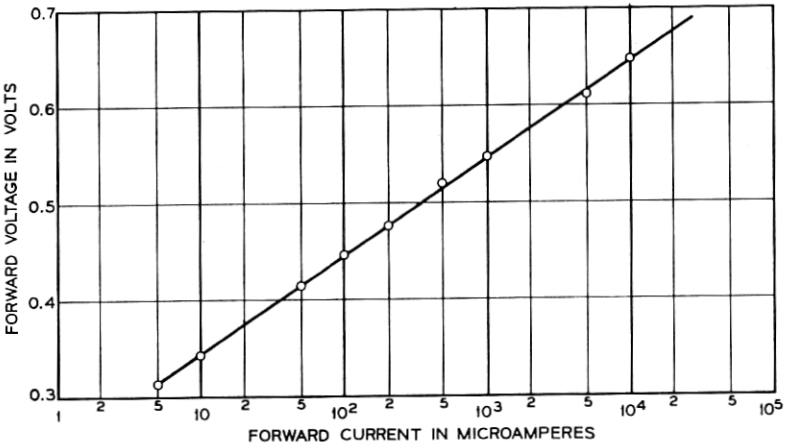

Fig. 19 — Forward current versus forward voltage for typical component diode.

during the development of the planar diode and the reasons for the noise improvement are discussed in the next section.

3.4.5 *Noise Discussion*

The decrease of noise voltage with increasing gold doping can be seen in Fig. 10.* Based on measurements made on units with measur-

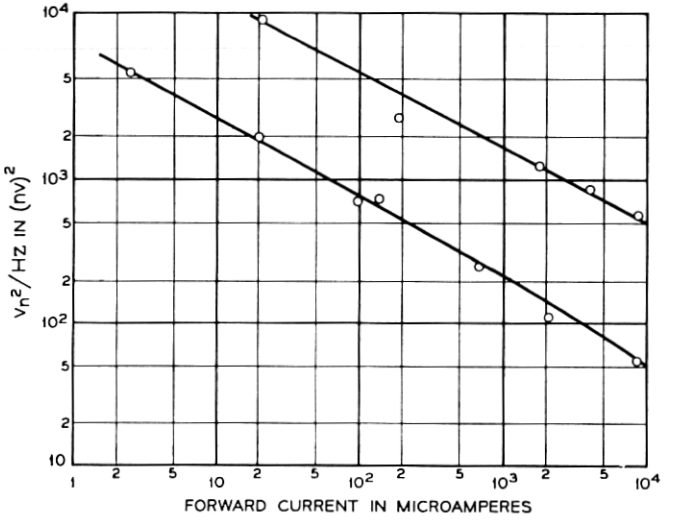

Fig. 20 — Noise voltage squared as a function of forward bias current, I_F, for two noisy development diodes.

able noise, the noise is $1/f$ noise over the audio frequency range, i.e.;

$$\Delta v_n^2 = (\text{const}/f)\Delta f$$

or

$$\Delta i_n^2 = (\text{const}/f)\Delta f,$$

where v_n = noise voltage, i_n = noise current and Δf = small frequency range.

Measurement as in Fig. 20 shows that the dependence of noise voltage on total dc current, I_F, is

$$v_n^2 = (\text{const})/I_F^{0.6}.$$

* Except for the noise voltages plotted in Fig. 10, which are measured as described in the last section, all noise voltages are equivalent open circuit voltages. All noise currents are equivalent short circuit currents.

Because of this dependence of noise voltage on forward current, the noise limit is specified at the low current of 2.5 μA.

Note that because $i_n = v_n/Z_f$ and $Z_f = nkT/qI_F$,

$$i_n^2 = (\text{const})I_F^{1.4}. \tag{12}$$

The decrease of noise at a given forward bias current, I_F, with increasing gold doping may be explained in the following manner. As recombination-generation centers are increased, the forward voltage, V_F, required to attain a given forward current decreases. If there is a secondary current (much less in magnitude than the recombination-generation current), which is the noise generating current, and if the noise due to this current increases with increasing forward bias voltage, then adding gold decreases the forward voltage for a specified current and the decreased forward voltage results in lower noise. This secondary current is quite likely associated with surface, bulk or channel leakage components or excess tunneling current derived from anomalous intermediate energy states.

If the above explanation is correct, the noise current measured at a specified forward voltage should be the same for various gold doping levels. The noise current is compared for a forward voltage of 0.463 volts for several groups from Fig. 10. The reason for comparing noise currents rather than noise voltages will be made clear shortly. Average noise voltages from Fig. 10 were corrected for test set noise and for the parallel 17,000-ohm resistor and converted to noise current.

$$v_n^2 \text{ (corrected)} = v_n^2 \text{ (measured)} - v_n^2 \text{ (set) where } v_n^2 \text{ (set)} = 2.4\mu V$$

$$v_n = v_n \text{ (open circuit)} = v_n \text{ (corrected)} \ (1.7 \times 10^4 + Z_f)/1.7 \times 10^4$$

$$i_n = v_n/Z_f .$$

The V-I characteristics of each group gave the bias current, I_F, for $V_F = 0.463$ volts for that group. The empirical equation (12) was used to find the noise current at this new current, since the constant in (12) could be found from the measurement at 2.5 μA above. Calculations were made for gold diffusion temperatures of 1150, 1200, 1225, and 1250°C where the greatest change in noise appeared to take place. The results, in Table II, are in rather good agreement with the hypothesis that the noise current depends only on the voltage V_F.

The fact that the noise must be described as a current generator (rather than a voltage generator) follows logically from a circuit analysis of the physical diode. An equivalent circuit for the diode is given

TABLE II — NOISE CURRENT AND DC CURRENT AT $V_F = 0.463$ VOLTS.

Gold diffusion temperature	1150°C	1200°C	1225°C	1250°C
I_F	3.75μA	2.5μA	6.0μA	21μA
i_n (short circuit)	1.05nA	0.95nA	1.03nA	1.36nA

in Fig. 21(a), where I_d is the diode current calculated earlier and I_x is an excess current.

An equivalent ac circuit including noise sources is given in Fig. 21(b), where x refers to excess current quantities and d to the dominant diode current quantities. If it is assumed that $I_x \ll I_d$, $Z_x \gg Z_d$ and $i_{nx} \gg i_{nd}$, the circuit of Fig. 21(c) results. The Thevenin equivalent of Fig. 21(c) is shown in Fig. 21(d). The noise voltage, v_n, is dependent on quantities related to two independent currents. The noise voltage measured at a specified voltage, changes with gold doping because Z_f (which equals nkT/I_F) changes with gold doping, while i_{nx} remains constant. Thus, the noise current is directly related to the noise mechanism, while the noise voltage is indirectly related.

As previously mentioned, there are several candidates for the current which produces the excess noise. It does not appear to be associated with bulk recombination current because gold doping does not change it. It could be associated with surface, channel or bulk leakage

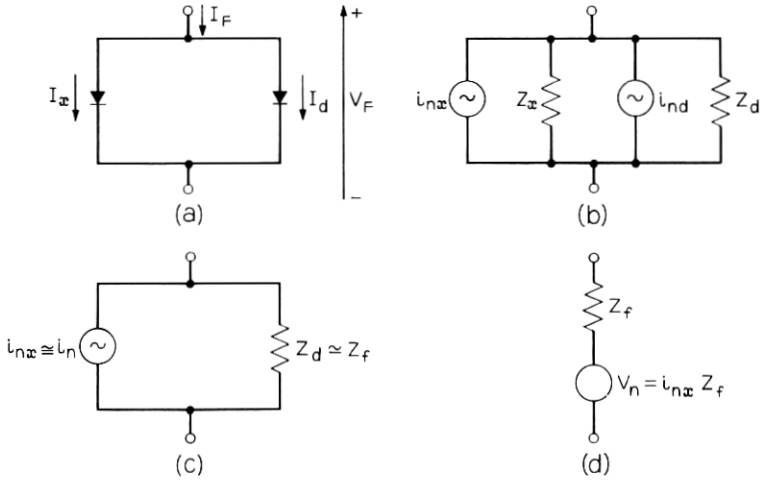

Fig. 21 — Equivalent circuits of diode with noise sources.

currents since $1/f$ noise has been widely reported for these components. It could also be the excess current associated with tunneling[20] since $1/f$ noise has been reported for this current in germanium.[21] While these diodes do not exhibit measurable tunnel current, they are near the tunnel diode doping levels.

IV. CONCLUSIONS

A new semiconductor compandor diode has been developed in which the critical small signal forward impedance characteristics are controlled by bulk material properties. The heavy gold doping employed in this design forces bulk recombination-generation currents to dominate over all surface, channel and diffusion currents and results in a low-noise device with well-controlled electrical characteristics. Oxide passivation and very low resistivity semiconductor material combine to produce an extremely stable device capable of being manufactured at yields governed almost exclusively by assembly workmanship. These devices were initially designed for use in the N2 and N3 Carrier Systems and have also been incorporated into the 3A Echo Suppressor System as a variolosser element.

V. ACKNOWLEDGMENTS

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