A New Reference Frequency Standard for the L Multiplex System

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Four precision quartz crystal oscillators form the heart of a new solid-state precision frequency standard, designed to meet the requirements of the present and next generation of L multiplex carrier equipment. The output frequencies of 64 and 512 kHz are derived from the 4.096-MHz oscillator outputs by binary frequency dividers. A master and standby divider chain form a redundant path linking two of the oscillators and the passive output distribution circuits. Intentional transfers between master and standby channels can be made without introducing significant phase hits at the output. Automatic transfer between channels occurs upon a catastrophic loss of the output signal. Two additional oscillators and dividers are provided as "hot spares" which can be manually patched into service. Critical points in the system are monitored by major and minor alarm circuits, and a very low frequency receiver-comparator provides a means for maintaining the oscillator frequencies to within one part in 10^9 of a vlf standard frequency broadcast.

I. INTRODUCTION

The L multiplex system is a single-sideband suppressed carrier system in which the carrier frequency supplies in the various offices are synchronized by the transmission of pilot frequencies over a tree-like network. At each office the carrier frequencies necessary to perform the modulation and demodulation steps are derived from the outputs of an "office master" supply which is phase-locked to the incoming synchronizing pilot tone. This "office master" supply, named the primary frequency supply in L multiplex terminology, has been described in previous literature.[1]

The tree-like synchronization network originates at a single primary frequency supply called the "system master." While relative frequency accuracy between offices depends on the phase-locked

synchronization network, the absolute frequency accuracy of the pilot tones is dependent upon the absolute frequency accuracy of the system master. Although the free-running accuracy of a primary frequency supply is such that fairly appreciable periods of pilot outage can be tolerated, a highly accurate reference frequency standard is still required to ultimately control the system master.

In the past this frequency standardization service has been provided by Bell Telephone Laboratories, Murray Hill, New Jersey, where the Bell System Primary Standard of Frequency has been maintained to an absolute frequency accuracy of one part in 10^9 by periodic corrections. In recent years the need has arisen to replace the Murray Hill frequency standard with a more reliable and rugged solid-state version which would be located and maintained in a hardened telephone office. The new Bell System Reference Frequency Standard described in this article has been designed to meet these immediate requirements of the present L multiplex system, including recent requirements of the new L-4 coaxial system. In addition, system objectives and requirements for the new standard have been selected in order to anticipate the needs of at least the next generation of multiplex equipment after L-4.

II. SYSTEM OBJECTIVES AND REQUIREMENTS

2.1 *Frequency Accuracy*

The absolute frequency accuracy requirement for the reference frequency standard has been established as one part in 10^9. This requirement meets the needs of the present L multiplex system (including L-4) and should be adequate for any future multiplex systems which may be developed over the useful life of the new standard.

A survey of recent developments in the field of frequency standards and frequency measurement techniques reveals that the above requirement can be met economically and reliably by the use of a solid-state double-oven quartz crystal oscillator as the frequency source and the very low frequency broadcasts of the National Bureau of Standards as a comparison for periodic corrections of the oscillator frequency. The technique of measuring frequency offsets using a vlf receiver-comparator is relatively simple, and accuracies of a few parts in 10^{10} can be obtained in a measuring interval of several hours (see Section IV).

The accumulated oscillator frequency drift during the time between corrections (maintenance interval) is equal to the oscillator drift

rate multiplied by the maintenance interval. This implies that for a minimum maintenance interval of one month, the oscillator drift rate must be less than approximately 5 parts in 10^{10} per week in order to maintain the accuracy requirement of one part in 10^9. This assumes that at the time of maintenance the oscillator is corrected to the lower limit if the drift rate is positive and to the upper limit if the drift rate is negative.

2.2 *System Reliability*

The overall reliability objective for the new standard is that it be able to provide continuous and accurate output signals to the L multiplex system. Although short periods of outage can be tolerated, the new standard has been designed to minimize their probability and duration. These reliability objectives have been met in the following manner:

(*i*) Solid-state circuits are used wherever possible.

(*ii*) Redundant circuits have been provided which are automatically switched into service in the event of catastrophic failures. Other redundant circuits can be manually patched into service in case of double failures or failures in the automatic switching circuits themselves.

(*iii*) Special circuits have been designed which allow routine maintenance checks of the redundant switching equipment to be performed without causing either interruption of service or phase perturbations in the L multiplex synchronization network.

(*iv*) Critical areas in the system are monitored by major and minor alarm circuits. Visual and audible indications of trouble conditions are provided.

(*v*) The equipment comprising the system has been designed to facilitate ease of replacement and repair.

2.3 *L Multiplex Interface*

The interface betweeen the reference frequency standard and the L multiplex synchronization network is the primary frequency supply which has been designated "system master." The requirements of the primary frequency supply thus determine the following requirements of the new standard:

(*i*) Output frequencies should be 64 and 512 kHz to meet the requirements of two existing versions of the primary frequency supply.

(*ii*) The 64- and 512-kHz output signals should be square waves

at an approximate level of −23 dBm (fundamental component) and an impedance of 135 ohms, balanced.

(*iii*) Phase hits introduced at the output because of intentional transfers between master and standby channels should be less than 20 nanoseconds. This requirement allows maintenance transfers to be performed without significantly perturbing the phase-lock circuits in the primary frequency supplies.

III. SYSTEM DESCRIPTION

3.1 *General*

Figure 1 is a block diagram of the circuits comprising the primary signal paths in the reference frequency standard. The output frequency of the precision oscillators is 4.096 MHz, hence binary frequency dividers are used in deriving the output signals of 512 and 64 kHz. There are four precision oscillators (1, 2, 3, and 4) and four frequency dividing channels (A, B, C, and D). A and B are master and standby channels in normal system operation. The outputs of these channels pass through gates which allow either channel A or channel B (but not both) to drive conjugate ports on the 64- and 512-kHz combiner hybrids. The output ports of the hybrids drive resistive distribution buses, and the conjugate ports drive the major alarm transfer circuit which detects a loss of signal at the hybrid output. The gates are under the control of the automatic switch circuit which initiates a channel transfer upon receipt of a command from the major alarm transfer circuit. Provisions are also made for manually reversing the state of the gates.

The phase align and channel transfer circuit in conjunction with the capacitive phase shifters and the magnetic clutch assembly allow intentional manual transfers to be performed which introduce phase hits of less than 20 nanoseconds (less than 4° at 512 kHz) at the output distribution buses. This type of "hitless" transfer is initiated by a pushbutton switch on the front panel which enables the phase align and channel transfer circuit and the magnetic clutch assembly. The shaft of the phase shifter in the off-line channel is then connected to the shaft of a knob on the front panel by energizing the appropriate magnetic clutch. The knob is rotated, and when phase coherence (less than 20 nanoseconds phase difference) of the 4.096-MHz square waves in the two frequency dividers is detected, the counters in the off-line channel frequency divider are reset to zero

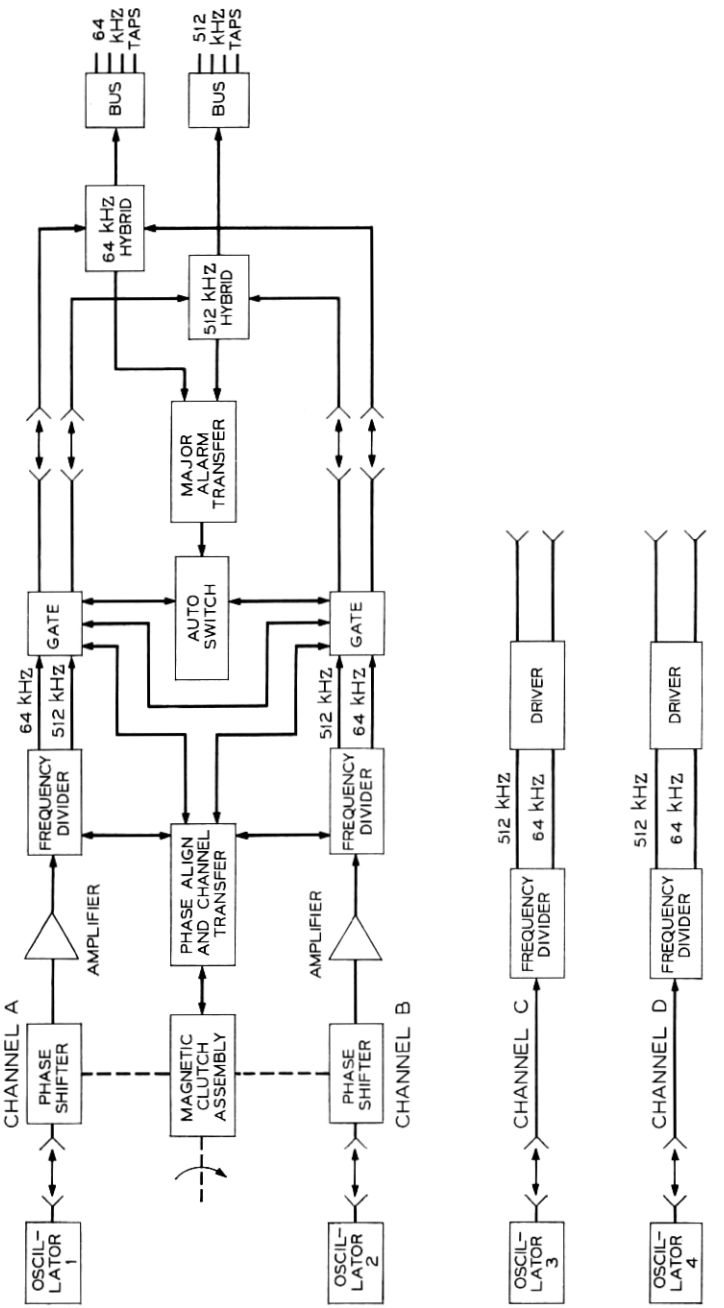

Fig. 1 — Block diagram of principal circuits in reference frequency standard.

upon detection of the all-zero code in the on-line divider. At this instant a command pulse changes the state of the channel gates, thereby effecting the "hitless" transfer. Upon completion of the above sequence, the magnetic clutch is de-energized, and the phase align and channel transfer circuit is returned to its normal state.

For additional redundancy, two "hot spare" channels have been included, either of which can be manually patched into the combiner hybrids should a failure occur in both channel A and B or the common control circuits. These hot spare channels, C and D, are complete with oscillator, divider, and driver circuits.

Manual patching allows any of the four oscillators to be associated with any of the four channels. Under normal conditions, the two most stable oscillators (determined by vlf measurements) would be patched into channels A and B, and the outputs of channels A and B would be connected to the combiner hybrids. The flexibility provided by the manual patches at both the oscillator outputs and the hybrid inputs allows frequency service to be restored under a wide variety of failure conditions.

In addition to the primary circuit functions there are a number of secondary functional blocks which are described in greater depth in sections to follow. They are: power supply circuits (Section 3.5), major alarm circuits (3.6), minor alarm circuits (3.7), vlf receiver-comparator circuits (3.8), and digital time-of-day clock (3.9).

3.2 *Precision Oscillators*

The solid-state precision oscillators used in the reference frequency standard are the double-oven quartz-crystal type.[2, 3] Figure 2 is a block diagram of the oscillator circuit. The crystal is an AT-cut polished plano-convex quartz plate designed to operate on its fifth mechanical overtone in the thickness-shear mode. The crystal is mounted in an evacuated enclosure and is housed in an inner temperature-controlled oven. A vernier frequency adjustment is provided which allows a variation of several parts in 10^7 about a nominal value of 4.096 MHz by changing the bias on a varactor diode. The circuits comprising the oscillator (including the inner oven assembly) are surrounded by an outer temperature-controlled oven for greater temperature stability.

The drift rate for the precision oscillators is a few parts in 10^{10} per week. Figure 3 shows a plot of frequency offset as a function of time over a period of several months for one of the oscillators. Drift rates such as these can only be realized after an initial warm-up

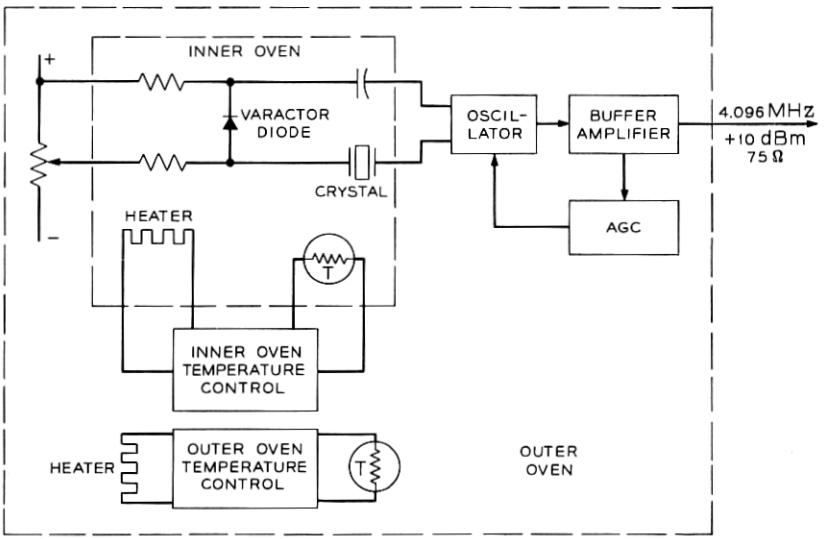

Fig. 2 — Precision oscillator block diagram.

period of approximately one month, during which the frequency gradually stabilizes. Any disruption of power after this time requires another period of stabilization before low drift rates can again be realized. For this reason considerable redundancy has been designed into the oscillator power supply arrangement (see Section 3.5).

3.3 *Binary Frequency Dividers*

The frequency dividers used in the reference frequency standard are six-stage binary counters with output taps at 512 and 64 kHz (see Fig. 4). The input to the counter chain is a 4.096-MHz square wave derived from the oscillator output sine wave signal. The input to the 512-kHz output flip-flop is the result of gating the 4096-, 2048-, and 1024-kHz signals. This technique reduces jitter and eliminates the cumulative delay uncertainty of several counter stages. A similar gating arrangement is provided at the input to the 64-kHz flip-flop. High speed switching transistors with storage times of less than 5 nanoseconds are used in the counter circuits to further reduce delay uncertainty. These techniques are required to insure accurate operation of the phase align and channel transfer circuit and to reduce jitter in the output signals.

Figure 5 is a schematic diagram of a single stage in the counter chain. The "toggle" input is triggered by negative-going pulses, and

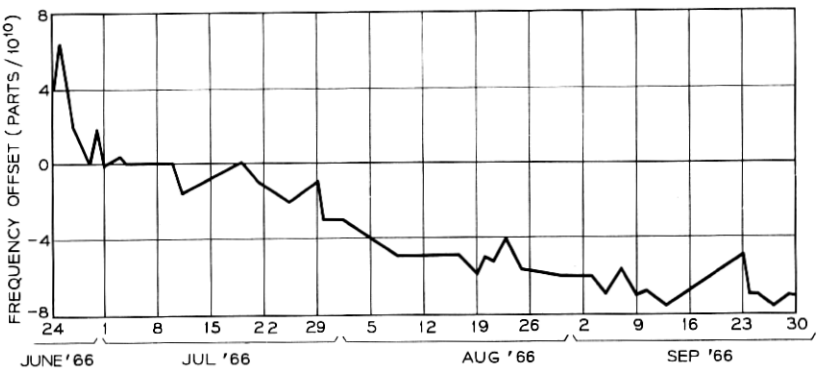

Fig. 3 — Typical precision oscillator drift characteristics.

a positive pulse at the "reset" input forces the output to a logic zero, corresponding to the saturation voltage of the transistor.

3.4 *Phase Align and Channel Transfer Circuits*

The purpose of the phase align and channel transfer circuits is to allow the initiation of an intentional transfer between channels A and B which introduces a phase hit of less than 20 nanoseconds at the output buses. The basic transfer sequence is described in Section 3.1. Fundamentally, the circuits must detect the phase coincidence of the 4.096-MHz square waves in both channels and the all-zero

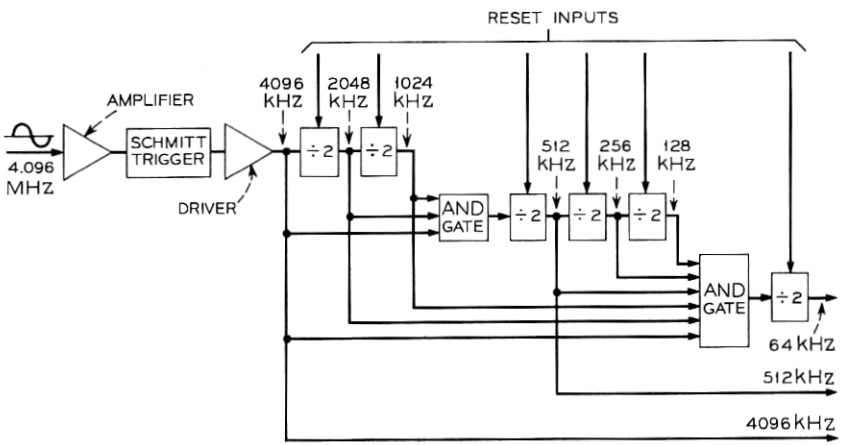

Fig. 4 — Frequency divider circuit.

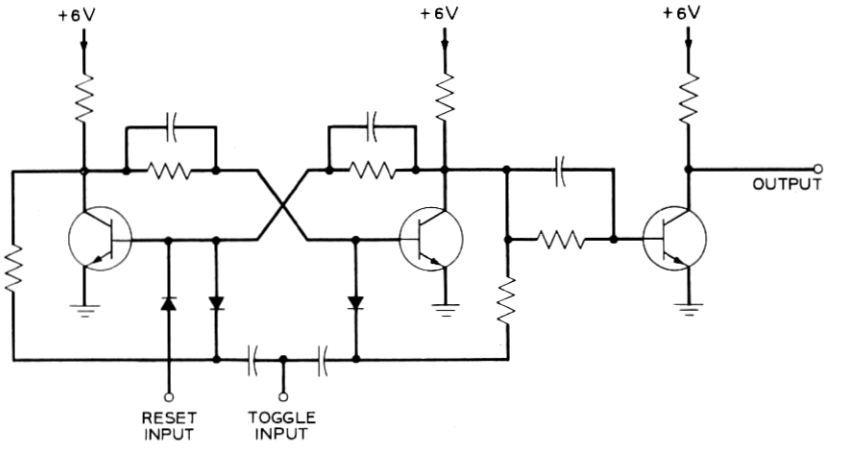

Fig. 5 — Binary flip-flop circuit.

code in the on-line channel in order to generate properly timed reset pulses for the off-line divider and channel transfer commands for the automatic switch circuit. Figure 6 is a block diagram of the detection and pulse generating circuit.

The shapers (see Fig. 7) generate narrow pulses of less than 10

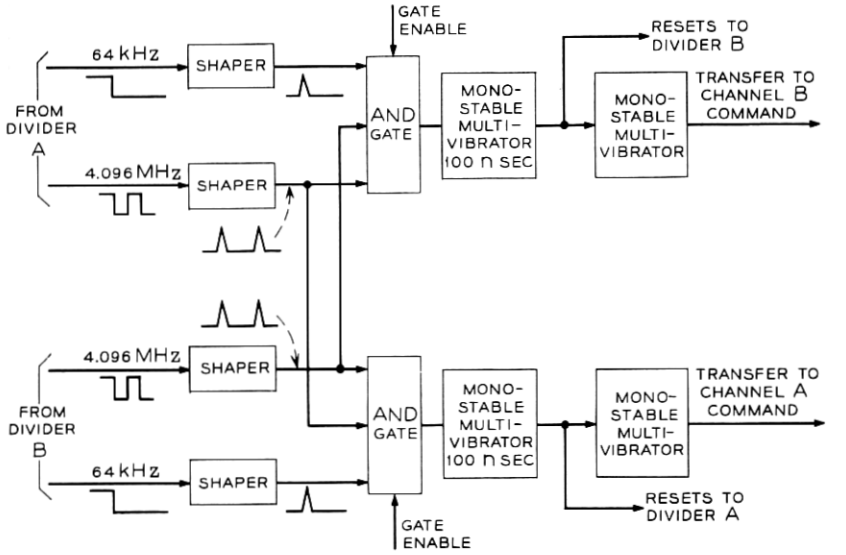

Fig. 6 — Phase align and channel transfer, phase coincidence circuit.

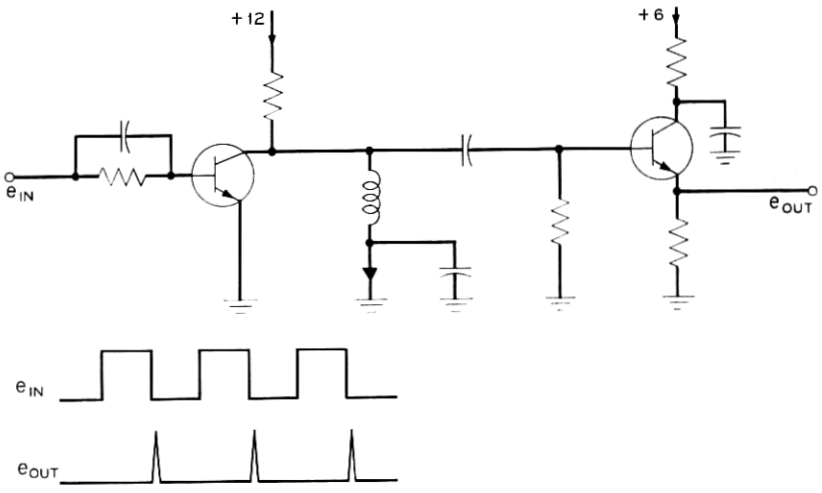

Fig. 7 — Shaper circuit.

nanoseconds basewidth from the negative-going portions of the input square waves. When the phase align and transfer circuit is activated, the appropriate diode AND gate is opened and the output of the gate is a properly timed trigger pulse which occurs only when the 4.096-MHz signals are in phase and at the precise instant of the all-zero code in the on-line channel frequency divider. A 100 nanosecond monostable multivibrator, which is triggered by the pulse, generates reset pulses for the off-line divider before the next 4.096-MHz cycle and inhibits the diode AND gate. A second monstable multivibrator which is triggered by the reset pulse generates the transfer signals for the channel gates. A special mode is provided for tests which allows the off-line counters to be reset but inhibits the output of the second monostable multivibrator, thus preventing an actual channel transfer.

3.5 *Power Supply Circuits*

In the frequency standard, dc-to-dc converters have been used to isolate critical circuits from noise and voltage fluctuations associated with the central office battery. A total of eight converters are used in the system. Four converters supply power to the oscillators and four to the digital circuits. The modular plug-in construction of the converters facilitates replacement.

A redundancy scheme is followed in the fusing and distribution of

the regulated voltages so that no single converter failure will cause a catastrophic failure at the output of the distribution buses. Figure 8 illustrates the redundant power feed arrangement for the precision oscillators. Office battery voltage is brought to the frequency standard cabinet over two independent fused paths from the battery bus. Two high-power silicon diodes form an OR gate which allows either path to fail (either open or short) without disrupting power to the dc-to-dc converters. The outputs of each pair of converters are also passed through OR gates so that any one of the four converters may fail without disrupting power to any oscillator. The fusing arrangement insures that no single failure in either a diode, a converter, or a fuse to the left of the dotted line in Fig. 8 disrupts power to any oscillator.[4] This fusing scheme also allows power to be temporarily removed from faulty diodes or converters, thereby allowing repairs to be made without disrupting power to the parts of the system not directly affected by the failure. A fuse alarm contact is provided on each fuse. This contact is connected to the fuse input if the fuse should blow, thereby notifying the appropriate minor alarm circuits.

3.6 *Major Alarm Transfer Circuits*

The major alarm transfer circuits monitor the output signal levels and generate a central office major alarm should the levels fall outside preset limits. Figure 9 is a block diagram of the circuit. The alarm circuits are driven from the ports of the 64- and 512-kHz hybrids which are conjugate to the ports driving the distribution buses. Two

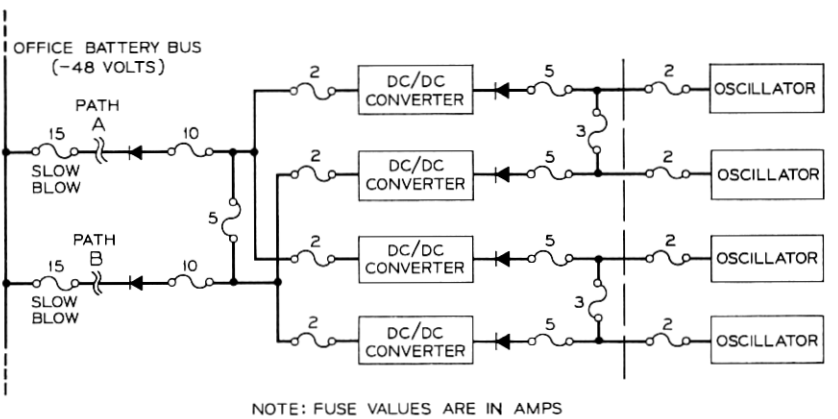

Fig. 8 — Oscillator power supply circuit.

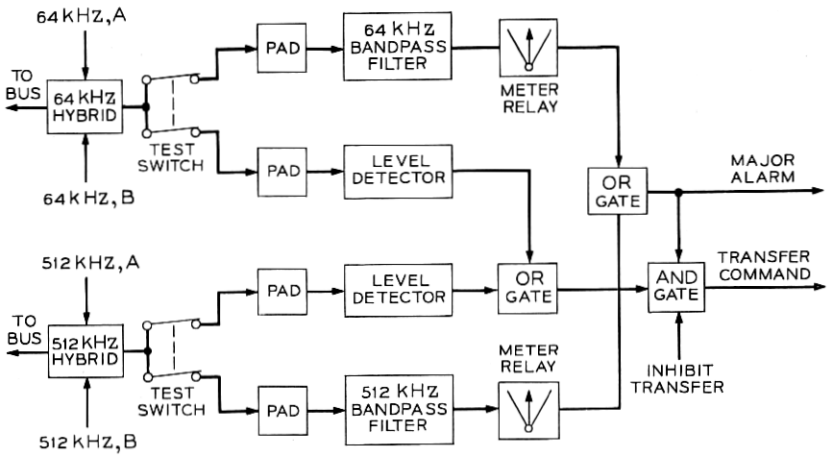

Fig. 9 — Major alarm transfer circuit.

monitoring channels are driven from each hybrid. One channel drives a meter-relay with adjustable upper and lower limits. The bandpass filter in series with the meter allows this channel to detect gross frequency shifts as well as level variations. The second channel contains a circuit which detects a catastrophic loss of level. A central office major alarm is generated if either or both the meter indications drift outside the present limits of a few dB above or below the nominal level of −23 dBm. A command which initiates an actual channel transfer is generated only if both monitoring channels detect a fault. This logic insures that a single failure in either monitoring channel does not generate a needless transfer and a possible phase hit at the output.

An input from the minor alarm circuits prevents an automatic transfer if a minor alarm condition exists in the off-line channel. Test switches are provided which allow a failure to be simulated, thereby verifying the proper operation of the major alarm circuits and the redundancy switch. This test can be performed without introducing a phase hit at the output by first using the phase align and channel transfer procedure to bring the two signals into phase coincidence.

3.7 *Minor Alarm Circuits*

The minor alarm circuits monitor critical points associated with the oscillators, frequency dividers, and power supplies. In case of a failure in any of the monitored circuits, the central office alarm is

activated and lamps on the front of the cabinet allow the trouble to be quickly isolated.

In order to insure a prompt indication of any significant shift in the output frequency of the oscillators driving channels A and B, the circuit shown in Fig. 10 constantly monitors the frequency offset between channels A and B. A similar circuit monitors the frequency offset between channels A and C. Two meter-relays with adjustable upper limits provide the alarm initiation. The meters are calibrated to read 12 parts in 10^9 full scale. Assuming that the frequency of only one of the three channels drifts out of limits, simple relay logic determines which of the three channels contains the fault. The monitoring circuit (Fig. 10) uses a balanced modulator followed by a low-pass filter to generate the difference frequency. Zero-crossings of the difference frequency are counted by a six-stage counter for a 10-minute interval, and the count is read into a register. The binary output of the register is translated by a digital-to-analog converter into a signal which is proportional to the number of zero-crossings of the difference frequency in a 10-minute interval. Each count represents a phase shift of 180° between the two 4.096-MHz signals, or 122 nanoseconds. This corresponds to a fractional offset of 2.04 parts in 10^{10} per count. With a six-stage counter, 63 discrete nonzero levels exist, hence a full count of 63 represents 12.9 parts in 10^9 frequency offset between channels. The signals which control the gates and reset the counters at 10-minute intervals are derived from the binary coded decimal time code outputs of the digital time-of-day clock by a decoder circuit.

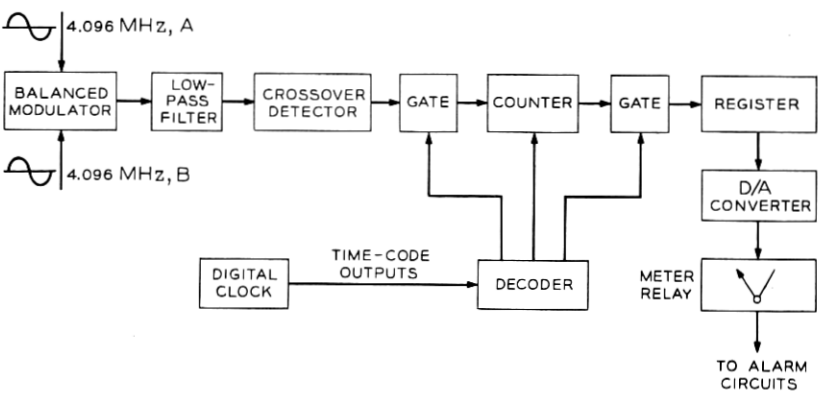

Fig. 10 — Difference frequency detector.

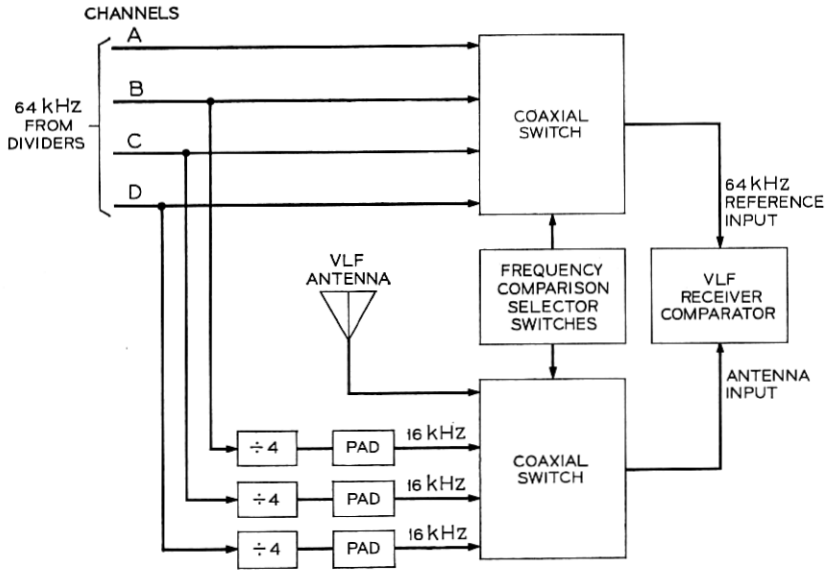

Fig. 11 — VLF receiver-comparator mode-select circuits.

Several other points in the system are monitored by various minor alarm circuits. They are:

(*i*) Inner oven heater voltage for each of the four oscillators (deviations about a nominal level of more than one volt generate a minor alarm).

(*ii*) Output of each frequency divider (loss of output of any off-line divider generates a minor alarm).

(*iii*) Oscillator power supplies (deviations of more than one volt generate a minor alarm).

(*iv*) Digital power supplies (loss of any supply generates a minor alarm).

(*v*) Fuses (any blown fuse generates a minor alarm).

3.8 *VLF Receiver-Comparator Circuits*

The vlf receiver-comparator circuits allow accurate frequency comparisons to be made between any of the four channels and any receivable vlf station. Frequency comparisons between any two channels are also possible. This feature allows frequency standardization to continue using any of the four oscillators as a local standard should

normal vlf receptions be impaired for significant periods of time, such as during a national disaster.

Figure 11 is a block diagram of the vlf receiver-comparator circuit. The selector switches on the front panel (see Fig. 17) allow any one of the ten possible frequency comparison modes to be selected. Intercomparisons between channels A and B, for example, are made by connecting the 64-kHz signal from channel A to the reference frequency input of the receiver and a low-level 16-kHz signal derived from channel B to the antenna input of the receiver. This frequency division to 16 kHz is necessary since neither 64 kHz or 32 kHz are valid received frequencies for the vlf receiver-comparator.

The vlf receiver-comparator accepts a 64-kHz reference signal input. The receiver then synthesizes a 1.1-kHz signal from this 64-kHz

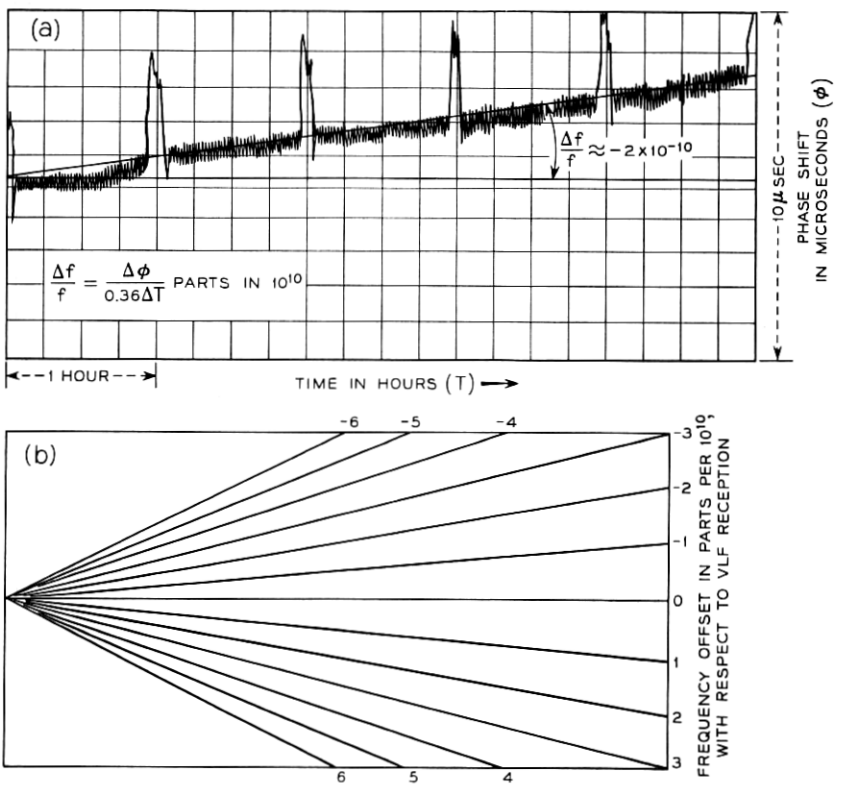

Fig. 12 — (a) VLF strip-chart recording and (b) frequency offset template.

input and phase corrects it to a 1.1-kHz signal derived from the antenna input. The accumulated phase difference between the two 1.1-kHz signals is plotted on a strip-chart recorder, from which accurate frequency offsets can be easily computed (see Section IV).

3.9 *Time-of-Day Clock*

The digital time-of-day clock is driven from the alarm port of the 64-kHz combiner hybrid (see Fig. 1). Days, hours, minutes, and seconds are displayed on the panel by indicator tubes, and controls are provided which allow the clock readout to be synchronized with a suitable time-standard broadcast. The digital clock also generates a time code (binary coded decimal) which is used by the difference frequency detecting circuits (see Section 3.7) in deriving the periodic control pulses.

IV. FREQUENCY STANDARDIZATION

The technique of accurate frequency offset measurements using a vlf receiver-comparator is relatively simple and has attained widespread use in recent years.[5, 6] Because of the effects of propagation anomolies during sunrise, sunset, and darkness, vlf measurements usually are made only when both the vlf transmitter and receiver are in daylight. A typical strip chart recording is shown in Fig. 12a. The plot shows the phase difference between the 1.1-kHz signal derived from the 64-kHz source and the 1.1-kHz signal derived from the vlf

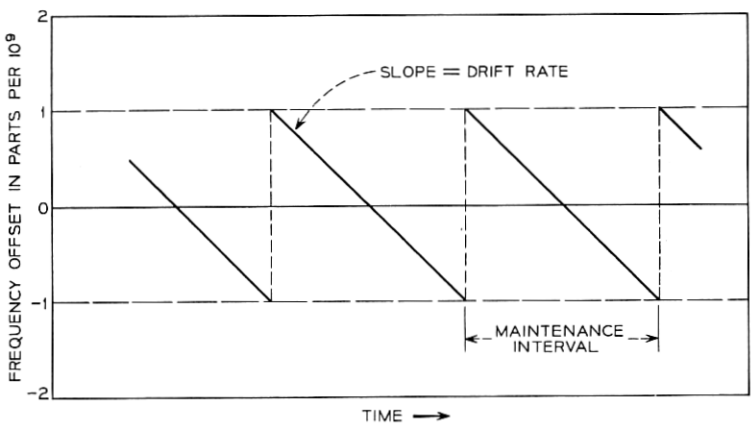

Fig. 13 — Maintenance of oscillator frequency accuracy by periodic corrections.

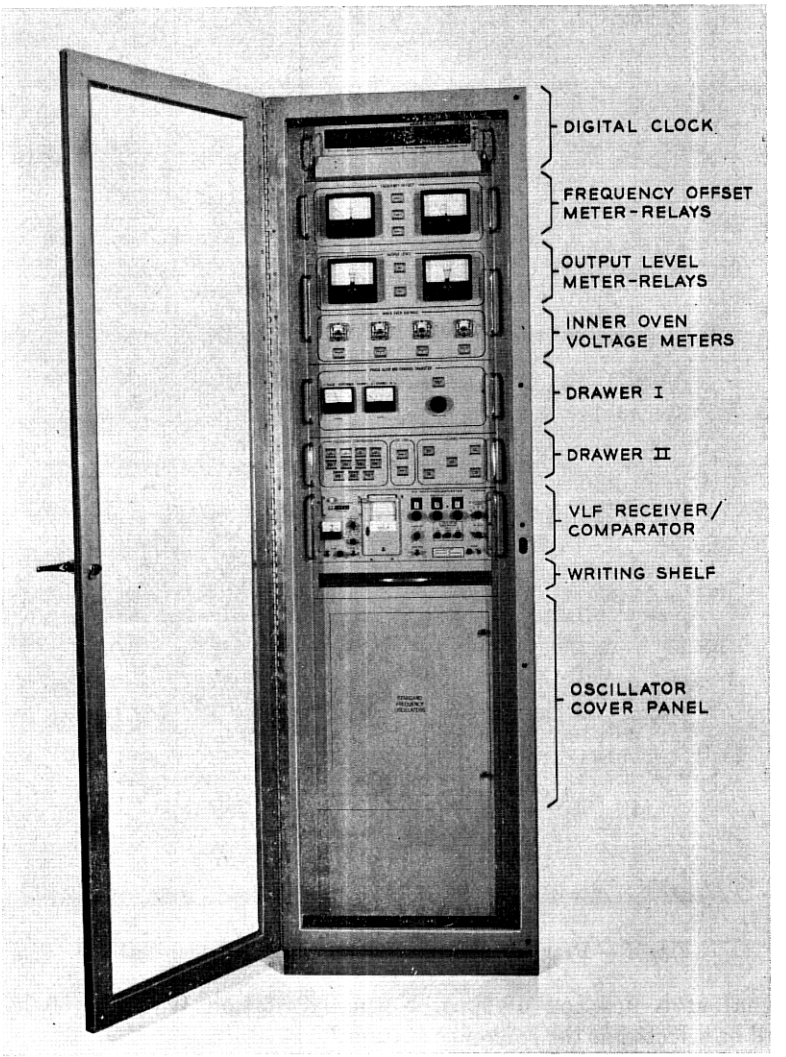

Fig. 14 — Front view of reference frequency standard cabinet.

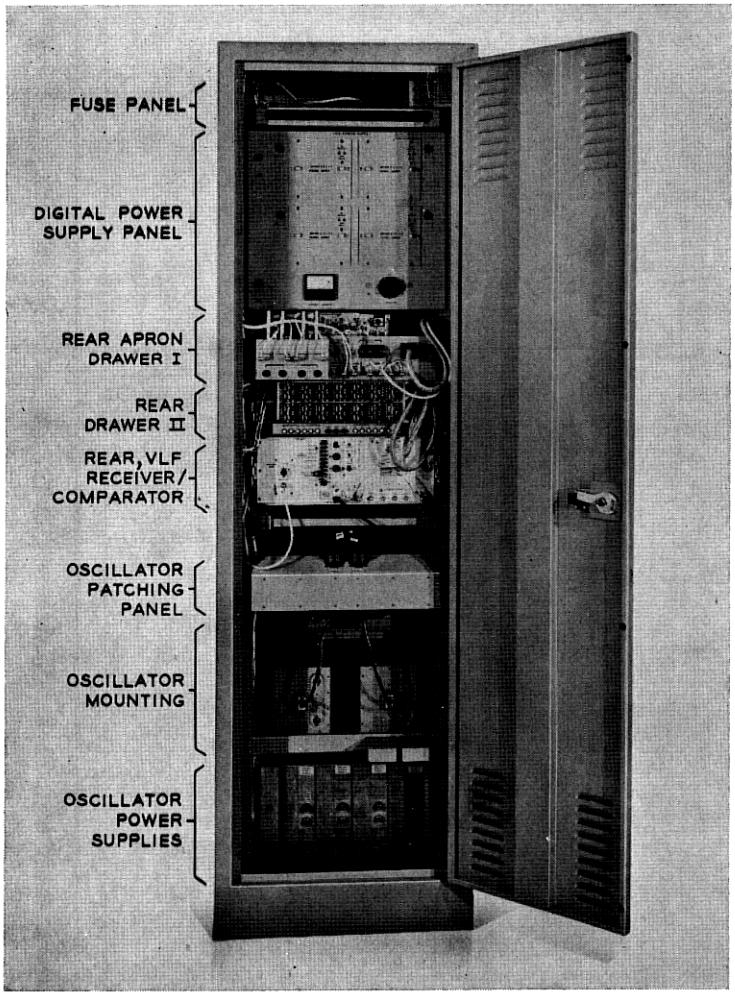

Fig. 15 — Rear view of reference frequency standard cabinet.

signal as a function of time. Normally, station WWVB (60 kHz) will be selected as the reference station.*

The phase offsets which occur every hour are introduced by WWVB to serve as identification. The fractional frequency offset is simply

* Station WWVB, Fort Collins, Colorado is operated by the National Bureau of Standards Time and Frequency Division at Boulder, Colorado. The 60-kHz transmitted signal is based on the atomic second which is defined in terms of a specified transition between electron energy levels of Cesium-133.

the ratio of the accumulated phase shift to the time interval over which the phase shift occurs. For the example shown in Fig. 12a this ratio is approximately 2 parts in 10^{10}, the sign of the slope indicating that the oscillator frequency is low with respect to WWVB. Measurements of this type can be quickly made with the aid of a special transparent template which is calibrated directly in fractional parts in 10^{10} as shown in Fig. 12b.

The procedure for maintaining an oscillator to within one part in 10^9 of WWVB transmissions is as follows. A series of weekly frequency offset measurements are made in order to establish the oscillator's approximate drift rate. The maximum allowable maintenance interval is then determined based on the drift rate and the accuracy requirement of one part in 10^9. A plot of frequency offset versus time for an oscillator being maintained to the above accuracy is shown in Fig. 13. The periodic correction of 2 parts in 10^9 is made using the calibrated vernier frequency adjustment on the oscillator.

V. EQUIPMENT DESIGN

The equipment comprising the reference frequency standard is housed in a special seven-foot high steel cabinet which is designed

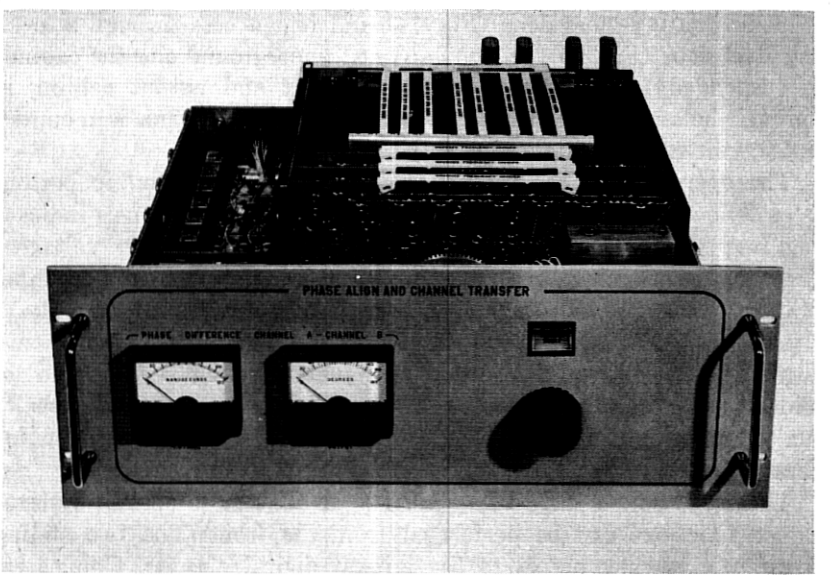

Fig. 16 — Drawer I.

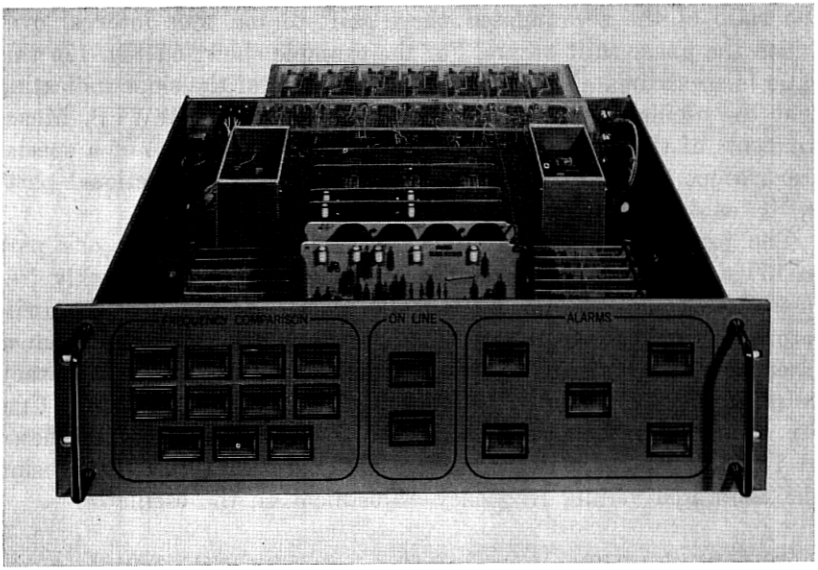

Fig. 17 — Drawer II.

to mount standard 19-inch panels or drawers. Front access is through a locking safety-glass door (Fig. 14) and rear access through a locking steel door (Fig. 15). In the hardened underground site the cabinet is suspended from shock mounts. All input and output cabling is through holes in the top of the cabinet. The vlf antenna is mounted outside the entrance to the site.

The overall front cabinet panel arrangement from top to bottom is as follows: digital clock (mounted on slides); meter panels indicating frequency offset, output levels, and inner oven heater voltages; drawer I containing frequency dividers, phase align and channel transfer circuits, and certain alarm circuits (mounted on slides); drawer II containing frequency comparison selector switches and logic, difference frequency circuits, and alarm circuits (mounted on slides); vlf receiver-comparator (mounted on slides); writing shelf; and oscillator panel which swings open for access to precision oscillators.

The front panels have been designed so that most normal maintenance functions can be performed from the front. The two sliding drawers give easy access to the critical digital circuits. Connectors at the rear of each drawer allow the entire drawer to be easily

removed from the cabinet should extensive maintenance be required.

Drawers I and II are shown in Figs. 16 and 17, respectively. The meters on the front panel of drawer I display the phase difference between the 4.096-MHz signals in dividers A and B and between the 64-kHz signals in dividers A and B. The pushbutton initiates the operation of the phase align and channel transfer circuits, and the knob allows the off-line phase shifter to be rotated. The meters indicate proper operation of the circuit when they read zero after the channel transfer has occurred.

The front panel of drawer II contains the frequency comparison selector switches which allow any possible frequency comparison to be made by the vlf receiver. On-line indicator lamps and various major and minor alarm lamps are also on this panel as well as the alarm cutoff pushbutton switch which silences the office alarm.

A major portion of the circuits in the frequency standard are mounted on printed wiring plug-in cards for ease and speed in replacement of defective units. The cards on which high-speed logic is performed have a solder-plated ground plane on the component side as shown in Fig. 18. This ground plane is returned to chassis ground via the connector. In this manner a good sink is provided for the large transient ground currents which are generated by the high-speed switching circuits. Other low-speed circuits are mounted on a more standard card of the type shown in Fig. 19.

The units which can be reached from the rear of the cabinet (see

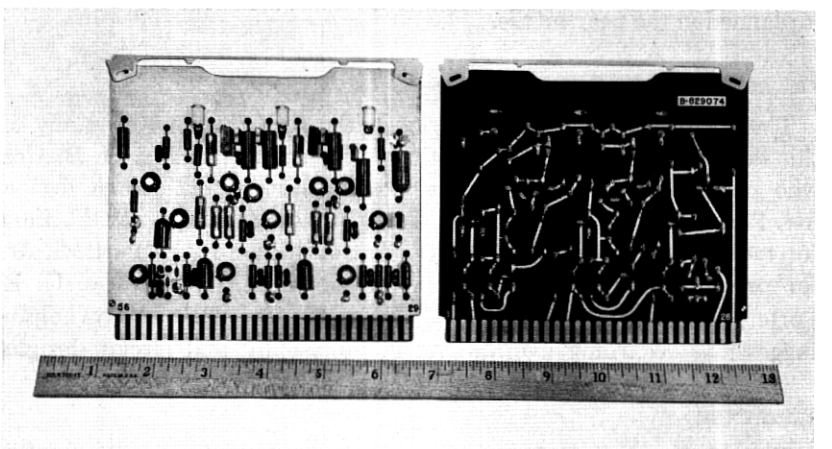

Fig. 18 — High speed plug-in card: (a) component side, (b) printed wiring side.

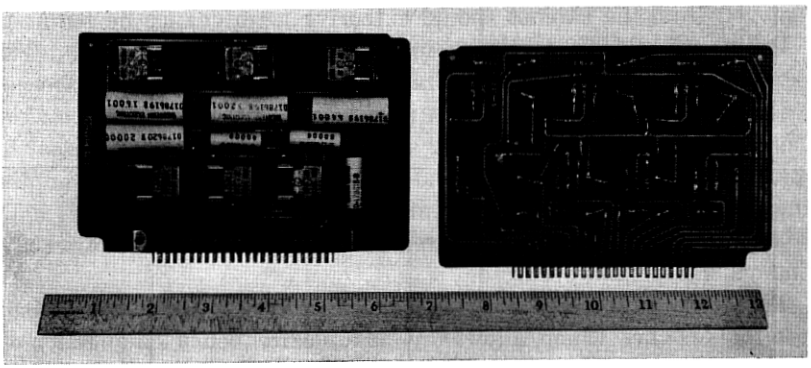

Fig. 19 — Standard plug-in card: (a) component side, (b) printed wiring side.

Fig. 15) are (from top to bottom): fuse panel; digital power supply panel; rear panels of Drawers I and II; rear panel of vlf receiver; oscillator patching panel; rear of oscillators; and oscillator power supply panel.

VI. CONCLUSIONS

The new Bell System Reference Frequency Standard has been designed to meet the frequency accuracy, reliability, and maintainability requirements of the present L multiplex system as well as the next generation of carrier equipment. The system has been installed and tested in the hardened underground telephone office, and a cutover is planned in the near future.

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