Analysis and Synthesis of a Digital Phase-Locked Loop for FM Demodulation

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A method of synthesizing a general nth order phase-locked loop is presented. In contrast to conventional phase-locked loops, the circuitry is digital rather than analog. The general circuit consists of an assembly of logic blocks (gates and storage elements) which, when driven by external clock signals, exhibits phase-locked loop properties. These properties, along with high stability and the absence of adjustments, make the digital phase-locked loop ideally suited for use in large systems which use monolithic integrated circuits for microminiaturization. Analysis and synthesis techniques make use of Z-transform methods in achieving the desired frequency response as the realization of an nth order difference equation. A general technique is developed and two specific cases, $n = 1$ and $n = 2$, are considered in detail. Analytic results relating to the phase-locked loop's static and dynamic performance are derived and found to correlate well with laboratory results for actual circuits.

I. INTRODUCTION

A new phase-locked loop (PLL) with interesting properties has been developed for potential application in large multiple data set installations which provide low speed serial data communications for time-shared computers. An objective for such data set arrangements is to minimize cost per channel by putting the major part of the required circuitry into a common section where it may be shared by all channels. This objective is achieved by using a digital PLL as an FM demodulator with low cost logic circuits located in the channel units and clocks with their associated driving amplifiers located in the common circuits. PLL's which use analog circuits have received considerable attention and analysis and synthesis methods

are available.[1, 2] However, the circuits covered here are digital, and the approach is similar to that of digital (or sampled-data) filters.[3, 4] By using a digital PLL, no low-pass filter or voltage-controlled oscillator, generally associated with the feedback loop of conventional PLL's is required.* This property, along with high stability and the absence of adjustments makes the digital PLL ideal for microminiaturization using monolithic integrated circuits.

This paper presents snythesis procedures for an nth order digital PLL. The PLL realized by such a procedure possesses a response which obeys a linear nth order difference equation. Analysis is performed using Z transform methods commonly encountered in sampled-data control systems.[5] The technique is that of establishing a mapping between the s plane and the z plane so that a correspondence between the coefficients of the controlling nth order difference equation and the desired s plane poles may be established. An iterative circuit is presented so that once the coefficients are determined, the nth order loop may be realized.

The remainder of the paper is devoted to the synthesis, realization, and analysis of two specific examples, $n = 1$ and $n = 2$. Both systems are analyzed to determine static and dynamic performance, and the results of data transmission tests are given. The out-of-lock behavior as well as internal noise resulting from jitter is characterized for the first order PLL. The second order PLL is representative of higher order systems and the analysis is easily extended. The "capture phenomenon" associated with underdamped systems is encountered. In both of the examples considered, experimental results are found to correlate well with theory.

II. THE DIGITAL PHASE-LOCKED LOOP

As a prelude to the synthesis procedure we show that the loop response of the PLL can be expressed as an nth order difference equation. Figure 1 is a block diagram of the loop. Among its basic components are an exclusive OR comparator which develops an output gating function dependent upon the phase relation of its inputs, and a transmission gate acting on several clock signals f_i, g_i to provide inputs to register circuitry. When the loop is locked, a shift circuit periodically transfers the contents of the $(i - 1)$th register to the ith register; the period is one half that of the input signal. The shift

* Although no internal loop filter is needed, a low-pass filter is required to recover the demodulated baseband signal.

TABLE I — SYMBOL

α_j	Real part of z-plane pole, z_j.
β_j	Imaginary part of z-plane pole, z_j.
γ, δ	Parameters pertaining to stability analysis of second order PLL.
Δ	Normalized total input frequency deviation.
Δf	Total input frequency deviation.
Δf_L	Lock range of PLL.
Δv	Voltage step.
Δv_N	Peak-to-peak noise voltage.
Δv_{sig}	Peak-to-peak signal voltage.
ϵ_0, ϵ_0', ϵ_1	Time errors resulting from phase discontinuity when switching between clocks.
μ	Real and imaginary parts of Butterworth characteristic with carrier frequency input.
$\xi(k)$	Duration of kth positive (logical "1") level of feedback (flip-flop) signal.
$\rho(k)$	Interval between kth and $(k + 1)$th zero crossing of input signal.
σ_j	Real part of s-plane pole, s_j.
$\tau(k)$	Duration of kth positive (logical "1") level at exclusive- OR output.
ω_c	Radial cutoff frequency of low-pass filter.
ω_j	Imaginary part of s-plane pole, s_j.
C	Counting capacity of N-stage counter.
E	Input voltage.
E_f	Feedback voltage.
E_0	PLL output voltage.
f	Frequency of input signal.
f_a, f_b	Discrete input frequency.
f_c	Cutoff frequency of low-pass filter.
f_m	Average input (carrier) frequency.
f_r	Rest frequency of PLL.
f_u, f_l	End point of frequency lock range.
f_i, g_i	Clock frequencies ($i = 1, 2, \cdots, n$); also denotes input to registers.
F_i, G_i	Normalized clock frequencies ($i = 1, 2, \cdots, n$).
$H(s)$	Transfer function (Butterworth).
i	$(-1)^{\frac{1}{2}}$.
i, j, k, l	Counting indices.
M	Threshold of final register.
n	Order of system; number of registers.
N	Number of counter stages per register.
N_m	Minimum N for stable operation.
s_j	jth s-plane pole.
t	Time.
T_d	Period of baseband data signal.
T_1, T_2, T_3, T_4	Signal durations for stability analysis.
$v(k)$	Average output voltage during kth interval
$v(t)$	Continuous time function.
v_2	Average output voltage for parasitic mode.
z	Argument of z-transform.
$Z[v(k)]$, $V(z)$	Z-transform of $v(k)$.

(and reset of the first register) is controlled by the nth register which provides an output pulse after the Mth clock pulse is counted. A flip-flop converts the output pulse train to a square wave and provides an input to the comparator.

The difference equation describing operation of this circuit is developed with the aid of waveforms shown in Fig. 2, which gives the

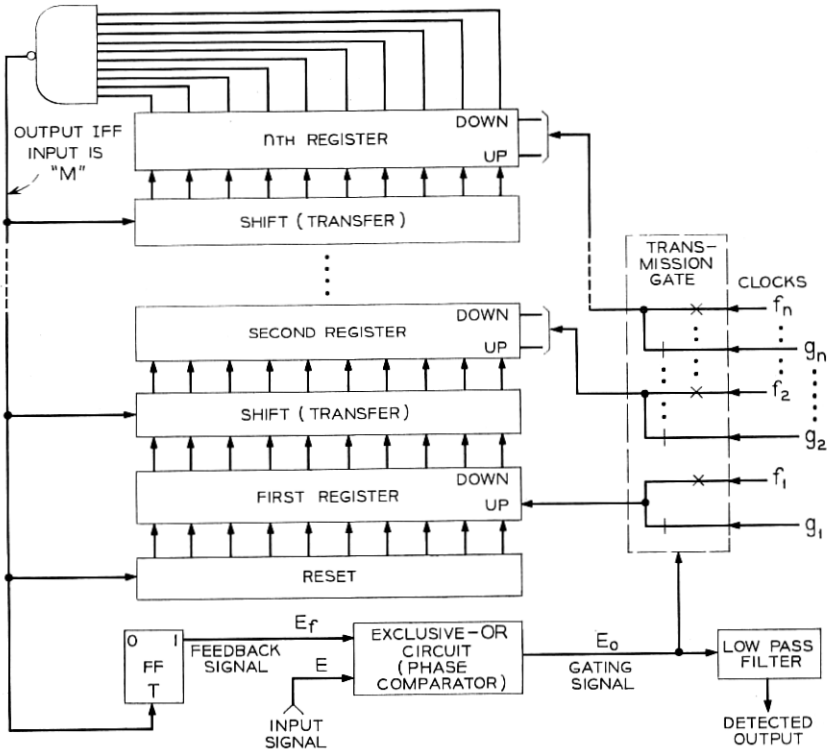

Fig. 1 — Block diagram of general digital PLL.

steady-state terminal signals for the comparator. The output signal is the gating function. Assume that clocks $g_1, g_2, g_3, \ldots, g_n$ are enabled during the "0" level, and all other clocks $f_1, f_2, \ldots, f_n$ are enabled during the "1" level. With the first register initially cleared, its count at the conclusion of the $(k+1)$th period of gating is $g_1[\rho(k) - \tau(k)] + f_1\tau(k+1)$. During each successive period, this count is shifted into the ith register and augmented by a count of $g_i[\rho(k+i-1) - \tau(k+i-1)] + f_i\tau(k+i)$ for $i = 2, 3, \ldots, n$. The count propagates through the n registers where, upon reaching the number M at the nth register, the count is reinitiated. Although n periods are required for a complete count cycle, the process may be thought of as the interleaving of cycles initiated ρ seconds apart.

III. GENERAL FORM OF THE DIFFERENCE EQUATION

It can be seen from Fig. 2 that the count of the nth register is the sum of pulses counted during the intervals $\rho(k) - \tau(k)$, $\rho(k+1) - \tau(k+1), \ldots, \rho(k+n-1) - \tau(k+n-1), \tau(k+1), \tau(k+2), \ldots, \tau(k+n)$. Summing the counts for the sources $f_1, f_2, \ldots, f_n$, $g_1, g_2, \ldots, g_n$ and equating the sum to M gives

$$\begin{aligned} g_1[\rho(k) - \tau(k)] + g_2[\rho(k+1) - \tau(k+1)] + \cdots \\ + g_n[\rho(k+n-1) - \tau(k+n-1)] \\ + f_1\tau(k+1) + \cdots + f_n\tau(k+n) = M, \end{aligned} \tag{1a}$$

or rewriting,

$$\begin{aligned} f_n\tau(k+n) + (f_{n-1} - g_n)\tau(k+n-1) + \cdots - g_1\tau(k) \\ = M - [g_n\rho(k+n-1) + g_{n-1}\rho(k+n-2) + \cdots \\ + g_2\rho(k+1) + g_1\rho(k)]. \end{aligned} \tag{1b}$$

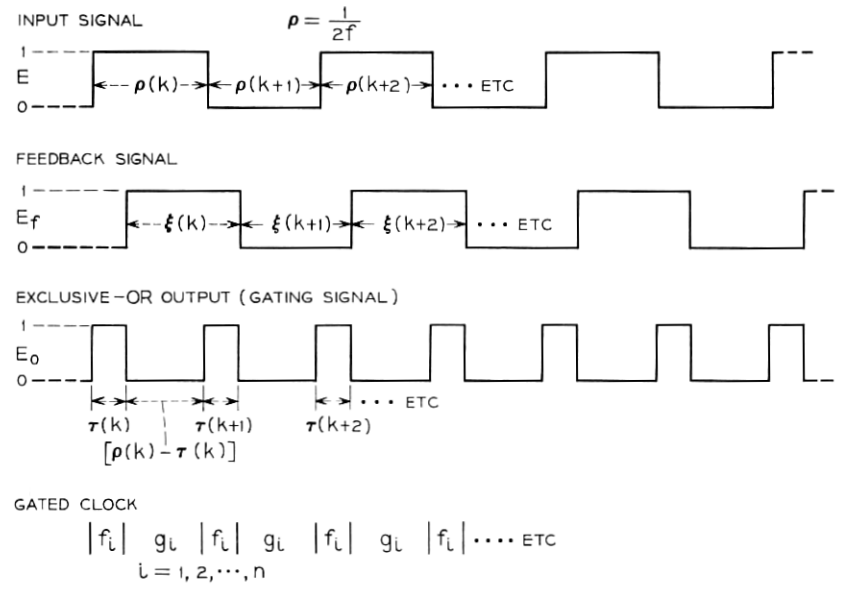

Fig. 2 — Input, feedback, and output waveforms for PLL which is assumed to be locked with constant input frequency. Gated clock signals are shown symbolically.

This is the system difference equation relating the response $\tau(k + i)$ to an excitation $\rho(k + i)$. In its general form this equation, when Z-transformed, is analogous to a Laplace transformed system equation in which polynomials in s multiplying the response and excitation functions result in poles and zeros, respectively. Since there is a one-to-one correspondence between the s and z planes with regard to poles and zeros, it is expected that by properly choosing coefficients, equation 1b may be synthesized to provide a desired frequency response (high-pass, low-pass, bandpass, and the like) possessing specified critical frequencies. As we show, it is the objective of this paper to exploit the low-pass properties of equation 1b. To achieve maximum high frequency attenuation, the coefficients g_i, $i = 2, 3, \ldots, n$ will be set equal to zero thereby locating all z-plane zeros at infinity.

$$f_n\tau(k + n) + f_{n-1}\tau(k + n - 1) + \cdots - g_1\tau(k) = M - g_1\rho(k). \quad (1c)$$

Equation 1c is normalized by letting $F_j = f_j/f_n$, $j = 1, \ldots, n - 1$ and $G_1 = g_1/f_n$. Also, notice that the cycle-by-cycle average voltage of the $\tau(k + j)$ interval expressed as a fraction of the maximum possible voltage is given by

$$v(k + j) = \frac{\tau(k + j)}{\rho(k + j)}. \quad (2)$$

Incorporating these substitutions gives

$$v(k + n) + F_{n-1}v(k + n - 1) + \cdots + F_1v(k + 1) - G_1v(k) = 2MF(k) - G_1, \quad (3)$$

where

$$F(k) = \frac{1}{2f_n\rho(k)}.$$

If it is assumed that $\rho(k)$ changes very little with k and that $\rho(k)$ is small with respect to the system response time (which it is), the $v(k)$ can be represented as a sampled continuous function of time, $v(t)$, letting $t = k\rho$. That is, $v(t)$ is a function whose value at the kth zero crossing of the input signal is $v(k)$.

This type of equation is best solved using z transform methods assuming that the input frequency is constant. In particular, the following transform pairs are noted:

$$Z[v(t)] = Z[v(k)] \equiv V(z) \equiv \sum_{j=0}^{\infty} v(j\rho)z^j. \quad (4a)$$

$$Z[A \exp(\alpha k)] = \frac{Az}{z - \exp(\alpha)}. \tag{4b}$$

$$Z[v(k + j)] = z^j[V(z)] - \sum_{l=1}^{j} z^l v(j - l). \tag{4c}$$

Accordingly, equation 3 is transformed as follows:

$$z^n[V(z)] - \sum_{l=1}^{n} z^l v(n - l) + F_{n-1}z^{n-1}[V(z)] - F_{n-1} \sum_{l=1}^{n-1} z^l v(n - 1 - l) + \cdots + F_1 z[V(z) - v(0)] - G_1 V(z) = (2MF - G_1)\left[\frac{z}{z - 1}\right]. \tag{5}$$

Combining terms,

$$[z^n + F_{n-1}z^{n-1} + \cdots + F_1 z - G_1]V(z) = (2MF - G_1)\left(\frac{z}{z - 1}\right) + \sum_{j=1}^{n} \sum_{l=1}^{j} F_j z^l v(j - l), \tag{6}$$

where

$$F_n = 1.$$

IV. GENERAL SYNTHESIS PROCEDURE

Before developing a synthesis technique for the digital PLL, it is of interest to review a specific application, that of FM demodulation. A "lock range" may be defined for the PLL whereby steady state input signals having constant frequencies lying within this range will cause a steady-state output, $v(k + j) = v(k + j + 1)$, all j, such that this output is linearly related to the input frequency $f = 1/2\rho$. This is the relation required for demodulation.

For dynamic behavior one may consider a binary baseband signal in which each of the two states is assigned a discrete frequency f_a, f_b within the lock range. If the baseband signal switches randomly between states with a maximum rate $1/T_d$ a new phenomenon is introduced. In this context the PLL may be regarded as a low-pass filter which should possess a bandwidth, ω_c, equal to or greater than π/T_d. By proper choice of the coefficients in equation 6 the desired filter shaping may be achieved. It is expected that the low pass filter characteristics will be a function of the input frequencies f_a, f_b. The resulting complication is

conveniently eliminated by making use of the narrowband approximation $f_a, f_b \approx f_m$ where $f_m = \frac{1}{2}(f_a + f_b)$. This is not unrealistic, because the PLL was developed for just such a narrowband system.* With this in mind, we now give a synthesis procedure. In using Z transform techniques it is assumed that the input frequency is approximately constant so that samples are taken at equal time intervals.

The coefficient of $V(z)$ in equation 6 is the "characteristic polynomial" of the system and using it, the desired low pass filtering properties of the loop can be synthesized. For example, assume that a transfer function with poles in the s plane at $s_1, s_2, \ldots, s_n$ is to be synthesized. Its characteristic polynominal is given by

$$\prod_{i=1}^{n} (s - s_i). \tag{7}$$

A conformal mapping between the s plane and z plane is given by the transformation

$$z = \exp(\rho s), \tag{8}$$

by which the pole $s_i = \sigma_i + i\omega_i$ is mapped into

$$\begin{aligned} z_i &= \exp[(\rho)(\sigma_i + i\omega_i)] \\ &= [\exp(\rho\sigma_i)][\cos(\omega_i\rho) + i \sin(\omega_i\rho)]. \end{aligned} \tag{9}$$

Since the complex s plane poles occur in conjugate pairs, and $\sin(\omega_i\rho)$ is an odd function, the corresponding z plane poles also occur in conjugate pairs, and the desired characteristic equation is transformed into

$$\prod_{i=1}^{n} (z - z_i) = z^n + A_{n-1}z^{n-1} + \cdots + A_1 z + A_0, \tag{10}$$

where each of the coefficients are real. Equating coefficients in equation 6 to those in equation 10 gives the required clock frequencies $g_1, f_1, \ldots, f_n$. A negative value implies an associated register which counts "down" while a positive value suggests a register which counts "up."

V. FIRST ORDER DIGITAL PLL

5.1 *Static and Dynamic Behavior*

The difference equation for an $n = 1$ PLL is easily written from equation 3:

* Full duplex transmission with $f_a = 1070$ Hz, $f_b = 1270$ Hz in one band, and $f_a = 2025$ Hz, $f_b = 2225$ Hz in the other band.

$$v(k+1) - G_1 v(k) = 2MF - G_1, \tag{11}$$

in which $M = 2^{N-1}$ and N is the number of counter stages in the register. For a steady state condition to exist, $v(k+1) = v(k)$ so that

$$v(k) = \frac{2MF - G_1}{1 - G_1} = \frac{2Mf - g_1}{f_1 - g_1}. \tag{12}$$

Since $0 \leqq v(k) \leqq 1$ the end points of the lock range are given by

$$f \mid_{v(k)=0} \equiv f_l = g_1/2M; \qquad f \mid_{v(k)=1} \equiv f_u = f_1/2M. \tag{13}$$

And so the lock range is

$$\Delta f_L = \mid f_u - f_l \mid = \frac{1}{2M} \mid g_1 - f_1 \mid. \tag{14}$$

The static response is diagrammed in Fig. 3.

The dynamic response to a step change in frequency is given by equation 6 for $n = 1$.

$$[z - G_1]V(z) = [2MF - G_1]\left[\frac{z}{z-1}\right] + zv(0). \tag{15}$$

A partial fraction expansion yields

$$V(z) = \left[\frac{2MF - G_1}{1 - G_1}\right]\left[\frac{z}{z-1}\right] + \left[v(0) - \frac{2MF - G_1}{1 - G_1}\right]\left[\frac{z}{z - G_1}\right]. \tag{16}$$

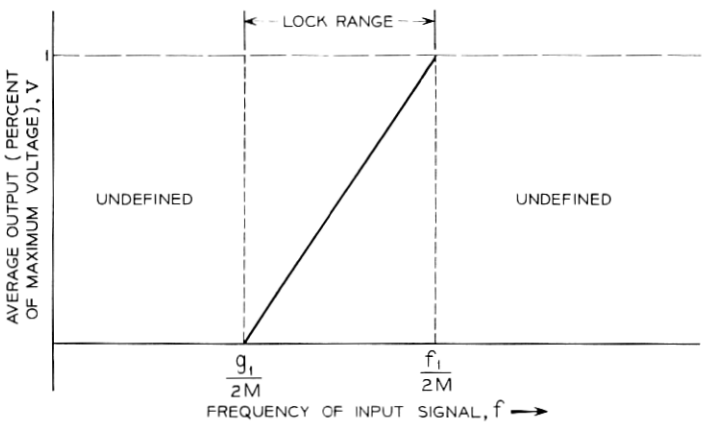

Fig. 3 — Average output voltage versus input frequency for first order PLL.

Assume that for time $t < 0$ the normalized input frequency is F_a. At $t = 0$ the input steps to F_b. Then from equation 12:

$$v(0) = \frac{2MF_a - G_1}{1 - G_1}. \tag{17}$$

Substitution into equation 16 gives the z transform of the response for $t \geqq 0$

$$V(z) = \left[\frac{2MF_b - G_1}{1 - G_1}\right]\left[\frac{z}{z - 1}\right] + \left[\frac{2M(F_b - F_a)}{1 - G_1}\right]\left[\frac{z}{z - G_1}\right]. \tag{18}$$

The inverse transform is easily found with the aid of equation 4a.

$$\begin{aligned} v(k) &= \frac{2MF_b - G_1}{1 - G_1} - \frac{2M(F_b - F_a)}{1 - G_1}(G_1)^k \\ &= \frac{2Mf_b - g_1}{f_1 - g_1} - \frac{2M(f_b - f_a)}{f_1 - g_1}\left(\frac{g_1}{f_1}\right)^k \quad \text{for} \quad k \geqq 0. \end{aligned} \tag{19}$$

Assuming that $v(k)$ is a continuous function of time, we let $v(k) = v(t)$ and $t = k\rho = k/2f_b$. This gives

$$v(t) = \frac{2Mf_b - g_1}{f_1 - g_1} - \frac{2M(f_b - f_a)}{f_1 - g_1} \exp\left[-2f_b t\right][\ln (f_1/g_1)]. \tag{20}$$

The resulting time constant is

$$T = \frac{1}{2f_b \ln (f_1/g_1)}, \tag{21}$$

and thus the half-power bandwidth is

$$f_c = \frac{1}{\pi} f_b \ln (f_1/g_1). \tag{22}$$

Notice the dependence of filter shaping upon input f_b. It follows that there is a somewhat different time constant for input frequency changes from f_b to f_a.

A simplified first order digital PLL has been built as shown in Fig. 4. It is a special case of the general system of Fig. 1. The FM input was composed of the discrete frequencies $f_a = 1070$ Hz and $f_b = 1270$ Hz. Clock frequencies g_1 and f_1 were chosen as $(2M)(970)$ Hz and $(2M)(1370)$ Hz, respectively, to provide a lock range of twice the total input frequency deviation. M was chosen to be 128 (see Section 5.3). The above values gave a time constant, T, of 1.13 ms. Interchanging f_a and f_b resulted in an increased time constant of 1.34 ms.

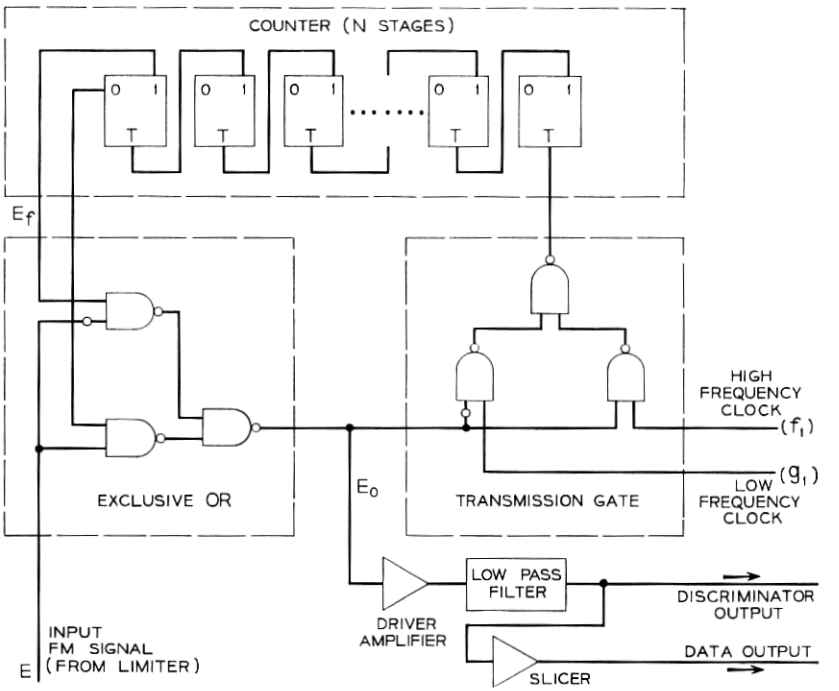

Fig. 4 — Block diagram of simplified first order PLL FM discriminator.

Oscilloscope photographs showing the two step responses of the actual loop are shown in Fig. 5.

5.2 *Out-of-Lock Oscillation*

If there is no input to the PLL, it will run at a rest frequency of

$$f_r = \left(\frac{M}{f_1} + \frac{M}{g_1}\right)^{-1} = \frac{1}{M}\,\frac{g_1 f_1}{g_1 + f_1}. \tag{23}$$

Notice, however, that one half cycle will be at $g_1/2M$ and the next at $f_1/2M$.

If an input to the PLL is present, but its frequency lies outside the lock range, that is, if $f < f_1/2M$ or $f > g_1/2M$, the output voltage $v(t)$ will oscillate between 0 and 1. Figure 6 shows waveforms for a loop which is out of lock. For time to the left of the dotted line, the loop is attempting to lock and the frequency of the feedback signal, E_f, is approaching that of the out-of-lock input E. Within this region,

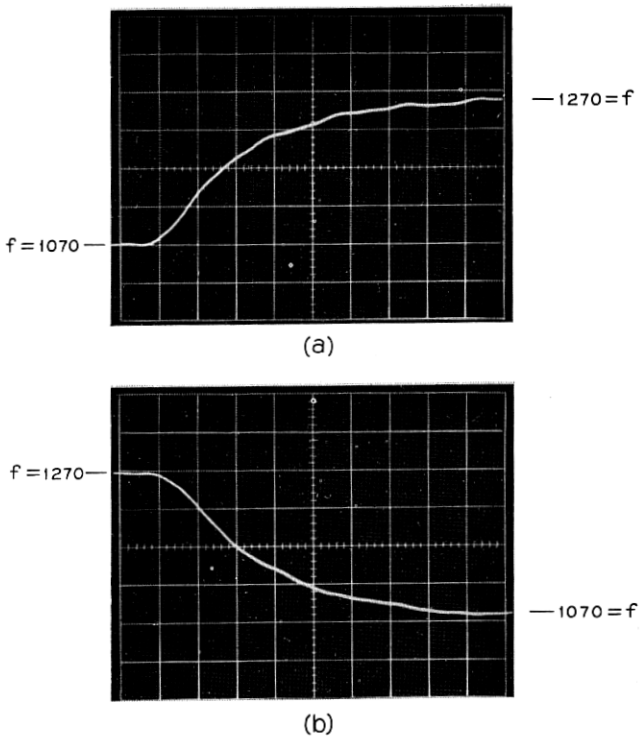

Fig. 5 — Output voltage response of first order PLL to input step frequency of (a) 1070 to 1270 Hz and (b) 1270 to 1070 Hz. Horizontal scale: 0.5 ms per cm.

equation 16 applies and is rewritten in the time domain as

$$v(k) = \left(\frac{2Mf - g_1}{f_1 - g_1}\right) + \left[v(0) - \frac{2Mf - g_1}{f_1 - g_1}\right]\left(\frac{g_1}{f_1}\right)^k. \tag{24}$$

For time to the right of the dotted line in Fig. 6, a new difference equation applies. It is written as

$$g_1[\rho(j) - \tau(j + 1)] + f_1\tau(j) = M \tag{25}$$

so that a derivation similar to that previously used results in

$$v(j) = \left[\frac{g_1 - 2Mf}{g_1 - f_1}\right]\left[\left(\frac{f_1}{g_1}\right)^j - 1\right] + v'(0)\left(\frac{f_1}{g_1}\right)^j. \tag{26}$$

Equations 24 and 26 are represented graphically in Fig. 7. M, g_1, and f_1 take on the values of the previous example and an out-of-lock

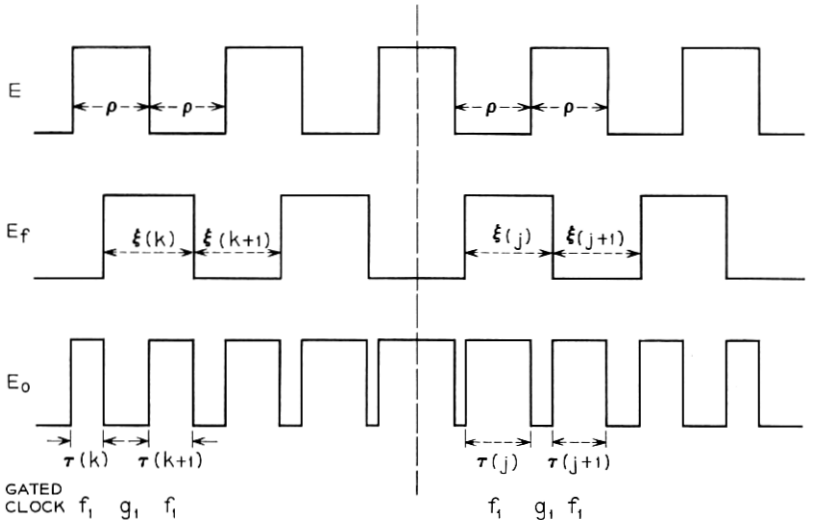

Fig. 6 — Input, feedback, and output waveforms of nonlocked first order PLL.

input frequency $f = 1400$ Hz is chosen as the input. The positive slope segment to the left corresponds to equation 24 with an initial voltage $v(0)$ assumed to be zero. When $v(k)$ reaches unity, the next segment is governed by $v(j)$ with an initial condition $v'(0) = 1$. When $v(j)$ reaches zero, the response is again given by $v(k)$ and with

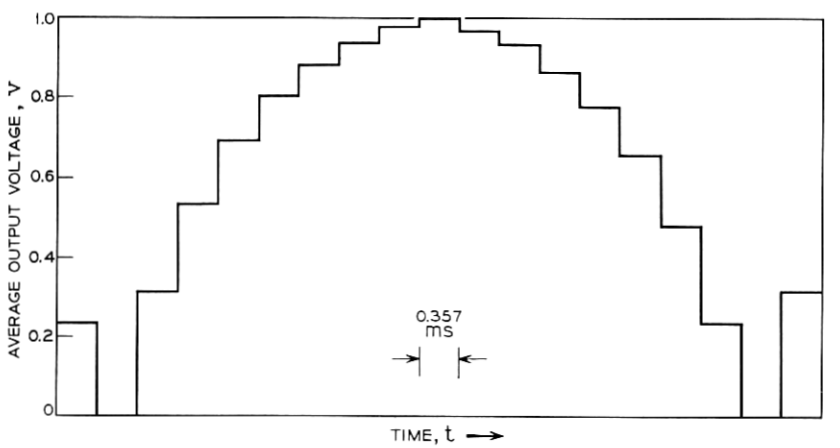

Fig. 7 — Single cycle of output average voltage oscillation for nonlocked first order PLL.

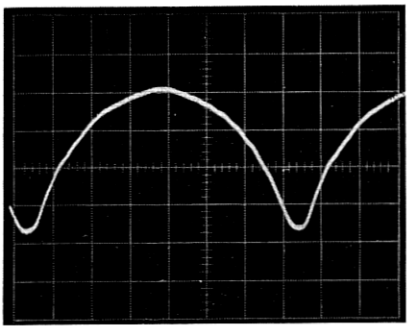

Fig. 8 — Actual output voltage of experimental first order PLL showing out-of-lock oscillation. Horizontal scale: 1 ms per cm.

initial condition adjusted accordingly. The actual waveform for the experimental PLL using this example is shown in Fig. 8.

5.3 *Internal Noise From Phase Discontinuity*

The clock signals are unsynchronized, and thus a random phase discontinuity results at the time of gating. This results in an internal noise voltage which exhibits itself as a fluctuation in the output voltage. This effect can be thought of as a quantization noise of the phase. A portion of Fig. 2 is redrawn in Fig. 9 to show the time errors ϵ_0, ϵ_0', and ϵ_1 at the instant of gating caused by differences in clock phases. It is assumed that the frequency of the ripple is low enough so as not to be attenuated by the PLL filtering property. With this in mind, difference equation 11 may be amended to account for the phase error.

$$[\tau(k+1) - \epsilon_1(k+1)]f_1 + [\rho(k) - \tau(k) - \epsilon_0(k) - \epsilon_0'(k)]g_1 + 2 = M. \quad (27)$$

For a constant input frequency and very slowly varying $\tau(k)$, $\tau(k+1) \cong \tau(k)$ so that

$$\tau(k)\,[f_1 - g_1] = M - g_1\rho + f_1\epsilon_1(k+1) + g_1[\epsilon_0(k) + \epsilon_0'(k)] - 2, \quad (28)$$

or

$$[v(k)]\,[f_1 - g_1] = 2Mf - g_1 + 2ff_1\epsilon_1(k+1) + 2fg_1[\epsilon_0(k) + \epsilon_0'(k)] - 4f. \quad (29)$$

Δv_N is defined as the difference in voltage for maximum and minimum (zero) phase errors. Thus

$$\Delta v_N = \left[\frac{2f}{f_1 - g_1}\right][f_1\epsilon_1(k+1)\,|_{\max} + g_1(\epsilon_0(k)\,|_{\max} + \epsilon_0'(k)\,|_{\max})]. \quad (30)$$

Since

$$\epsilon_1(k+1)\,|_{\max} = \frac{1}{f_1} \quad \text{and} \quad \epsilon_0(k)\,|_{\max} = \epsilon_0'(k)\,|_{\max} = \frac{1}{g_1},$$

then

$$\Delta v_N = \frac{6f}{f_1 - g_1} = \frac{6f_m}{f_1 - g_1}, \quad (31)$$

where f is approximated by the carrier f_m for the narrowband case.

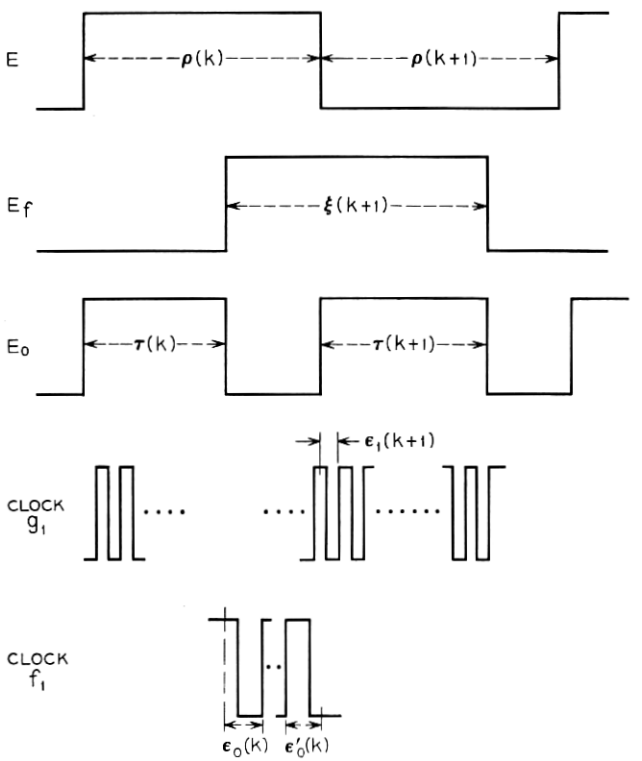

Fig. 9 — Waveforms for locked first order PLL showing how time jitter is caused by phase differences in clock signals.

It may be seen that the peak-to-peak output for an incoming FM wave with phase continuity in the clock signals is given by equation 12 as

$$\Delta v_{sig} = \left| \frac{2Mf_a - g_1}{f_1 - g_1} - \frac{2Mf_b - g_1}{f_1 - g_1} \right| = 2M \frac{\Delta f}{f_1 - g_1}, \tag{32}$$

where Δf is the total frequency deviation $| f_a - f_b |$. Thus the minimum peak-to-peak voltage signal-to-noise ratio within the loop is

$$S/N = \frac{\Delta v_{sig}}{\Delta v_N} = \frac{2M(\Delta f)}{6f_m} = 2^N \frac{\Delta f}{6f_m}. \tag{33}$$

Continuing the previous example with $\Delta f = 200$Hz and $f_m = 1170$ Hz, it is desired that the internal noise be 20 dB below the signal so that $2^N \geqq 361$. This suggests a nine stage counter ($2^9 = 512$); however, it should be pointed out that a worst case of phase jitter has been assumed and the average phase jitter is less than this. Laboratory experiments have shown satisfactory results with an eight stage counter thus giving a minimum signal-to-noise ratio of 17.2 dB.

It is apparent from equation 33 that the internal noise may be made as low as desired by choosing a sufficiently large value of N. Thus a direct relationship exists between equipment cost (number of counters) and performance (jitter distortion).

VI. SECOND ORDER DIGITAL PLL

The location of the desired s-plane poles must be specified and mapped into the z-plane. The following example is concerned with synthesizing the familiar Butterworth response, but the procedure is certainly applicable to other filter classes.

A second order PLL is to be synthesized so that its response is that of a Butterworth low-pass filter with cutoff at ω_c. The $2n = 4$ poles of $H(s)H(-s)$ lie on a circle of radius ω_c and subtend equal arcs such that the filter's characteristic equation is

$$s^2 + (2)^{\frac{1}{2}}\omega_c s + \omega_c^2 = 0, \tag{34}$$

with poles at

$$s_{1,2} = \frac{\omega_c}{(2)^{\frac{1}{2}}}(-1 \pm i). \tag{35}$$

The corresponding poles in the z plane are

$$z_{1,2} = \exp(s_{1,2}\rho) = [\exp(-\alpha)][\cos(\alpha) \pm i \sin(\alpha)]$$

where

$$\alpha = \frac{\omega_c \tau}{(2)^{\frac{1}{2}}} = \frac{\pi}{(2)^{\frac{1}{2}}} \frac{f_c}{f}. \tag{36}$$

Digressing for a moment, it is of academic interest to map the entire Butterworth circle into the z plane. This is easily done by letting s be a circle of radius ω_c, that is, $s = \omega_c \exp(i\phi)$, $0 \leqq \phi \leqq 2\pi$. Substituting $z = \exp(s\rho)$ and approximating f by f_m gives

$$z = \left\{\exp\left[\frac{\omega_c}{2f_m}\cos(\phi)\right]\right\}\left\{\cos\left(\frac{\omega_c}{2f_m}\sin(\phi)\right) + i\sin\left(\frac{\omega_c}{2f_m}\sin(\phi)\right)\right\}. \tag{37}$$

The resulting cardioid-like shape is shown in Fig. 10 with f_c/f_m as a parameter. The angle ϕ is also shown so that portions of the Butterworth circle may be conveniently translated into the z plane.

Returning to the specific example, the characteristic polynominal is written using equation 36 as

$$(z - z_1)(z - z_2) = z^2 - [2\exp(-\alpha)][\cos(\alpha)]z + \exp(-2\alpha). \tag{38}$$

The resulting coefficients are equated to the respective coefficients in equation 6, namely $z^2 + F_1 z - G_1$ so that:

$$F_1 = f_1/f_2 = -2[\exp(-\alpha)][\cos\alpha] \tag{39}$$

and

$$G_1 = g_1/f_2 = -\exp(-2\alpha).$$

A third equation is arrived at by fixing the steady-state voltage $v(k)$ for a specific input frequency, f. The choice is arbitrary, and since the system's input spectrum is symmetrical about the carrier frequency, f_m, it is reasonable to fix the corresponding output voltage at 0.5. The equation is obtained from equation 6 by noting that steady-state implies periodicity so that $v(k) = v(k+j)$. Thus:

$$v(k)[1 + F_1 - G_1] = 2M\frac{f_m}{f_2} - G_1 . \tag{40}$$

Solving equations 39 and 40 gives

$$f_2 = \frac{2Mf_m \exp(\alpha)}{\cos(\alpha) - \sinh(\alpha)}, \tag{41}$$

$$f_1 = \frac{4Mf_m \cos(\alpha)}{\cos(\alpha) - \sinh(\alpha)}, \tag{42}$$

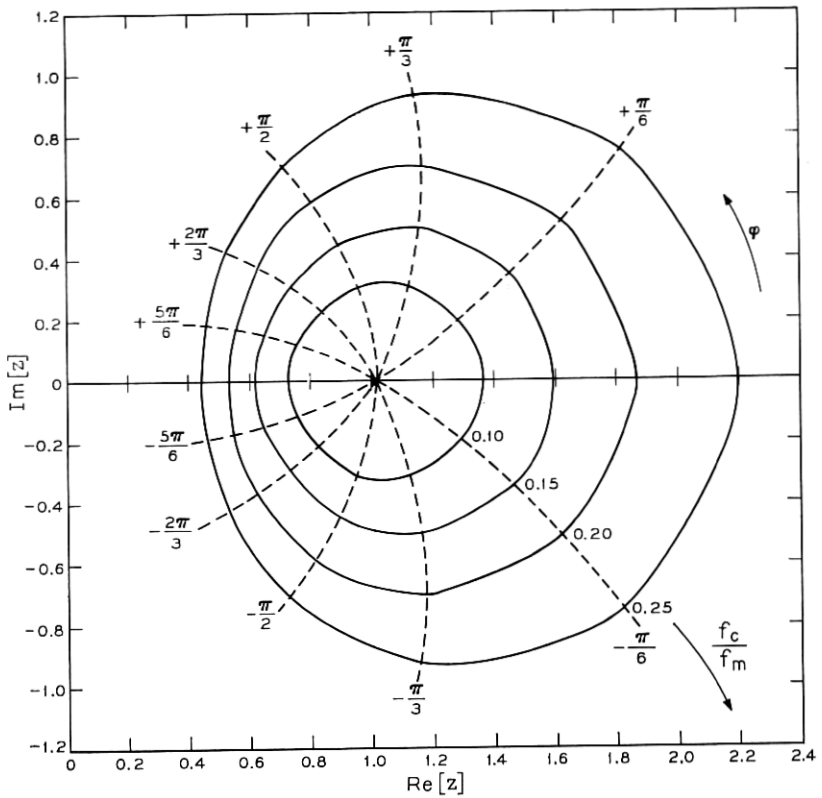

Fig. 10 — Mapping of the s-plane Butterworth circle into the z-plane.

and

$$g_1 = \frac{2Mf_m \exp(-\alpha)}{\cos(\alpha) - \sinh(\alpha)}. \tag{43}$$

As a practical example, consider the demodulation of a narrowband FSK wave whose spectrum is centered about a carrier of 2125 Hz. The signaling rate is limited to $\leqq 300$ baud so that a cutoff frequency of 250 Hz should prove adequate. As previously noted, the choice of M is dependent upon the maximum baseband jitter (quantizing noise) which can be tolerated. This must be weighed against the added circuitry and higher clock frequencies imposed by large values of M. A convenient choice is $M = 128$. Thus

$$\alpha = \frac{\pi}{(2)^{\frac{1}{2}}} \frac{f_c}{f_m} = 0.262$$

so that

$$g_1 = 598 \text{ kHz},$$

$$f_1 = 1504 \text{ kHz},$$

and

$$f_2 = -1012 \text{ kHz}.$$

As previously mentioned, the negative value for f_2 requires a "down counter" for the second register. This example is continued in subsequent sections.

6.1 *Step Response of the System*

Once the coefficients $g_1, f_1, \ldots, f_n$ are determined, the characteristic equation is uniquely specified and the system's time response to a step in input frequency is easily found. The step response of a second order system is now derived in the interest of providing further insight into the characteristics of the loop.

Equation 6 is written for $n = 2$ as:

$$[z^2 + F_1 z - G_1]V(z) = (2MF - G_1)\left(\frac{z}{z-1}\right) + v(1)z + v(0)z^2 + zF_1 v(0). \quad (44)$$

Assume that the input frequency steps from F_a to F at $t = 0$ (as before, capitalization denotes normalization so that $F_i = f_i/f_2$, $G_i = g_i/f_2$). Thus for $t \geqq 0$ we have

$$V(z) = (2MF - G_1)\left[\frac{z}{(z^2 + F_1 z - G_1)(z-1)}\right] + v(0)\left[\frac{z^2}{z^2 + F_1 z - G_1}\right] + [F_1 v(0) + v(1)]\left[\frac{z}{z^2 + F_1 z - G_1}\right]. \quad (45)$$

The initial conditions $v(1)$ and $v(0)$ are determined from the difference equation

$$v(k+2) + F_1 v(k+1) - G_1 v(k) = 2MF - G_1. \quad (46)$$

Assume that the system is in steady state for $t \leqq 0$ so that $v(k) = v(k-i)$, $k \leqq 0$. For $k = -2$

$$v(0)[1 + F_1 - G_1] = 2MF_a - G_1, \quad (47)$$

so that

$$v(0) = \frac{2MF_a - G_1}{1 + F_1 - G_1}. \tag{48}$$

Now let $k = -1$:

$$v(1) = 2MF - G_1 - [F_1 - G_1]\, v(0), \tag{49}$$

which may be written as

$$v(1) = v(0) + 2M\Delta, \tag{50}$$

where

$$\Delta = [F - F_a]. \tag{51}$$

Substituting equations 50 and 51 into 45 and simplifying leads to

$$\begin{aligned} V(z) = &\left[v(0) + \frac{2M\Delta}{1 + F_1 - G_1}\right]\left[\frac{z}{z - 1}\right] \\ &- \left[\frac{2M\Delta}{1 + F_1 - G_1}\right]\left[\frac{z^2}{z^2 + F_1 z - G_1}\right] \\ &- \left[\frac{2M\Delta G_1}{1 + F_1 - G_1}\right]\left[\frac{z}{z^2 + F_1 z - G_1}\right]. \end{aligned} \tag{52}$$

The following substitutions are made so that $V(z)$ may be easily transformed. Let

$$F_1 = -2[\cos \beta] \exp(-\alpha); \qquad G_1 = -\exp(-2\alpha). \tag{53}$$

Substituting and rearranging gives

$$\begin{aligned} V(z) = &\left[v(0) + \frac{2M\Delta}{1 + F_1 - G_1}\right]\left[\frac{z}{z - 1}\right] \\ &- \left[\frac{2M\Delta}{1 + F_1 - G_1}\right]\left[\frac{z^2 - z(\cos \beta) \exp(-\alpha)}{z^2 - 2z(\cos \beta) \exp(-\alpha) + \exp(-2\alpha)}\right] \\ &- \left[\left(\frac{4M\Delta G_1}{1 + F_1 - G_1} - F_1\right)(-4G_1 - F_1)^{-\frac{1}{2}}\right] \\ &\cdot\left[\frac{z(\sin \beta) \exp(-\alpha)}{z^2 - 2z(\cos \beta) \exp(-\alpha) + \exp(-2\alpha)}\right]. \end{aligned} \tag{54}$$

This is transformed into

$$v(k) = \left[v(0) + \frac{2M\Delta}{1 + F_1 - G_1}\right]u(k)$$

$$- \exp(-\alpha k)\left[\left(\frac{2M\Delta}{1 + F_1 - G_1}\right)\cos(\beta k) + \left(\frac{4M\Delta G_1}{1 + F_1 - G_1} - F_1\right)(-4G_1 - F_1)^{-\frac{1}{2}}\sin(\beta k)\right], \quad (55)$$

where $u(k)$ is the unit step. The time response is found by again assuming that $v(k)$ is a continuous function of time $v(t)$, $k \approx 2ft$. Substitution gives the familiar response of an underdamped second order system:

$$v(t) = \left[v(0) + \frac{2M\Delta}{1 + F_1 - G_1}\right]u(t) - \exp(-2\alpha ft)\left[\left(\frac{2M\Delta}{1 + F_1 - G_1}\right)\cos(2\beta ft) + \left(\frac{4M\Delta G_1}{1 + F_1 - G_1} - F_1\right)(-4G_1 - F_1)^{-\frac{1}{2}}\sin(2\beta ft)\right]. \quad (56)$$

The experimentally determined step response of the actual $n = 2$ PLL closely approximates the Butterworth response and is shown in Fig. 11.

6.2 *Lock Range for the Second Order System*

As was the case for the $n = 1$ PLL, the loop is said to be in "lock" if, for a steady input frequency, the output $v(k)$ is constant. Although there are many frequency ranges for which the loop exhibits this property, there is a "fundamental" lock range over which $v(k)$ varies linearly with frequency between its defined limits, and the output frequency equals the input frequency. In steady state, $v(k+2) = v(k+1) = v(k)$ so that from equation 40:

$$v(k) = \frac{2MF - G_1}{1 + F_1 - G_1} = \frac{2Mf - g_1}{f_2 + f_1 - g_1} \quad \text{if} \quad 0 \leqq v(k) \leqq 1. \quad (57)$$

The end points of the lock range are

$$f\,|_{v(k)=0} \equiv f_u = \frac{g_1}{2M} \quad (58)$$

and

$$f\,|_{v(k)=1} \equiv f_l = \frac{f_1 + f_2}{2M}. \quad (59)$$

The lock range is given by

$$\Delta f_L = |f_u - f_l| = \frac{1}{2M}|g_1 - f_1 - f_2|. \quad (60)$$

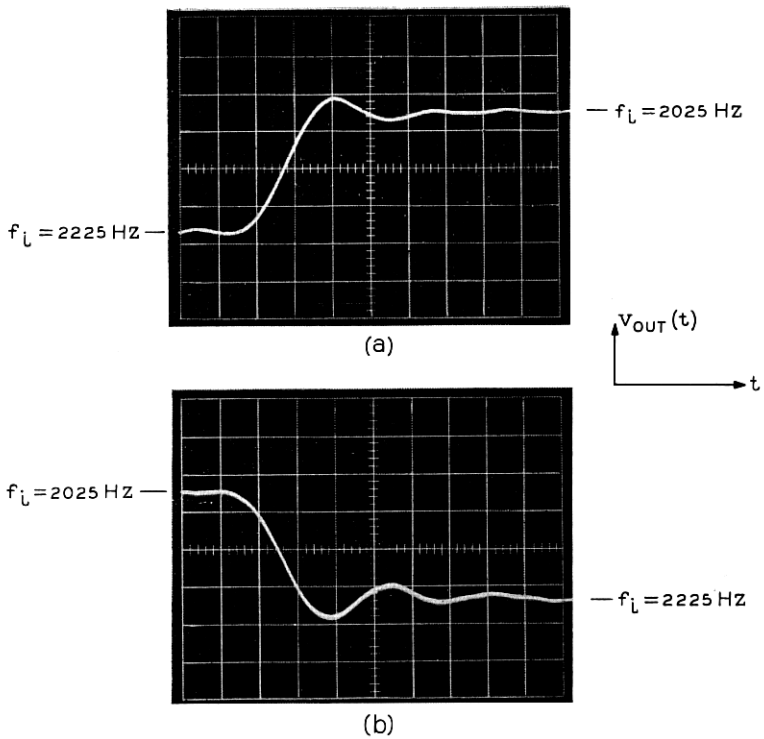

Fig. 11 — Output voltage response of second order PLL to input step frequency of (a) 2225 to 2025 Hz and (b) 2025 to 2225 Hz. Horizontal scale: 1 ms per cm.

Substituting the values calculated previously gives a lock range of 414 Hz which is approximately twice the bandwidth required. The useful bandwidth is reduced still further as will be shown.

6.3 *Bound on Cutoff Frequency*

For a step in frequency $f_a - f_b$ we have a corresponding step in voltage,

$$\Delta v = \frac{2Mf_a - g_1}{f_2 + f_1 - g_1} - \frac{2Mf_b - g_1}{f_2 + f_1 - g_1} = \frac{2M(f_a - f_b)}{f_2 + f_1 - g_1}. \tag{61}$$

Δv is defined to have a maximum value of unity so

$$f_2 + f_1 - g_1 \geqq 2M(f_a - f_b) \tag{62}$$

and

$$1 + F_1 - G_1 \leqq \frac{2M}{f_2}(f_a - f_b) \quad \text{for} \quad f_2 < 0. \tag{63}$$

If f_a and f_b are symmetrically distributed about the carrier frequency, f_c, we can let $v = \frac{1}{2}$ at $f_1 = f_m$ so that from equation 40

$$f_2 = \frac{4Mf_m}{1 + F_1 + G_1}. \tag{64}$$

Substituting equation 64 into 63 gives

$$1 + F_1 - G_1 \leqq (1 + F_1 + G_1)\left(\frac{f_a - f_b}{2f_m}\right). \tag{65}$$

Substituting equation 53 for F_1 and G_1 gives

$$1 - 2[\exp(-\alpha)]\cos\beta + \exp(-2\alpha)$$
$$\leqq \left(\frac{f_a - f_b}{2f_m}\right)[1 - 2(\cos\beta)\exp(-\alpha) - \exp(-2\alpha)]. \tag{66}$$

The constants α and β are related to the filter shaping desired and are a function of the input frequency for $t > 0$. For the case of a Butterworth response ($n = 2$)

$$\alpha = \beta = \frac{\pi}{(2)^{\frac{1}{2}}}\left(\frac{f_c}{f}\right).$$

For a narrowband system the input frequency may be approximated by the carrier f_m. Thus

$$1 - 2(\cos\mu)\exp(-\mu) + \exp(-2\mu)$$
$$\leqq [1 - 2(\cos\mu)\exp(-\mu) - \exp(-2\mu)]\left[\frac{\Delta f}{2f_m}\right], \tag{67}$$

where

$$\mu = \frac{\pi}{(2)^{\frac{1}{2}}}\frac{f_c}{f_m}.$$

This may be written as

$$\cos\mu \geqq \frac{\exp(\mu) - \left[\dfrac{f_m + \dfrac{\Delta f}{2}}{f_m - \dfrac{\Delta f}{2}}\exp(-\mu)\right]}{2}. \tag{68}$$

Thus for a given f_a, f_b and f_m, the cutoff frequency f_c is bounded. For example let f_a and f_b be 2025 Hz and 2225 Hz, respectively, and be symmetrically distributed about the carrier f_m. Then

$$\cos \mu \geqq \frac{\exp(\mu) + (0.91) \exp(-\mu)}{2}. \tag{69}$$

Solving this transcendental equation gives

$$\mu \geqq 0.19 \tag{70}$$

and

$$f_c \geqq 182 \text{ Hz}.$$

An upper bound on f_c is found by requiring that the end points of the lock range be positive frequencies. The lower edge of the lock range is required to be greater than zero so that from equations 59, 41 and 42

$$\frac{f_1 + f_2}{2M} \geq 0 \quad \text{or} \quad 2 \cos \mu - \exp(\mu) \geqq 0. \tag{71}$$

This is satisfied if $\mu \leqq 0.54$ which gives positive value for equation 71 as well as for the upper edge of the lock range $g_1/2M$. Thus $0.19 \leqq \mu \leqq 0.54$ so that for $f_m = 2125$ Hz

$$182 \leqq f_c \leqq 542 \text{ Hz}. \tag{72}$$

The bounds on f_c/f_m are loose in the sense that it is assumed that the full lock range is available to input frequencies. This is not the case for underdamped systems, where a hysteresis effect known as "capture" reduces the effective lock range available, and so the bound might be tightened accordingly.

6.4 *The Capture Phenomonen*

When the PLL is "out of lock" its output voltage oscillates between 1 and 0. The "pull-in" frequencies are those frequencies furthest removed from the carrier for which the PLL will ultimately lock. In general, the PLL will exhibit a hysteresis so that the pull-in range will be smaller than the lock range; also, the upper and lower pull-in frequencies will generally not be symmetrically distributed about the carrier f_m. In general, solution of the capture range (for conventional phase-locked-loops) results in a nonlinear integrodifferential equation. Solution for conventional PLL's requires phase plane techniques

and is documented in Ref. 2. An analysis to determine capture range for the digital PLL has not been performed.

6.5 *Stability of the Second Order System Within the Lock Range*

Thus far there has been no restriction placed on N, the number of counters required per shift register. For N less than some critical value N_m it is possible for stable modes of operation, different from that of Fig. 2, to exist. These modes do not exploit the PLL to its fullest advantage and thus in previous derivations it has been assumed that $N \geqq N_m$.

A possible parasitic mode is shown in Fig. 12. The input frequency is constant, as is the frequency of the flip-flop signal, E_f, but the waveform of E_f is no longer square. This operation is caused by the limited length of the registers. Assume that the lengths (number of counter stages) for the $n = 2$ system are equal, and of value N. Each time the feedback flip-flop (see Fig. 1) is triggered, register 1 is reset to zero. During the period T_1+T_2 (see Fig. 12) this register is advanced to a count of $[T_1g_1+T_2f_1]$ modulo C where $C = 2^N$. This number is shifted into the second register where one of two conditions may exist:

$$T_1g_1 + T_2f_1 \geqq M,$$

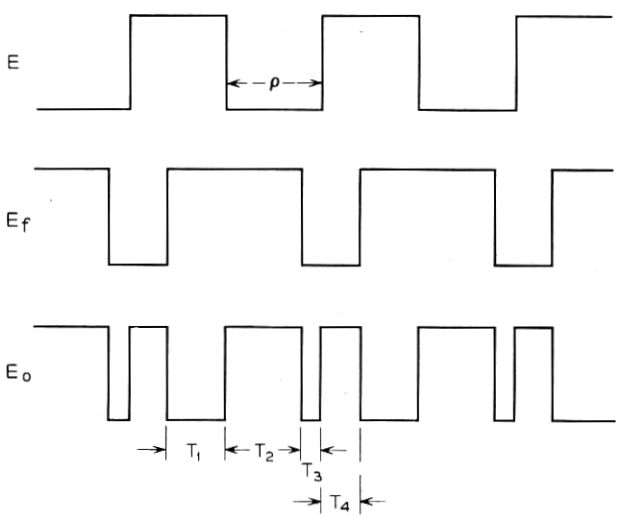

Fig. 12 — Waveforms for parasitic locked mode of second order PLL.

or

$$T_1 g_1 + T_2 f_1 \leqq M.$$

The first equation results in normal operation, analyzed in previous sections. During T_4 the count is reduced by a negative f_2 so that

$$[T_1 g_1 + T_2 f_1 + T_4 f_2] \bmod C = M.$$

The second equation requires that the second register count down to zero (which is congruent to C) and then further reduce the count by $C - M$. Thus

$$[T_1 g_1 + T_2 f_1 + T_4 f_2] \bmod C = M - C.$$

These equations may be combined by introducing the parameter $\delta = -1, 0$ depending upon the mode of operation:

$$T_1 g_1 + T_2 f_1 + T_4 f_2 = M - \delta C. \tag{73}$$

Similarly, an equation similar in form to equation 73 covers the intervals T_2, T_3, and T_4:

$$T_3 g_1 + T_4 f_1 + T_2 f_2 = M - \gamma C, \tag{74}$$

where $\gamma = 0, 1$.

The period, T_2, may be explicitly solved for by noting that

$$T_1 + T_4 = T_2 + T_3 = \rho. \tag{75}$$

Thus

$$v_2 = \frac{T_2}{\rho} = -\frac{g_1}{f_1 + f_2 - g_1} + \frac{(-\delta C + M) f_1 - (-\gamma C + M)(f_2 - g_1)}{f_1^2 - (f_2 - g_1)^2} 2f. \tag{76}$$

Under normal conditions $\delta = \gamma = 0$ so that

$$v_2 = \frac{2Mf - g_1}{f_1 + f_2 - g_1},$$

which is identical to equation 57. The parasitic mode of operation is given by $\delta = -1$, $\gamma = 1$ so that equation 76 may be rewritten as

$$v_2 = \frac{2Mf - g_1}{f_1 + f_2 - g_1} + \frac{2Cf}{f_1 + f_2 - g_1}. \tag{77}$$

Graphical examination (see Fig. 13) of equations 57 and 77 shows that

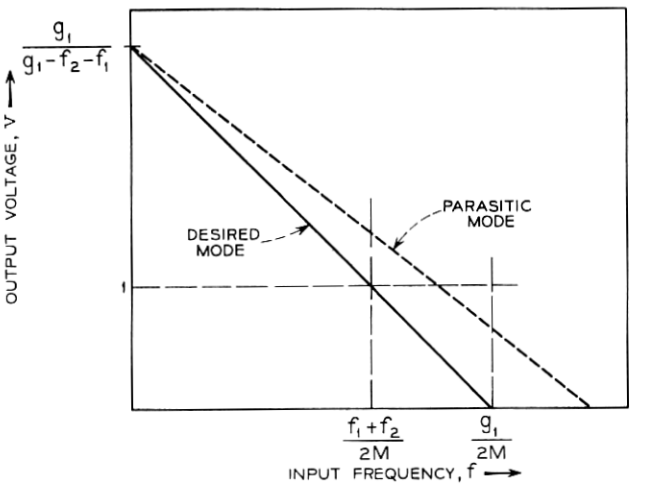

Fig. 13 — Comparison of parasitic and normal mode voltage versus frequency characteristic for second order PLL.

two modes of operation may exist within the lock range. To insure that this will not happen, C must be chosen so that the frequency range for which $0 \leqq v_2 \leqq 1$ lies outside the normal lock range. Thus at the upper lock range edge, $f = g_1/2M$, it is required that $v_2 > 1$ so that from equation 77,

$$\frac{2C\left(\frac{g_1}{2M}\right)}{f_1 + g_1 - f_2} > 1.$$

Hence

$$\frac{C}{M} > \frac{f_1 + g_1 - f_2}{g_1}$$

and thus the minimum number of counters required is

$$N_m = 1 + \text{integer value}\left[\log_2\left(\frac{f_1 + g_1 - f_2}{g_1}\right)M\right]^* \tag{78}$$

VII. PERFORMANCE

In a laboratory test, an FM digital signal with mark and space frequencies of 1270 and 1070 Hz was fed into an $n = 1$ PLL which had

* That is, the integer value of 2.3 is 2.

an 8-stage counter and clock frequencies for which $g_1 = 2M(970)$Hz and $f_1 = 2M(1370)$Hz. The output of the exclusive-OR was fed to an amplifier which clipped the signal to precise levels and provided a constant output impedance. The signal then went to a Butterworth low-pass filter with $n = 3$ and cutoff of 200 Hz. The filtered signal was sliced to give a digital output which could be compared with the original digital input. The FM modulator used in these tests was from a Bell System Data Set 103E1. The eye pattern for this circuit with an input at 300 baud is given in Fig. 14a. When the lock range was increased to $\pm$300 Hz about the carrier, the eye pattern improved, as shown in Fig. 14b. This effect results from the increased bandwidth, f_e.

Start-stop distortion, as measured with a Bell System 911A data test set for bit rates of 150 to 300 baud, was 2 and 5 percent, respectively. Performance with additive gaussian noise is as shown in Fig. 15,

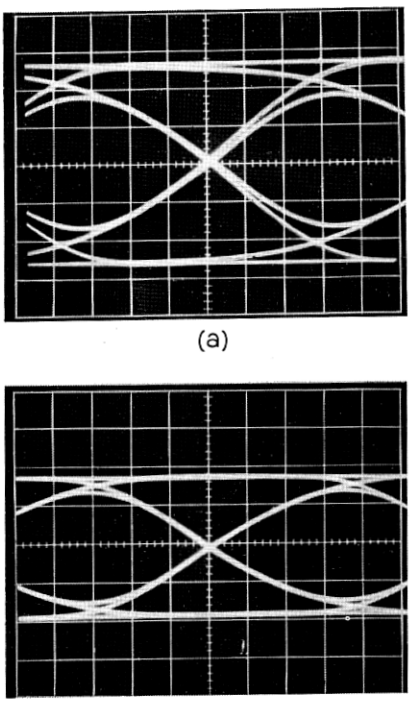

Fig. 14 — First order PLL eye patterns for 300 baud random digital data. Lock range of (a) 400 Hz, (b) 600 Hz. Horizontal scale: 0.5 ms per cm.

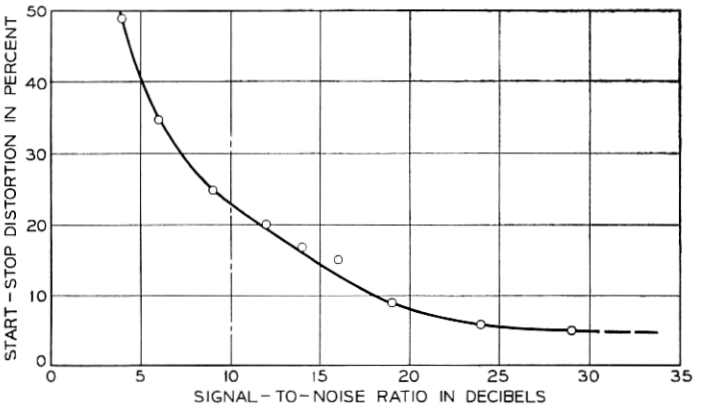

Fig. 15 — Distortion performance of first order PLL with input signal degraded by 3 kHz band-limited white noise.

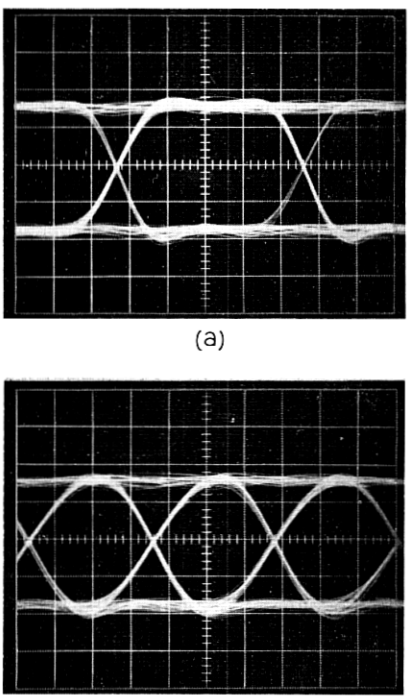

Fig. 16 — Second order PLL eye patterns for (a) 150 baud and (b) 300 baud random digital data. Horizontal scale: 1 ms per cm.

where start-stop distortion is plotted versus signal-to-noise ratio. The noise is 3 kHz band-limited white noise and the bit rate is 300 baud. This performance is similar to that of the receiver in Data Set 103E1. Start-stop distortion for a single frequency (2025 Hz) interference was measured and, as might be expected, single frequency interference is a strong function of frequency, the worst values being at odd multiples of the channel frequency.

Laboratory tests indicated that the second order PLL, with characteristics described in Section VI, performed in accordance with theoretical expectation. The eye patterns for an input of a modulated random data signal at 150 and 300 baud are shown in Fig. 16. It was found that noise performance of the second order system was not much better than that of the first order system. This probably resulted from the counter length falling just short of the value indicated in equation 78, thereby allowing noise perturbations to randomly shift operation between the stable and parasitic modes of operation.

VIII. CONCLUSIONS

A synthesis procedure for the realization of an nth order digital phase-locked loop has been described. Such systems find application in FM demodulators, filters, and in extremely stable locked oscillators. Various loop properties have been theoretically derived and experimental performance has been found to be consistent with these results. The advantages of such circuits for use in large multichannel data sets are:

(*i*) Filtering property—(6n) dB per octive.

(*ii*) Small size—completely integrable using one or more monolithic chips.

(*iii*) Requires no adjustment—permitting lower manufacture and repair costs.

(*iv*) Excellent stability and reliability—the PLL circuit either works or does not, since it is completely digital. Stability of the entire system is dependent upon clock stability which may be as good as required.

(*v*) Multichannel economy—accurate clocks can be used to drive many channel circuits.

In addition, this circuit has two inherent advantages over other types of phase-locked loops. First, it requires no low-pass filter generally found between the phase comparator (multiplier) and voltage-

controlled oscillator in conventional phase-locked loops. Second, it includes, in effect, an ideal voltage-controlled oscillator, the frequency of which is linearly related to voltage.

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