Design of a Simulator for Investigating Organic Synchronization Systems

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This paper describes circuits and devices designed for a real time simulator that was used to study a network synchronization scheme. The simulator represents a system of four geographically-separated stations with compound interconnections. The system clock rate is a function of the states of each local clock and the interconnecting paths. Component parts for the simulation system were built to specifications exceeding requirements of an actual system so that the operating states could be precisely determined. The simulator performed reliably during the series of experiments which provided the data described in a companion paper.[1]

I. INTRODUCTION

The problem of maintaining synchronism in a pulse code modulation network has been of interest for some time.

One technique for synchronizing the geographically separated clocks of a network is known as organic synchronization. In this scheme, the frequency of each clock is controlled to maintain a phase lock between its signal and the average phase of signals arriving from other stations.

The next article in this issue describes a design of such controls and also describes simulations that demonstrate the practicality of the technique.[1] This paper describes the analog simulator used in that work.

The organic synchronizing method compensates the slow phase drift caused by discrepancies in the clock frequencies and the phase changes brought about by changes of transmission delays. The fast phase jitter introduced by changes in the PCM word patterns is not the concern of this study.[2] Therefore, in the simulator, it is convenient to use the cycles of a constant amplitude sinusoid to represent the

PCM frames. The sinusoids are generated by independent oscillators, one situated at each station, and the transmission paths between them are simulated by delay lines.

The particular network simulated is shown in Fig. 1. It comprises four stations interconnected with 12 links. Each link has a large fixed delay representing a transmission path typical of transcontinental distances. A small variable delay is added for simulation of slow delay changes.

II. A STATION DIAGRAM

The control functions for a single station are illustrated in Fig. 2. This station is designated station i. The other stations are labeled j, k, and l. In Fig. 2, only the link from station j is shown in detail, but similar equipment is provided in all links arriving at each of the four stations. The function of the system blocks will be described while tracing a signal through the network.

The sinusoidal output of oscillator j comes to station i through a cascade of fixed delay elements selected to represent a particular path length. The last delay element in the path is servodriven and is continuously variable under control of an external signal to simulate transmission delay variation.

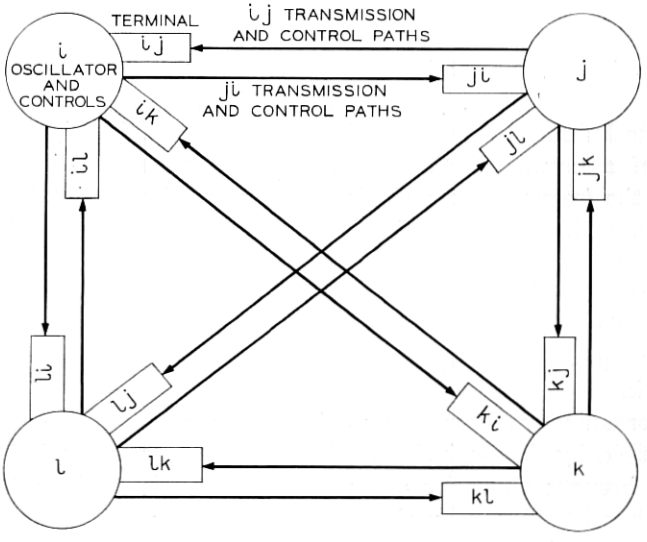

Fig. 1 — A network for simulating organic synchronization of four geographically-separated stations.

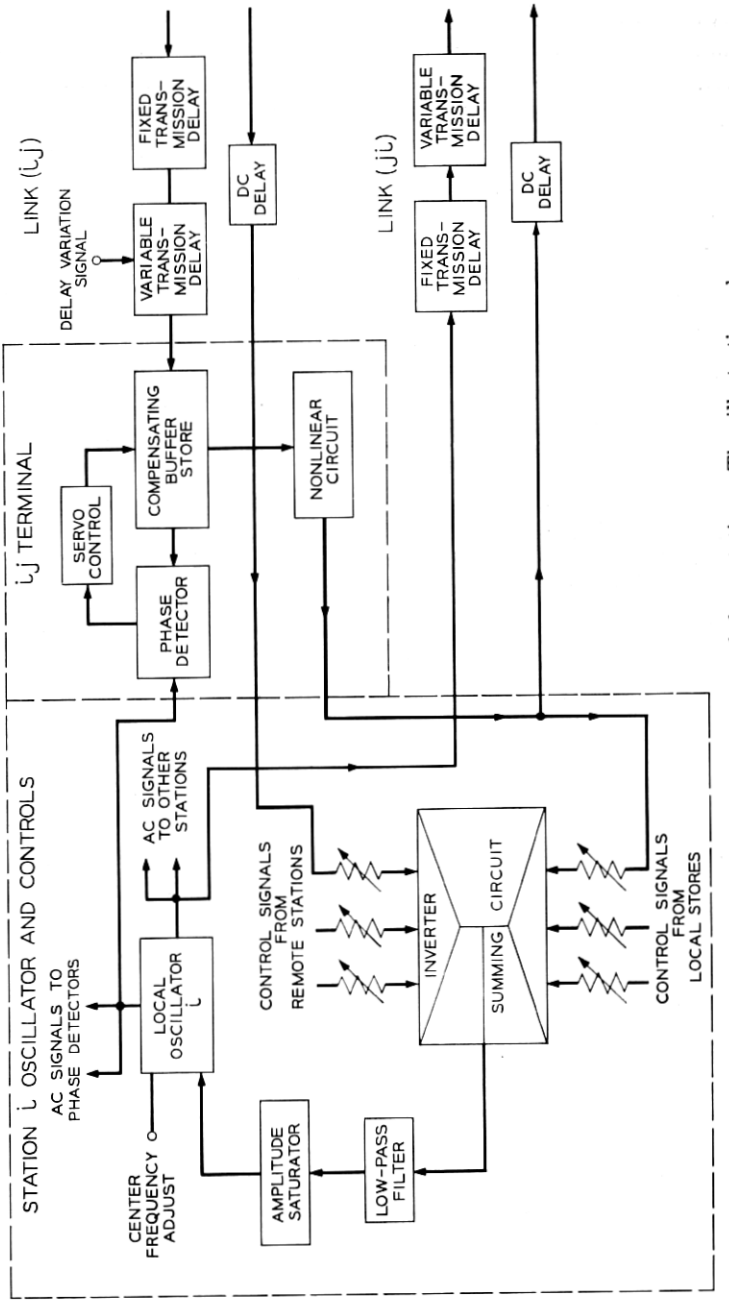

Fig. 2 — Control functions for one of four stations. The illustration shows station i and the simulated transmission links connecting with station j.

At station i the signal is fed to a second continuously variable delay, the compensating buffer store, that is servodriven to maintain the required phase lock. The drive for this delay is derived from the principal phase difference between the output of the delay itself and the local clock. Sufficient gain is provided to keep the phase tracking error less than 3 degrees.

After synchronization of the phases is acquired, change in the delay position is a continuous measure of phase change between the signal arriving from j and the i oscillator. A voltage proportional to this delay position eminates from the compensating buffer store (see box representing this store in Fig. 2). This voltage, designated x_{ij}, is transformed in a series of signal processing operations and used to control the i and j oscillator frequencies in such a way as to reduce the long term frequency differences and minimize the deviation of the compensating delays from their center positions.

The control signal, x_{ij}, may first be modified in a nonlinear circuit that emphasizes the large amplitudes in order to enhance the control influence of delays approaching overflow. Then it is fed separately to two summing circuits, one located at station i and the other at station j. These circuits generate weighted sums of all control voltages derived from links arriving at a station and subtract from the total a weighted sum of the control voltages from links departing the station. The controls returned from remote ends of the departing links are delayed in the simulator, as they would necessarily be in a real system.

The output of the summing amplifier is filtered and applied to a saturating circuit that limits the maximum amplitude excursions. It is then used to adjust the oscillator frequency proportionately.

III. DESIGN SPECIFICATION

In designing simulators, it is unnecessary to copy specifications of realistic systems. Indeed, it is often advisable to use scaling factors that make the simulator convenient to operate. However, for this work, realistic specifications for a possible continental network are followed in order to gain practical experience in designing and operating a network, and to discover any factors of practical importance that may have been overlooked in theoretical studies.

An important component of a PCM center is the local clock which determines the timing of all switching actions at the center. In the simulator, no digital processing is performed, therefore, the clock is simply a 1 megahertz sinusoidal oscillator, one cycle of which represents a frame of information in the digital system. A frequency con-

trol range of one part in 10^6 would be acceptable in practice. A suitable crystal tuned clock would typically have a long term stability of a little less than one part in 10^8. This sets a limit of about 1 per cent on the realizable control accuracy. To maintain this accuracy, noise and zero drift introduced into the low-pass control signals must be less than 1 per cent of full amplitude.

Transmission delays lie in the range 5 to 8 microseconds per mile, depending on the transmission medium. Thus, delays in a continental system may typically lie in the range 0 to 24 milliseconds. In typical conditions, such delays would vary by amounts up to 10 microseconds, largely because of temperature change. The synchronizing system compensating for this variation would have storage capacity in excess of the expected variation in order to have some control margin.

Components of the simulator have properties similar to those discussed above, but the range of parameter variation and disturbances have been increased in order to provide adequate margin for tests under extreme conditions. For measuring convenience, all sources of noise and drift in the system have been made much less than 1 per cent of signal, so that representative disturbances can be introduced in a controlled fashion.

The servodrive for the compensating delay is designed so that its filtering action on the frequency control signal can be neglected. For this approximation to hold, the low-frequency linear response of the servo has been made equivalent to a delay of less than 2 milliseconds. Hysteresis and other tracking errors are less than 1 per cent of a cycle.

IV. THE OSCILLATORS

It is necessary to have very stable oscillators in order to keep spurious phase errors small. The 1 megahertz crystal oscillators purchased and modified for this application deviate, on average, less than one cycle of phase in ten minutes. This is the approximate duration of an experiment.

Each oscillator is individually mounted in a temperature-stabilized enclosure, and is electrically screened from the other units.

The oscillator frequencies are controlled linearly over a range ± 1 cycle per second (that is, one part in 10^6), by changing the voltage on a varactor diode that is loosely coupled to the crystal. The center frequency and voltage sensitivity are both adjusted by precise potentiometers connected as shown in Figure 3. Figure 4 gives an oscillator control characteristic.

When the simulator is in use, the zero settings of the oscillators are

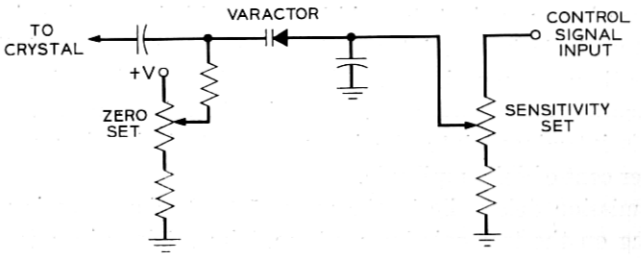

Fig. 3 — Circuit for controlling the 1 MHz station oscillator. The oscillator is controlled linearly through a range of ±1 hertz.

checked before each experiment and their sensitivities are measured about once per week. Realignment, which seldom is necessary, is accomplished by observing Lissajou ellipses which portray the oscillator phases with respect to one another and to an atomic clock.

Zero settings are adjusted to give stationary ellipses when the control voltage is zero. Next, the sensitivities are equalized by adjusting the control voltage to give stationary patterns when all the oscillators are modulated simultaneously with a low-frequency sine wave. In this measurement one oscillator is used as a reference. Its absolute sensitivity is set using calibrated dc inputs and timing beats with respect to the atomic clock.

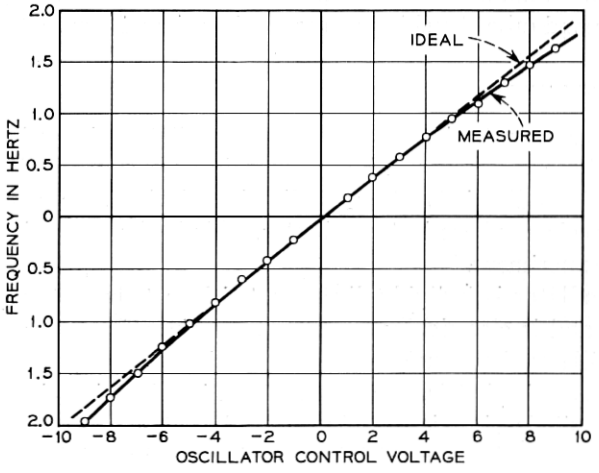

Fig. 4 — Normalized frequency response to a control signal for a typical station oscillator.

V. SIMULATION OF FIXED TRANSMISSION DELAY

Fixed transmission path delays are simulated with commercially available magnetostrictive lines of 2, 6, and 8 milliseconds. Each link uses three of these in tandem. Thus, values of delay from 0 to 24 milliseconds are available in increments of 2 milliseconds. Each delay line is accompanied by an amplifier that makes up the amplitude loss in the magnetostrictive line and its transducers. The net loss is about $(40 + 3\tau)$ dB where τ is the nominal delay in milliseconds. A representative delay unit is shown in Fig. 5.

The gain of each of these amplifiers is tailored to match the associated delay loss. A patching coaxial cable is used to couple the amplifier output to the next delay unit. A filter circuit is incorporated that reduces the effect of using cables of different lengths.

To simulate the fixed delay in the return dc control signal paths, lumped constant LC delays are used. Values of 2, 6, and 8 milliseconds are provided by π-sections selected in sets to equal the corresponding ac delay.

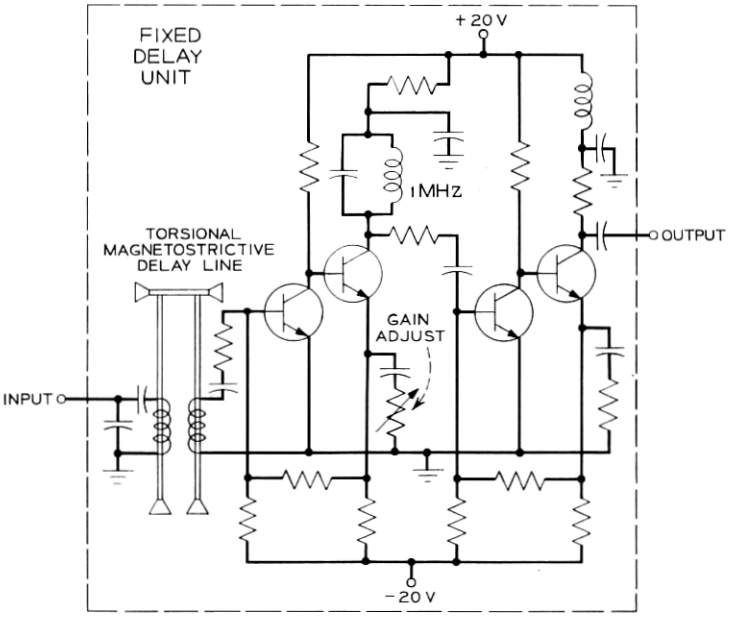

Fig. 5 — Transmission delays are simulated with fixed magnetostrictive delay lines. Associated amplifier compensates for insertion loss.

VI. THE CONTINUOUSLY VARIABLE DELAYS

Continuously variable magnetostrictive delay lines are used to simulate the compensating buffer stores that would be used in a real PCM network. Similar delay lines are also used to introduce variation in the length of the simulated transmission links.

Fig. 6 is a simplified diagram of the compensating buffer store. Each sonic delay wire is mounted horizontally and is paralleled by two resistive potentiometers. Potentiometer A is used to monitor the state of the delay. Potentiometer B is used to generate control signals. Terminal C is the output for the delayed ac signals. Correspondingly-labeled terminals are joined by a flexible cable. A sliding carriage holds the potentiometer wipers, a magnetostrictive receiving transducer, and signal preamplifier. It is driven along a steel rail by a 400-cps motor through a gear train, windlass, and steel cable.

The preamplifier, together with a main amplifier, compensates for approximately 66 dB of loss in the transducers. The loss in the sonic wire is insignificant; therefore, the output is virtually independent of delay position. The variable line has a larger transducer loss than a fixed line because of the inefficiency of the mobile receiver transducer.

Torsional mode lines, rather than conventional longitudinal lines were selected for their greater delay per unit length, that is, approximately 3.3 microsecond per centimeter. The maximum delay is a little more than 200 microseconds. Because of the need to resolve small fractions of a cycle (that is, 1 per cent), the electromechanical drive requires great precision. This is further complicated by the need, already mentioned, for a short time constant in its linear response to slow disturbances. Design details of the servomechanism for the compensating delay shown in Fig. 6 are given in the Appendix.

The "variable transmission delay" simulator has less stringent requirements. It is controlled by a conventional positioning servomechanism shown in Fig. 7. The motor drives these delays so that the potentiometer voltage at B approximately equals the applied voltage V_1. Six volts are needed to fully deflect the lines and the tracking error corresponds with an input of less than 50 mV.

Fig. 8 shows a completed unit which is representative of the 24 that are used for both transmission delay variations and for compensating buffer storage.

VII. THE NONLINEAR FUNCTION

Nonlinear shaping of the frequency control signal is conveniently accomplished by loading the potentiometer output at B with a

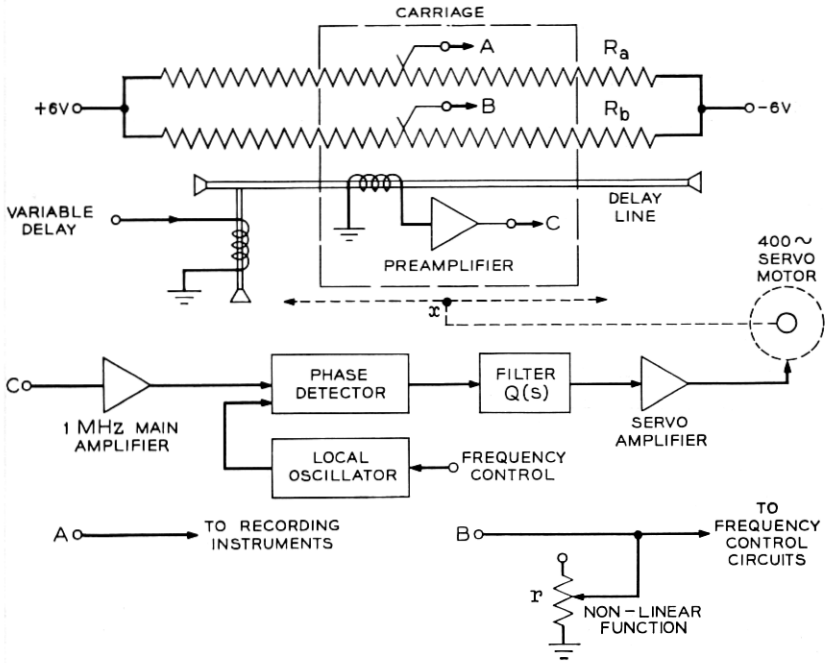

Fig. 6 — The compensating buffer store is a servo-controlled, continuously variable magnetostrictive delay line. The maximum delay is slightly more than 200 microseconds.

variable resistor, as shown in Fig. 6. The control voltage is then given by

$$\partial(x) = x \frac{(\mu - 1)}{(\mu - x^2)} V$$

where

$$\mu = \frac{4r}{R_b} + 1,$$

x is the fractional deviation of the delay from center, $+V$ and $-V$ are the voltages applied to the potentiometer, R_b is the potentiometer resistance (5K), r is the load resistor which is variable from 220 Ω to 10K.

Use of this potentiometer loading introduces contact noise into the control, but this has not been a serious problem during the 6 months the system has been in use.

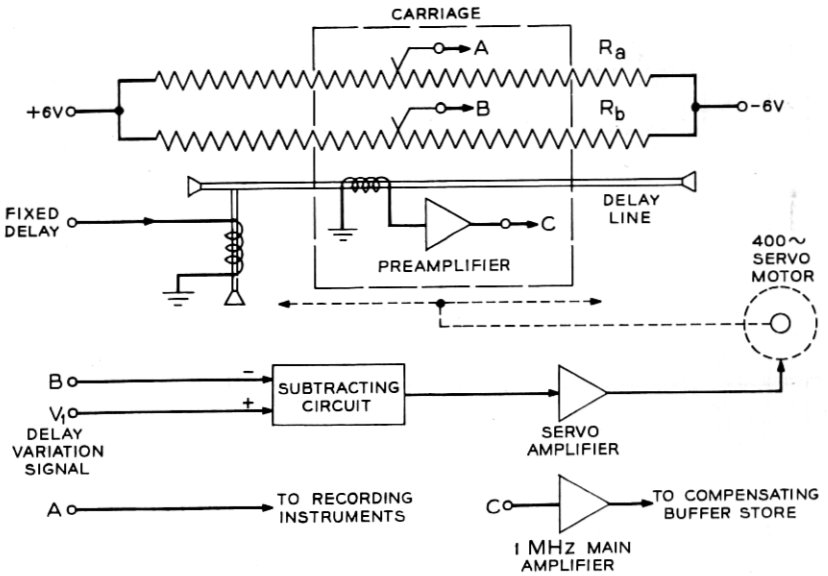

Fig. 7 — Variable transmission delay simulator. The variable delay line assembly is identical to the type used in the buffer store but differs in the control circuits.

VIII. THE PHASE DETECTORS

The phase detector circuit is intended to measure the small phase discrepancy between two supposedly locked sinusoids. For this purpose, a linear response is needed only over a small part of a cycle. However, it is important that the phase indication be independent of input amplitude. Otherwise, spurious amplitude changes, such as might be caused by delay line imperfections, would perturb the control and could possibly cause instability.

Fig. 9 shows the phase detector schematically. The two input sig-

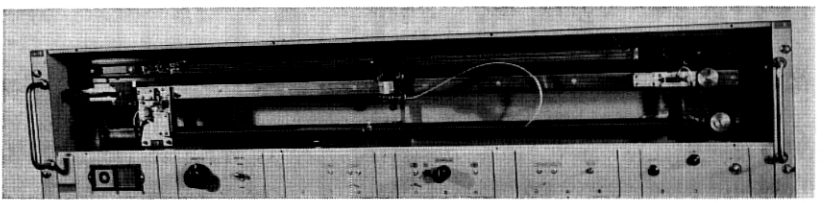

Fig. 8 — One of 24 variable delay units. Twelve are used as buffer stores, the remainder serve as transmission delay simulators.

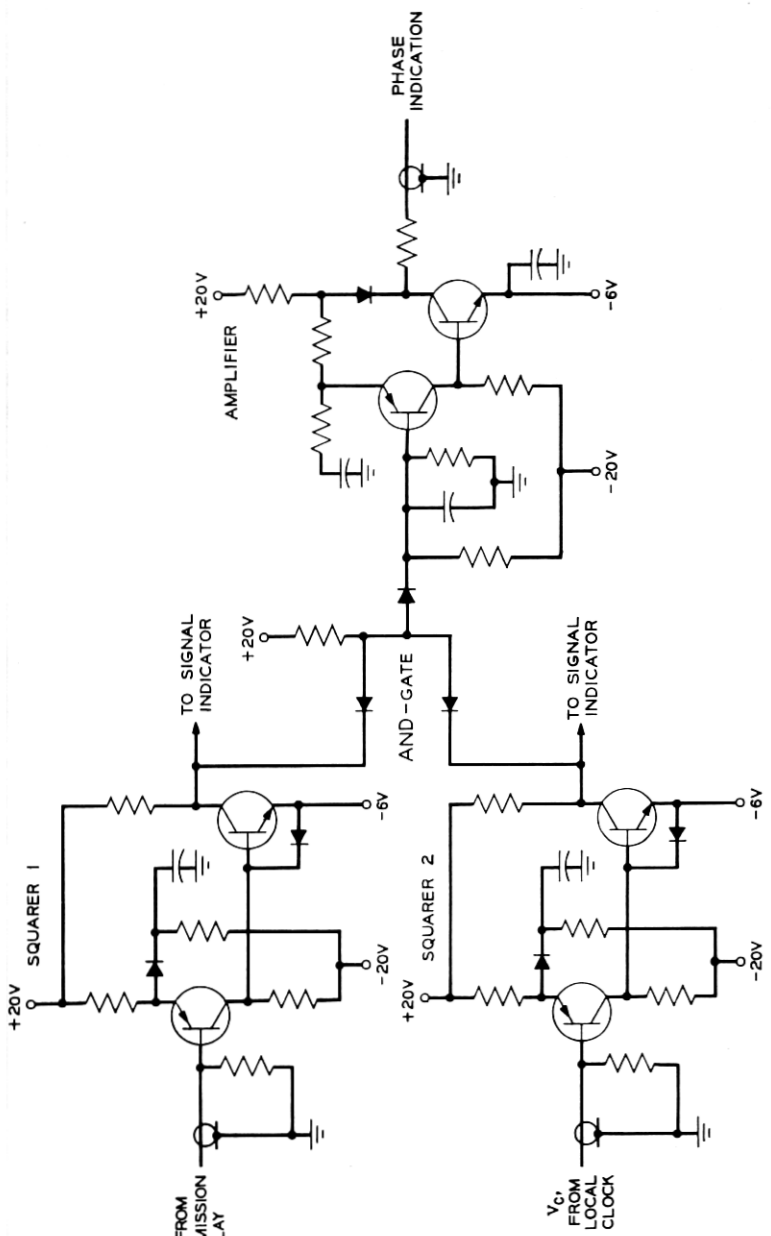

Fig. 9 — Phase detector for measuring small phase discrepancies between two sinusoidal signals.

nals are applied directly to individual waveform squaring circuits.[3] The phase difference between the resulting squarewaves is measured by determining the duration of their time overlap in an *and* gate. This gate is biased to give zero mean output when the two inputs are in quadrature, that is, have 50 per cent overlap, as seen in Fig. 10(a). This figure shows the net output which has been smoothed and fed through the dc amplifier. The amplifier incorporates the filter needed to stabilize the servo, specifications of which are derived in the Appendix.

The fact that the system synchronizes with the signals in quadrature at each phase detector is inconsequential to the simulator experiments. A linear phase response is available for almost ±90 degrees deviation from the quiescent phase. This is more than ample because 3 degrees phase displacement drives the motor to full speed.

Fig. 10(b) shows that the phase indication is sensibly independent of input amplitudes within a large range.

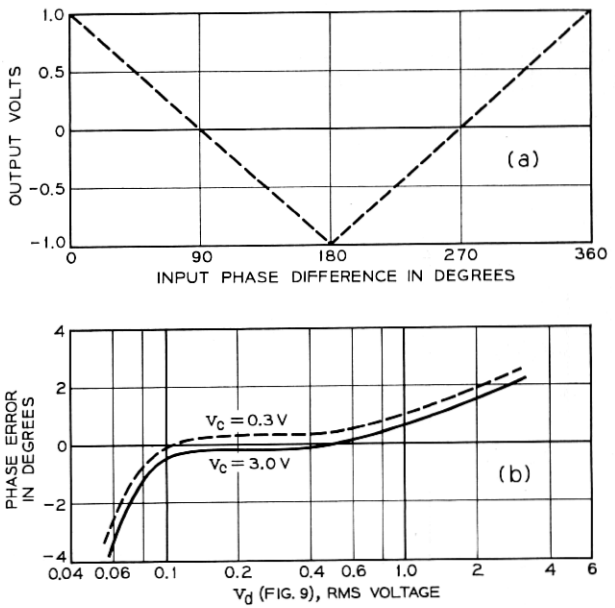

Fig. 10—(a) Output of the phase detector as a function of phase difference between two input signals. (b) Phase errors resulting from amplitude variations in the local clock, v_c, and delayed signals, v_d, are negligible over the required operating range.

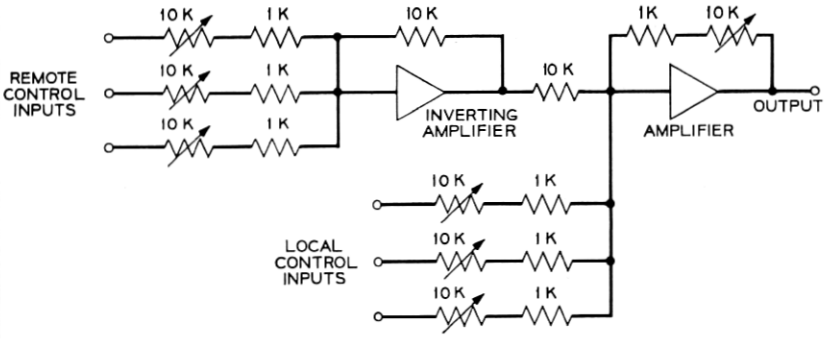

Fig. 11 — Summing of weighted amplitudes.

IX. THE OSCILLATOR CONTROL PATH

The signals used to control the oscillator frequency are combined and shaped in a series of operations depicted here. The summing of weighted amplitudes is performed by conventional operational amplifier circuits, Fig. 11. Similar amplifiers are also used in the filter circuit, Fig. 12, and the amplitude saturator, Fig. 13.

The properties of these circuits can be summarized as follows. The electrical gain in each limb of the summing amplifier is continuously variable over the range 1/11 to 11. The filter has a simple low-pass characteristic, $1/(1+pT)$, for signals below 100 cycles per second. The time constant T is continuously variable from 0.2 to 200 seconds. The saturator clipping levels are continuously variable from 0.1 to 10 volts and they automatically remain symmetrical about zero.

The zero drift and low-frequency noise in these circuits is less than

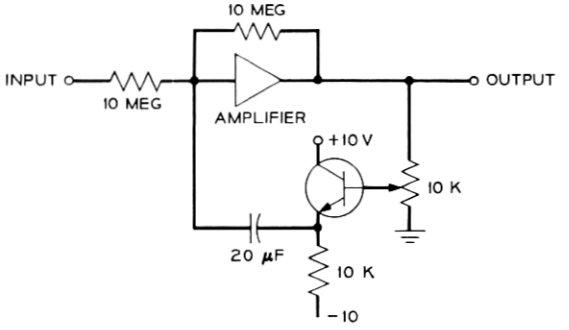

Fig. 12 — Low pass filters.

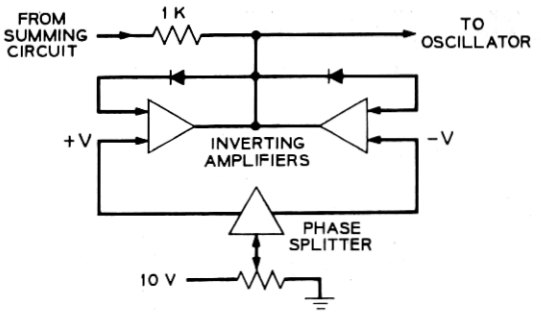

Fig. 13 — Amplitude saturator.

50 mV at the oscillator control inputs and they are designed to accommodate 10 volt peak amplitudes.

X. OPERATION OF THE SIMULATOR

The simulator is arranged to have two active states: standby and run. In the standby condition, the external disturbances are disconnected from all the variable delay simulators and from the oscillators. The compensating delay control servos are disconnected from the phase detector outputs and are connected instead as simple position servos. In this quiescent state the positions of all delays and the oscillator frequencies are determined by preset controls.

To operate the system in the test mode two switches are provided. One connects the externally-provided disturbance signals to the variable delays (Fig. 7) and to the oscillators. The other switch connects the compensating buffer stores (Fig. 6) in the normal run position.

XI. REACTION TO FAILURES

In a real PCM network it is imperative that a failure in any one section of the system not disable the entire network. One assurance against such a catastrophe is to provide an interlock that requires an output from both square-wave generators in the phase detector before the associated servodrive can take the delay from its quiescent setting. Then, if a transmission link fails or an oscillator signal is lost, all the associated compensating delays immediately go to their quiescent states and have no further influence on the frequency control of the remaining operating system.

This facility is part of the simulator. It is used to simulate response in various fault conditions.

XII. SUMMATION

The simulator has been used to investigate a large number of networks and control parameters. It has performed reliably and functions close to theoretical prediction. Some specific results that have been obtained are reported in the article which follows this.[1]

Figs. 14 and 15 give a general view of the complete simulator. Fig. 14 shows the array of 24 servodriven transports which serve as variable delay units and Fig. 15 shows the master control and recording equipment.

ACKNOWLEDGMENTS

This work was done under the supervision of M. Karnaugh. We are grateful to J. C. Candy for his counsel with much of the design.

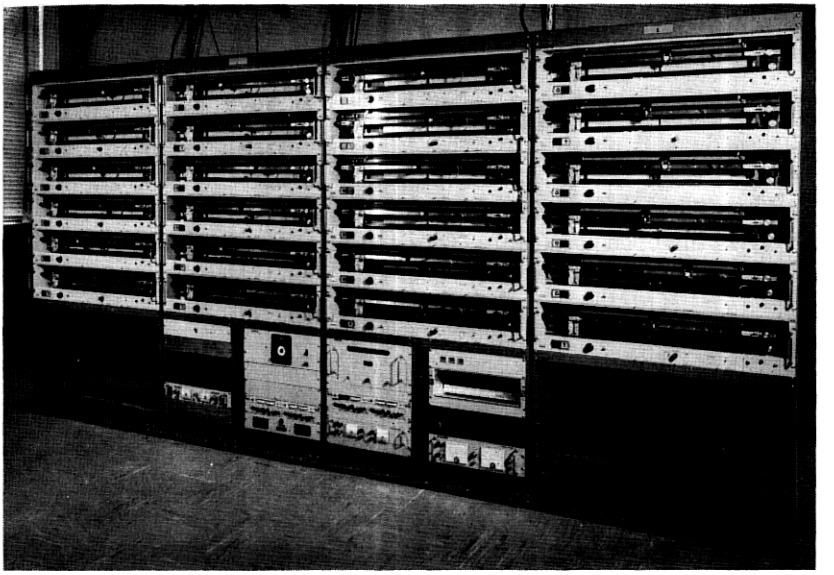

Fig. 14 — Bays containing the 24 servo-controlled variable delay lines.

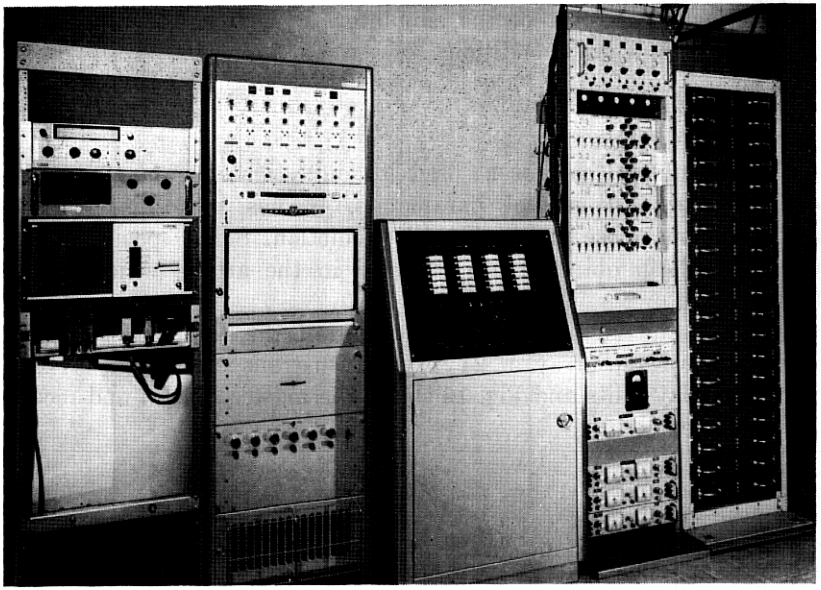

Fig. 15 — Left to right: recording equipment, master control, and the fixed transmission delay simulators.

APPENDIX

Design of the Servodrive for the Buffer Stores.

The gain and phase properties required in the servodrive loop are described here. Let Δx be the departure of the shuttle from perfect tracking. Then using capitals to denote Laplace transforms, $X(s)/\Delta X(s)$ is the open loop gain, G, of the servo in Fig. 6 and the closed loop response will then be

$$\frac{X(s)}{X(s) + \Delta X(s)} = \frac{G(s)}{1 + G(s)}$$

where

$$G(s) = \frac{G_0 Q(s)}{s(1 + sT_1)}$$

where

$G_0 = ab$ is the gain constant

a is the volts per unit error in x out of the phase detector

b is the shuttle velocity per volt into the servo amplifier
T_1 is the mechanical time constant of the motor and drive mechanism.

The stabilizing filter has the form

$$Q(s) = \frac{(1 + sT')}{(1 + sT_2)(1 + sT_3)}$$

Where the phase advancing time constant T' is necessary to stabilize the control and the two retarding time constants ensure a falling gain characteristic at high frequencies. This falling gain is needed to reduce noise and to limit below 200 cps the band of signals fed to the 400 cps motor drive.

The loop can be written

$$\frac{G}{1 + G} = \frac{(1 + sT')}{1+s\left(\frac{1}{G_0}+T'\right)+\frac{s^2}{G_0}(T_1+T_2+T_3)+\frac{s^3}{G_0}(T_1T_2+T_2T_3+T_3T_1)+s^4\frac{T_1T_2T_3}{G_0}}$$

and at low frequency as s tends to zero this resembles a simple delay G_0^{-1}. It is concluded that a gain G_0 greater than 500 is needed to meet the delay specification of 2 milliseconds. But the condition for stability as given by Routh is

$$\frac{1}{G_0} + \frac{T_1T_2T_3G_0\left(T' + \frac{1}{G_0}\right)^2}{(T_1T_2 + T_2T_3 + T_3T_1)(T_1 + T_2 + T_3)} > \frac{T_1T_2 + T_2T_3 + T_3T_1}{T_1 + T_2 + T_3} - T'$$

Given $T_1 = 5$ msec and selecting $T' = 5$ msec, $T_2 = 1$ msec, $T_3 = 0.8$ msec, the system is marginally stable with $G_0 = 2250$ and in practice was satisfactory for applications using gains up to 10^3.

Experimental measurements confirmed that the effective low frequency delay approximates $1/G_0$, it was also noted that tracking errors decreased approximately as $1/G_0$ when the amplifier gain was varied. This tracking error is less than ± 0.003 centimeter on the magnetostrictive wire with a loop gain of 10^3.

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