Diode and Transistor Self-Analogues for Circuit Analysis

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A new method of circuit analysis based on the time-scaling of actual circuits has been proposed. Audio-frequency self-analogues of microwave frequency transistors can be constructed using charge control theory, and these accurately model transistor performance in the active region. Scaling of storage times in diodes and transistors requires multiple-lump modeling. The multiple lump model developed by Linvill is reformulated here on the basis of an analogy between charge density in the semiconductor and charge density in the model, rather than between carrier density and voltage. Only two parameters, time constants corresponding to lifetime and a diffusion transit time in the semiconductor, need be specified in the reformulated model. This simplified multiple-lump model should be generally useful for device calculations. We describe a diode self-analogue which is an exact physical realization of the multiple-lump model. Separation of active and saturation region stored charges can be achieved in a transistor self-analogue, so that a single-lump model can be used for the active, and a multiple-lump model for the saturation region stored charges.

I. INTRODUCTION

A new approach to circuit analysis has been poposed which allows high-frequency circuits to be characterized using simple low-frequency models.[1] With this approach, nanosecond diodes and transistors can be slowed down to audio frequencies and interconnected in audio frequency breadboard models of the high-frequency circuits. Thus, high-frequency circuits can be evaluated and optimized with the convenience afforded by low-frequency breadboard techniques.

According to charge-control theory,[2] the frequency and transient responses of diodes and transistors are determined by the charges stored within the devices. Nanosecond diodes and transistors can be slowed down to millisecond models simply by multiplying their stored charge by a factor of 10^6 or some other convenient value. Charge

storage in the devices can be classified broadly as terminal voltage dependent (fixed charge in depletion layers) and terminal current dependent (charge in transit). The former can be multiplied by connecting large capacitors between the device terminals, as described by Levine.[3] The latter can be multiplied by using small resistors as current sensors in series with device terminals, and using the voltage developed across these resistors, suitably amplified, to cause charge storage in capacitors connected to the device.[1] Models thus constructed have given excellent results for transistors operated in their active regions.[4]

The models also give time-scaled storage times when representing diodes or transistors operated in their saturation regions, but the values may be in error by a factor of two or more. One difficulty is that the charge-control model does not provide any means for representing the distribution of charge throughout bulk semiconductor regions. It is shown here that by replacing the storage capacitors in the model by resistance-capacitance networks, an exact physical realization of the multiple-lump Linvill model can be obtained. A second difficulty in the case of the transistor is that the time constants for charge storage in the saturation region and in the active region are different in general. Section 3 describes means for overcoming this difficulty.

II. DIODE SELF-ANALOGUES

2.1 *Charge-Control Self-Analogue*

Fig. 1 shows a simple self-analogue of a diode. The diode itself, D, is its own dc model. Capacitor C_D is used to multiply depletion layer

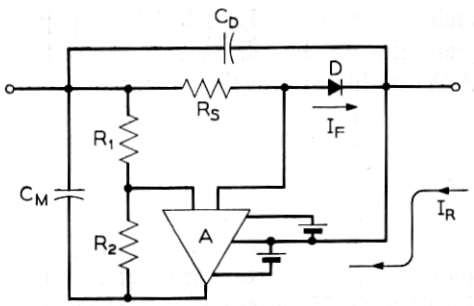

Fig. 1 — Diode self-analogue with scaling of charge storage.

stored charge in D, with,

$$C_D = KC_J \tag{1}$$

in which C_J is the junction capacitance of the diode. C_D would ideally have the same voltage dependence as C_J. (A large area junction might possibly be used, with a battery to avoid forward bias).

Resistor R_S, amplifier A (whose gain is R_2/R_1) and capacitor C_M are used to multiply minority carrier storage effects. Minority carrier charge storage Q_M within the diode itself is given by

$$Q_M = I_F\tau \tag{2}$$

in which I_F is the forward current in the diode and τ is an effective lifetime which will usually be dominated by the bulk minority carrier lifetimes in the P and the N regions. The charge Q'_M stored in C_M in the model is

$$Q'_M = I_F R_S \left(\frac{R_2}{R_1}\right) C_M \tag{3}$$

in which parameters in the model are chosen to give

$$R_S \left(\frac{R_2}{R_1}\right) C_M = K\tau. \tag{4}$$

K is the desired time-scaling factor.

During turn-on and turn-off transients, Q_M in the diode and Q'_M in the model obey the charge control equations

$$\frac{dQ_M}{dt} = I - \frac{Q_M}{\tau} \tag{5a}$$

$$\frac{dQ'_M}{dt} = I - \frac{Q'_M}{K\tau} \tag{5b}$$

in which in which I is the terminal current. In the model, a current I_F which is proportional to Q'_M, flows in the actual diode at all times, maintaining the correct bias voltage on the diode at all times (assuming that series resistance gives negligible voltage drops).

Provided that amplifier A has good common-mode rejection, the diode voltage has negligible influence on the charge stored on C_M. Fig. 2 shows a slightly modified version of the analogue in which the full diode voltage appears across the plates of C_M. In this modified version stored charge on C_M is the analogue of both the depletion

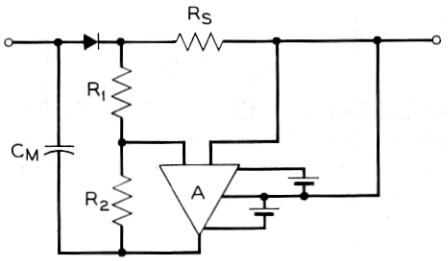

Fig. 2 — Alternative diode self-analogue with scaling of charge storage.

layer stored charge and the minority carrier stored charge; therefore, capacitor C_D has been eliminated. This version cannot be used if non-linear depletion layer effects are to be represented.

The analogue of Fig. 1 is satisfactory whenever the charge control equation (suitably time-scaled) satisfactorily describes the transient behavior of the actual diode. This is true in at least two important types of diode: epitaxial diodes with epitaxial layers which are thin compared with a diffusion length, and diodes formed in integrated circuits using the emitter-base junction of a transistor whose base-collector junction is shorted. In the second type of diode, minority carrier storage is confined to the thin base layer.

2.2 *Multiple Lump Analogues*

Although thin epitaxial layers are generally used for high speed switching diodes, such diodes are often so heavily gold doped that the diffusion length for minority carriers is even less than, or at least comparable with, the epitaxial layer thickness. In this case diffusion delays comparable with diode storage times occur during turn-off. The charge-control equation (5) is not satisfactory then, and the simple model shown in Fig. 1 is inadequate. For example, in the extreme case of a diode formed on a uniformly doped substrate, and for a reverse current equal to the forward current, Kingston's analysis,[5] which includes diffusion delays, gives a storage time $t_s = 0.25\ \tau$, and a fall time $t_f = 0.6\ \tau$, whereas equation (5) gives $t_s = 0.7\ \tau$ and $t_f = 0$.

Diffusion delays can be taken into account by using a multiple-lump Linvill model.[6] Figure 3 shows a diode self-analogue which can be made an exact physical realization of such a model. This self-analogue is justified later by its node equations which are expressed

in terms of the stored charge at each node, rather than the voltage:

Node 1. $$I - I_F = I - \frac{Q_1}{rAC} = \frac{Q_1 - Q_2}{RC} + \frac{dQ_1}{dt}$$

Node X. $$\frac{Q_{X-1} - Q_X}{RC} = \frac{Q_X - Q_{X+1}}{RC} + \frac{dQ_X}{dt} + Q_X \cdot \frac{G}{C}$$

Node N. $$\frac{Q_{N-1} - Q_N}{RC} = \frac{dQ_N}{dt} + Q_N \cdot \frac{G}{C} + \frac{Q_N}{R_S C}.$$

In this case the output of the amplifier is double-ended; each output has the polarity of the input opposite to which it is drawn.

The Linvill model is based on an analogy between carrier density in the diode and voltage in an *r-g-c* line. The well-known continuity and current equations for the uniformly-doped semiconductor region adjacent to the transition region in a diode are

$$\frac{\partial(N - Ne)}{\partial t} = -\frac{N - Ne}{\tau} - \frac{\partial I/qA}{\partial x} \tag{6}$$

$$\frac{I}{qA} = -D \frac{\partial(N - Ne)}{\partial x} \tag{7}$$

in which

$N - Ne$ = carrier density in excess over equilibrium density
τ = lifetime
I = current
q = particle charge
A = cross sectional area of diode
D = diffusion constant
Drift current is assumed negligible.

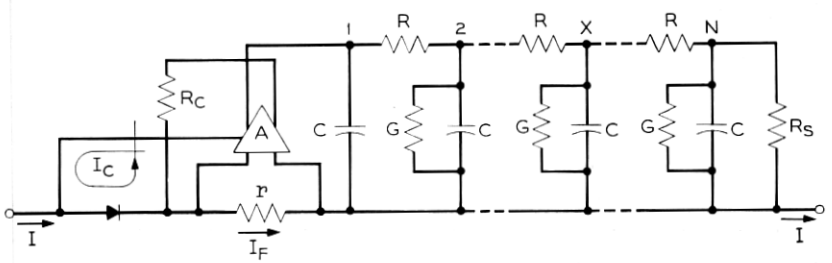

Fig. 3 — Physical realization of Linvill model as a diode self-analogue.

The voltage-current equations for the analogous r-g-c transmission line are

$$\frac{\partial I}{\partial X} = -G'V - C'\frac{\partial V}{\partial t} \tag{6a}$$

$$\frac{\partial V}{\partial X} = -R'I \tag{7a}$$

in which

		Analogue of
V	= voltage	$N - Ne$
I	= current	I
G'	= conductance (combinance) per unit length	qA/τ
C'	= capacitance (storance) per unit length	qA
R'	= resistance (1/diffusance) per unit length.	$1/qAD$

The analogy can be expressed in a simpler, dimensionally-consistent way if the equations are written in terms of charge per unit length, Q', in both cases. Then equations 6 and 7 become

$$\frac{\partial(Q' - Q'e)}{\partial t} = -\frac{Q' - Qe'}{\tau} - \frac{\partial I}{\partial X} \tag{8}$$

$$I = -D\frac{\partial(Q' - Qe')}{\partial X} \tag{9}$$

and Equations 6a and 7a become

$$\frac{\partial I}{\partial X} = -\frac{G'Q'}{C'} - \frac{\partial Q'}{\partial t} \tag{8a}$$

$$\frac{\partial Q'}{\partial X} = -R'C'I. \tag{9a}$$

Analogous quantities are now

Diode	r-g-c line
$Q' - Qe'$	Q'
I	I
τ	C'/G'
D	$1/R'C'$

The length of the r-g-c line is equal to the length of the semiconductor region which it represents. Redundancy caused by introducing area A in Equations 6 and 7 has been removed and only two param-

eters of the r-g-c line need be specified. The elements $1/R$, G, and C correspond to the diffusance, combinance, and storance in the Linvill model.

Fig. 4 shows the lumped version of the r-g-c line. Its node equations are:

Node 1. $$I = \frac{Q_1 - Q_2}{RC} + \frac{dQ_1}{dt} + \frac{Q_1 G}{C}$$

Node X. $$\frac{Q_{X-1} - Q_X}{RC} = \frac{Q_X - Q_{X+1}}{RC} + \frac{dQ_X}{dt} + \frac{Q_X G}{C}$$

Node N. $$\frac{Q_{N-1} - Q_N}{RC} = \frac{dQ_N}{dt} + \frac{Q_N G}{C} + \frac{Q_N}{R_s C}$$

These are expressed in terms of charge stored on the capacitors connected to each node rather than node voltages. It may be assumed that the line and diode have been cut into equal lengths δx, so that

$$C/G = \tau \tag{10}$$

$$RC = \delta x^2 R'C' = \delta x^2/D. \tag{11}$$

The RC product in equation 11 is the analogue of a diffusion transit time between sections of the diode.

Resistor R_s can be used to represent a surface with recombination velocity v_s (or a collector junction in which carriers travel with scatter limited velocity v_s). Then R_s is given by

$$\frac{\delta x}{R_s C} = v_s \, . \tag{12}$$

The node equations for the lumped network are identical with the node equations for the diode self-analogue represented by Fig. 3, provided $rA = 1/G$. The charge distribution in the self-analogue is then the same as that in the Linvill model under the same boundary

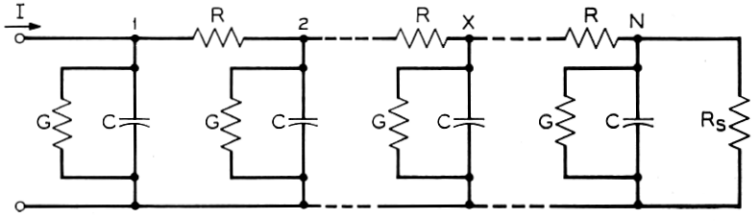

Fig. 4 — Multiple-lump model.

conditions. If the self-analogue is to operate at low frequencies, appropriate scaling factors are needed. We discuss an example in the appendix and in Section 2.3. It remains to be shown that the correct diode voltage is maintained at all times.

In the actual diode, the applied junction voltage is

$$V_J = \frac{kT}{q} \ln \frac{Q_1}{Qe} \tag{13}$$

in which

Q_1 = charge in lump closest to the junction
Q_e = equilibrium charge in that lump.

In the self-analogue, neglecting internal resistance, and assuming that r is chosen to be small, the analogue diode voltage is:

$$V_{JA} = \frac{kT}{q} \ln \left[\frac{I_F + I_C}{I_{sat}} + 1 \right].$$

With I_C being the current so designated in Fig. 3,

$$V_{JA} = \frac{kT}{q} \ln \left[\frac{I_F\left(1 + \frac{rA}{R_C}\right)}{I_{sat}} + 1 \right]$$

$$= \frac{kT}{q} \ln \left[\frac{\left(1 + \frac{rA}{R_C}\right) \frac{Q_1}{rAC}}{I_{sat}} + 1 \right]. \tag{14}$$

Bearing in mind that Q in the model is the analogue of $Q - Qe$ in the diode, (13) and (14) are identical if

$$R_C = rA \Big/ \left(\frac{rACI_{sat}}{Qe} - 1 \right). \tag{15}$$

Rather than evaluate (15) directly, it is easier to proceed as follows. If R_C is chosen correctly for one condition, (13) and (14) show that the diode voltage will be correct under all conditions. Under dc conditions it is required that the full current I should flow in the diode. The current through R_C should therefore replace that lost through the dc resistance of the rGC network, and R_C should be set equal to this dc resistance.

2.3 *Numerical Example*

Figure 5b shows a two-lump self-analogue of the typical diode shown in Figure 5a. Numerical values for the parameters are derived

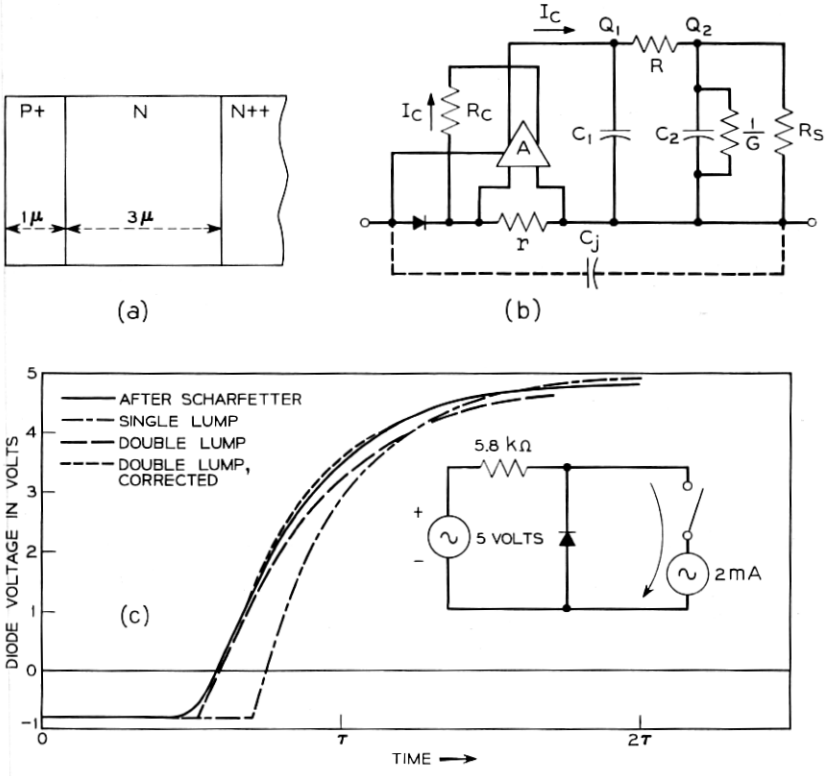

Fig. 5 — (a) Typical epitaxial diode. (b) Model of epitaxial diode. (c) Diode circuit and response curves.

in the appendix, where the behavior of the two-lump analogue under transient conditions also is described. Figure 5c shows the behavior of the actual diode, a single-lump and a double-lump model in the circuit shown inset. This circuit gives equal forward and initial reverse currents, and 5 volts reverse bias when the diode is switched off.

The solution for the diode was provided by D. L. Scharfetter from an exact solution of the semiconductor equations using the well-tested procedures that he and Gummel developed.[7] The single-lump model gives only a rough approximation to the actual diode and cannot be adjusted to give reasonable agreement because of its incorrect storage time. The two-lump model, as first calculated from the diode parameters is still not in good agreement, but a 20 per cent reduction in the assigned value of the junction capacitance gives ex-

cellent results. This agreement is, in fact, better than might be expected and results from compensating errors.

Transient calculations for the three-lump model give a storage time of 0.44τ. For the infinite lump model the storage time is presumably shorter. However, current-dependent stored charge in the "depletion" region was found by Scharfetter to be a significant proportion of the total. Also, the "depletion" layer capacitance is very large in the storage regions. Both effects lead to a longer storage time, and compensate for the over-estimation resulting from representing the epitaxial layer by only two lumps.

III. TRANSISTOR SELF-ANALOGUES

3.1 *Transistor Operated in Active Region*

Figure 6 shows the simplest way of time-scaling a transistor. Charge stored on C_M is the analogue of control charge stored in the transistor. Capacitors connected between B and C, and between B and E can obviously be used to represent fixed depletion layer capacitance. They have been omitted from the diagram for the sake of simplicity and will not be discussed further.

The analogy holds even under base-widening conditions[8] and in saturation provided that the control charge recombines everywhere within the transistor according to a single lifetime. In that case,

$$I_B = \frac{Q}{\tau_Q} \tag{16}$$

in which

I_B = base current
Q = in-transit control charge
τ_Q = lifetime.

In the analogue r, R_1, R_2 and C_M should satisfy

$$r\left(\frac{R_2}{R_1}\right)C_M = K\tau_Q \, . \tag{17}$$

The distribution of controlled and control charge in high-frequency, double-diffused transistors is quite complicated and does not lend itself well to separation into "base" stored charge, "collector" stored charge, or even into "current" controlled charge and "voltage" controlled charge. This can be seen from the results of numerical analysis of charge distribution in such transistors, as given by Gummel.[7]

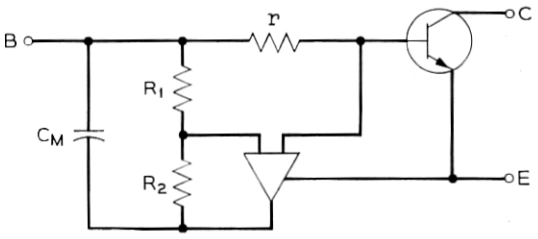

Fig. 6 — Transistor self-analogue.

To a first approximation however, the "current dependent" control charge in an npn transistor consists of (*i*) a component of base charge Q_B associated with electrons in transit through the base, and (*ii*) a component of base charge Q_c associated with charge in transit through the collector transition region. Recombination current associated with Q_c is very small, and equation 16 is not applicable in the sence described above. However, since

$$Q_B = I_B \tau_B \,, \tag{18}$$

and

$$Q_c = I_c \frac{t_c}{2} = I_B h_{FE} \frac{t_c}{2} \tag{19}$$

in which

τ_B = effective base lifetime
I_c = collector current
t_c = transit time through collector depletion layer, equation 16 is still applicable provided that τ_Q is interpreted as

$$\tau_Q = \tau_B + \frac{h_{FE} t_c}{2}. \tag{20}$$

In spite of the difficulties in modeling described above, the simple model illustrated in Fig. 6 has been shown to give a remarkably accurate representation of transistor operation in the active region.[4]

The multiple-lump Linvill model cannot be used to represent diffusion delay in the base of the transistor in the same way that it was used for the diode. Suppose lump 1 represents the base section closest to the emitter, lump N that closest to the collector. Emitter junction voltage should be related to the charge stored on lump 1 if the effects of emitter transition region storage on high frequency

response is to be correctly reproduced; collector current should be related to charge stored on lump N, and the two requirements conflict with one another. Two-pole representation of the transistor can be obtained if necessary, however, using two amplifiers as Fig. 7 shows.[1]

3.2 *Transistor Operated in Saturation Region*

When transistors operate in their saturation regions, excess control charge is stored in the device. Excess control charge is also stored in the model because of the excess base current. But equation 16 is not generally valid in this region because the majority of the excess control charge in double-diffused transistors is stored in the collector region in which the lifetime ordinarily differs from that of the base. Also, because the collector region is much thicker than the base, a multiple lump model is usually needed to represent the charge distributed throughout the collector region even though a single lump model is satisfactory for the base.

If the primary problem is that the collector life-time τ_c is not equal to τ_B, then the model shown in Fig. 8 can be used, in which

$$R' \cdot \frac{R_2}{R_1} \cdot C_M = \tau_Q \tag{21}$$

$$R'' \cdot \frac{R_2}{R_1} \cdot C_M = \tau_c \, . \tag{22}$$

In this model, two time constants are obtained with a single operational amplifier. The simplicity of the model is, however, achieved at the cost of loss of accuracy in the dc collector voltage in saturation.

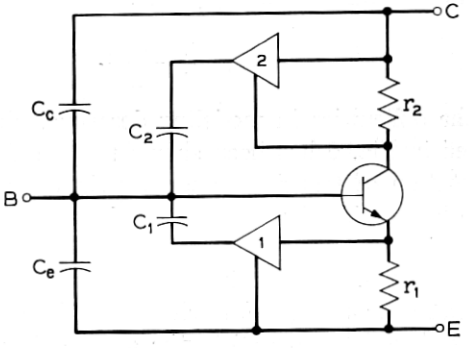

Fig. 7 — Two-pole transistor self-analogue.

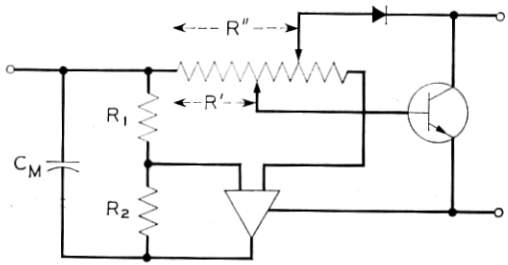

Fig. 8 — Transistor self-analogue with different time constants for active and saturation region storages.

As in the case of diodes, charge distribution in the collector layer of epitaxial transistors in saturation is likely to be troublesome. For example, an npn transistor which gives a storage time of 5 ns (measured with $I_{BF} = I_{BR} = I_C$) has an effective lifetime of 7 ns according to charge control theory. This, however, gives a diffusion length of about 3 μm (with $D = 10$ cm^2/sec), which is about equal to typical epitaxial layer thicknesses, and is inconsistent with the assumption of charge-control theory that charge is stored close to the junctions. Digital programs for circuit analysis commonly use the Ebers-Moll model,[10] which uses a similar assumption. Predicted storage times are too long and current fall times are too short in this situation. A multiple-lump model similar to that proposed for the diode is needed for more accurate representation of storage and fall time. In this case, it is necessary to represent simultaneously (*i*) active region storage with a single-lump model and (*ii*) saturation region storage with a multiple-lump model.

In the model shown in Fig. 9, active and saturation region storages are separated by the following means. The combination R_1 , A_1 , C_1 represents active region storage, R_2 , A_2 and its associated $R - G - C$ network represent saturation region storage. Active region storage which would otherwise occur because of base current flowing in R_2 is cancelled by feedback via R_4 . Thus, the feedback current I_f in R_4 , which flows only in R_2' because of the ground connection of amplifier A_1 , is

$$I_f = \left(\frac{I_e R_1 A_1}{R_4}\right) \tag{23}$$

in which I_e = emitter current.

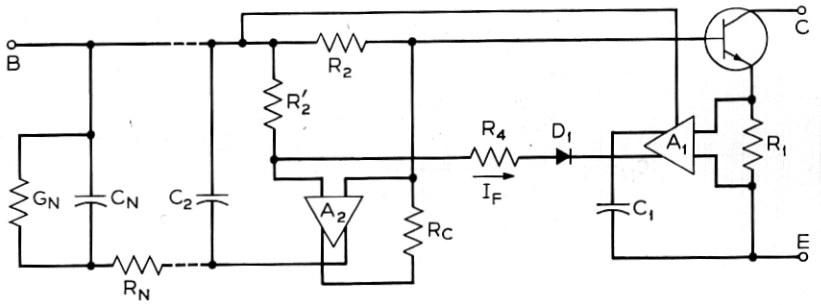

Fig. 9 — Separation of active and saturation region storage.

Diode D_1 is chosen to compensate for the forward bias voltage across the base-emitter junction of the transistor, and voltages across R_1, R_2, and R_2' are designed to be negligible. Then if $R_4/R_1A_1 = h_{FE} + 1$ the desired cancellation will be achieved. Cancellation can only be partial since h_{FE} depends on i_e.

CONCLUSIONS

A new technique of circuit analysis, by which high-frequency circuits can be evaluated and optimized using simple audio frequency breadboard techniques has been demonstrated. It is based on the use of audio frequency self-analogues of diodes and transistors, which can be formed by multiplying the stored charge in the devices by some suitable factor such as 10.[6] Self-analogues based on charge-control models can satisfactorily represent (*i*) the base region of a transistor and (*ii*) diodes and transistors formed in epitaxial layers which are thin compared with a diffusion length. The latter condition is not satisfied by most switching diodes and transistors. Self-analogues can be constructed which are exact physical realizations of the multiple-lump Linvill model. These can be used to represent diodes and transistors formed on epitaxial layers of arbitrary thickness.

APPENDIX

Specific Design Example

Figure 5a shows an epitaxial diode with typical dimensions. Other parameters used in this section are:

Lifetime, $\tau = 3$ns
Diffusion constant, $D = 10$ cm^2/sec

Epitaxial layer doping $= 10^{17}/\text{cm}^3$
Surface concentration of diffused layer $= 10^{20}/\text{cm}^3$.

The effective recombination velocity at the epitaxial interface can be expected to be low because outdiffusion from the substrate creates a built-in field which keeps minority carriers away from the interface. 1000 cm per second is used as an illustration.

Figure 5b shows the two-lump self-analogue of the diode. We will assume that each of the lumps represents half of the epitaxial layer, so that $C_1 = C_2$. With a scaling factor of 10^6:

$$\frac{C_1}{G} = K\tau = 10^6 \times 3 \times 10^{-9} = 3 \text{ ms}$$

$$RC_1 = K\frac{\delta \times 2}{D} = 10^6 \times \frac{(1.5 \times 10^{-4})^2}{10} = 2.25 \text{ ms}.$$

Both r and A can be arbitrarily chosen. A gain of 100 and resistance of a few ohms, say 5Ω, are convenient values to use in practice. Since $rA = 1/G$, this gives $1/G = 500\Omega$, and $C_1 = 3ms$ $G = 6\ \mu F$, and $R = 2.25ms/C_1 = 275\Omega$. Finally, equation 12 with a scaled value for saturation velocity gives $R_S = 25{,}000\Omega$, which is too high to have a significant effect on the model and will be neglected.

Current-dependent charge storage will also occur in the p-layer and the depletion layer. The p-layer is typically diffused and a charge stored in it will lie close to the junction. Both effects could therefore be represented by an additional capacitor in parallel with C_1, with rA reduced in value to $\gamma\ r\ A$, in which γ is the efficiency of injection into the n-layer. This complication was not introduced into the present model.

The behavior of the two lump model was calculated assuming a steady-state forward-bias current I_f followed instantaneously at $t = o$ by a reverse bias current I_r. Solutions for Q_1 and Q_2 during storage time t_s are then:

$$Q_1 = -I_r\tau\left(\frac{GR+1}{GR+2}\right) + \frac{\tau}{2}(I_r + I_f)e^{-t/\tau} + \frac{GR\tau}{2(GR+2)}(I_r + I_f)\exp\left(-\frac{GR+2}{GR}\frac{t}{\tau}\right)$$

$$Q_2 = -\frac{I_r\tau}{GR+2} + \frac{\tau}{2}(I_r + I_f) - \frac{GR\tau}{2(GR+2)}(I_r + I_f)\exp\left(-\frac{GR+2}{GR}\frac{t}{\tau}\right).$$

Storage time ts is defined as the time at which Q_1 goes to zero. After T_s:

$$Q_1 = 0$$

$$Q_2 = Q_2(t_s) \exp\left(-\frac{GR+1}{GR}\cdot\frac{t}{\tau}\right).$$

The behavior of the model inset in Figure 5c was compared with that of an actual diode in the following way. The response of the diode was obtained from an exact computer solution of the semiconductor equation using the procedures developed by Gummel and Scharfetter.[7] This solution is given in Figure 5c. The area of the diode, 3.33×10^{-6} square centimeters, corresponds to a current density of 300Å per square centimeter.

Using the Lawrence-Warner[10] curves, the average junction capacitance, defined as total charge per total voltage, in the range from 0 to 5.8 volts is 0.153pF. Using the equations and numerical values for the two-lump model given previously, this leads to the double-lump curve in Figure 5c. A 20 per cent reduction of C_j to obtain best fit led to the corrected double-lump curve. The figure shows the solutions for a single lump model for comparison. These results are discussed in Section 2.2.

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