# Recirculating Ultrasonic Stores: An Economical Approach to Sequential Storage with Bit Rates Beyond 100 MHz

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(Manuscript received September 30, 1968)

*State of the art integrated circuits and ultrasonic delay lines can be combined to form batch-fabricated digital storage modules having random access to sequentially stored blocks of information. Greatest economy is indicated if such stores are designed for as high a bit rate as is technologically feasible, at present limited by the speed of available integrated circuitry. A store of optimum design will have a block size of approximately 1000 bits which, for a bit rate of 100 MHz, gives a maximum latency time of approximately 10 microseconds. Such designs are realizable with zero temperature coefficient material. The stores can be used as main memories for small computers or as fast transfer stores shuttling information between a slow external bulk memory and a very fast random access memory in large computers.*

*A variety of accessing modes permit these stores to operate over a large range of access rates without requiring large buffer stores.*

## I. INTRODUCTION

In a computer of conventional organization, a central processor communicates with a large array of randomly accessible storage locations, each of which contains one word of a given number of bits. The assembly of these locations, the "random access memory," typically consists of one discrete element for each bit stored, which occupies a fixed location in space. This approach is comparatively costly. At present, the cycle time for such a memory of megabit size is of the order of one microsecond.

Since cost and size normally prohibit providing storage for more than a few million bits in this form, additional bulk memory is pro-

vided in which bits are stored in homogeneous media at lower cost and higher density. Since the bit locations in this bulk memory are basically defined by sequential scanning from a given addressable starting location, the information has to be stored or read out sequentially as a block. Therefore, once the desired block is addressed, a certain latency time passes until the information is available. This typically ranges from 10 to 100 milliseconds in mechanically scanned systems such as drums or disks and is even longer if heads have to be repositioned. If the information is stored on magnetic tape, this latency time may be several minutes.

The present trend is to have shorter processor cycle times and multiple access facilities in evolving computers; increasing emphasis is put on the ability to transfer blocks of information quickly between a bulk store and the random-access memory with which the processor interacts. In order to avoid a bottleneck in the throughput of information, transfer stores of lower capacity but shorter latency time are provided; these transfer stores can be loaded from a slower store without intervention of the central processor but can also transfer data on demand with minimum waiting time. Drum stores and random access memory blocks are often used for this application.

It is the purpose of this paper to point out that ultrasonic delay line stores have been developed to the point where bit rates of 100 MHz and higher have become feasible; therefore, stores with operational properties similar to those of a drum can be built which have maximum latency times of about 10 microseconds. Organized in parallel tracks, these stores can transfer many giga bit per second. In contrast to magnetic storage, these stores share with semiconductor stores the disadvantage of volatility with respect to power failure; but they have the advantage of high storage density and absence of moving parts.

These devices appear to be a strong contender for buffer stores of relatively short latency time. Since they are sequential stores with the information stored in a homogeneous medium, one may expect that the storage cost could be considerably lower than would be the case for a random access memory. This paper will show this to be the case. As a matter of fact, the higher the frequency of operation the more economical a delay line store becomes since its components become more and more compact. At 100 MHz bit rate, for example, stores with packing densities exceeding 6000 bits per cubic centimeter are readily possible.

In optimizing a store, the interrelation between delay line and

auxiliary circuitry needs to be considered. Details of delay line design analysis have been discussed elsewhere.[1] The present paper uses the delay line design analysis in an optimization with the auxiliary circuitry to find a combination which is optimized from functional and economical considerations.

The most repetitive elements in a delay line store are individual recirculating delay line loops. Accordingly, the optimization of individual loops will be considered first. This will be followed by giving detailed design considerations for the delay lines meeting such requirements. Finally, operational characteristics of a delay line store will be covered.

## II. GENERAL TRADE-OFF CONSIDERATIONS FOR A SINGLE DELAY LINE LOOP

A basic recirculating delay line loop typically has the configuration shown in Fig. 1. Binary coded data in the form of pulses appearing at terminal DI are inserted into the delay line through gates B and A when a "write" command pulse appears at terminal W. As the pulses appear at the other end of the delay line, they are amplified to make up for the insertion loss of the line and are detected in the amplifier-detector AD. In gate E the detected signals are retimed with respect to an external clock frequency inserted at terminal Cl. They can be monitored at the data output terminal $DO_1$ or gated

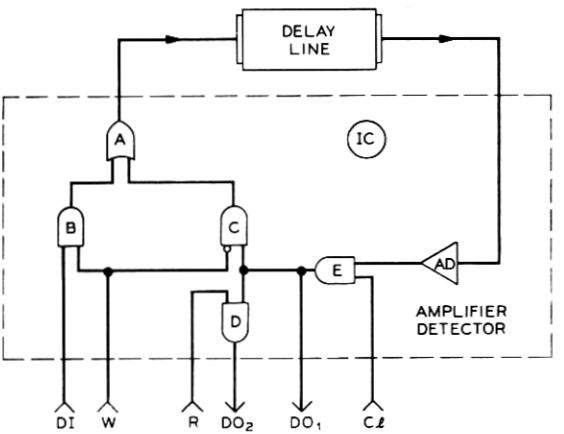



Fig. 1 — Basic recirculating storage loop. The terminals are as designated: DI, data insertion; W, write command; R, read command; $DO_1$, $DO_2$, data output; Cl, external clock frequency.

through D to the output terminal $DO_2$ by a "read" command applied at R. Gate C provides reconnection to the input of the delay line unless disabled by the write command at W while reading in new data. Storage loops of similar configuration have in the past been used with bit rates of a few MHz and storage capacities of up to about 20,000 bits in electronic desk calculators and the like.

A large store will have to contain a multiplicity of identical storage loops, and a limited number of control circuits, registers, and clock frequency supplies which are common to all loops. To minimize the over-all cost of the system, it is most important to minimize the cost and complexity of the components constituting the individual loops. In principle a given storage capacity may be obtained by using many relatively simple delay lines with a corresponding number of regeneration circuits or by using fewer but more complex delay lines usually requiring more complex circuitry. As long as the circuits have to be built from discrete components, it is more economical to use long and fairly complex delay lines so that maximum use could be made of the expensive circuitry.

As an example of this approach, a store has been built with a capacity of $1.3 \times 10^6$ bits, using 48 delay lines, storing 28,000 bits each at a bit rate of 40 MHz, which gives a resulting latency time of approximately 707 microseconds.[2] The materials available for such a large storage capacity per delay line exhibit a sizeable absorption loss and a temperature coefficient of delay around 80 ppm per centigrade degree. With such a large temperature coefficient some form of temperature stabilization is necessary. The high insertion loss of the delay lines—typically 50 dB pulse-to-pulse—requires amplifiers with carefully controlled linear gain at the output of each delay line to bring the signal back up to logic level. To retime unavoidable drift in temperature between the individual delay lines, the regeneration circuitry, in addition, has to provide the largest retiming margin possible.

These stringent requirements might be relaxed considerably by an alternative approach using delay lines which store only about 1000 bits each, so that the individual lines can be of a simple rectangular block configuration; the rectangular block configuration, in contrast to the polygons required in the above-mentioned example, can readily be batch fabricated in large numbers. Thus a cost saving appears possible in spite of the 28-fold increase in the number of delay lines over the example mentioned before. Also, the shorter delay line length permits the use of a delay medium, with higher absorption but with a lower temperature coefficient, so that temperature stabilization equip-

ment becomes unnecessary. Finally, with shorter individual delay lines a 28-fold reduction in the latency time is achieved which, if combined with lower cost for the devices, could make it more attractive for computer applications.

This approach will only be economical if the concomitant increase in the number of regeneration circuits can be obtained at minimal cost. This should be feasible if each circuit could be built as an individual integrated circuit of reasonable size. In order to make this practical, certain requirements are posed on the delay line performance. Since with an integrated circuit level detector pulses of 30 millivolts amplitude or more can easily be detected, and since an integrated circuit driver can deliver readily pulses of the order of 1 volt amplitude, the delay line pulse-to-pulse insertion loss should not exceed 30 dB. If kept to such levels, closely gain-controlled linear amplifiers can be avoided. Also, the transducers of the delay line should have an impedance falling into the range of 10 to 100 ohms so as to permit coupling the delay line to integrated circuitry without the use of transformers or tuning inductors.

## III. DESIGN CONSIDERATIONS FOR THE ULTRASONIC DELAY LINES

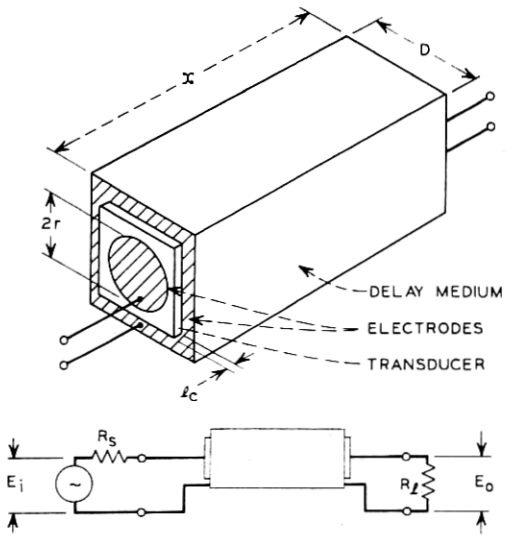
The simple delay line to be considered has the configuration shown in Fig. 2; two equal piezoelectric transducers of thickness $\ell_c$ and active diameter $2r$ are affixed to a delay medium in the shape of a bar of length $x$ and square cross-section having a width $D$. The delay medium is characterized by its sound velocity $c_d$, density $\rho_d$ and amplitude absorption index $\mu$ (absorption per wavelength). The transducer material is characterized by its sound velocity $c_c$, density $\rho_c$, permittivity $\epsilon$, and electromechanical coupling factor $k$. At the frequency $f_o$, for which the thickness of the transducer equals half a sound wave length, that is, for

$$f_o = c_c/2\ell_c \tag{1}$$

the electrical impedance $Z_i$ appearing at its electrical terminals is

$$Z_i = \frac{1}{\omega_o C_o}(-j + 4k^2/\pi z_t), \tag{2}$$

where $C_o = \pi r^2 \epsilon/\ell_c$ and $z = \rho_d c_d/\rho_c c_c$ is the acoustic impedance ratio of the delay medium with respect to the transducers. Without tuning networks, maximum power is transferred between a source of impedance $R_s$ and the delay line, and likewise between the line and a




DELAY LINE WITH PIEZOELECTRIC TRANSDUCERS

Fig. 2 — The basic delay line configuration. Two transducers of thickness $l_c$ and diameter $2r$ are attached to a delay medium of length $x$ and lateral dimension $D$. This delay line is connected between a source of resistance $R_s$ and load $R_\ell$ without tuning networks.

load resistance $R_\ell$, if

$$R_s = R_\ell \approx 1/\omega_o C_o ; \qquad \omega_o = 2\pi f_o . \tag{3}$$

provided that $4k^2/\pi z \ll 1$ which is fulfilled in all the cases of interest here.

As shown in detail in Ref. 1, with these electrical terminations one obtains a reasonably linear phase response and a pass band centered near $f_o$ which rolls off approximately like $\sin^4 (\pi f/f_o)$ on either side of $f_o$ if $z$ is selected to fulfill the condition

$$z = 1 - k^2. \tag{4}$$

With this pass band, a unipolar input pulse of rectangular envelope and a nominal width

$$T = 1/2f_o \tag{5}$$

gives rise to an output pulse having the shape shown in Fig. 3. The center lobe of this pulse is about 6.5 dB below the amplitude of the

input pulse. This reduction in pulse amplitude is due to side lobes being generated by the band limiting characteristic of the delay line.

Pulses can be inserted at a maximum bit rate equaling $f_o$ with adequate margin for binary detection. Thus one bit can be stored for each sound wave length $\lambda_d$ in the delay medium so that the storage capacity $N$ is given by

$$N = x/\lambda_d = c_d x/f_o \,. \tag{6}$$

The transducer insertion loss would be minimized if $k$ is chosen as large as possible. This is evident from (2) in that more of the input voltage is dropped across the resistive part of the input impedance. However, $k = 0.6$ is about the maximum available in transducer materials with reasonable technological properties so that a transducer insertion loss minimum of a few dB seems unavoidable. An attempt to trade off bandwidth for a reduction of loss would, as a rule, impair the detection margin of the output signal, and would probably increase the pulse amplitude insertion loss due to the pass-band characteristic above the value of 6.5 dB mentioned before.

Within these limitations one may now choose a transducer-delay medium combination by criteria such as a small temperature coefficient and adequate sound absorption. As shown in Ref. 1 one can combine the expressions for the length of the delay line $x$, the thickness of the

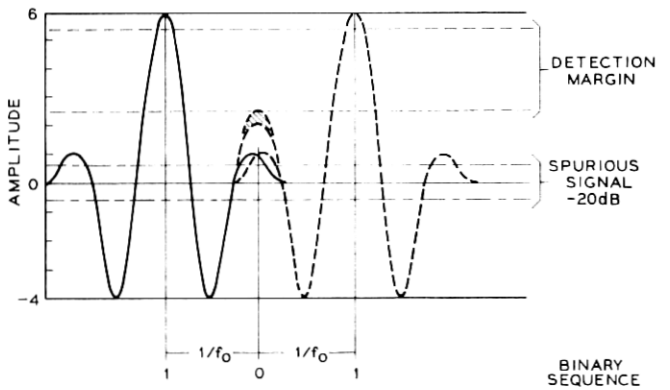



Fig. 3 — Output signal from a delay line when rectangular pulses of duration $1/2f_o$ are applied to its input. The worst case for detection is obtained when such pulses are entered at the rate $f_o/2$ representing a binary 1–0–1 sequence as shown; since the outermost sidelobes of the nearest neighbors will fill in the "zero" slot between "one" pulses, this creates intersymbol interference. A spurious signal at a —20 dB level further reduces the detection margin to the one shown.

transducer $\ell_e$, its capacitance $C_o$, and the length of its Fresnel zone $x_o$ which determines its directivity, namely

$$x = N\lambda; \qquad \ell_e = c_e/2f_o\,; \qquad C_o = \epsilon 4\pi r^2/\ell_e\,; \qquad x_o = r^2/\lambda, \tag{7}$$

to obtain a compatibility condition

$$N = m \cdot \omega_o C_o \cdot x/x_o \tag{8}$$

with a materials constant

$$m = c_e/4\pi^2 \epsilon c_d^2\,. \tag{9}$$

This condition implies that the beam spreading loss $L_b$ (which is approximately $x/x_o$ in dB if $x/x_o \leqq 10$) and the impedance levels of the delay lines are interrelated for a given material combination and storage capacity.

The total delay path loss $L_d$ is composed in part of the absorption in the delay medium $L_a$ and the beam spreading loss $L_b$ .

$$L_d = L_a + L_b \approx x/x_o + \mu N \tag{10}$$

with $\mu$ in dB per bit. In order to keep the total loss below 30 dB, the above loss should be restricted to about 20 dB, since in addition there are a few dB transducer loss and the 6.5 dB loss in pulse amplitude due to the band-pass characteristic of the delay line.

The absorption loss $L_a$ increases with increasing frequency and thus introduces by itself additional distortions. Since, the beam spreading loss $L_b$ decreases with increasing frequency, it is possible at least to first order, to compensate these two losses by choosing them approximately equal at the center of the pass band leading to the condition

$$x/x_o = \mu \cdot N. \tag{11}$$

By restricting the total loss to 20 dB, one is limited to $x/x_o \leqq 10$. To reduce the spurious signals, (primarily the triple travel signal due to multiple reflection between the transducers) to at least 20 dB below the main response, a minimum propagation loss $L_a$ of 10 dB is necessary. This requirement limits the design range to

$$5 \leqq x/x_o \leqq 10. \tag{12}$$

The lateral dimension $D$ of the delay medium is determined by the requirement that the directional response of the transducers suppresses glancing reflections from the side walls by at least 20 dB. This is assured if[1]

$$D/r = x/x_o . \tag{13}$$

The above relations contain all information necessary for a complete design of an optimized delay line.

It is interesting to note that (7), (9), and (11) do not contain the frequency explicitly. It enters only in implicit form through the absorption index $\mu$ which for most suitable materials increases less than linearly with frequency.

The other factor to consider is the potential cost of the delay line when compared to other methods of information storage. The technology required in fabricating delay lines is very similar to the semiconductor device technology and, as in that case, the variable giving a measure of the cost is the area that has to be precision finished, plated, and so on. For delay lines this is the area of the two end faces, each of which is given by

$$D^2 = N\lambda_d^2 x/x_o , \tag{14}$$

a relation obtained by combining (6), (7) and (13).

Thus, the area per bit to be finished, $2D^2/N$, is seen to decrease as $1/f_o^2$ . Moreover, (6) and (14) combined state that the delay line volume $xD^2$ decreases like $1/f_o^3$ . Thus at high frequencies the materials cost can be expected to be negligible compared to the finishing cost. These relations imply that, for economical reasons, the delay line should be operated at as high a frequency as possible, in spite of the reduction in storage capacity with increasing frequency which is imposed by the loss limit.

With present-day technology, delay lines have been made with storage capacities of approximately 1000 bits and pulse-to-pulse insertion loss in the vicinity of 30 dB with bit rates beyond 100 MHz.[3] There is no reason that this frequency could not be further increased. However, at present integrated circuitry with toggle rates much above 100 MHz has barely become available commercially so that at present 100 MHz is the highest frequency that can be considered from a practical point of view.

Once the frequency $f_o$ , the material constant $m$, and the impedance $1/\omega_o C_o$ have been chosen, (9) indicates that the storage capacity $N$ can only be varied in proportion to $x/x_o$ . This in combination with (14) implies that the finished area per bit $2D^2/N$ increases with the storage capacity $N$. The permissible range of $N$ is limited by the considerations leading to (12). As mentioned before, in the optimum case the beam spreading loss should equal the bulk loss, a condition which usually can

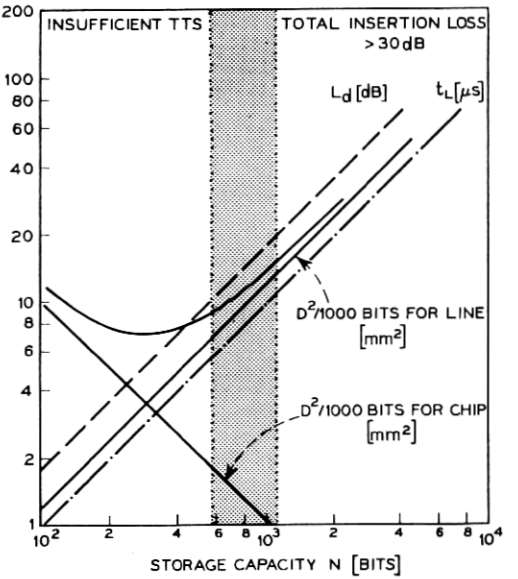



Fig. 4 — For a delay line consisting of sodium-potassium niobate transducers attached to a Bausch & Lomb T-40 glass delay medium and $f_o = 100$ MHz: the loss in the delay medium $L_d$, the latency time $t_L$, the combined endface area of the delay line, silicon chip area both per 1000 bits, and their sum. Outside the shaded region either the loss is too high or the triple travel suppression too low.

be met only approximately since the conditions imposed by (4) and (9) on the materials data will also have to be considered.

A useful compromise on all counts consists of a delay line using as a delay medium, a glass with nearly zero temperature coefficient of delay, such as Bausch & Lomb's T40 glass, and using ceramic sodium potassium niobate transducers. The materials constants for this system are as follows:[1,4] T40 glass: $c_d = 2.58$ millimeter per microsecond, $z = 0.51$, $\mu = 9 \times 10^{-3} \times (f/f_0)^{0.3}$ dB at $f_o = 100$ MHz; sodium potassium niobate ceramic: $c_c = 3.68$ millimeter per microsecond, $\epsilon \approx 500\epsilon_o$, $k = 0.6$. This combination fulfills (4) closely enough to be usable at bit rates up to $f_o$ with adequate detection margins. Figure 4 shows the delay medium loss $L_d$ of (10), the maximum latency time $t_L$, and the processed area per 1000 bit, $2D^2$ of (14) as a function of the storage capacity $N$ for $f_o = 100$ MHz. Condition (12) in this case limits the value of $N$ between 560 and 1100 bits as is also indicated in Fig. 4.

For $N = 1000$ the delay medium length is $x = 25.8$ millimeters and the lateral dimension $D = 2.45$ millimeters, so that the material

cost can be considered insignificant compared with the processing cost of the end faces. These, however, tend to be proportional to the end face area $2D^2$, but will certainly be less than the cost of an equal area of integrated circuit chips, in view of the less complex procedures involved in fabricating the delay lines. The regeneration circuit comprises about 30 transistors and should, at the present state of the art, require about 1 square millimeters of silicon.[5] One circuit of this area is required for each delay line loop. The processed area per bit decreases, therefore, inversely with the number of bits stored in a single delay line as indicated in Fig. 4. As a result of this the sum of the processed area of the chip and the delay line itself has a minimum near $N = 300$ bits. If the processing costs per unit area were equal for the delay line and the chip, this minimum would correspond to the cost minimum. If, as appears likely, the cost per unit area is lower for the delay line, this minimum shifts to a higher $N$, close to the values of $N$ between 560 and 1100 bit, permitted by the spurious signal supression and insertion loss limit. With a transducer impedance of 28.5 ohms the bulk loss in the delay medium at 100 MHz can be made equal to the beam spreading loss. This impedance will pose no difficulty with standard integrated circuitry.

It appears, therefore, that some presently available materials have close to optimum properties for the design of delay line storage loops operating at a bit rate of 100 MHz and storing 1024 bits with a resulting latency time of 10.24 microseconds. If such delay lines were produced by batch techniques, their cost should be comparable to those of a few square millimeters of silicon integrated circuits. The storage density in these devices is approximately 6000 bits per cubic centimeter of volume. Individual storage loops with delay lines storing 1024 bits have been built and operated at bit rates of 100 MHz.[5]

## IV. ORGANIZATION OF A DELAY LINE STORE

Delay lines of the design described above are highly compact and could be built in modules of, for example, 18 delay lines built in a single glass plate of approximate dimensions 2 inches by 1 inch by 0.1 inch. The transducers would be mounted on the 2 inch by 0.1 inch faces while the 2 inch by 1 inch faces would be available as the substrate for interconnections, and the integrated circuit chips performing the recirculation, clock, and control functions. If one uses two of the 18 tracks for parity check and timing functions, then each module would store 16,384 bits. Such a module might constitute a

repetitive element of any larger store so that the latency time for any randomly accessible block of information need not exceed 10.24 microseconds at a bit rate of $f_o = 100$ MHz, regardless of the store size.

It thus seems sufficient to discuss the organization of an individual module. The simplest organization would consist of providing random access by a 4-bit track selector to each track which stores a block of data words in a word and bit sequential organization. The start of each track would be delineated either by a 10-bit cyclic counter, counting off the clock frequency, or by reading signals from one or two additional delay lines serving as timing tracks. By adding an address register and a circuit, comparing its content with the counter, individual words in each track can be addressed individually. This type of organization, shown schematically in Fig. 5 using as elements the storage loops of Fig. 1, is natural for bit-serial processing with its economy of equipment so that it may well find application as main memory in small computers, where a cycle time of 10 microseconds is quite adequate.

Faster data transfer at the cost of more equipment is obtained in the word serial, bit parallel organization shown in Fig. 6. There the bits of any one word are contained in parallel tracks, so that a complete word is accessed by comparing its address with the counter reading. Data input and output have to be provided by parallel registers; transfer of words to the outside world can occur at the bit rate $f_b$. The store, whatever its size, can be written or read completely

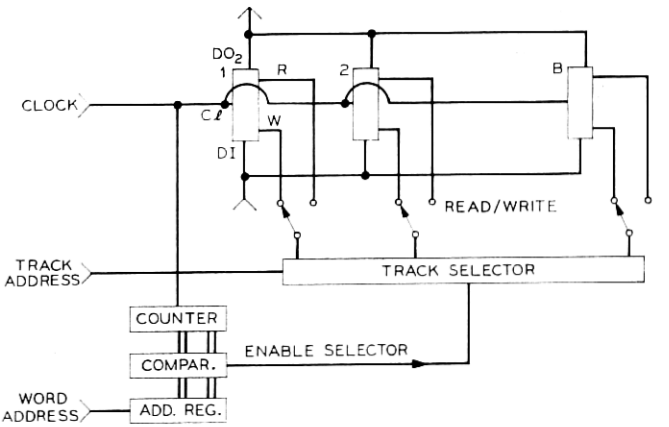



Fig. 5 — Bit-serial, word-serial organization of B storage loops as in Fig. 1.

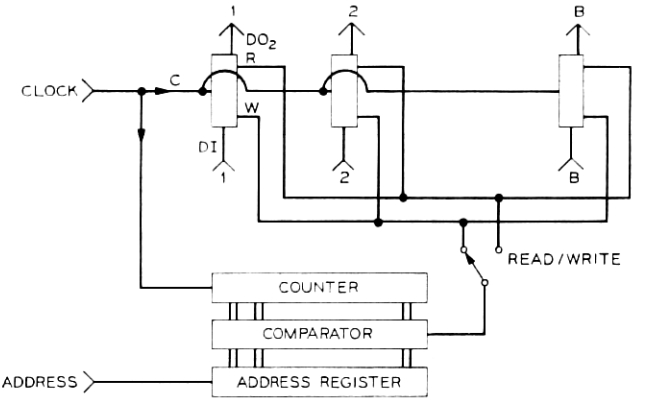



Fig. 6 — Bit-parallel, word-serial organization of B storage loops.

within 10.24 microseconds. In this form the store would cooperate best with a random access memory of about 10 nanoseconds cycle time without excessive buffer pile-up. As will be discussed in the Section V, slower, nonsequential operating modes can provide a match with memories of any cycle time between 10 nanoseconds and 10 microseconds.

Finally, like any sequential memory the delay line store can be organized associatively as shown in Fig. 7. All words are compared with a word preselected in the content register during the 10.24 microseconds it takes for all words to pass by the test location. If the comparison extends only over a part of the bit forming a word, these bits can serve as a pointer address for sorting sequences, and so on. In this version the store acts as an associative memory with a cycle time of 10.24 microseconds.

## V. TIMING PROBLEMS

In the operation of a delay line store, the timing requires careful attention since in contrast to a digital shift register the delay line has a characteristic recirculation time. This time is dominated by the delay time $t_d$ of the individual delay lines while the circuitry will contribute only a minor additional delay. A delay line designed for a characteristic frequency $f_o$ can be operated at a bit frequency $f_b$ up to the frequency $f_o$. If the frequency is chosen below $f_o$, it is important that the pulse width is nevertheless maintained at $1/2f_o$. Deviation to longer or shorter values causes the insertion loss to increase, since less

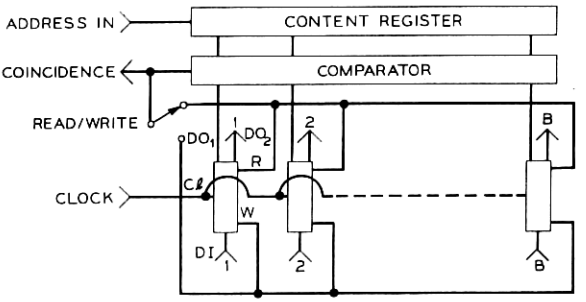



Fig. 7 — Bit-parallel, word-serial organization of B storage loops with associative addressing. A coincidence signal is produced when the content register agrees with a stored word, as the latter passes through the comparator.

of the spectral energy of the input pulse falls into the pass band of the delay line. Storage capacity $N$ and bit rate $f_b$ are interrelated by

$$N = f_b \cdot t_d \,, \tag{15}$$

so that within certain limits storage capacity can be traded off in order to synchronize the store with an external clock frequency determining the bit rate. However, usually it will be more advantageous to operate the store asynchronously with respect to the outside world. One then avoids the problems in distributing frequencies of 100 MHz over an extended system with a predetermined phase. Moreover, one can then slave the store clock to a delay line used as a timing track.[2]

As in any asynchronous organization, buffer registers must be provided which temporarily store information entered at one transfer rate and withdrawn at a lower one. Information accumulates in the buffer at a rate equal to the difference between the two rates until the complete block is transferred. This determines the buffer capacity required. It is therefore of advantage to know how a delay line store can be accessed at rates nearly equal to those of the equipment it serves, so that the buffer capacity can be kept low.

If bits are loaded every $t_\ell$ second into a delay line loop of capacity $N$, bit $(N + 1)$ will coincide in time with the first bit loaded if

$$Nt_\ell = pt_d \tag{16}$$

where $p \geqq 1$ may be any positive integer. However, if $p$ has common factors with $N$, bits earlier than the $(N + 1)$-st one will already coincide in time, so that such values of $p$ should be avoided. For $N = 1024$, $p$ may thus assume all odd numbers.

Combining (16) and (15) one obtains

$$f_\ell = 1/t_\ell = f_b/p \tag{17}$$

as the permissible loading rates. These generally cause the bits to be stored internally in a scrambled sequence, with the exception of the choices

$$p = qN + 1 \qquad q = 1, 2, 3, \cdots, \tag{18}$$

which cause storage in the original sequence, and

$$p = qN - 1 \qquad q = 1, 2, 3, \cdots, \tag{19}$$

which cause storage in time-inverted sequence. Equation (18) is the basis of the well known delay line time compression (DELTIC) signal processing systems described in the literature in which digital data are written into storage at a slow rate $f_\ell$ but are read at the fast bit rate $f_b = (qN + 1)f_\ell$.[6] Also, all pairs of loading rates $f_{\ell 1}$ and $f_{\ell 2}$ given by

$$f_{\ell 1}/f_{\ell 2} = p/(qN + p) \tag{20}$$

cause storage in the same, although internally scrambled, sequence so that the bit addresses can be set by sequential counting rather than address comparison.

Series-parallel conversion can be utilized to keep the difference of transfer rates between stores at a minimum. For instance, certain core memories provide access to, say, 72 bits every cycle with a cycle time of 1 microsecond. Parallel to serial conversion would make use of a bit rate of 72 MHz quite feasible, which would increase even further if various checking bits were added to each 72-bit word.

## VI. CONCLUSIONS

Sequential storage in recirculating loops, consisting of ultrasonic delay lines in combination with integrated regeneration circuitry of medium scale complexity, has reached a state of the art where bit rates can be obtained which are, at present, unattainable with large scale integrated circuit registers. At bit rates around 100 MHz and beyond such storage appears economically competitive with LSI implementations operating at much lower speeds. Such bit rates have already been demonstrated.

With modules storing blocks of 1000 bits at 100 MHz bit rate, larger stores can be built with latency times of about 10 microseconds,

for possible use as main memory in small computers or as fast transfer stores shuttling information between a slow external bulk memory and a fast random access memory in large computers.

In spite of the inherently fixed recirculation time of such a store, it should be adaptable to various processor and bulk store speeds without having to provide more than a few words of buffer storage by a judicious combination of measures such as clock frequency variation, DELTIC modes, and series-parallel conversion. This opens the prospect of using only one or a few basic types of storage modules with a standardized delay time so that maximum advantage could be taken of the savings inherent in mass fabrication.

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