B.S.T.J. BRIEF

Electrochemically Controlled Thinning of Silicon

By H. A. WAGGENER

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A method for precision thinning silicon integrated circuit slices has been developed whereby either n or p type regions may be selectively removed from material of opposite conductivity. The existence of a simple and economical means to attain precise thickness control permits more complete advantage to be taken of many silicon IC structures. For example, precise thickness control, together with anisotropic[1] etching of isolation/separation slots, is expected to permit economical fabrication of high component density, air-isolated monolithic[2] integrated circuits.

This method differs from previous electrochemical techniques[3] in that unwanted silicon is removed chemically, while the regions to be retained are passivated electrochemically. Accordingly, etchants are used for which silicon to be retained is passive when biased above some critical voltage, V_{pass}, while regions to be removed are at a potential below V_{pass}.

Hot aqueous alkaline solutions form a useful class of etchants for this application, for orientations other than (111). These etchants are characterized by a relatively sharp active/passive transition ($V_{cell} = V_{pass} \approx 0.5$ volt) and by a large ratio of silicon etch rates between the active and passive states. Ratios of greater than 200 : 1 are readily obtained. The ratio of active etch rate/passive etch rate is very important, because this quantity in part determines the thickness uncertainty.

Application of the technique to the formation of thin, uniformly thick n type silicon slices is illustrated in Fig. 1. If $V_{cell} > V_{pass}$, then $V_n = V_{cell} > V_{pass}$ and the n region will be retained. If V_{cell} is restricted to voltages such that the leakage of the reverse biased junction is

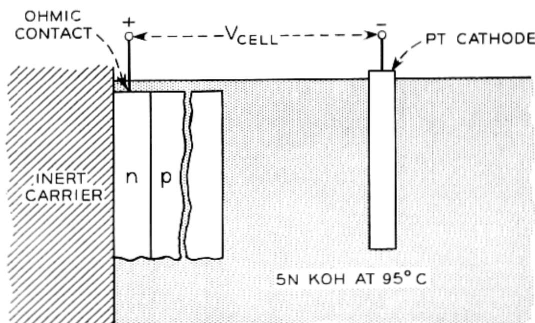

Fig. 1 — Schematic illustration of the thinning technique as used to form n type slices with accurately controlled thickness. An n region is formed by epitaxy or by diffusion. The starting material is high-resistivity p material. When the cell is biased as described in the text, the p region can be removed while the n region is retained. Neither the exact composition nor temperature of the etching solution is critical.

sufficiently small, then $V_p < V_{pass}$, and the p region will be removed. It is assumed that the contacts are arranged so that the lateral ohmic drop in the n type silicon is small enough to be negligible.

For the cell arrangement shown, V_{pass} is about 0.5 volt for either n or p material. Thus thin p-type slices can be formed by reversing the location of the n and p layers as shown in Fig. 2. The maximum allowable cell voltage is reduced because the controlling junction is now forward biased.

Structures of this type have been made where the n layer was formed by diffusion into a background approximately 2.5×10^{-2} cm thick.

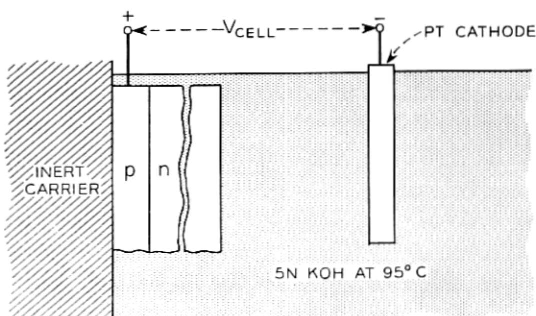

Fig. 2 — Schematic illustration of the thinning technique as used to form p type slices with accurately controlled thickness. Cell polarity is unchanged.

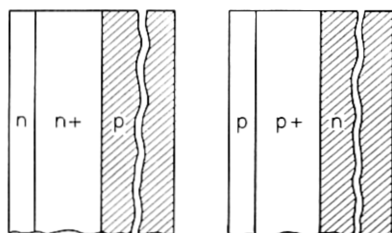

Fig. 3 — Multilayered structures which can be fabricated using the thinning technique. These structures are particularly suitable for making npn and pnp integrated circuits.

After thinning, the difference between the thickness of the remaining n layer and the depth of the diffusion was about 3×10^{-5} cm.

Multilayered structures can also be fabricated as illustrated in Fig. 3. These structures are particularly suitable for fabrication of npn and pnp air-isolated or dielectric-isolated integrated circuits. The thickness control is determined by the combined thickness of the diffused and epitaxial layers, and is expected to be easily controllable to within 10 percent.

Experimental beam leaded, air-isolated monolithic integrated circuits have been made on n/n+/p starting material and have been thinned by the technique described. A total of approximately 2.5×10^{-2} cm of p material was removed in one step, without prior mechanical operations.

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