The authors wish to thank D. Kahng, C. N. Berglund and E. I. Gordon for stimulating discussions during the course of this work.

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Experimental Verification of the Charge Coupled Device Concept

By G. F. AMELIO, M. F. TOMPSETT and G. E. SMITH

(Manuscript received February 5, 1970)

Structures have been fabricated consisting of closely spaced MOS capacitors on an n-type silicon substrate. By forming a depletion region under one of the electrodes, minority carriers (holes) may be stored in the resulting potential well. This charge may then be transferred to an adjacent electrode by proper manipulation of electrode potentials. The assumption that this transfer will take place in reasonable times with a small fractional loss of charge is the basis of the charge coupled devices described in the preceding paper.[1] *To test this assumption, devices were fabricated and measurements made. Charge transfer efficiencies greater than 98 percent for transfer times less than 100 nsec were observed.*

The basic principles of the charge coupled device, as already described,[1] are very simple indeed, but it is not clear whether the properties of an MIS system are adequate to give viable devices. The purpose

of this paper is to describe experiments which have been carried out using the silicon-silicon dioxide system to investigate these properties and their effect on device performance in terms of charge transfer speed and efficiency.

The requirements on the silicon-silicon dioxide interface and on the oxide itself are very demanding. One essential feature is a long storage time which is the time required for a pulsed MOS element to reach the steady state condition. The storage time is a function of the flat-band voltage, the pulse voltage and the number of generation-recombination centers at the interface and in the neighboring bulk. Ignoring bulk states and using the capacitance of a 1200 Å thick oxide, it is readily calculated that for zero threshold voltage, a pulse voltage of 20 V and the surface recombination current[2-4] of 3.7×10^{-8} A cm^{-2} appropriate to a fast state density of $2 \times 10^{+10}$ states/cm^2, the storage time is about 16 seconds.

The operational requirement of a charge coupled device is that it must be able to transfer charge with only minimal loss at high speeds. The object of our experiments has been to evaluate this. Estimates of the rate of charge transfer have been made[1] but estimates of transfer efficiency are much more speculative on account of ambiguity in the density of surface states in the energy region near the band edge for a particular oxide.

Several types of oxide on nominal 10 Ω-cm n-type (100) and (111) orientated silicon have been tried. Steam grown oxides with a fast surface state density as low as $N_{ST} = 2 \times 10^{10}$ states/cm^2 gave oxide storage times less than 100 msecs for a 20 V pulse. This unexpected result was attributed to generation-recombination centers caused by impurities which had diffused into the bulk. A silane deposited oxide had storage times greater than one second but was not stable with respect to migration of positive charge. The oxide which has given the best results so far is a dry oxide 1200 Å thick grown in oxygen at 1100°C for one hour and annealed in a nitrogen atmosphere for one hour at 400°C. The flatband potential for this oxide is typically −5 V.

The initial device configuration used in the experiments described below is a linear array of Cr-Au squares 0.1 × 0.1 mm and separated by 3 μm gaps. These squares were produced by conventional photolithography on the oxidized silicon slice. The slice was diced, each die mounted on a 10 pin header and each square gold-wire bonded to a pin.

The device as described above was designed principally for ease of fabrication and is in no way optimized in either material processing

or geometry. Indeed, there are reasons for supposing that p-type material might be preferable since the minority carrier mobility will be greater than in n-type silicon.

Evaluation of charge coupled device performance is based on the measurement of several parameters including percentage of charge transferred (efficiency), the limiting speed of transfer and the storage time. For times greater than about one-half second, the latter property is easily measured by applying a negative step voltage and observing the change of capacitance with time using a capacitance bridge and an xy recorder. Storage times less than one-half second are normally associated with high interface state density oxides or a large number of bulk generation-recombination centers and are of no interest in the present application.

Observation of charge transfer including the determination of efficiency and speed requires a different approach. The experimental configuration chosen in the measurements is shown in Fig. (1). Capacitor P_0 in this figure is used to supply a source of holes to the other units (P_1, P_2, $\cdots$) by surface avalanching. The avalanching pulse, is adjustable 0-200 volts with a full width half maximum of 60 nanoseconds. For the 10 Ω-cm substrate material and 1200 Å oxide thickness used, avalanching occurs in the vicinity of -165 volts. Unit pulse generators are attached to pads P_1, P_2, and P_3. In a many

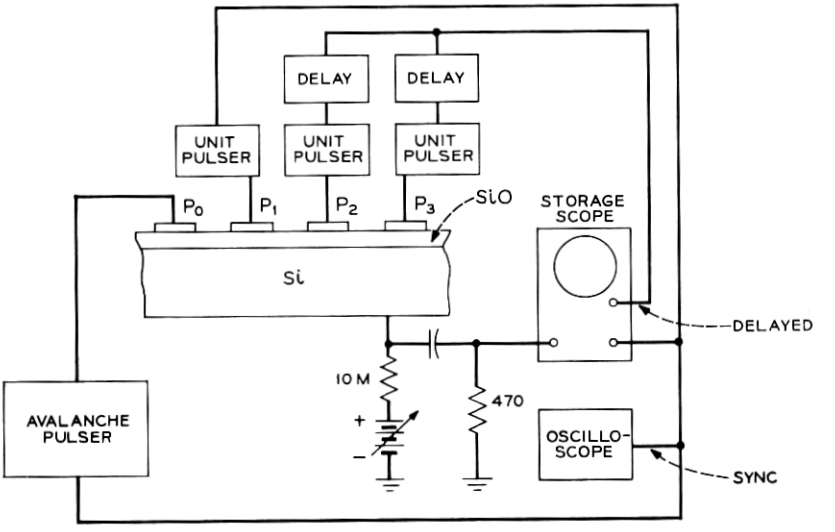

Fig. 1—Schematic of experimental configuration used to evaluate charge transfer.

transfer application, P_1 is attached to each P_{1+3n}, P_2 attached to each P_{2+3n} and P_3 attached to each P_{3+3n}.[1] The substrate is connected to a load resistor and a positive potential for the purpose of biasing the MOS elements beyond threshold voltage. The output signal is capacitively coupled to a relatively low impedance so that response times on the order of 100 nanoseconds are achieved. As each MOS capacitor is pulsed by the supply generators, a charging and discharging spike is observed at the oscilloscope which, for the circuit shown, is proportional to the current flow. The pulsing sequence for capacitors P_0, P_1 and P_2 is illustrated in Fig. (2) for the conditions when the P_1 and P_2 pulse voltages (V_{P_1} and V_{P_2}) do and do not overlap in time. Note the avalanche pulse occurs shortly after P_1 is turned on. Of interest is the charge transfer from P_1 to P_2, all others being ignored for the sake of simplicity. Below each pulse sequence is shown the expected (idealized) oscilloscope display with a positive going signal taken in the downward direction.

For the nonoverlap condition, there are two essentially separate events. Notice that the turn-off pulse of P_1 is larger than the turn-on pulse when avalanching of P_0 occurs during the on-time of P_1. This is easily understood. Each current pulse is given by the relation

$$i(t) = \frac{dQ}{dt} = \frac{dQ}{dV}\frac{dV}{dt} = c(V)\frac{dV}{dt} \tag{1}$$

where $c(V)$ is the differential capacitance of the device, V is the voltage across the capacitor and Q is the charge flowing from ground. Assuming the turn-on and turn-off characteristics of each voltage pulser are made the same, the magnitude of the current is determined by the differential capacitance $c(V)$. At turn-on, the capacitance which must be charged to an additional V_p volts from the bias voltage V_b is represented by the oxide and depletion capacitance in series. When P_0 is avalanched, the holes generated diffuse to P_1 and invert the surface there. The depletion region under P_1 diminishes and the associated capacitance increases. Now at turn-off when the voltage across the device is returned to V_b, the relaxation pulse is of greater magnitude than the turn-on pulse by an amount related to the change in differential capacitance. When no holes are stored, as in the case of P_2, the turn-on and turn-off pulses are of equal amplitude.

Consider now the overlap case. There, instead of the turn-off pulse of P_1 resulting in a large hole injection into the bulk, the holes are transmitted to the adjacent MOS capacitor. The turn-off pulse amplitude of P_1 should therefore decrease. On the other hand, the turn-off

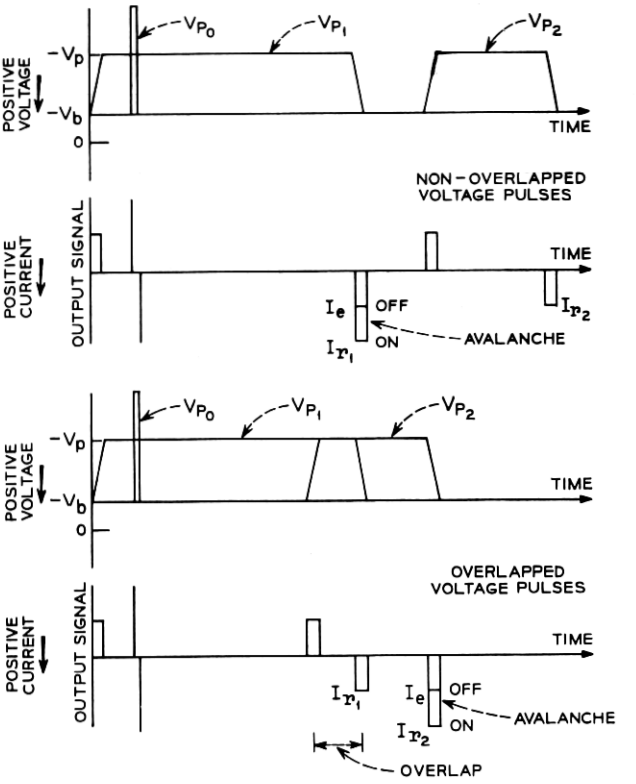

Fig. 2—The pulsing sequence for capacitors P_0, P_1 and P_2. Below each pulse sequence is shown the expected (idealized) oscilloscope display with positive going signal taken in the downward direction.

pulse of P_2 is expected to increase as a result of the charge transmitted to it from P_1.

The efficiency of a single charge transfer can be defined as

$$\eta = \frac{\text{charge arriving at } P_2}{\text{charge originally stored in } P_1} \tag{2}$$

where the charge is given by the integral from V_b to $V_b + V_p$ of the difference in differential capacitance during turn-off and turn-on. This charge can be approximately related to the current pulses discussed above if equal voltage pulses and similar MOS capacitance properties for the two pads are assumed. Thus, for bias voltages significantly beyond threshold where the $c(V)$ curve is relatively flat, the efficiency

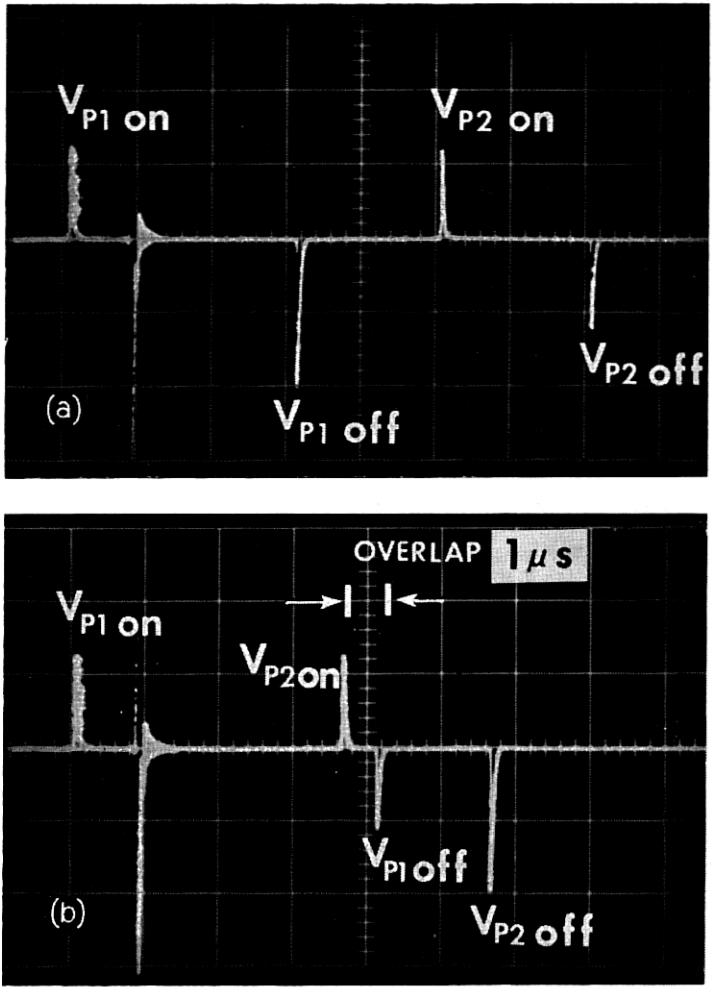

Fig. 3—Oscilloscope traces showing the (a) nonoverlap and (b) overlap charging pulses for an actual device with $V_b = -5$V and $V_p = -20$V. The time base is 2 μs/cm.

can be reasonably approximated in terms of the peak amplitudes of the relaxation current pulses as

$$\eta \approx \frac{I_{r2} - I_e}{I_{r1} - I_e} \tag{3}$$

where I_{r2} is the turn-off pulse when P_2 contains charge, I_{r1} is the turn-

off pulse when P_1 contains charge and I_e is the turn-off pulse when either is empty.

In Figs. 3(a) and (b), the nonoverlap and overlap charging pulses for an actual device with $V_b = -5$ V and $V_p = -20$ V are given. The threshold voltage for this unit is -1.5 volts. The evidence of charge transport is unmistakable. In Fig. 4 a similar, although somewhat more complicated, photograph shows the superposition of many events (using a storage oscilloscope) in which the pulse duration of V_{P_1} is increased until it overlaps V_{P_2} by one microsecond. Following this, V_{P2} is additionally delayed until there is once again no overlap. The rounding seen in the turn-off pulse of P_2 after it goes out of overlap is attributable to holes remaining in the vicinity of P_1 and P_2 after P_1 is turned off. The high transfer speed of the device is seen by the rapidity with which the relaxation pulse P_1 falls off as the pulses overlap. Although not evident in Fig. 2, the charge transfer efficiency is not a function of time for overlap times greater than 100 nanoseconds (the rise time of the pulses used in the experiment). Using enlarged photographs similar to that shown in Fig. 3 and equation (3), the measured efficiency in $\eta = 94 \pm 6$ percent. Measurements made in this manner have been performed on devices with wet, dry and deposited oxides on ⟨111⟩ and ⟨100⟩ oriented surfaces. To date, the best results have

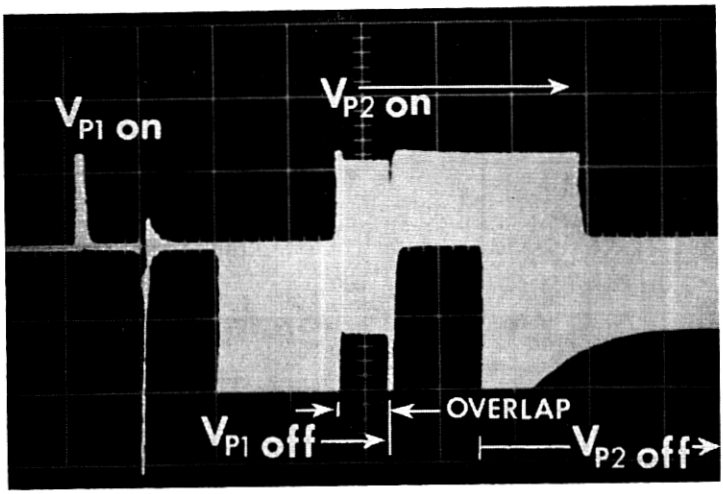

Fig. 4—Oscilloscope traces showing the superposition of many events (using a storage oscilloscope) in which the pulse duration of V_{P_1} is increased from 4 μs until it overlaps V_{P_2} by one microsecond. The turn-on of V_{P_2} is then additionally delayed until there is once again no overlap. The same device is used as for Fig. 3.

been obtained for a 1200 Å dry oxide on the ⟨100⟩ surface of silicon.

More recently, multiple transfer measurements have been conducted for which efficiencies greater than 90 percent have been demonstrated after five transfers, again with pulse widths of 3 μs and overlap times of 1 μs. This implies an η of over 98 percent. For these measurements, current integration has been employed for more accurate determination of the charge transferred.

The authors wish to acknowledge the help of R. A. Furnanage in fabricating the devices and the assistance of P. M. Ryan and E. J. Zimany, Jr. in making the measurements.

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