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Zero Loss Transfer Across Gaps in a CCD

By R. H. KRAMBECK

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When a charge-coupled device is made with a single layer of metallization, adjacent electrodes must be placed several micrometers apart. As a result there may be some difficulty in moving the charge from one electrode to another. In this paper it will be shown that, for any substrate material, there is a wide range of interface charge for which complete transfer can be achieved regardless of electrode separation. It will further be shown that for a p-substrate with a doping of less than $10^{15}/cm^3$, the natural charge found in a good quality thermally grown layer of SiO_2 is always of the appropriate sign and magnitude to ensure complete transfer. Therefore, for simple fabrication of a CCD with one layer of metal, this substrate material is the appropriate choice.

I. INTRODUCTION

In a charge-coupled device,[1] charge is transferred from a potential well under one metallization to a deeper potential well under an adjacent metal. Since the metals cannot touch one another, this process involves passing through an interelectrode gap. If the potential pattern is such that there is a potential barrier or a potential well in the space at the end of transfer, then complete charge transfer is impossible. If two layers of metallization are used (which are separated by an insulating layer of 1000 Å), no barrier or well can form. This requires a more complex technology, so it would be desirable to make a CCD with one layer of metallization.

In this paper the effect of interface charge and substrate doping on potential well and barrier formation will be analyzed. It will be shown that, for any given substrate doping and drive voltages, there is an interface charge for which neither well nor barrier forms. The calculations in this paper will assume an infinitely long gap which will ensure that no yield losses will result from small variations in gap width or surface charge magnitude.

II. ANALYSIS

The objective of this analysis will be to find the conditions which will permit complete charge transfer. It is therefore necessary to examine the state of the CCD at the end of the transfer of only the largest ONE that can be accommodated. That is, if the largest ONE is transferred without loss, then any piece of information could be transferred with no loss of charge. Our objective then is to find free-carrier density vs position at the end of transfer. If there is neither a peak nor a minimum of free-charge density in the space, then the space is not interfering with transfer.

To find free-carrier density on the surface, we must find total surface charge density and subtract fixed charge density. The first part of the problem is to find charge density vs position at the end of transfer. This is simplified by the fact that at the end of transfer of the largest possible ONE, the semiconductor surface is an equipotential (the movement of free charge will not stop until an equipotential is achieved).

The geometry of the interelectrode space is shown in Fig. 1. Just below the semiconductor surface the field is uniform because the surface is an equipotential. The displacement field is given by

$$D_s = \sqrt{2N\epsilon_s Vq} \tag{1}$$

where N is the semiconductor doping, ϵ_s is the semiconductor dielectric constant, V is the surface potential, and q is the electronic charge. Just above the surface the field is

$$D_{ox} = D_s + qn - Q_{ss} \tag{2}$$

where n is the free-electron density (cm^{-2}) and Q_{ss} is the density of charged states either in the oxide or at the semiconductor surface (p-type substrate has been assumed with electrons as free carriers). From equations (1) and (2)

$$qn = D_{ox} - \sqrt{2N\epsilon_s Vq} + Q_{ss} . \tag{3}$$

Since Q_{ss} and V are constants, differences in electron density from one point to another are directly related to changes in D_{ox} by

$$\Delta n = \frac{\Delta D_{ox}}{q}. \tag{4}$$

This means that if D_{ox} varies monotonically from the region under one electrode to the region under the adjacent electrode, then electron density also varies monotonically and no barrier or well exists. In Fig. 2

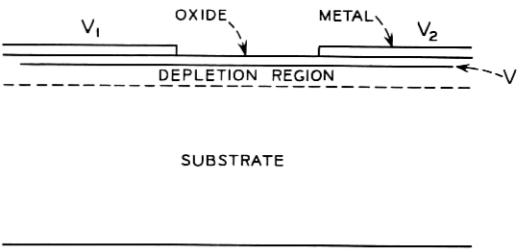

Fig. 1—Cross section of a charge-coupled device showing the interelectrode gap

the three possible variations of D_{ox} with position are shown. First, in Fig. 2a $V < V_1$ and $V < V_2$ where V_1 and V_2 are the voltages applied to the two metals. In this case, D_{ox} is positive under both metals but drops to zero in between (for sufficiently large separation). This means electron density is lower in the space between the electrodes than it is under either of them, and as a result a barrier must be holding back charge. Second, in Fig. 2b $V > V_1$ and $V > V_2$. Here D_{ox} is negative under each electrode but is again zero in the gap. This means electron density is higher in the space than under either electrode, so a potential

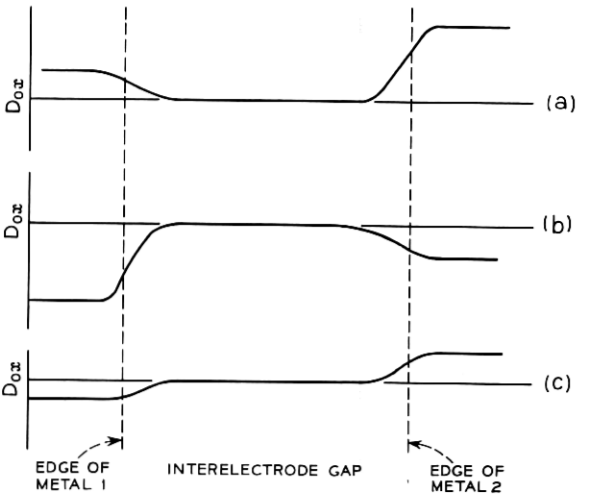

Fig. 2—The variation of oxide field at the surface of the semiconductor, D_{ox}, vs position along the surface when the interelectrode gaps are arbitrarily large. The curves are for three combinations of applied voltages, V_1 and V_2, and surface potential, V: (a) $V < V_1$, $V < V_2$, (b) $V > V_1$, $V > V_2$, (c) $V \geqq V_1$, $V \leqq V_2$.

well must be present. Finally, in Fig. 2c $V \geqq V_1$ and $V \leqq V_2$. Here $D_{ox} \leqq 0$ under metal 1, $D_{ox} \geqq 0$ under metal 2, and $D_{ox} = 0$ somewhere in between. This is the situation desired. It is therefore necessary to find only what value of Q_{ss} will cause the surface potential at the end of transfer to be in between the two metal voltages.

Let us assume metal 1 is giving its charge to metal 2. Then at the end of transfer free-electron density under metal 1 is zero. Therefore from equation (3)

$$D_{ox_1} = \sqrt{2N\epsilon_s V q} - Q_{ss} . \tag{5}$$

Also the difference between V_1 and V is given by

$$V_1 - V = \frac{D_{ox_1}}{\epsilon_{ox}} \delta \tag{6}$$

where δ is the oxide thickness. Since we need $V \geqq V_1$, $D_{ox_1} < 0$. Therefore

$$Q_{ss} \geqq \sqrt{2N\epsilon_s V q}. \tag{7}$$

The minimum value of Q_{ss} is obtained when $V = V_1 (D_{ox_1} = 0)$ which gives:

$$Q_{ss} \geqq \sqrt{2N\epsilon_s V_1 q}. \tag{8}$$

As an example, with $N = 10^{14}/\text{cm}^3$, $\epsilon_s = 10^{-12}$ F/cm, and $V_1 = 1$ volt, $Q_{ss}/q \geqq 3.5 \times 10^{10}/\text{cm}^2$.

This specifies the minimum for N_{ss}. Any lesser value would give rise to a barrier. To prevent formation of a well, we have $V \leqq V_2$. Under electrode 2

$$D_{ox_2} = D_s - Q_{ss} + qn$$

$$D_{ox_2} \geqq 0.$$

Therefore

$$Q_{ss} \leqq \sqrt{2N\epsilon_s V q} + qn. \tag{9}$$

If the largest allowable Q_{ss} is being used, $D_{ox_2} = 0$ and $V = V_2$. Also, from equation (4)

$$D_{ox_2} - D_{ox_1} = qn.$$

Therefore

$$V_2 - V_1 = \frac{qn}{\epsilon_{ox}} \delta$$

where ϵ_{ox} is the oxide dielectric constant. The maximum value of Q_{ss} is therefore

$$Q_{ss} \leqq \sqrt{2N\epsilon_s V_2 q} + \frac{\epsilon_{ox}}{\delta}(V_2 - V_1). \tag{10}$$

Using $V_2 = 10$ volts and the same numbers as above for the other parameters gives

$$\frac{Q_{ss}}{q} \leqq 2.0 \times 10^{12}/\text{cm}^2.$$

Equations (8) and (10) specify the allowable range for Q_{ss} which is the result needed.

III. DISCUSSION

The previous section showed that a specific range of Q_{ss} is appropriate for any given substrate doping and pair of driving voltages. In this section the attainability of this range will be discussed. The range is shown graphically in Fig. 3 for the driving voltages $V_1 = 1$ volt and $V_2 = 10$ volts.

It turns out that for a thermally grown oxide on silicon Q_{ss}/q in

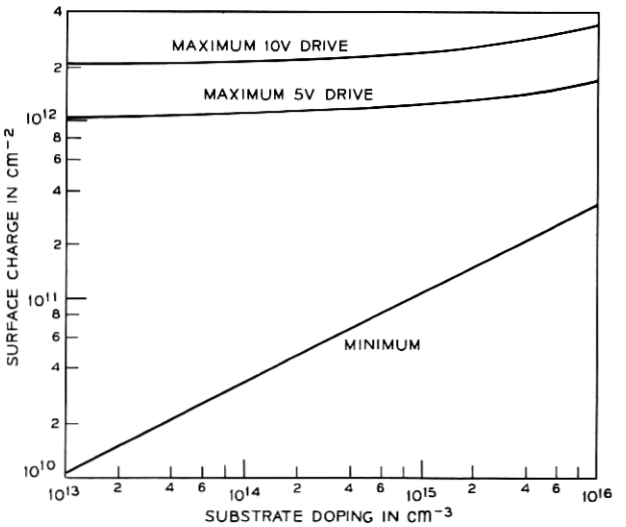

Fig. 3—Minimum and maximum surface charge vs substrate doping for $V_1 = 1$ volt and for $V_2 = 5$ volts and 10 volts.

the oxide is normally in the range 10^{11} to $6 \times 10^{11}/cm^2$. Therefore for a p-type substrate any doping under $10^{15}/cm^3$ will ensure complete transfer. For other substrates and oxides some doping must be introduced. Probably the easiest way would be a uniform ion implant chosen so the total charge including oxide charge lies in the allowed range.

An important point about Fig. 3 is the width of the allowed range. For drive voltages of 1 volt and 10 volts the allowed range of charge extends over at least one order of magnitude for any substrate doping below $10^{16}/cm^3$ which ensures that a proper amount of charge can be obtained even with substantial slice-to-slice variations in charge. It also means that aging effects are unlikely to change the amount of charge to a value outside of the desired range.

In the analysis it was assumed there is sufficient time for complete transfer to occur. An appropriate question is how much longer transfer takes if a gap separates the metals. R. J. Strain and N. L. Schryer[2] have shown that in a CCD the rate of carrier flow is inversely proportional to the sum of the capacitances between surface and substrate and between surface and metal. Since this sum is much higher when the surface is covered by a metal, the low capacitance gap will not significantly increase transfer time as long as the gap is shorter than the metal.

IV. CONCLUSIONS

From the above discussion it can be seen that the simplest way to obtain complete transfer in a charge-coupled device, with a thermal SiO_2 layer used as insulator, is to use as substrate material p-type silicon with a doping of less than $10^{15}/cm^3$.

It can be further concluded that for other substrate materials and for other insulators an appropriate charge range always exists, and that this charge range can be obtained by ion implantation over the entire surface of the slice without use of a photographic masking step. Selective implantation of the region between the metals and the regions under the edges of the metals could also eliminate potential barriers and wells. However, because of fringing fields, this can be achieved only by extension of the tail of the charge distribution for a specific distance under each metal, but this would be a more difficult way to achieve complete transfer.

Summarizing, it should be clear that potential barriers and wells in the spaces between electrodes in charge-coupled devices can be eliminated easily. Therefore the possibility of incomplete charge transfer

should not be cited as a reason for spacing electrodes abnormally closely or using two layers of metallization. For most applications future CCD's should be made on p-type substrates with less than $10^{15}/cm^3$ doping since the proper charge is automatically obtained.

REFERENCES

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