The *Picturephone*® System:

A Digital Transmission System for TD-2 Radio

By C. W. BRODERICK

(Manuscript received September 2, 1970)

A terminal for transmitting digital signals over TD-2 microwave radio relay routes has been designed and evaluated in a recent field trial. This paper details some of the radio system characteristics which influenced the design, describes the major features of the terminal, and reports the trial results. The terminal will be used in the toll network to provide intercity Picturephone® *trunks and data circuits.*

I. INTRODUCTION

The TD-2 Radio Relay System is the major trunk carrier system in the Bell transcontinental network, interconnecting every major metropolitan center in the United States.[1] Therefore, as digital transmission grows, it is natural to consider how TD-2 might be used to distribute these signals.

A terminal that applies the digital bit stream to TD-2 has been designed to transmit at a rate of 20.2 megabits per second (Mb/s) using a four-level, 10.1-megabaud pulse format to modulate standard TD-2 terminal equipment. The input is arranged to accept up to three 6.312-Mb/s bipolar streams from such sources as *Picturephone* coders and data sets. Design features include the use of pulse stuffing for multiplex synchronization, dedicated pulses for timing recovery, a transversal filter for optimizing the received eye pattern and the use of self-synchronizing scramblers for testing.[2,3] The signal is regenerated at baseband about every 400 miles to limit the accumulation of unequalizable pulse distortion.

A number of digital terminals have been constructed and tested in conjunction with the New York-Pittsburgh *Picturephone* product trial. Test results on this 450-mile trial route, using one regenerator station, have indicated that performance of better than one error in 10^{10} bits,

in the absence of significant fading, has been realized. The error rate increases to about one error in 10^6 bits when the received signal on any radio hop fades to the point where transmission is switched automatically to a protection radio frequency channel.

II. TD-2 MICROWAVE SYSTEM

The TD-2 microwave radio system has been described previously.[1] It operates in the 3,700- to 4,200-MHz band, with the 20-MHz-wide channels spaced 20 MHz apart. The system employs frequency modulation of an IF carrier centered at 70 MHz, prior to conversion to the microwave spectrum. The baseband frequency response is constant to within 0.5 dB to about 5 MHz for a 300-mile system.

The reliability of the radio channel is maintained to a high degree through the availability of automatic switching to standby protection channels in the event of a signal-to-noise ratio (S/N) below minimum requirements.[4]

III. DESIGN CONSIDERATIONS

It was desired to use the existing TD-2 microwave equipment including the 3A FM terminals and to make the digitally modulated microwave channel compatible with regular analog message and television signals on adjacent microwave channels.[5,6] This makes it possible to use the existing TD-2 nationwide network in providing *Picturephone* toll trunking and digital data circuits and it imposes the following signal constraints:

(*i*) The baseband signal must not interfere with the radio protection switching system which uses a 7-MHz pilot tone and a 9-MHz noise slot. This is accomplished by using a baseband transmitter filter whose cutoff frequency is below 9 MHz.

(*ii*) The IF signal spectrum must not interfere with the noise slot frequency or the top message frequency of the adjacent channel. This limits the peak frequency deviation.

(*iii*) The limiting S/N is determined by the protection switching system initiator setting used for analog message service.

(*iv*) The digital signal must be regenerated to limit the unequalizable baseband distortion encountered in RF transmission.

The coded *Picturephone* signal has a 6.312-Mb/s rate.[7] This rate was chosen to match a standard line rate which is evolving as part of the Bell System's digital transmission network and which will be used by the T2 digital line. The digital transmission system capacity therefore was chosen in increments of this 6.312-Mb/s rate.

The initial use of the terminals, in support of the *Picturephone* product trial between New York and Pittsburgh required an error rate of $< 10^{-6}$. A plot of the required S/N for fixed error rates and of the available S/N due to the above restrictions, both as a function of the system bit rate, is shown in Fig. 1. The available S/N is calculated at the fading threshold of the radio protection switching system. To meet the signal constraints above, the peak frequency deviation and therefore the available S/N must decrease as the system bit rate increases.

The digital signal eye pattern distortion increases with increasing system bit rate due to the sharper rolloff in the baseband filtering. Therefore, the required S/N for constant error rate increases as the system bit rate increases. From the intersection of the required S/N curve and the available S/N curve, it can be seen that the system capacity is about 21 megabits for an error probability of 10^{-6} at the fading threshold of the radio protection switching system. The digital terminal input therefore was set at three 6.312-Mb/s lines. The system parameters are specified in Table I.

The controlling signal constraint at the intersection in Fig. 1 is IF signal spectral overlap onto the noise slot frequency of the adjacent

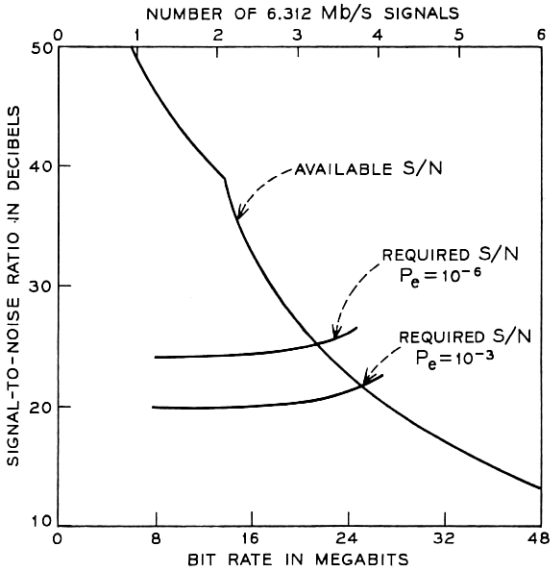

Fig. 1—Available S/N and required S/N for constant probability of error, P_e, versus system bit rate.

channel. This is a form of near-end adjacent channel interference involving a receiver at a center frequency 20 MHz away from a transmitter. The interference path includes the side-to-side coupling of adjacent horn reflector antennas and the loss in waveguide runs from transmitter to antenna and antenna to receiver. The coupling loss is typically about 100 dB which results in a reduction of fade margin equal to 0.8 dB. In some circumstances siting difficulties lead to coupling losses that are several dB smaller, and therefore a further reduction in fade margin.[8]

IV. TERMINALS

4.1 *Transmitting Terminal*

A simplified block diagram of the transmitting terminal is shown in Fig. 2 with typical waveforms. The digital transmitter accepts three 6.312-Mb/s pulse streams in parallel and multiplexes them into a single serial pulse stream.

TABLE I—DIGITAL TRANSMISSION SYSTEM PARAMETERS

1. Transmitting Digital Terminal	
Input	Three 6.312-Mb/s lines in bipolar format
Output	10.1-megabaud, 4-level signal band limited to 7.5 MHz at −15.7 dBm on 124 Ω balanced pair
2. Receiving Digital Terminal	
Input	10.1-megabaud, 4-level signal at +0.4 dBm on 124 Ω balanced pair
Peak baseband signal-to-rms noise ratio (worst case) at detector input	27 dB (includes effect of receiver filter)
Output	Three 6.312 Mb/s lines in bipolar format Error rate: 10^{-10} nominal; 10^{-6} at protection switching point
3. TD-2 Microwave Radio	
RMS carrier-to-noise ratio at protection switching point (37.5-dB fade)	96 dB/Hz
99% power bandwidth for digital modulation	12 MHz

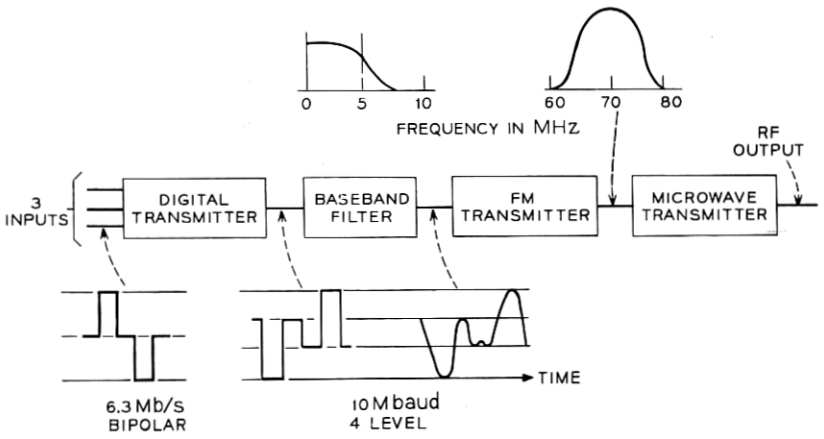

Fig. 2—Digital transmission over microwave radio transmitting terminal.

The output of the digital transmitter is a 10.1-megabaud, four-level signal which is made up of information pulses, framing pulses, and synchronization pulses. This composite signal is then shaped by the baseband filter into the signal which will deviate the FM transmitter. The output spectrum of the FM transmitter, centered around 70 MHz, is shown in a simplified form.

4.2 *Receiving Terminals*

At the receiving terminal, the digital signal is recovered from the FM terminal receiver at baseband, filtered, equalized and demultiplexed into three 6.312-Mb/s signals. A simplified block diagram of the receiving terminal, together with its appropriate waveforms, is shown in Fig. 3. The functional operation of the receiver is essentially the inverse of the transmitter.

4.3 *Filters*

The overall shaping and filtering of the four-level, 10.1-megabaud baseband signal is obtained by splitting the baseband filtering and locating a portion of it in the transmitting terminal to band limit the signal and the remainder in the receiving terminal to limit noise. The combined transmission characteristic of the baseband filters produces a pulse with a raised cosine spectrum which has a high tolerance to interference.[9]

The transmitter baseband filter characteristic is given by

$$H_t(f) = \begin{cases} \dfrac{\pi f/f_B}{\sin(\pi f/f_B)}, & |f| \leqq f_{B/2} - f_x ; \\ \dfrac{\pi f/f_B}{\sin(\pi f/f_B)} \cos\left(\dfrac{\pi}{4}\dfrac{f - (f_{B/2} - f_x)}{f_x}\right), & \\ & f_{B/2} - f_x < |f| < f_{B/2} + f_x . \end{cases}$$

The receiver baseband filter characteristic is given by

$$H_r(f) = \begin{cases} 1, & |f| \leqq f_{B/2} - f_x ; \\ \cos\left[\dfrac{\pi}{4}\dfrac{f - (f_{B/2} - f_x)}{f_x}\right], & f_{B/2} - f_x < |f| < f_{B/2} + f_x ; \end{cases}$$

where $f_B = 10.1$ MHz.

For the 50 percent rolloff filter used in these terminals, f_x equals $f_{B/4}$. The $x/\sin x$ term in the transmitter filter characteristic is a correction for the spectrum of the square-wave input.

V. BASIC FUNCTIONS—TRANSMITTER

The digital transmitter block of Fig. 2 is shown in expanded block diagram form in Fig. 4. The functions of bit stream synchronization, multiplexing, and modulation shown in Fig. 4 are described below.

To time multiplex the three independent 6.312-Mb/s inputs, each input must be synchronized to the same clock frequency. This is accomplished by the method of pulse stuffing. Each input is written into a separate eight-cell elastic store under the control of an input

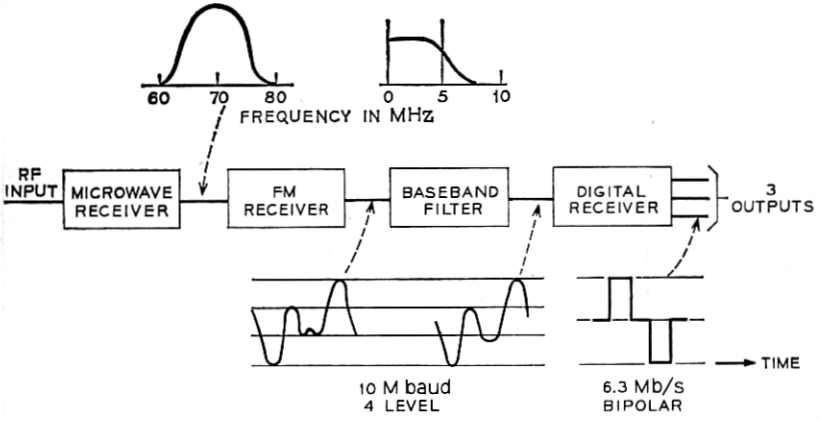

Fig. 3—Digital transmission over microwave radio receiving terminal.

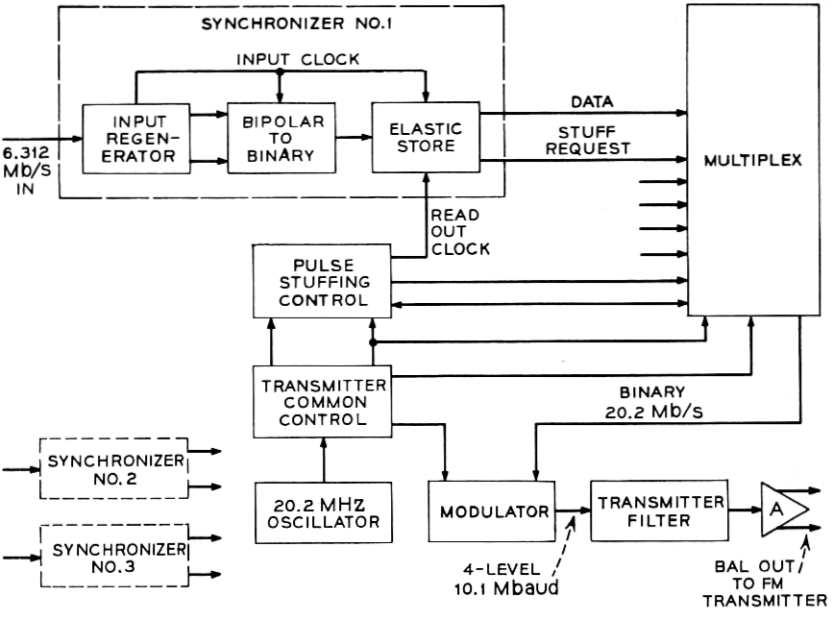

Fig. 4—Block diagram of digital transmitter.

clock derived from the average frequency of the respective input signal. The input frequency is 6.312 MHz ±30 ppm which is a tolerance of about ±190 Hz. The reading function for each synchronizer is performed by one of three read clocks generated in the pulse stuffing control. Each of these read clocks over a long period of time has exactly the same number of clock pulses as there are information pulses written into the storage cells of the associated elastic store. Furthermore, each read clock has been blanked appropriately to allow the insertion of the framing and synchronizing pulses. Sixteen bits out of every 256-bit frame are allocated for these purposes. The nominal pulse stuffing rate is 500 stuff pulses per second. This rate is variable from a minimum of zero to a maximum rate of one stuff every 12 frames. The actual synchronization is performed by the pulse stuffing control through the monitoring of stuff requests generated by nearly empty elastic stores. These stuff requests reach the pulse stuffing control via the multiplex. All of the periodic waveforms required to perform the functions of synchronizing, multiplexing and modulating are generated in the transmitter common control. The basic system clock frequency is 20.2 MHz ± 30 ppm and is generated by the 20.2-MHz crystal oscillator.

The multiplex accepts the three properly synchronized information

pulse streams with their associated stuff request pulses. It also receives the required periodic waveforms from the pulse stuffing control and the transmitter common control and time multiplexes them together with the information pulses and stuff pulses into a 20.2-Mb/s binary stream. Included in this stream are the necessary control signals to allow the receiver to remove the added stuff pulses.

The final digital operation in the chain is to modulate the 20.2-Mb/s binary signal to a four-level, 10.1-megabaud signal. This takes place in two steps. The 20.2-Mb/s binary signal is first converted into two parallel 10.1-Mb/s binary streams which are then converted into a single, four-level 10.1-megabaud signal. A simplified schematic diagram of the modulator is shown in Fig. 5. The serial bit pairs, B_1B_2, are mapped to pairs of parallel bits, D_1/D_2, through the functions;

$$D_1 = \overline{B_1}$$

and

$$D_2 = \overline{B_1 \oplus B_2}.$$

The parallel bit pairs then control the emitter-coupled transistors which route the proper amount of current from the current generators into the load resistor to produce the four-level output signal.

The digital signal format at the binary output of the multiplex and the corresponding four-level signal out of the modulator are illustrated in Fig. 6. The contents of one frame are shown, including dedicated

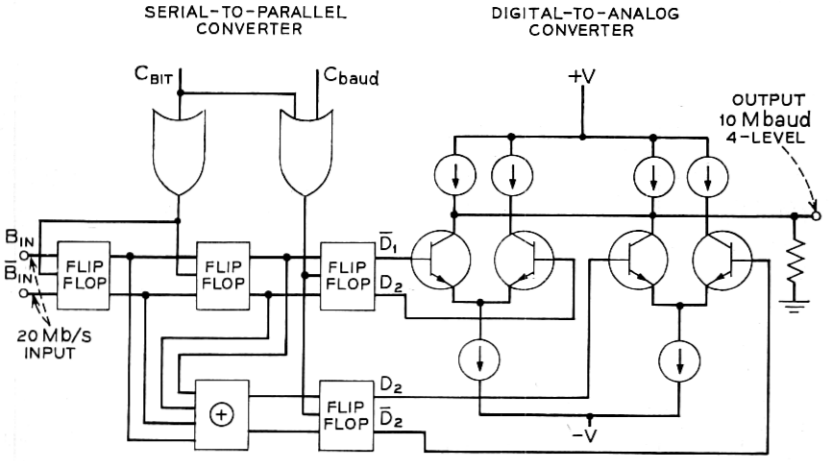

Fig. 5—Modulator. C_{BAUD} = 10.1-MHz baud clock; C_{BIT} = 20.2-MHz bit clock; B_{IN}, $\overline{B_{IN}}$ = 20.2-Mb/s binary bit stream and its complement; $D_1 = \overline{B_1}$; $D_2 = \overline{B_1 \oplus B_2}$.

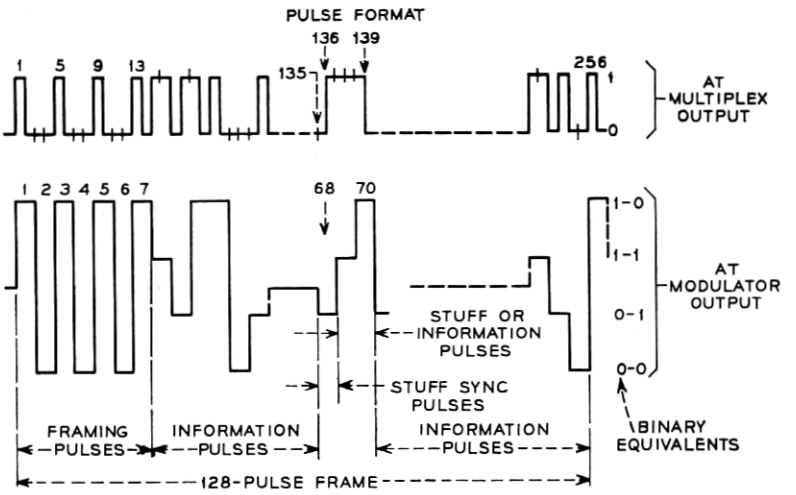

Fig. 6—Pulse format of digital signal.

framing pulses, stuff sync pulses, stuff pulses, and information pulses. The stuff sync pulses of 12 successive frames make up a triply redundant word which indicates to the receiver when and where stuff pulses are inserted for each of the three information channels. From the modulator, the signal passes through the transmitting filter, which restricts the baseband frequencies and provides the desired pulse shaping, and then to an FM transmitter through an unbalanced-to-balanced amplifier.

VI. BASIC FUNCTIONS—RECEIVER

The digital receiver block of Fig. 3 is shown in expanded block diagram form in Fig. 7. At the digital receiver, the four-level, 10.1-megabaud signal, from the FM receiver, is converted to an unbalanced signal and then passes first through the receiver baseband filter and into the transversal filter. The baseband filter, together with the filter in the transmitting terminal, provides optimum shaping of the baseband response characteristic. The transversal filter simplified schematic is shown in Fig. 8. The input signal passes through a 12-section tapped delay line. The gain of each tap, except for the center tap, is manually adjustable so that the output signal $S_0(t)$ is given by

$$S_0(t) = \sum_{n=-6}^{+6} K_n S_i(t - n\tau),$$

where

$$K_0 = 1, \qquad -1 < K_n < +1$$

and

$$S_i(t - n\tau)$$

is the input signal at the nth tap.

Adjustment of the tap gains, K_n, compensates for the nonfading distortion encountered by the signal in transmission over the radio channels. The equalized output signal drives the digital section of the receiver.

The operation of the receiver is, in general, the inverse of the transmitter. The receiver converts the 10.1-megabaud, four-level input signal into three 6.312-Mb/s pulse streams by first demodulating the signal into a 20.2-Mb/s binary data stream, and then separating and adjusting the timing of, or desynchronizing, the three individual output signals.

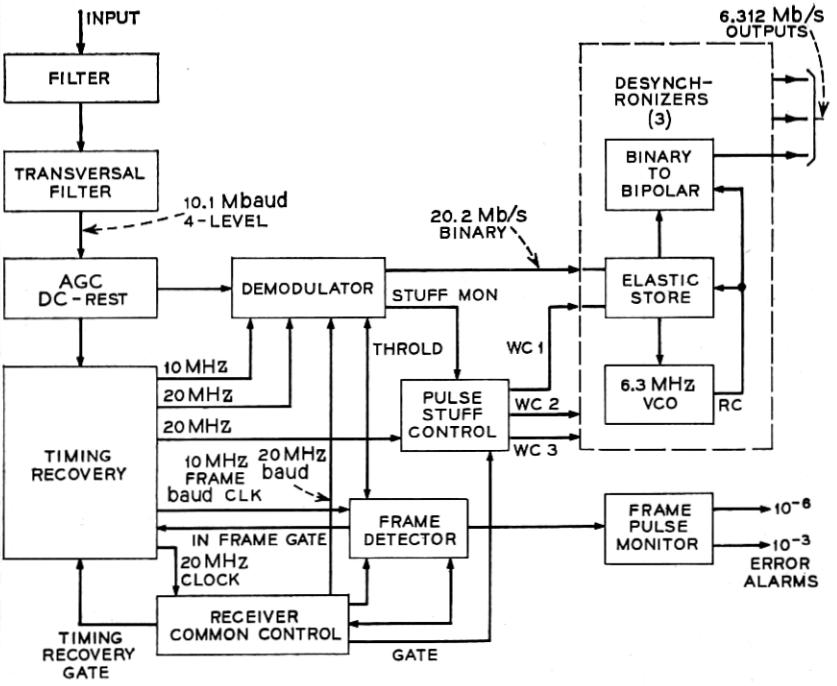

Fig. 7—Block diagram of receiving terminal.

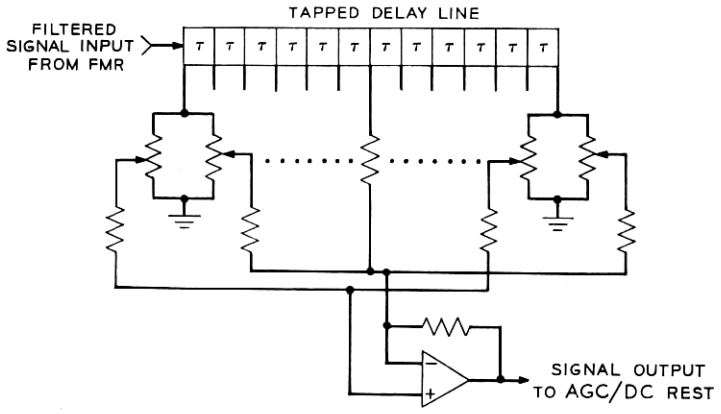

Fig. 8—Transversal filter.

Demodulation is accomplished through the AGC/DC restoration, timing recovery, demodulator, frame detector, and receiver common control circuitry. The AGC/DC restoration circuit reduces the effect of input signal level variations and assures that the signal is at the proper dc level.

The timing recovery circuit produces 10.1-MHz sinewave outputs which are synchronous with the 10.1-megabaud input signal. Timing is initially recovered using the complete signal. However, when the receiver is in frame, only selected zero crossings of the dedicated framing pulses (Fig. 6) are used. This results in a more stable recovered clock because the dedicated pulses always have the same pattern. This clock is converted to 20.2 MHz by the frequency doubler circuitry.

The demodulator converts the 10.1-megabaud, four-level signal into a 20.2-Mb/s binary data stream. A simplified schematic is shown in Fig. 9. The 10.1-MHz sample clock is converted into a narrow strobe pulse of about 15-ns width that operates the sample-and-hold flip-flops at the output of the threshold detectors. There are three threshold detectors, each of which consists of two stages of emitter-coupled transistor pairs. High-speed silicon transistors ($f_t = 4$ GHz) are used in the last stage to minimize errors caused by timing inaccuracies. The outputs of the sample-and-hold flip-flops are converted logically in the parallel-to-serial converter to a 20.2-Mb/s binary data stream.

The relative phase of the 10.1-MHz sample clock and the 10.1-megabaud signal is adjustable to permit sampling to occur at the minimum distortion point of the eye pattern.

The frame detector is used to establish proper framing of the receiver common control. When the framing pulses are in the demodulator sample-and-hold circuit, a fixed pattern appears at the frame detector. To establish initial framing when the system is put into service, or to reinitiate framing when an outage occurs, the dedicated pulse pat-

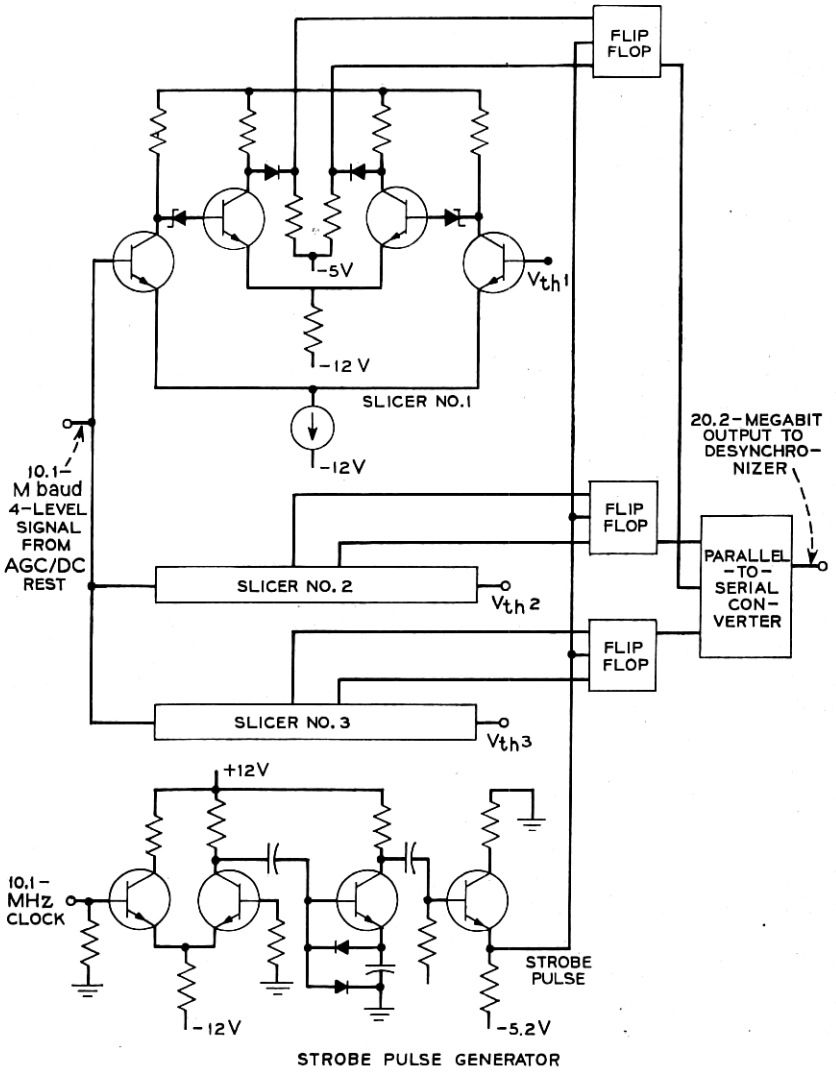

Fig. 9—Demodulator.

tern must be detected correctly in two successive signal frames. The master counter in the receiver common control will then be automatically set to its proper phase with respect to the input signal stream. In the absence of errors in the incoming four-level pulse stream, the in-frame condition is achieved in no more than 25 microseconds. Once the in-frame condition is established, the time of occurrence of the dedicated pulse pattern as seen by the frame detector is compared with the time of occurrence of a frame sync pulse from the receiver common control. If they are in phase, a signal appears on the in-frame gate lead to the timing recovery. If they are not in phase during four successive signal frames, a frame reset pulse resets the common control and continues to reset until the correct framing pattern is noted again in two successive frames. In addition, when an error occurs in the framing pulses, a signal is sent to the framing pulse error monitor.

The framing pulse error monitor keeps track of the rate of errors of the framing pulses. When the framing pulse error rate is equivalent to a data error rate less than one in 10^6 bits, performance is considered acceptable. When the equivalent error rate becomes greater than one in 10^6 bits, an alarm is activated as described in Section 10.2.

Circuits used for separating and adjusting the timing of the three channels are the pulse stuffing control, receiver common control, and three sets of desynchronizers each set consisting of an elastic store, voltage-controlled oscillator, and binary-to-bipolar converter.

The purpose of the pulse stuffing control in the receiver is to provide the three write clock (WC) signals, each clock having pulses corresponding to a different information channel. In addition, the pulse stuffing control determines when a channel has an added stuff pulse to be ignored. Information as to whether a stuff has occurred is contained in two dedicated "Sync" bits of the 20.2-Mb/s binary data stream. When the presence of a stuff pulse is indicated by the sync bits, the appropriate pulse of the output clock is blanked in the time slot where the stuff pulse has been inserted by the digital transmitter. Only one channel will have been stuffed in any single frame.

Data is written into the elastic store of desynchronizer channel No. 1 by WC1. Thus only those bits belonging to channel No. 1 get into this elastic store. The data is then read from the elastic store by the smoothed read clock generated by the voltage-controlled oscillator. This is a crystal controlled oscillator, the frequency of which is locked to the average frequency of WC1. The smoothed binary data stream out of the elastic store is finally converted back to bipolar format.

VII. ERROR-RATE MEASUREMENT

To measure the system error performance, a pseudo-random word generator called a scrambler is used with a complementary descrambler. As shown in Fig. 10, the scrambler consists of a 15-stage shift register with feedback connections that cause it to generate a word of 32,767 bits in length when the input is "0." The descrambler has the same basic configuration and performs the inverse function, i.e., when the descrambler input is the 32,767-bit word, the output of the descrambler is "0." Errors in the 32,767-bit word will cause a pulse to appear at the descrambler output.

The frequency of operation of the scrambler-descrambler combination is determined by the clock frequency that is supplied to it. To test the overall system error rate, a 20.2-MHz clock with appropriate blanking is used and the scrambler output drives the transmitter multiplex. The receiver demodulator drives the descrambler and the output of the descrambler is monitored to measure the error rate. To test a single 6.312-Mb/s channel, an appropriately blanked 6.312-

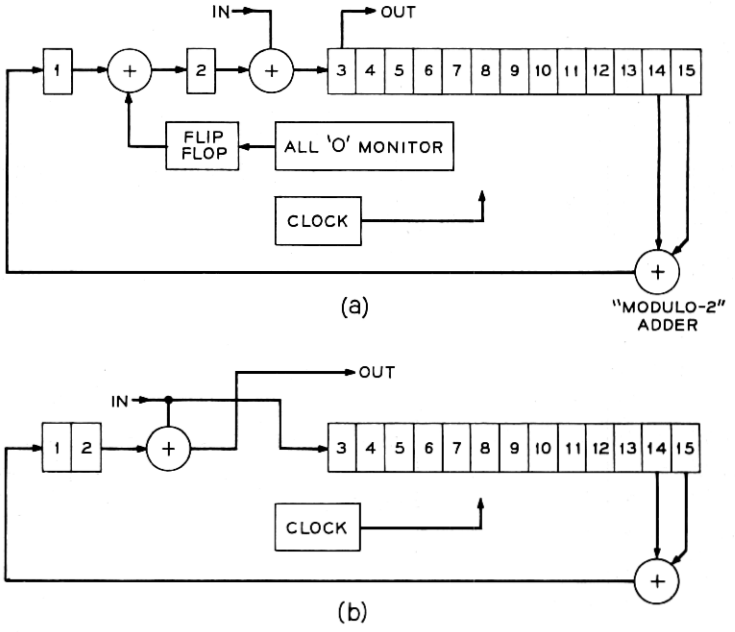

Fig. 10—Word generator: (a) scrambler, and (b) descrambler.

MHz clock is used and the scrambler replaces the elastic store in the channel being tested. The receiver elastic store in the same channel is replaced by the descrambler and the output of the descrambler is monitored to measure the single-channel error rate. Since this last test does not check the pulse-stuffing operation in the channel being tested, a third test mode, which uses a scrambler driven by an asynchronous 6.312-MHz clock, is used. The output of this test source drives a single 6.312-Mb/s channel, replacing the normal input. The descrambler in the receiver is used in the binary-to-bipolar converter position. In this way the pulse stuffing operation of a single 6.312-Mb/s channel can be tested.

VIII. DISCUSSION OF FIELD TEST RESULTS

A *Picturephone* product trial was conducted between New York and Pittsburgh from February 1969 to August 1969. As part of the product trial, digital terminals were installed at New York and at Pittsburgh with a digital regenerator at Alma, New York. The digital terminals were in operation from July 1968 to August 1969 and during the first 6 months of this period, before the product trial started, error-rate measurements were made. Data accumulated during the test period have indicated that the performance has exceeded the original design objectives. Error performance over several periods of two to three days has indicated an error rate of 10^{-9} to 10^{-11}. Over 99.5 percent of the 10-second samples recorded were error free during a total of over 200 hours of measuring time. Among the small percentage of samples containing errors, about 90 percent contained five or less binary digit errors, which corresponds to an error rate of less than 10^{-7} errors per bit.

A plot of actual error-rate results on the radio circuit between Pittsburgh and New York, obtained by injecting equivalent noise at baseband in the digital receiver to simulate a fading condition, is shown in Fig. 11. The center curve is the overall circuit with the regenerator in at Alma and equalized for overall optimum performance. The other curve shows the performance when the regenerator at Alma was bypassed. No change in equalization was made between the two conditions.

A photograph of an actual eye pattern is shown in Fig. 12. The eye closure due to intersymbol interference is clearly evident.

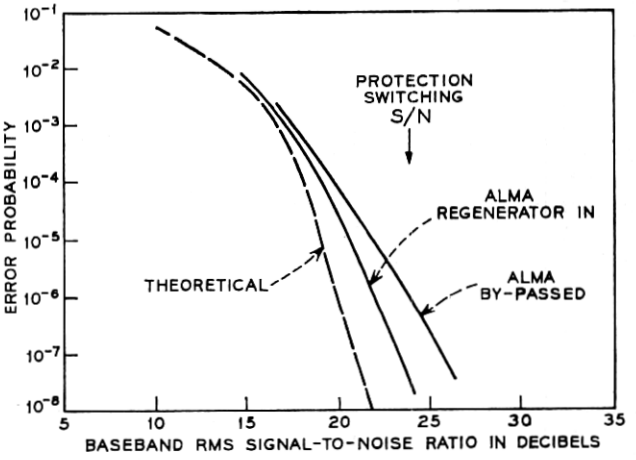

Fig. 11—Error rate versus baseband S/N.

IX. PHYSICAL DESIGN ASPECTS

9.1 *General Description*

The digital terminal shelf includes a digital transmitter and receiver and is shown in Fig. 13. It is constructed of three 17.8-cm-high (7-inch) aluminum castings and is designed for relay rack-type mounting on standard 58-cm-wide (23-inch) duct type bays. Plug-in printed

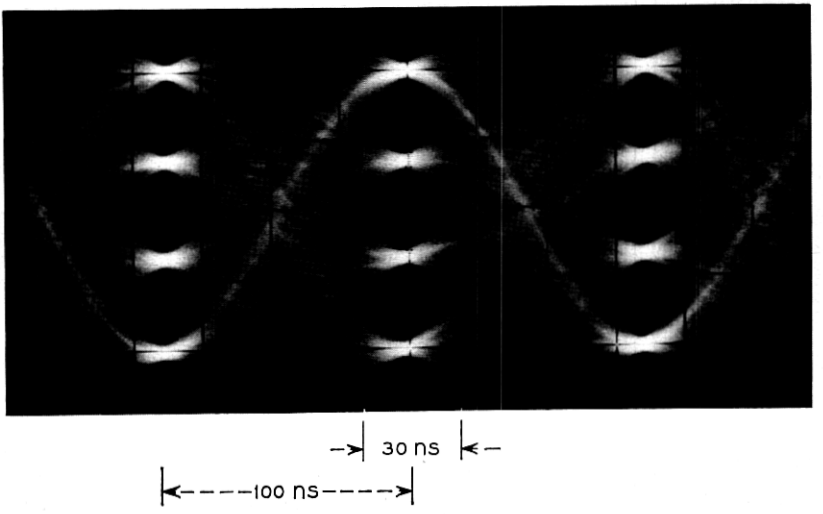

Fig. 12—Eye pattern.

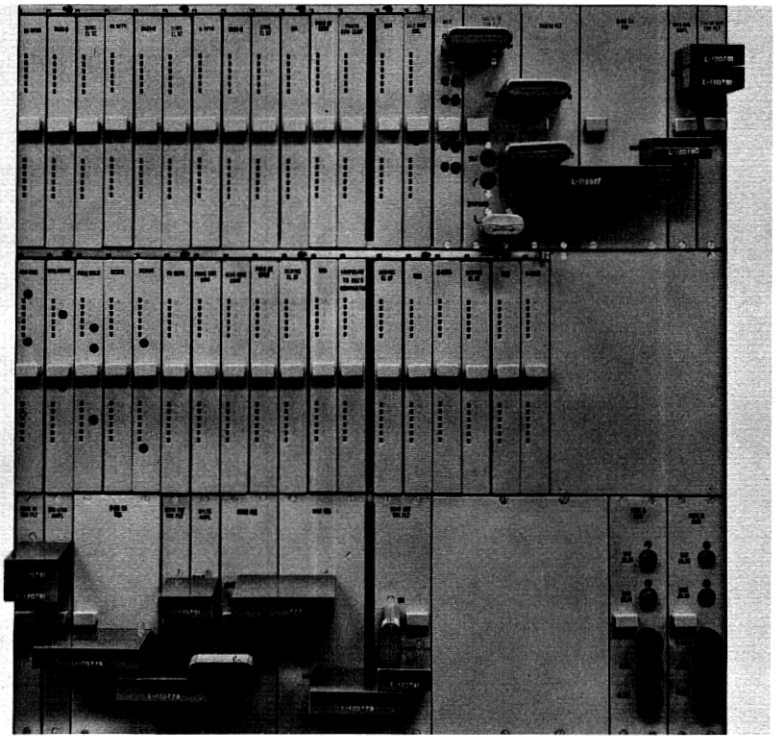

Fig. 13—Digital terminal shelf.

circuit boards with a nominal size of 16.5 cm by 27.9 cm (6.5 inches by 11 inches) mounted with horizontal spacings in multiples of 2.16 cm (0.85 inches) are used for individual circuits.

9.2 *Maintenance Considerations*

Monitor jacks for the diagnosis of trouble and routine servicing are provided on the test and alarm panel. Manual switching of a failed digital terminal shelf is provided for at terminal locations. A failed digital regenerator may be bypassed at IF using a 223B switch.

Use of plug-in circuit packs permits quick repair of a shelf.

X. POWER AND ALARM ARRANGEMENTS

10.1 *Power Supplies*

Three dc voltages are required for the operation of digital transmitters, receivers, and regenerators. They are +12V, −12V, and −5.2V.

An ac distribution panel located at the top of the bay feeds each power supply. To prevent the interruption of service resulting from the failure of a power supply, two supplies are provided for each voltage. They are wired in parallel via a diode bridge as shown in Fig. 14. A failed power supply unit may be replaced without disrupting service.

10.2 *Alarm Arrangements*

All alarm conditions register as a major alarm on the office alarm system. The bay alarm on the test and alarm panel is transferred to either a "DIG CKT" or an appropriate "PWR" alarm indication when the "ACO RST" button on the panel is operated.

A "PWR" alarm indication results from an overvoltage turn off of a dc supply or from the tripping of a power supply circuit breaker on the ac distribution panel.

A "DIG CKT" alarm indication is further subdivided into a major alarm or a minor alarm by an indication on the appropriate fuse and alarm circuit pack. A major alarm results when the signal error rate is greater than 10^{-3} error/bit or from a blown fuse in the fuse and alarm circuit pack. A minor alarm results when the signal error rate is greater than 10^{-6} error/bit.

XI. CONCLUSION

A four-level, 10.1-megabaud digital transmission system consisting of a digital terminal transmitter, a digital regenerator and a digital

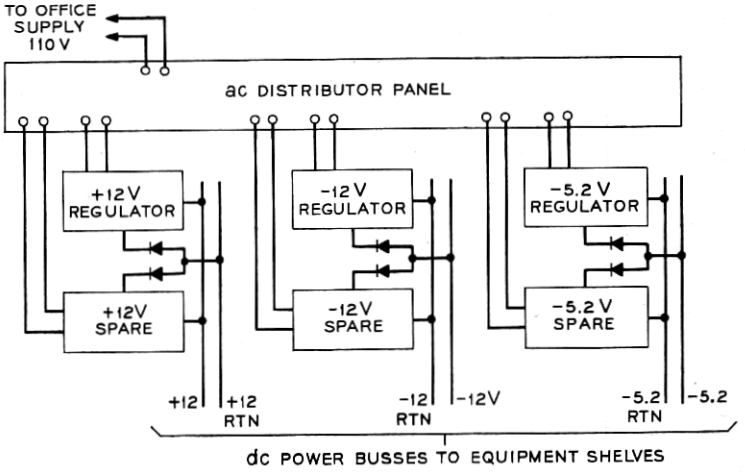

Fig. 14—Power supply arrangement.

terminal receiver capable of transmitting digital signals at a rate of 20.2 million bits per second over the TD-2 microwave system has been built and has undergone a successful field trial. An interim physical design permits early availability to the operating companies.

Operating over a radio route maintained under standard plant maintenance procedures, an error probability of the order of 10^{-10} error/bit has been realized. Experience on this route indicates the compatibility of a broadband digital system with other analog systems on the same radio route.

XII. ACKNOWLEDGMENT

The digital terminals were developed by the members of the Digital Transmission Design Department.

REFERENCES

1. Roetken, A. A., Smith, K. D., and Friis, R. W., "The TD-2 Microwave Radio System," B.S.T.J., *30*, No. 4 (October 1951), pp. 1041–1077.
2. Witt, F. J., "An Experimental 224 Mb/s Digital Multiplexer-Demultiplexer Using Pulse Stuffing Synchronization," B.S.T.J., *44*, No. 9 (November 1965), pp. 1843–1885.
3. Savage, J. E., "Some Simple Self-Synchronizing Digital Data Scramblers," B.S.T.J., *46*, No. 2 (February 1967), pp. 449–487.
4. Griffiths, H. D., and Nedelka, J., "100A Protection Switching System," B.S.T.J., *44*, No. 10 (December 1965), pp. 2295–2236.
5. Barry, J. F., Gammie, J., Lentz, N. E., and Salvage, R. C., "3A FM Terminal Transmitter and Receiver," B.S.T.J., *47*, No. 7 (September 1968), pp. 1423–1458.
6. Curtis, H. E., Collins, T. R. D., and Jamison, B. C., "Interstitial Channels for Doubling TD-2 Radio System Capacity," B.S.T.J., *39*, No. 6 (November 1960), pp. 1505–1528.
7. Millard, J. B., and Maunsell, H. I., "The *Picturephone*® System: Digital Encoding of the Video Signal," B.S.T.J., this issue, pp. 459–479.
8. Hathaway, S. D., Hensel, W. G., Jordan, D. R., and Prime, R. C., "TD-3 Microwave Radio Relay System," B.S.T.J., *47*, No. 7 (September 1968), pp. 1143–1188.
9. Bennett, W. R., and Davey, J. R., *Data Transmission*, New York: McGraw-Hill, 1965, chapters 5 and 7.