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Statistical Circuit Design:

Characterization and Modeling for Statistical Design

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Analysis of the variation in the electrical performance of integrated circuit structures requires a knowledge of the distributions and interrelationships of device parameter values. This article presents new techniques for more accurate transistor modeling and describes the statistical characterization procedure developed to describe the integrated circuit manufacturing process as far as the measurable electrical parameters are concerned.

I. INTRODUCTION

In statistical design work involving discrete passive elements, nominal parameter values and production distributions give an adequate description. The situation is more complicated for active devices in which the equivalent circuit used to describe these devices requires parameters which are interrelated.

With integrated circuits, conditions are further compounded by the fact that the parameters of different devices on an IC chip are interdependent. Experimentally, however, it has been found that the integrated circuit case can be conveniently decoupled to a manageable degree of complexity even when temperature effects are considered.

In the following sections, the philosophy underlying both our modeling approach and the measurement techniques is outlined. This is followed by a description of the transistor model favored for statistical analysis work, highlighting some popular misconceptions arising from inadequate past measurements. The implications for device modeling in an integrated circuit environment are then considered, followed by a description of the practical methods which have been successfully used to predict the variability in circuit performance arising from variations in the manufacturing process.

II. PRACTICAL MODELING

2.1 *Modeling Philosophy*

The modeling approach found to be most effective is to carry device physics as far as possible, then verify or modify the results by practical experience. To be truly useful, modeling has to be considered simultaneously from three fronts, in that the model must:

(*i*) Give an adequate qualitative description of the electrical behavior of the device.
(*ii*) Have efficient* parameters which are readily measurable (or calculable) and amenable to statistical description.
(*iii*) Be compatible with numerical circuit analysis techniques.

In the literature most attention has been given to items (*i*)[1,2] and (*iii*)[3,4]; in fact, the greatest impediment to meaningful statistical design work is the lack of attention to item (*ii*). In consequence, this discussion will dwell on the hard facts of what has to be done in practice when real data is required to get meaningful results.

There are at least two schools of thought on the subject of device modeling: modeling to get an understanding of the device physics and modeling for the purpose of circuit analysis. Although it is desirable to have one model for both situations, it is frequently expedient to make simplifications in the case of circuit analysis. In a statistical design, particularly one involving integrated circuits, the general properties of the system have to be represented. With transistors, the important points are:

(*i*) The matching of characteristics such as gain or junction voltages.
(*ii*) The tracking of parameters within a device and from device to device on an integrated circuit chip.
(*iii*) The temperature characteristics, vitally important in Bell System work, both from the standpoint of the variation of system performance with temperature and also for any aging effects which may be temperature dependent.

A general description of the above properties is therefore required in statistical design rather than an elaborate precision model which may greatly exceed the accuracy of available data.

Comparisons[1,2] of generic model types, which appear to indicate a mathematical equivalence, neglect some very important facts applicable to transistor models in common use. These facts relate to

* Efficient parameters are ones whose values are simply related to changes in device environmental conditions—preferably constants.

the choice of the independent variables in the model and the significance of this is discussed in Section III.

2.2 *Measurement Philosophy*

From the measurement standpoint the most important consideration is that of effectively decoupling the model parameters. This is done such that each measurement, or set of measurements, uniquely defines specific parameters. The ability to do this depends very much on the complexity of the model structure and may be difficult to achieve in more detailed physical models.[5]

Statistical data is expensive; it is necessary, then, to depend on the minimum set of data points and to maximize their use. In addition, it is expedient to identify parameters which are consistently the same in a given family of devices. This is considered further in Section III which to some extent dictates the form of model desired. Further, to minimize measurement effort, it is essential to use the same statistical data for both nonlinear and small signal models. The development of a suitable small signal model for this purpose is considered in Section IV.

Two approaches exist for determining the model parameters.

(*i*) Obtain the physical properties of the device, such as geometry and doping profile, and calculate the theoretical parameter values for the model.

(*ii*) Derive the parameters from electrical measurements at the device terminals.

In statistical work, item (*ii*) is more attractive as the process variability may not be well known. In addition, complex interactions may be compensated for in the direct measurement technique. For device design prior to fabrication, obviously a combination of (*i*) and (*ii*) has to be used, drawing on measured data from previous similar devices.

III. NONLINEAR TRANSISTOR MODELS

3.1 *Models in Common Use*

At the present time, two forms[6,7] of nonlinear transistor models appear to be in vogue in general purpose network analysis programs. The major difference between the two approaches lies in the reference currents used in the representation of the dependent parameters. The two manifestations have been identified as:

(*i*)[6] The injection model, based on the diode currents injected at the junctions.

(*ii*)[7] The transport model, based on the currents traversing the base region.

In the past it has been said[7] that since the two models appear to be mathematically equivalent, there is a simple transformation between the parameters and it makes little difference which one is used. In fact, this ignores the approximations inherent in the model derivation. It turns out that the functional dependencies of the model parameters in case (*ii*) are more realistic from a physical viewpoint and at the same time simplify the measurement procedures required for parameter determination.

3.2 *Evaluation of the Popular Models*

To stress the significance of the claim for the transport model, the following argument is presented to show the simpler measurement requirements and the more accurate dynamic characterization of this model.

3.2.1 *DC Model*

Figure 1 shows the equivalent circuits of the intrinsic transistor for the two models under consideration; the elements making up the two equivalent circuits are identical, consisting of two semiconductor diodes to provide for minority carrier injection and two current sources to account for minority carrier transport across the base region. The coefficients α_F , α_R , B_N , B_I are current dependent and are represented by either functional or tabular dependence on the currents I_F , I_R , I_N , and I_I respectively. The important differences between the two models are the reference currents used as mentioned in Section 3.1.

The defining equations* are

(a) *Injection Model*	(b) *Transport Model*	
Emitter junction injection:	Transport from emitter to collector:	
$I_F = I_{EF}[\exp(qV_{be}/n_e kT) - 1].$	$I_N = I_{ES}[\exp(\theta_N V_{be}) - 1].$	(1)
Collector junction injection:	Transport from collector to emitter:	
$I_R = I_{CR}[\exp(qV_{bc}/n_c kT) - 1].$	$I_I = I_{CS}[\exp(\theta_I V_{bc}) - 1].$	(2)

The equations for the terminal currents representing the transistor

* The choice of parameter names for the transport model are identical with the CIRCUS[7] convention; the injection model parameter names are selected to prevent ambiguity. The parameters used are defined in Table I.

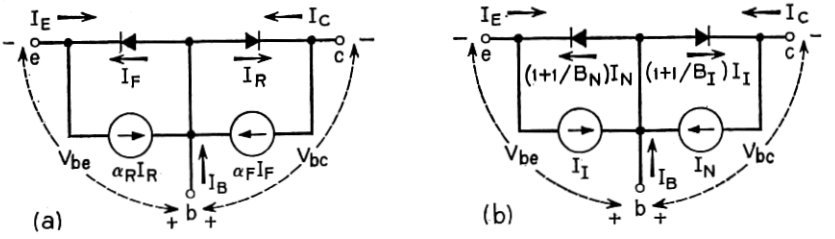

Fig. 1—Equivalent circuits for transistor models. (a) Injection model, (b) Transport model.

nonlinearities are

$$I_E = -I_F + \alpha_R I_R , \qquad I_E = -\left(1 + \frac{1}{B_N}\right) I_N + I_I , \tag{3}$$

$$I_C = \alpha_F I_F - I_R , \qquad I_C = I_N - \left(1 + \frac{1}{B_I}\right) I_I , \tag{4}$$

$$I_B = (1 - \alpha_F) I_F + (1 - \alpha_R) I_R , \qquad I_B = \frac{I_N}{B_N} + \frac{I_I}{B_I} . \tag{5}$$

If the emitter junction is forward biased with $V_{bc} = 0$ such that $I_R = 0$, and $I_I = 0$, then,

$$I_F = -I_E = I_C + I_B , \qquad I_N = I_C . \tag{6}$$

(ideal component) (nonideal component) (ideal component)

Equation (6) shows the fundamental difference between the two models by virtue of the make-up of the reference currents I_F and I_N. I_N represents an ideal component of current in the sense that the collector current and emitter-base voltage are related[5] by the "ideal" diode law. I_F, on the other hand, is made up of two components of currents of which I_B, the base current, is nonideal.[8]

This gives the first reason for preferring the transport model, in that it is intuitively more satisfying to work with the components approximating theoretical behavior. Other experimental reasons now follow:

By measuring I_E and I_C as functions of V_{be}, it is possible to plot the voltage dependence of I_F and I_N as shown on the semilogarithmic plots in Fig. 2.

TABLE I—COEFFICIENTS USED IN COMPARING NONLINEAR MODELS

α_F	Common base current gain in normal mode.
α_R	Common base current gain in inverse mode.
B_N	Common emitter current gain in normal mode.
B_I	Common "emitter" current gain in inverse mode.
I_{CR}	Collector intercept current for the injection model.
I_{CS}	Collector intercept current for the transport model.
I_{EF}	Emitter intercept current for the injection model.
I_{ES}	Emitter intercept current for the transport model.
k	Boltzman's constant.
n_c	Collector injection factor.
n_e	Emitter injection factor.
q	Charge on electron.
T	Absolute temperature.
θ_N	Slope factor for normal mode.
θ_I	Slope factor for inverse mode.

In the inverted mode of transistor operation, if the collector junction is forward biased with $V_{bc} = 0$, then $I_F = 0$ and $I_N = 0$ giving

$$I_R = -I_C = I_E + I_B, \qquad I_I = I_E. \tag{7}$$

(ideal component) (nonideal component) (ideal component)

In this situation I_I represents an ideal component of current and I_R is made up of ideal and nonideal terms. Measurement of I_E and I_C for the inverted transistor gives the voltage dependence of I_I and I_R as shown in Fig. 2.

The redundancy in the injection model is shown by the fact that the slopes and intercepts are different for I_F and I_R in the linear portion of the curves where leakage and high-level effects are not significant. The transport model gives identical slopes and intercepts as a result of the common dependency on the base charge.[9] Thus

$$I_{ES} = I_{CS} \tag{8}$$

and

$$\theta_N = \theta_I = \frac{q}{kT}. \tag{9}$$

This has been found to be the case experimentally within the accuracy of the measurements, and follows from the one-dimensional model derivation in elementary transistor theory. In the interests of generality, however, four parameters rather than two are retained in the model used in nonlinear analysis[10] to allow for possible deviations[11] in very high-frequency transistors. It is important to note that the redundancy in the injection model is absorbed in the current dependent

parameters $B_N(I_N)$ and $B_I(I_I)$ used in the transport model to define the base current in equation (5).

3.2.2 *Dynamic Behavior*

In a transistor, charge storage can be divided into two types:

(*i*) Fixed charge in the depletion regions (voltage dependent).
(*ii*) Mobile charge in transit (current dependent).

To account for the charging currents which flow under dynamic conditions, two capacitances are included across each junction as shown in Fig. 3. C_{ej} and C_{cj} are the voltage dependent capacitances representing the emitter and collector depletion regions.

Capacitances C_{de} and C_{dc} are current dependent and represent the minority carrier charge stored on account of the current flow.

According to charge control theory[12] the charges are directly proportional to the reference currents such that the capacitances, which are the incremental changes of charge with junction voltage, then become

(a) *Injection Model* (b) *Transport Model*

$$C_{de} = \frac{qT_{EF}}{n_e kT}[I_F + I_{EF}], \qquad C_{de} = \theta_N T_{CN}[I_N + I_{ES}], \tag{10}$$

$$C_{dc} = \frac{qT_{CR}}{n_c kT}[I_R + I_{CR}]. \qquad C_{dc} = \theta_I T_{CI}[I_I + I_{CS}]. \tag{11}$$

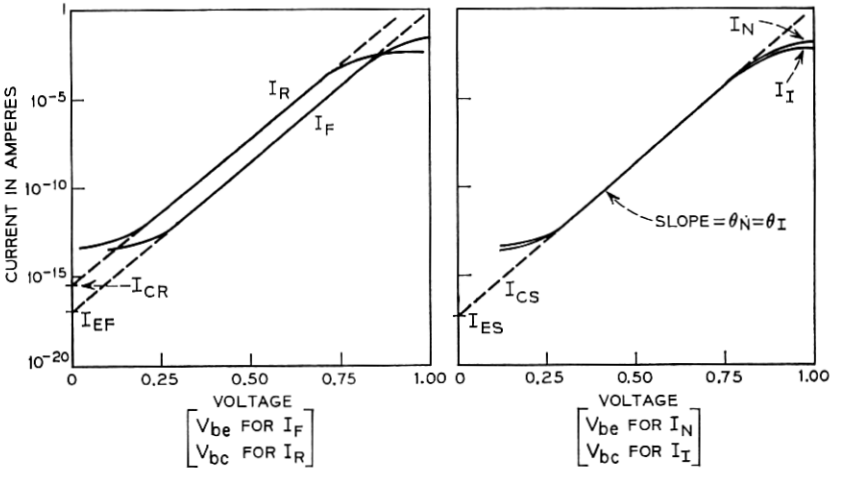

Fig. 2—Transistor nonlinear behavior. (a) Injection model, (b) Transport model.

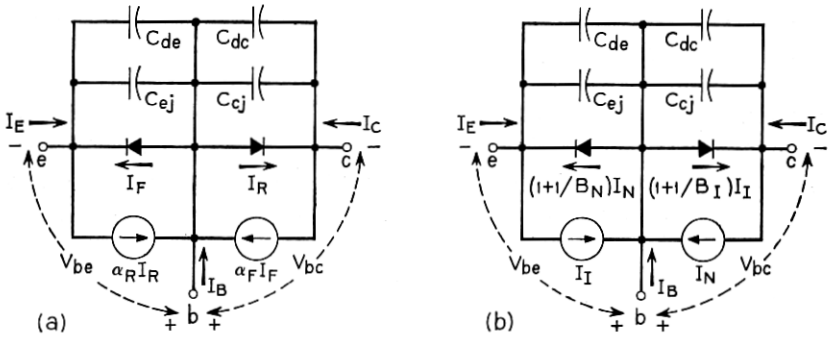

Fig. 3—Dynamic transistor model. (a) Injection model, (b) Transport model.

In practice the parameters* $T_{EF}(I_F)$, $T_{CR}(I_R)$, $T_{CN}(I_N)$, $T_{CI}(I_I)$ have to account for a multitude of effects, for example high-level injection effects, and storage in the collector remote from the base. To represent these effects the parameters are made functions of current as shown.

The parameters $T_{EF}(I_F)$ and $T_{CR}(I_R)$ depend on current terms which consist of ideal and nonideal components. More importantly these characteristic times describe both transit time and recombination time effects. This is both bad and unnecessary.

It is bad since the recombination phenomena are not nearly as well understood (mainly because of surface effects) as transit times; hence, large variations from unit to unit can be expected and in fact are found in practice.

It is unnecessary since the information relating the transit time and recombination time is already contained[13] in the nonlinear current gain terms B_N and B_I (or α_F and α_R). Thus, the effect of basing the characteristic times on the injection currents is to force the introduction of redundant nonidealities in the dynamic parameters. This is much more significant for $T_{CR}(I_R)$ than for $T_{EF}(I_F)$.

3.2.3 *Experimental Evidence*

Indication that the injection model was in trouble came about from actual storage time measurements on high-frequency devices. These showed that $T_{CR}(I_R)$ was a strong function of I_F which could not be

* D. Koehler[2] has defined a consistent set of characteristic time parameters which gave the rationale for the parameter terminology for the injection model. The parameters T_{CN} and T_{CI} for the transport model follow the familiar CIRCUS[7] format, but strictly speaking for consistency[2] these should be T_{CN} and T_{EI}, where C and E refer to collector and emitter, respectively. If T_C signifies "time constant," then perhaps a better unambiguous pair of time parameters would be T_N and T_I.

accounted for in the model and, in fact, it was impossible to assign meaningful values to T_{CR}.

The parameter $T_{CI}(I_I)$, in the transport model on the other hand, was found to be essentially independent of I_N. More importantly, for the devices in question, T_{CI} was constant over a wide range of I_I and in fact showed little variation from device to device. In addition, it was found that devices of the same family which had different gold spiking treatment gave approximately the same value of T_{CI}. Differing amounts of gold doping control the recombination lifetime which is already accounted for by the dc parameter $B_I(I_I)$.

3.2.4 *Important Properties for Tolerance Analysis*

Consistency of T_{CI} for families of device types is vitally important in tolerance analysis work since it requires fewer measurements, and can be given a simple statistical description, yet still yields good answers. The explanation for this superior performance of the transport model parameters is that T_{CN} and T_{CI} are effective transit times which, as mentioned earlier, are much better behaved than recombination times. Thus for the dynamic response as well as the dc situation, the transport model description eliminates the redundancy of the injection model.

3.2.5 *Transistor Model Most Suited to Statistical Design*

The conclusion drawn from these experimental results is that the transport model as outlined above is to be preferred for the following reasons:

(*i*) Nonideal components of current do not occur in the equations relating input voltage and output current.

(*ii*) Intercept currents and slope factors are obtained from one set of measurements instead of two.

(*iii*) Parameters are decoupled in that the dc nonlinearities are contained only in the parameters $B_N(I_N)$ and $B_I(I_I)$.

(*iv*) Characteristic time parameters describing dynamic behavior are constant over a wider range of currents and vary less from device to device, thereby simplifying the measurement procedure.

(*v*) Dynamic behavior is more accurately modeled and the effect of process variation is decoupled from T_{CI} and contained predominantly in $B_I(I_I)$.

Thus from considerations of both accuracy and measurement convenience, the transport model is preferable and has, in fact, been used with considerable success in network analysis programs.[10]

3.3 *Transistor Output Characteristics*

3.3.1 *Defects of the Model*

To account for the effects of bulk material in the base, collector and emitter, resistances R_B , R_C and R_E are added to the intrinsic model of Fig. 3(b) as shown in Fig. 4.

Two effects not accounted for in this model as it stands are:

(*i*) Collector output resistance.
(*ii*) Avalanche multiplication.

Collector avalanche multiplication is usually accounted for by multiplying the parameter I_{CS} by a factor of the form $1/[1 - (V_{cb}/V_B)^n]$ where n and V_B are constants. Since the avalanche mode is not of concern in most circuit analysis encountered in this discussion, it will not be considered further.

Item (*i*) is very significant, particularly for devices in high-resistance circuits, and some simple means had to be found to represent the output resistance. The approach used is described in Section 3.3.2 and the equivalent output resistance is calculated in Appendix C.

3.3.2 *Thermal Considerations*

Measurements of B_N as a function of V_{CB} for constant base current are shown in Fig. 5 where two important effects should be noted.

(*i*) Heating effects due to increased power dissipation greatly increase the change in B_N .

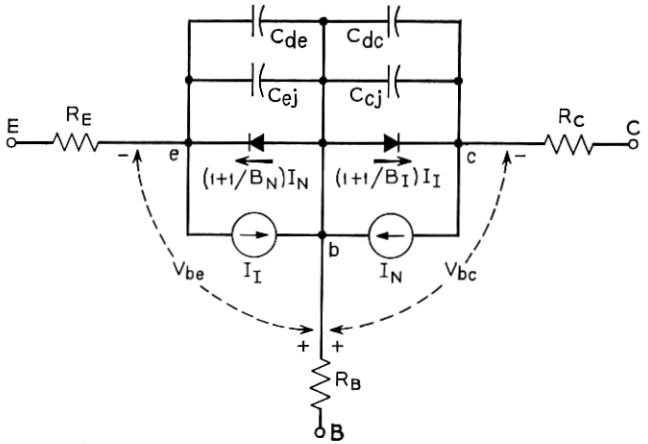

Fig. 4—Nonlinear transistor model.

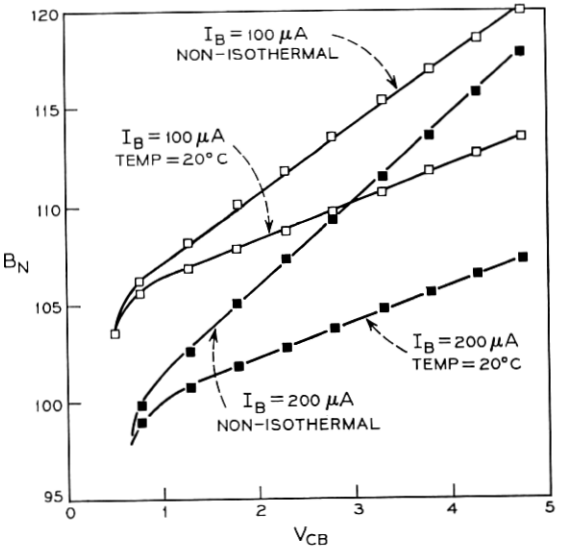

Fig. 5—Variation of B_N with V_{CB}.

(*ii*) When junction temperature is held constant the change in B_N is considerably reduced but more importantly the curves are essentially parallel.

This suggested representing the current gain term in the form

$$B_N = \beta_N(I_N , T) + V_{cb}/V_N \tag{12}$$

where $\beta_N(I_N , T)$ is a function of current and temperature and V_N is a constant.

Further investigation of a range of devices of different structural and manufacturing processes yielded three useful results.

(*i*) At constant junction temperature* the curves for B_N as a function of V_{CB} with I_B as a parameter were parallel [Fig. 6(a)].

(*ii*) At different constant temperatures the curves remained parallel [Fig. 6(b)].

(*iii*) Devices with the same geometry but different gold spiking gave parallel curves (Fig. 7).

* Note that it is not adequate to hold a transistor can or substrate at constant temperature and assume that the junction remains at constant temperature even under pulsed conditions. V_{be} at a low reference current was used as a temperature monitor and a "Themospot" probe (manufactured by EG&G Boston, Mass.) was used to adjust the environment temperature such that V_{be} remained constant.

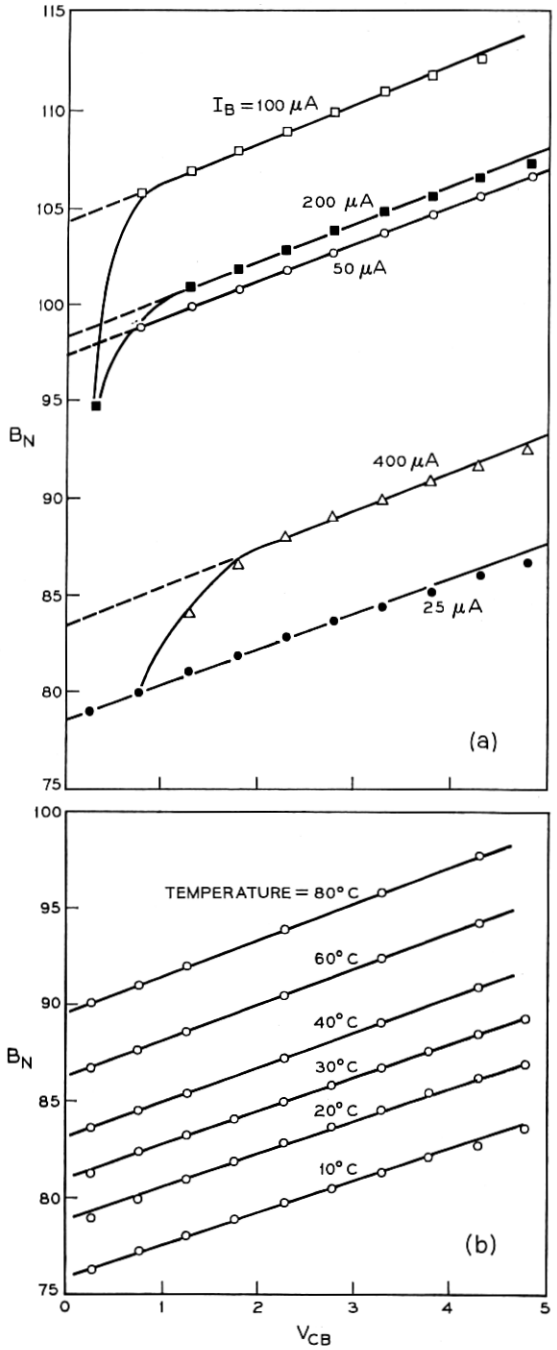

Fig. 6a—B_N as a function of V_{CB} at temperature of 20° C.
Fig. 6b—Variation of B_N with V_{CB} and temperature for base current $I_B = 25\ \mu A$.

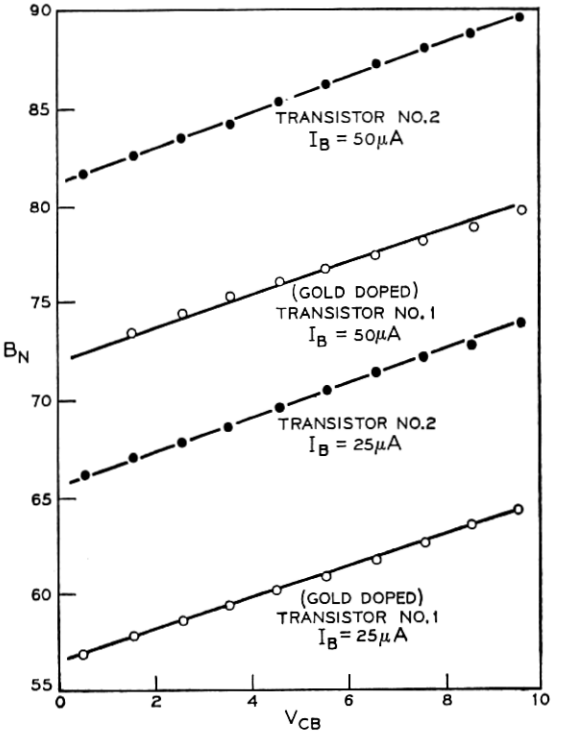

Fig. 7—Variation of B_N with V_{CB} for two devices with the same geometry.

Thus equation (12) has vital properties for statistical design in that the current and temperature dependence is contained in $\beta_N(I_N, T)$ and parameter V_N can be regarded as a constant for a given device geometry. Since the lines in Fig. 6 are all parallel, it is only necessary to take measurements for one value of I_B at room temperature to determine V_N. This value of I_B can be small enough that no significant heating occurs on pulsed measurements obviating the need for a heat sink.

Equation (12) was very easily added to the model in the computer program[10] and Fig. 8 shows a comparison of measured curves and computer predictions.

IV. SMALL SIGNAL TRANSISTOR MODELING

4.1 *Types of Models*

Small signal models used in linear steady-state analysis programs may be divided into two categories:

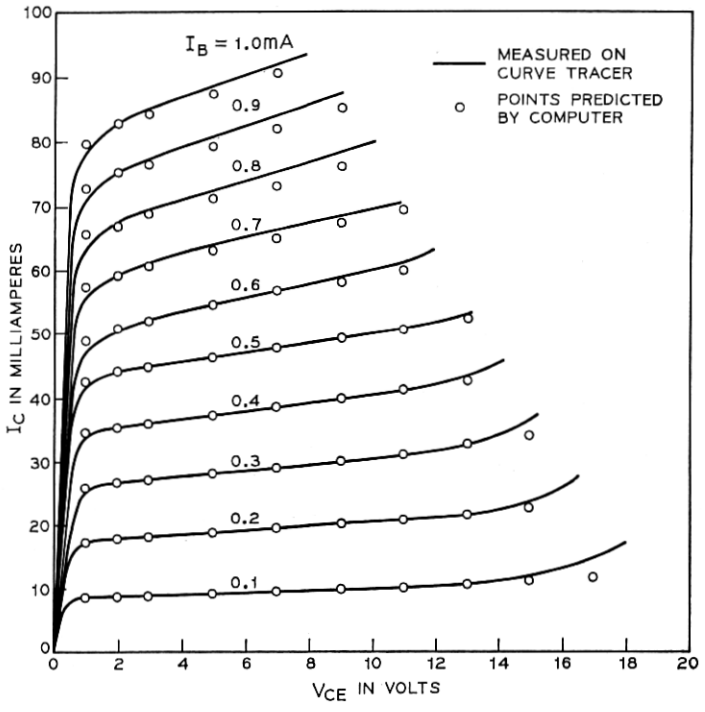

Fig. 8—Transistor output characteristics.

(*i*) Terminal models—measured two-port parameter data at the required operating point over the desired frequency range.
(*ii*) Physical models—equivalent circuit representation of the device at the operating point in question.

Both approaches have advantages and disadvantages for variability analysis.

4.1.1 *Terminal Models*

The measured data can be obtained extremely precisely and used directly in linear analysis programs to investigate circuit performance. This gives no loss of accuracy in the representation of the specific transistors in question.

The main problems with this technique are:

(*i*) Data at different temperatures at several bias points over a range of frequencies imposes a prohibitive storage problem.

(*ii*) Devices have to be available on which measurements can be made and hence new devices cannot be handled this way.

(*iii*) Statistical descriptions of devices cannot be generated, but have to depend on past measured data.

4.1.2 *Equivalent Circuit Model*

The equivalent circuit model eliminates a number of these difficulties and has the following advantages:

(*i*) The number of parameters at a given bias point is dependent only on the complexity of the model for all frequencies in the range of applicability. In addition, the model can easily be made a function of bias, as shown below.

(*ii*) Reasonable first-order estimates for the equivalent circuit model of new devices can be made from a knowledge of similar previously characterized devices.

(*iii*) Variability and interdependence of the equivalent circuit elements of the model can be characterized to give a statistical description for Monte Carlo analysis.

The main problem with the equivalent circuit is its range of applicability, usually requiring more complexity for adequate representation as the frequency is increased.

4.2 *The Hybrid-Pi Model*

Many forms of equivalent circuit representation for the transistor are possible.[14] The hybrid-Pi model is particularly attractive and can be readily derived from the nonlinear model of Fig. 4 showing that the hybrid-Pi model is simply the incremental version of the nonlinear model. Thus, once we have a statistical characterization of the nonlinear model, by appropriate choice of the parameters for the hybrid-Pi model, we have complete statistical information for small signal analysis work.[15]

In the active region of operation, the collector junction is reverse-biased, and from equations (2) and (11)

$$I_I \approx 0,$$

$$C_{dc} \approx 0.$$

Figure 4 can then be simplified and redrawn as Fig. 9. At low frequencies, the currents are:

$$I_E = -(1 + 1/B_N)I_N ,$$
$$I_C = I_N ,$$
$$I_B = I_N/B_N .$$

Thus, the current generators in Fig. 9 can be rearranged to give the configuration of Fig. 10 and satisfy the above equations.

The incremental behavior of the two current sources in Fig. 10 has to be evaluated to give the small signal model. The linear equivalents of the current sources are derived from the following equations:

$$\delta I_B = \delta V_{be} \frac{\partial I_B}{\partial V_{be}} , \qquad (13)$$
$$= \delta V_{be}/R_{be} ,$$

$$\delta I_C = \delta I_B \frac{\partial I_C}{\partial I_B} + \delta V_{ce} \frac{\partial I_C}{\partial V_{ce}} , \qquad (14)$$
$$= i\beta + \delta V_{ce}/R_0 ,$$

where δ signifies an incremental change and i is the incremental change in the low frequency base current I_B.

The hybrid-Pi model incorporating the linear elements defined in equations (13) and (14) is shown in Fig. 11. Also included in the model are capacitances C_1, C_2 and C_3 to account for header capacitances in discrete devices and parasitic capacitances in integrated circuits.

The relationship between the linear elements in Fig. 11 and the parameters previously used for the nonlinear model of Fig. 4 are:

$$C_{be} = C_{ej} + C_{de} , \qquad (15)$$

$$\left.\begin{aligned} \beta &= B_N/[1 - S/B_N] \\ R_{be} &= \beta/[I_N\theta_N] \\ R_0 &= B_N V_N/I_N \end{aligned}\right\} . \qquad (16)$$

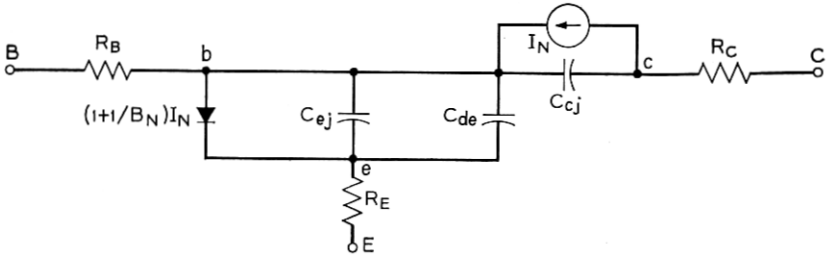

Fig. 9—Simplified model for active region.

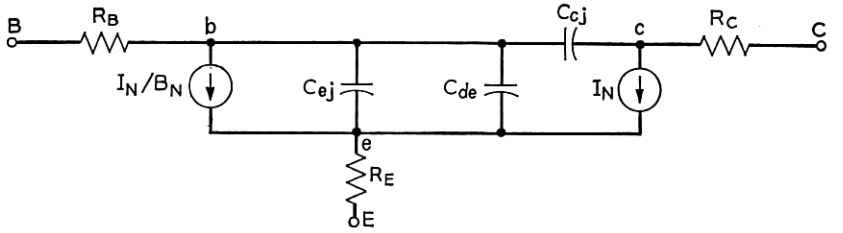

Fig. 10—Equivalent π model.

The derivation of the relationships constituting equation (16) are given in Appendices A, B and C. Thus at any bias condition, the value of C_{cj} is determined by the voltage V_{bc} ; the value of C_{ej} is determined by the voltage V_{be} ; and the collector current I_N determines the values of C_{de} , β, R_{be} and R_0 .

The model in Fig. 11 represents the transistor at any bias condition over the desired frequency range of applicability. No parameters other than those required for the nonlinear model are used in this representation. In consequence, all the relationships for temperature dependence, parameter variation and correlation which are developed in Section 6.3 for the nonlinear model, can be applied directly for small signal tolerance analysis work.

4.2.1 *Excess Phase*

The frequency dependences of the junctions are represented by the single pole type of response in each case. Excess phase resulting from

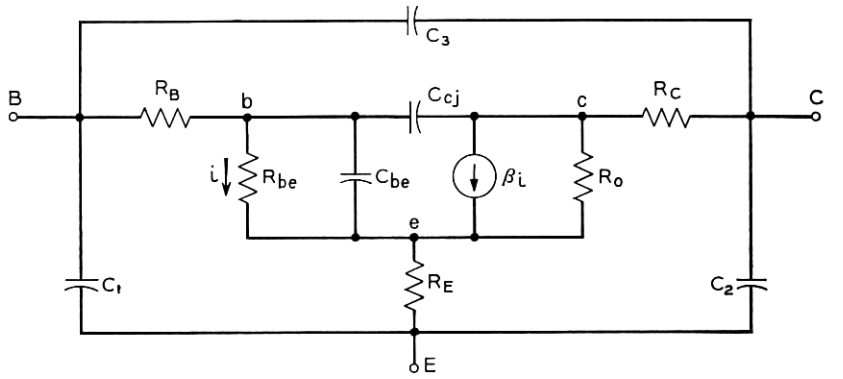

Fig. 11—Hybrid-Pi small signal model.

other nondominant poles is not accounted for explicitly in the model of Fig. 11. However, the additional capacitors C_1, C_2 and C_3 have been found to give the additional degrees of freedom to account not only for the stray capacitances but also to satisfy the excess phase requirement. The model in Fig. 11 has in fact been very accurate up to 1 GHz, the highest frequency at which reliable measurement data is currently available.

V. INTEGRATED CIRCUIT DEVICE MODELING

5.1 *Monolithic Integrated Circuit Environment*

Passive components, such as resistors and capacitors, are used in three forms: discrete, thin-film and planar diffused, along with discrete and planar diffused transistors. Of these, the monolithic integrated circuit situation imposes the greatest requirement on both device modeling[16] and statistical characterization. Modeling problems arise from the junction isolation which result in various parasitic elements in addition to the desired components. Characterization difficulties occur because of the parameter interdependence resulting from the simultaneous fabrication of complete circuits in which the components have a common dependency on the various processing steps. The effect of the integrated circuit environment is considered in the next sections.

5.2 *Resistor Models*

The integrated circuit resistor consisting of a base diffusion, as shown in Fig. 12(a), is really a distributed diode which is reverse-biased. However, the pnp structure also gives rise to a possible parasitic transistor and distributed capacitance as shown in Fig. 12(b). Under normal circumstances, C is taken to the most positive circuit voltage and S to the most negative which effectively eliminates the transistor and leaves only the distributed capacitance. This can be lumped at each

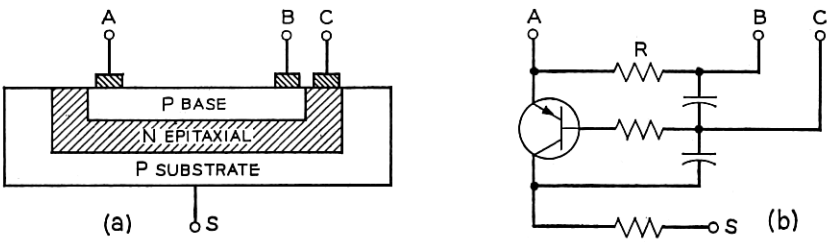

Fig. 12—(a) Diffused resistor, (b) Resistor equivalent circuit.

end of the resistor. Long narrow resistors, however, would be poorly modeled by such an approximation and a distributed representation would be more appropriate.

In manufacture, the variation in resistor values depends on a number of factors, of which the most important are

(*i*) Error in the resistor shape calculation.
(*ii*) Error in the photomask.
(*iii*) Variation in the processing.

Items (*i*) and (*ii*) relate to the resistor geometry and will result in different variations depending on the shape, dictated by the resistor magnitude. Item (*iii*) accounts for the tracking of resistors on an IC chip and is discussed further in Sections 6.3.1 and 6.3.5.

Thin-film resistors can be modeled by ideal resistors except at higher frequencies where stray capacitances become significant. These are obviously layout dependent and have to be estimated in each particular situation. One advantage of the thin-film situation is that resistors can be trimmed to value when required. Such an adjustment has frequently to be performed in simulations[17] and greatly influences the analysis procedure.

An important source of common variation in integrated circuits results from temperature changes on the chip which causes the resistance to change according to the formula

$$R_T = R_{T_0}[1 + \alpha(T - T_0)] \tag{17}$$

where α is the temperature coefficient.

It should be noted in passing that thermal modeling should be performed in integrated circuit structures to account for possible thermal feedback. The electrical parameters of the various devices are temperature dependent and if the devices dissipate significant power, there is coupling between the thermal and electrical behavior of the system. In practice, this can be a prohibitively expensive study and it is either assumed that thermal feedback poses no problem or a very crude static thermal analysis is performed.

5.3 *Capacitor Models*

Two forms of capacitors are in common use in integrated circuit work.

(*i*) Reverse-biased junctions.
(*ii*) Oxide film dielectric.

For item (*i*), any of the three junctions, emitter-base, base-collector or collector-substrate, can be used. The collector-base situation and its equivalent circuit are shown in Fig. 13.

The main problems with the junction capacitance are the variation with voltage, the need to stay reverse-biased and the high series resistance.

The oxide film capacitor overcomes these disadvantages since it is constant and nonpolar. As shown in Fig. 14, it also has a simpler equivalent circuit.

5.4 *Transistors*

As with passive elements, the main difference between the integrated circuit transistor model and its discrete counterpart described in Sections III and IV relates to the parasitic elements encountered in the junction isolation environment. As Fig. 15 shows, the IC transistor should really be considered as a four-layer device to fully account for the device behavior. This is particularly true for transistors which saturate and forward-bias the collector junction such that the substrate behaves like the collector of a poor transistor. Figure 15(b) shows the equivalent circuit for this situation. Steps are usually taken in the processing to minimize the effect of the parasitic pnp transistors. Characterizing this equivalent circuit is difficult since there is no way of identifying the currents in the two transistors to obtain the parameters for each device. Several authors have considered this problem[18] and some computer programs[7] provide four-layer device capability for the IC structure. In many applications, as with the passive elements, only the capacitance effects of the collector-substrate isolation need be taken into consideration in computer analysis. Another characteristic of the integrated circuit environment is the top collector contact which results in parasitic resistance between the collector terminal and

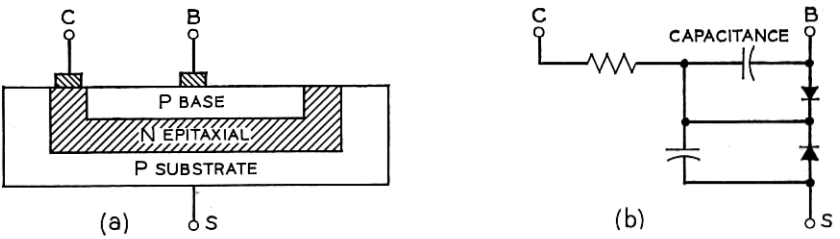

Fig. 13—Diffused junction capacitance. (a) Collector-base capacitor, (b) Equivalent circuit.

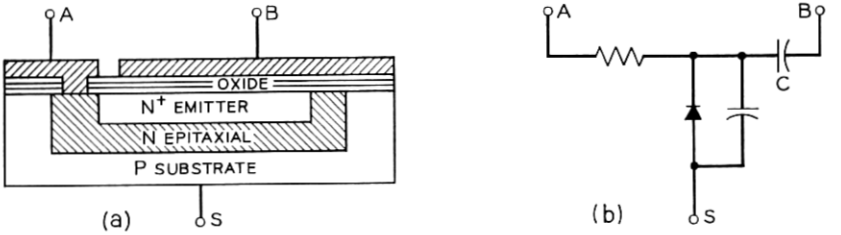

Fig. 14—Oxide capacitor. (a) Oxide film capacitor, (b) Equivalent circuit.

the active region of the collector junction. This can be accounted for by R_c in Fig. 4.

VI. STATISTICAL CHARACTERIZATION

6.1 *Monte Carlo Analysis*

In Monte Carlo analysis, the objective is to predict the electrical behavior of circuits in the light of device variability resulting from a manufacturing process. When the process is well understood, a statistical description of the device behavior in terms of the process variables is desired. Some attempts along these lines have been made[19,20] in semiconductor device work but the transformation from process variables to electrical parameters is complex. The result of these studies has generally been to guide device designers in the optimization of their fabrication process rather than to provide circuit designers with statiscal information on device parameters.

Assuming that the process is under good control, a practical solution to the problem of describing the electrical parameters of the devices in terms of the process variability is to measure the actual electrical parameters of a statistically significant quantity of the product. This

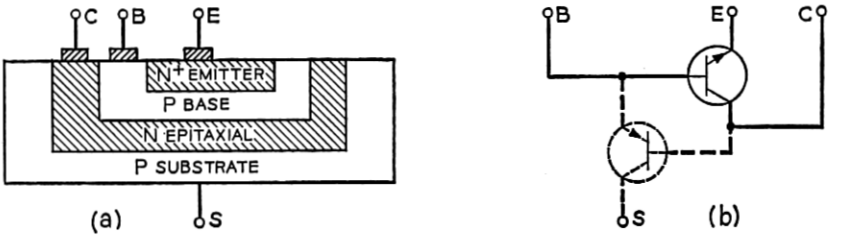

Fig. 15—Integrated circuit transistor. (a) Transistor structure, (b) Equivalent circuit.

eliminates the uncertainty in transformation and, more importantly, puts the statistical description as close as possible to the desired objective. The only requirement of this statistical description is that it must permit the generation of groups of devices with parameters which have the same statistical characteristics as the output from the process.

The problem, then, is divided into two parts:

(*i*) Measurement procedures to estimate the device parameters.

(*ii*) Statistical analysis of the measured parameter values to find their distributions and interrelationships and synthesis procedures for computer generation of parameter values with the same distributions and interrelationships.

Item (*i*) is reasonably well understood and will be described briefly. Item (*ii*) is more of an evolving art with much left to expediency at the present time. It will be described in some detail to show the current state of this art as applied to very significant Bell System Projects.[10,17]

6.2 *Transistor Parameter Measurement*

6.2.1 *Model Parameters*

The most difficult integrated circuit device to characterize is undoubtedly the transistor. Earlier sections have described an adequate model for this device and the modifications required to account for the integrated circuit environment.

For convenience, the essential parameters of the model* of Fig. 4 are listed in Table II along with the measurement techniques used to evaluate the parameters. The model parameters are related as closely as possible to the measurements, both to minimize the amount of data reduction and also to provide parameters, the significance of which is well understood by circuit designers. In addition, the measurements are highly decoupled such that parameters are uniquely defined by each set of measurements. This eliminates the need for optimization to sort out parameters on a best-fit basis which is not practical for a system geared to measuring statistically significant quantities of data.

6.2.2 *DC Measurements*

Figure 4 shows that terminal measurements will always result in at least two of the bulk resistances appearing in series. In principle, by

* Note that the additional capacitance C_{cs} between collector and substrate is included to account for the integrated circuit environment.

TABLE II—PARAMETERS FOR THE NONLINEAR TRANSISTOR MODEL

R_B	Base bulk resistance,	DC Measurements.
R_C	Collector bulk resistance,	
R_E	Emitter bulk resistance,	
I_{ES}	Intercept current,	
θ_N	Slope factor,	
V_N	Gain voltage factor in nominal mode,	
β_N	Current gain factor in normal mode,	
β_I	Current gain factor in inverse mode,	
C_{ej}	Emitter depletion capacitance,	Capacitance Bridge.
C_{cj}	Collector depletion capacitance,	
C_{cs}	Collector-substrate junction capacitance,	
T_{CN}	Characteristic time for normal mode,	frequency domain.
T_{CI}	Characteristic time for inverse mode,	time domain.

making two or more measurements, it should be possible to solve the simultaneous equations for the bulk resistances. In practice, R_E is very much less than R_B or R_C such that conductivity modulation, emitter crowding and other second-order effects cause small changes in R_B and R_C which may exceed R_E. A consistent set of measurements does not exist and severe errors would result from estimating the parameters under such circumstances. For discrete devices, R_E is frequently neglected as a first approximation, but for statistical design involving integrated circuit transistors, the technique described in Section 6.3.4 gives an effective way of estimating R_E.

The equation for the collector-emitter saturation voltage in terms of the variables in Fig. 4 is

$$V_{CE(\text{sat})} = I_C R_C + \frac{1}{\theta_N} \ln \left\{ \frac{1 + 1/B_I + I_C/I_B B_I}{1 + I_C/I_B B_N} \right\}. \tag{18}$$

If B_N and B_I have small variation in the current range of interest, then measurements of $V_{CE(\text{sat})}$ as a function of I_C with constant I_C/I_B will give a straight line with slope R_C. Figure 16 shows typical results.

There are many ways[21] of estimating R_B. For statistical design, it is essential to evaluate this parameter from readily available measured data. R_B is estimated from the plot of log I_C versus V_{BE} similar to Fig. 2(b). The initial deviation from the ideal exponential function at high currents is assumed to result from ohmic voltage drop such that at any current level

$$\Delta V_{BE} = I_B R_B + I_E R_E , \tag{19}$$

$$\approx I_B R_B . \tag{20}$$

Since I_B and ΔV_{BE} are known, R_B can be calculated.

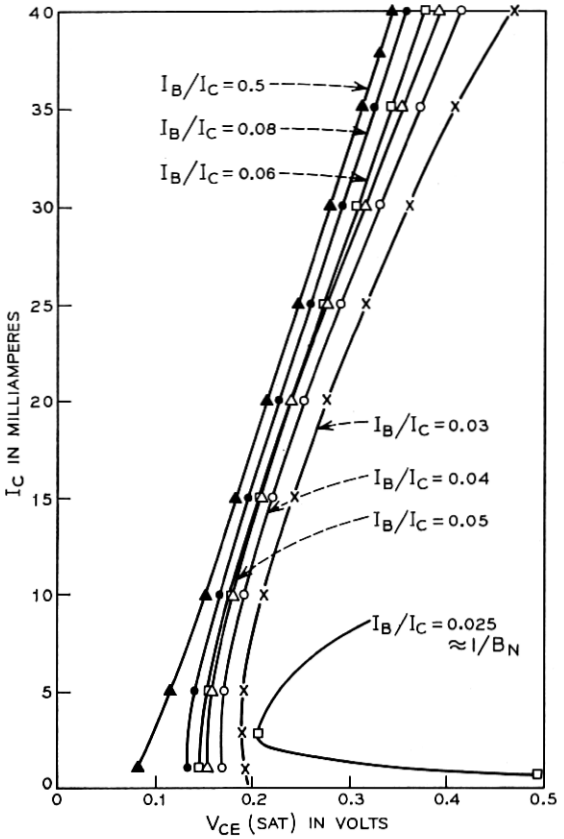

Fig. 16—I_C dependence on V_{CE} (SAT).

The parameters I_{ES} and θ_N are also estimated from Fig. 2(b) for the portion where equation (1) applies. The dc measurements* have to be made over a wide enough range and with sufficient accuracy particularly to resolve equation (20).

The current gain terms B_N and B_I and the voltage factor V_N are determined by dc measurements and evaluated as outlined in Section 3.3.2. To minimize the data reduction, a tabular format is used for the current gain terms in analysis programs[7,10] with interpolation for inter-

* An EAI 680 analog computer has been used to evaluate measurement techniques, since voltage and current sources are very easily programmed on such a machine and its digital voltmeter gives four-digit readout. The logic capability and sample and hold configuration enables pulsed measurements to be made and temperature monitored, where heating effects are significant.

mediate values.[10] As mentioned earlier, interpolation on a logarithmic current scale gives a very good estimation, minimizes the number of data points required and eliminates any curve fitting.

6.2.3 *Capacitance Measurements*

In reverse-bias, the capacitances C_{ej} and C_{cj} dominate and are measured on a capacitance bridge. In forward-bias, the shunt conductance of the junction makes bridge balance difficult and, in addition, the capacitances C_{de} and C_{dc} will become effective. A technique for estimating C_{ej} in forward-bias is given in Section 6.2.4. As with current gain terms, the measured capacitances C_{ej} and C_{cj} as functions of voltage are used in tabular format. With as few as three or four points and log-log interpolation, this gives an adequate representation and eliminates curve fitting difficulties.

6.2.4 *Frequency Domain Measurements*

Frequency domain measurements involve the small signal linearization of device behavior about some bias point. The model of Fig. 11 is then appropriate and it can be shown that the transistor cutoff frequency f_T is related to the collector current I_C in the active region by:

$$\frac{1}{2\pi f_T} = T_{CN} + \frac{1}{\theta_N I_C}(C_{ei} + C_{ci}) + R_C C_{ei} \; . \tag{21}$$

If f_T is measured at several values of I_c, then all the parameters in equation (21) are known except for T_{CN} and C_{ej}. These may be estimated from a plot of $1/2\pi f_T$ against $1/I_C$ as shown in Fig. 17 from which $T_{CN} + R_C C_{cj}$ is obtained as the intercept and C_{ej} in forward-bias can be calculated from the slope.

At high current levels, T_{CN} increases as shown by the curvature in Fig. 17. This is accounted for in the model by the tabulated function $T_{CN}(I_N)$.

Figure 18 shows the behavior of current gain $| h_{fe} |$ with frequency, indicating the cutoff frequency f_T at which the high-frequency asymptote extrapolates to unity. It is generally not possible to measure f_T directly since the actual curve deviates at high frequency as a result of capacitance effects. However, the characteristic of the asymptote is that the gain-frequency product is a constant from which

$$f_T = | h_{fe}(f) | \times [f]. \tag{22}$$

This measurement of $| h_{fe} |$ at a known frequency on the asymptote is sufficient to estimate f_T and such measurement is very quickly and

accurately done on computer-operated transmission measurement sets[22] which allow measurements up to 1 GHz.

6.2.5 *Storage Time Measurements*

If the transistor were symmetrical, T_{CI} could be estimated by the techniques of Section 6.2.4 for the inverted mode of operation. This approach does not work with planar diffused transistors on account of the charge storage mechanism, and a more satisfactory method is based on storage time measurements.

If t_s is the storage time for collector current I_C with base current drive I_{B1} and turn-off base current I_{B2}, then the storage time[23] in terms of the parameters of Fig. 4 is

$$t_s = \frac{B_N(B_I + 1)}{B_N + B_I + 1}\left[T_{CN} + \frac{B_I T_{CI}}{B_I + 1}\right] \ln\left\{\frac{|I_{B1}| + |I_{B2}|}{|I_C/B_N| + |I_{B2}|}\right\}. \quad (23)$$

Thus by measuring[13] storage time for a range of values of I_C and I_{B1} and knowing the other parameters in equation (23), the value of T_{CI} can be calculated.

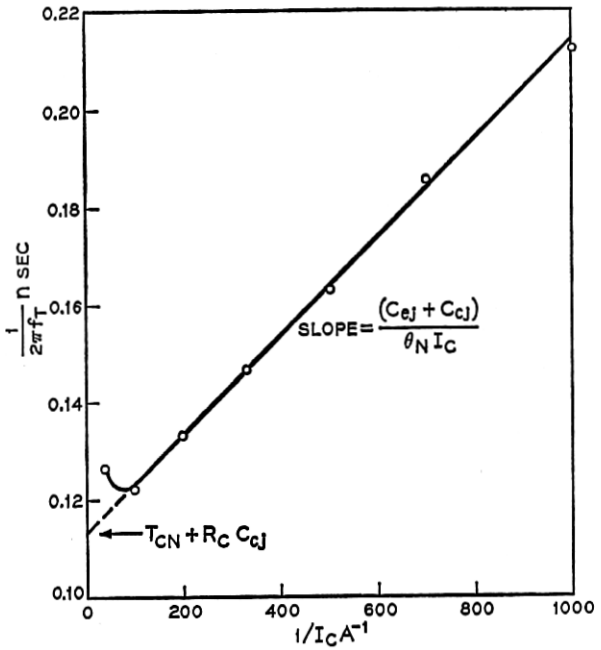

Fig. 17—Graphical solution for T_{CN}.

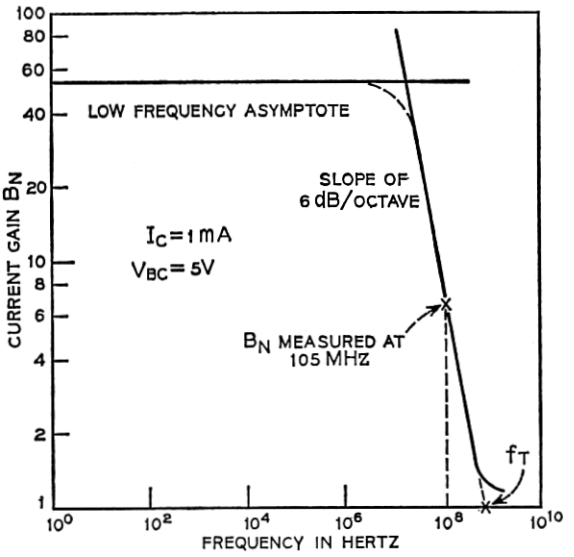

Fig. 18—Common emitter current gain B_N as a function of frequency.

6.2.6 *Parameter Verification*

The model of Fig. 4 is a simple model in which the parameters have to account for many second-order effects which were not considered in the simple one-dimensional analysis of transistor physics used to derive the model. Functional dependencies of the parameters on bias current or voltage provide the necessary degrees of freedom to match actual device performance. The continuing success of the model also depends on the measurement procedures used to estimate the parameters. These take account of the way the model behaves—which may not be the precise way microscopic effects in the physical device occur. The model, however, gives the same terminal performance, which is the most important consideration in circuit design.

For any specific device, it is essential to verify the adequacy of the measured parameter set and the most satisfactory approach is to simulate the test procedures. Just as these test procedures decoupled the parameters for measurement, so they give the maximum sensitivity to these same parameters in simulation.

6.3 *Statistical Analysis*

In this section, the problems encountered in "Monte Carlo" analysis of integrated circuits are considered. Nominal values, distribution

spreads and parameter interdependence have to be accounted for. The approach used to represent the production variability of parameters for transistor nonlinearities and resistor values is described and additional work to account for the statistical behavior of the dynamic parameters is outlined.

6.3.1 *Parameter Variation*

When many transistors of a given type are measured, one is usually asked for the parameters of a typical device. There is no simple answer to this request on account of possible interaction between parameters. For example, it would be meaningless to use some form of average for each of the transistor parameters as this could well result in a physically impossible combination of parameters.

With discrete passive elements, such as resistors described by a single parameter, the problem is much simpler, as the median of the distribution would probably be a good value to use. In integrated circuit work, resistor ratios are held within closer limits than nominal values on account of the common fabrication steps so that there are two variations to consider.

(*i*) Total variation in a component value for all the product, known as *global variation.*

(*ii*) Variation of the value of a component on an integrated circuit, given the value of another component, known as *local variation.*

Local variation results from the common dependence on processing steps and is the harder variation to characterize. In theory, parameter data for all components on many integrated circuit chips from a given process facility is desired. In practice, the statistical analysis required to pin down the exact form of interdependence would be prohibitive. Instead, the practical approach adopted was to develop a mathematical expression or statistical model for which the coefficients could be easily estimated. It will be shown that this expression yielded groups of parameters having the spreads and interdependence matching the little measurement data readily available.

The mathematical expression is:

$$P_{mn} = P_{on}(Y)\{1 + \lambda X_m + (1 - \lambda)X_n\}, \tag{24}$$

where

P_{mn} is a parameter of the nth device on the mth integrated circuit chip.

$P_{on}(Y)$ is the nominal parameter (having functional dependence on variables Y) for the nth device.

X_m is an independent random number whose selection amounts to picking a specific chip.

X_n is an independent random number whose selection accounts for picking a specific device on that chip.

λ is a tracking coefficient ($0 \leqq \lambda \leqq 1$) to account for the division between the free and dependent part of the permissible variation.

Two comments about equation (24) are in order. First, in the absence of better information, the numbers X_m and X_n are selected from the global distribution, normalized so that the median is zero. The effect, then, is for the selection of X_m to move the median value of parameter P away from nominal for the mth chip and narrow the range by the factor λ. The global distribution of P, normalized and narrowed by the factor $(1 - \lambda)$, is then placed about this new median and the selection of X_n determines the actual parameter value P_{mn}. It should be noted that the resultant distribution of P may differ from the global distribution since the distribution of the sum of two random variables is not necessarily of the same form as the distribution from which these random variables were selected. However, the mean and the variance of the resulting distribution are easily controlled.[10]

The second comment relates to the form of the expression. To obtain the relationship between two parameters, a visual technique was used in that a two-dimensional scatter plot of the measured values was compared with the scatter plot indicated by equation (24). Typical results are shown in Fig. 19. The coefficient λ was adjusted to get a good match and the summation form of equation (24) maintained the median value and range of the total distribution independent of λ.

An alternate method of estimating λ is to evaluate the correlation coefficient[10] for the parameter set $[P_{m_1n}, P_{m_2n}]$ in terms of λ and equate this to the measured correlation coefficient, solving for λ.

6.3.2 *The Nominal Device Parameters*

Returning to the question of the typical transistor, one approach has been to measure the dc properties of a number of devices and take the transistor having median current gain B_N. This device is then completely characterized and its parameter set used as nominal values for the transistor type. This is more meaningful than averaging and goes part way to solving the interdependence problem in that the parameter set is consistent. What it does not do is give any indication

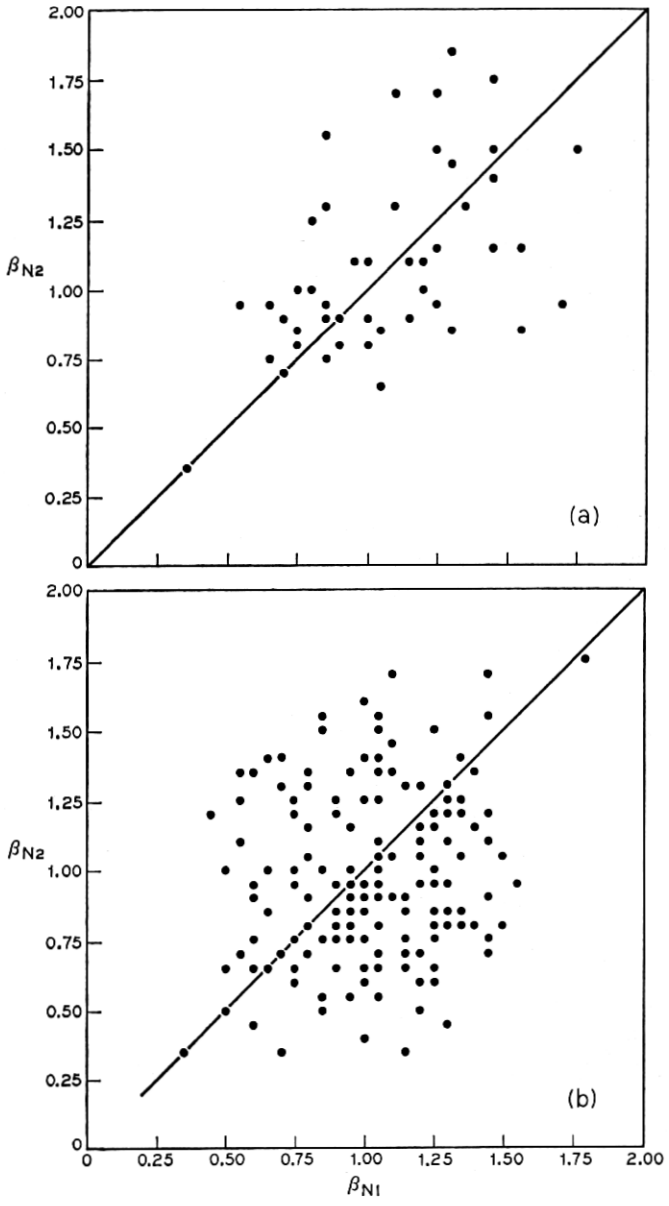

Fig. 19a—Normalized Beta scatter plot measured data.
Fig. 19b—Normalized Beta scatter plot computed data.

of the range of parameter sets to be expected. The technique could be expanded by characterizing the devices having maximum and minimum B_N values, but this would only give an indication of the range for situations where current gain is the controlling parameter. In addition, nonlinear combinations of device parameters may result in a "worst-case" circuit design for other than these types of limit values.

The only realistic solution is to gain some understanding of the transistor parameter combinations and interdependencies and characterize these in the format of equation (24). For a first attempt, it seemed reasonable to assume that the sheet resistance of the active base region would be a fairly basic entity affecting a number of the model parameters. It would certainly affect the current gain B_N and since this is a measurable parameter and one that is very significant in circuit design, B_N was chosen as the base parameter upon which to look for correlation.

6.3.3 *The Behavior of Current Gain β_N*

By equation (12), B_N depends on two coefficients, $\beta_N(I_N, T)$ and V_N. It was shown in Section 3.3.2 that V_N can be regarded as a constant and that variability is attributable to $\beta_N(I_N, T)$.

Figure 20 shows the measured dependence of β_N on current and temperature for the IC transistors used in the *Touch-Tone*® oscillator[17] which suggests a linear dependence on temperature. A good

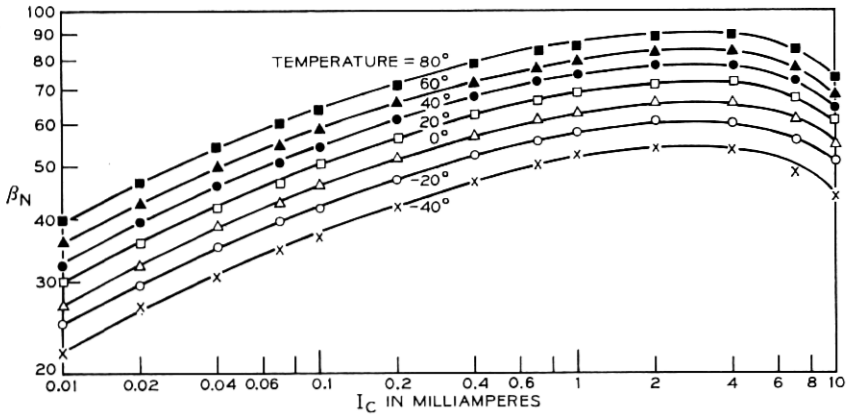

Fig. 20—β_N as a function of I_C and temperature for *Touch-Tone* transistor.

fit for this particular device is shown in Fig. 21 to result from the expression

$$\beta_N(I_N , T) = \beta_{N20}(I_N)[1 + 0.0039(T - 20)] \quad (25)$$

where β_{N20} is the value at 20°C and T is in °C.

The coefficient 0.0039 may well differ for different transistor structures depending on the dominant physical mechanism controlling β_N.

The distribution of values of $\beta_{N20}(I_N)$ to be expected in production results in percentiles shown in Fig. 22. Since the curves are essentially parallel, the same distribution function can be assumed for all current levels. The distribution function is obviously skewed toward the lower values and an important decision relates to the cutoff points for the tails. The lower tail is particularly significant since it is here that most marginal circuits may intuitively be expected to fail. Figure 22 shows that the 10th percentile and 90th percentile occur at 0.667 and 1.667 times the 50th percentile or median value. It seemed reasonable to use a lower limit of 0.2 times the median value and an upper limit of 2 times the median value. The form of the cumulative distribution is then as shown in Fig. 23. This completes the information necessary for the current gain form of equation (24) which is

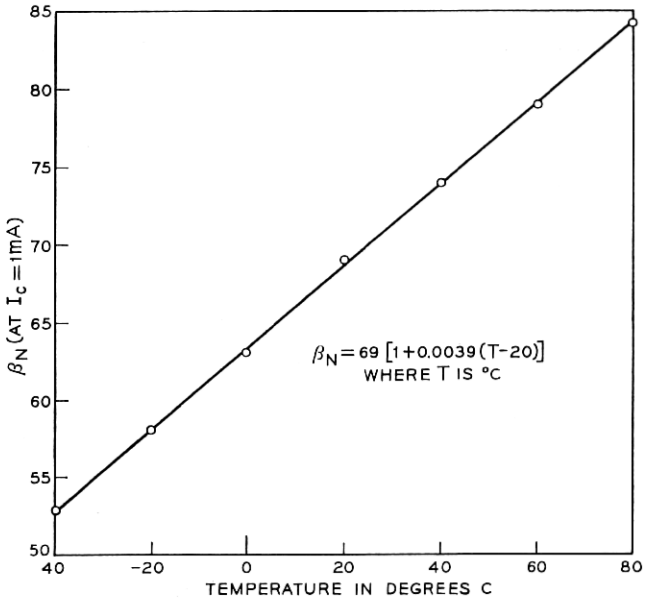

Fig. 21—Temperature variation of β_N for *Touch-Tone* transistor.

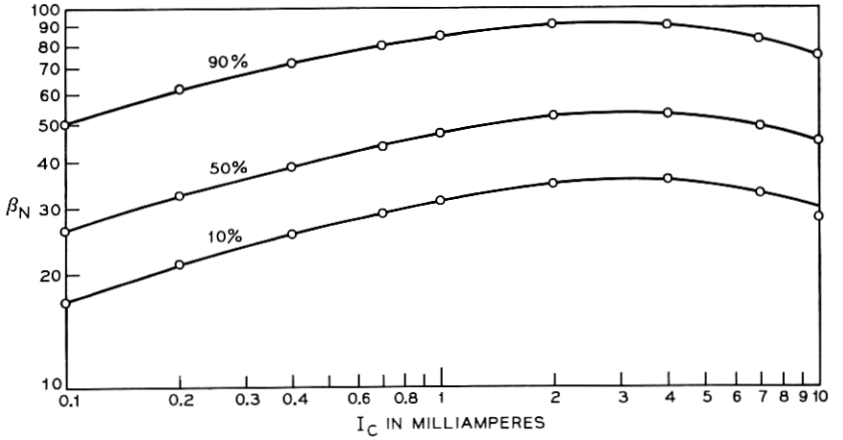

Fig. 22—Percentiles for distribution of β_N.

$$\beta_{Nmn} = \beta_{Non}(I_N, T)[1 + \lambda X_m + (1 - \lambda)X_n] \tag{26}$$

where the terms are as defined for equation (24) and X_m and X_n are selected from the distribution corresponding to Fig. 23, normalized such that the median is zero.

To determine the tracking coefficient λ, the β_N values for pairs of transistors on integrated circuit chips were plotted as shown in Fig. 19a from which $\lambda = 0.3$ was found to give a reasonable "match" as shown in Fig. 19b. This low value of λ means that the current gains for near neighbor transistors have fairly weak interdependence.

The current gain β_I for the inverted mode of operation is handled in the same way as β_N pending further measurements to evaluate the actual behavior of a statistically significant sample.

6.3.4 *The Behavior of Bulk Resistances*

Scatter plots were used to look for dependence of R_B on B_N and Fig. 24 shows an example for the *Touch-Tone* oscillator output transistor.[17] There is obviously, a strong relationship between the two parameters: In fact it almost appears to be a functional dependence. The resistance was measured by the technique outlined in Section 6.2.2 according to equation (19) which gives the clue to one possible interpretation. Equation (19) can be expanded to

$$\begin{aligned} \Delta V_{BE} &= I_B R_B + (B_N + 1) I_B R_E , \\ &= I_B[R_B + (B_N + 1)R_E]. \end{aligned} \tag{27}$$

So

$$R = R_B + (B_N + 1)R_E \,. \tag{28}$$

A technique to separate R_B and R_E can be developed from equation (28). Assume that integrated circuit transistors fabricated on a given slice may be expected to have values of R_B which are quite tightly distributed about some nominal value. Then on a scatter plot of R against B_N ; the "best" straight line drawn through points for devices from one slice will have an intercept which estimates the nominal value of R_B and a slope equal to the value of R_E. The plots in Fig. 24 are for three devices from a "low B_N slice" and two devices from a "high B_N slice." The parallel straight lines indicate a value for R_E of 0.45 ohm in both cases. It is reasonable to regard R_E as a constant since it is primarily a contact resistance and the value is consistent with the small emitter contact area in these devices.

The intercepts indicating the values for the nominal R_B for the two slices show a tracking between R_B and B_N in that devices with high B_N have high R_B . This might be expected from the common dependence on base impurity concentration. Unfortunately, data of the type shown in Fig. 24 on several devices from a number of different slices are not readily available and at this time it is not possible to estimate the

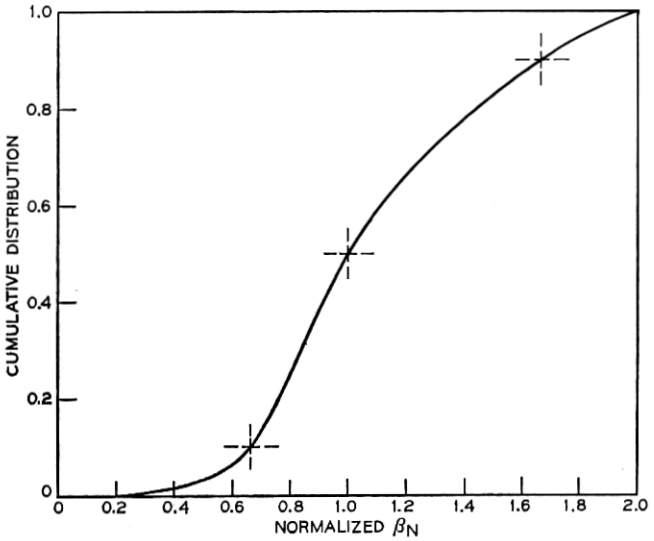

Fig. 23—Distribution for β_N.

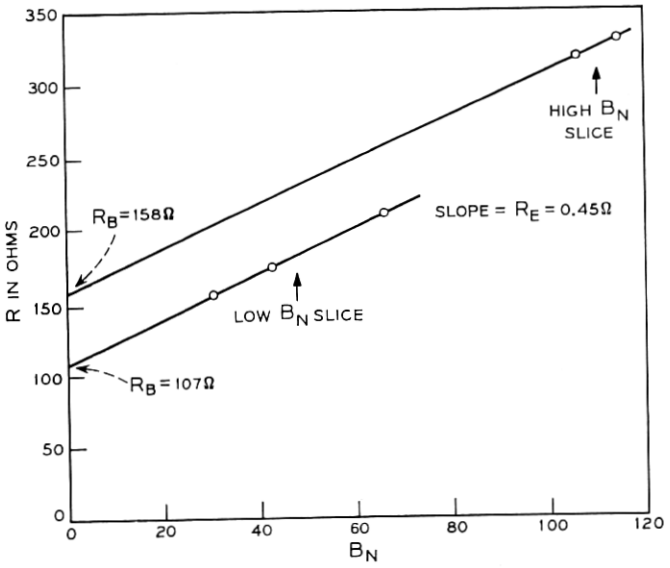

Fig. 24—Scatter plot for R and B_N.

value for the tracking coefficient. Until such information becomes available, it has been customary to treat R_B in exactly the same way as the silicon resistors described in Section 6.3.5.

This technique of resolving R_B and R_E from a scatter plot of R versus B_N requires further comment. First, the interpretation is well suited to statistical work since, as far as R_E is concerned, the regression lines in Fig. 24 perform the averaging required to specify the value to be used for R_E in simulations. Secondly, the loose interdependence of B_N for devices from one slice has been used to advantage since the spread in B_N at a given current level for different devices spreads the points out widely in Fig. 24. As the measurements are made at the same injection level on these devices, conductivity modulation and other second-order effects should not influence R_B, resulting in a realistic estimate for the nominal value of this parameter.

The collector resistance R_C is treated in the manner described in Section 6.3.5 with the appropriate temperature coefficient.

6.3.5 *Silicon Diffused Resistors*

It was expected that diffused resistors on the same chip as transistors would exhibit some correlation with B_N of the transistors because of

the common dependence on the base resistivity under the emitter. It was thought that chips with high B_N would have high resistance values, but in the limited measurement data available it was impossible to determine the nature of any such relationship and, pending further measurements, it was decided to assume independence.

The silicon resistors (base diffusion) are given a gaussian distribution truncated at $\pm 3\sigma$. The maximum total deviation of the resistors is $3\sigma = 15$ percent. The maximum deviation of resistors on one chip is only $3\sigma = \pm 5$ percent. The formula used for computation of resistors is

$$R_{mn} = R_{on}[1 + \alpha(T - T_0)][1 + \lambda X_m + (1 - \lambda)X_n] \tag{29}$$

where X_m and X_n are selected from a gaussian distribution with $3\sigma = \pm 0.15$, $\lambda = 0.667$, and $\alpha = 0.002/°C$ for nominal $200\Omega/\square$ base sheet resistance.

6.3.6 *The Intercept Current I_{ES} and Slope Factor θ_N*

Equation (1) and Fig. 2b give the basis for estimating the parameters I_{ES} and θ_N. Experience with integrated circuit devices has shown that if the junction temperature is known and controlled, then θ_N comes out very close to the theoretical value shown in equation (9). It has therefore been decided to use the theoretical values for θ_N (and θ_I) in simulations and attribute all the variability to I_{ES} (and I_{CS}).

From Fig. 4 and equation (27)

$$V_{BE} = V_{be} + I_B[R_B + (1 + B_N)R_E].$$

At low currents, as shown in Fig. 2b, the measured V_{BE} may be taken as V_{be}. Measurements of this V_{BE} on many devices shows a global distribution which is gaussian with $4\sigma = 36$ mV at 20°C. From equation (1), since $\exp(\theta_N V_{be}) \gg 1$, for transistors at the same current I it follows that

$$I = I_{ESO} \exp(\theta_N V_{beo}) = I_{ES} \exp(\theta_N V_{be})$$

where I_{ESO} is the reference intercept current (nominal value).

If $V_{beo} = V_{be} + \Delta V$, then

$$I_{ES} = I_{ESO} \exp(\theta_N \Delta V) \tag{30}$$

where ΔV is normally distributed with 4σ of 36 mV.

If N has a gaussian distribution with 4σ limits of ± 1, then equation (30) can be transformed to

$$I_{ES} = I_{ESO} K^N \tag{31}$$

where $K = e^{40 \times 0.036} = 4.2$.

The intercept currents are found to be highly correlated for transistors on an integrated circuit and the form of equation (24) for this situation is

$$I_{ESmn} = I_{ESon}(T)K^{[\lambda X_m + [1-\lambda] X_N]}, \tag{32}$$

where

$\lambda = 0.85$,
$K = 4.2$,
X_i = random number with a gaussian distribution truncated at $\pm 4\sigma$ normalized to $4\sigma = 1$.

Equation (32) results in transistors on a chip with V_{BE} match normally distributed with $4\sigma = 5.4$ mV at 20°C.

The temperature dependence of $I_{ES}(T)$ is evaluated from R. J. Widlar's[24] expression for V_{be}

$$V_{be} = \left(1 - \frac{T}{T_0}\right)V_{go} + \frac{T}{T_0} V_{BEO} + \frac{kT}{q} \ln \frac{T_0}{T} + (n - 1) \frac{kT}{q} \left(1 - \frac{T}{T_0}\right), \tag{33}$$

where

V_{go} is the extrapolated energy gap (1.205 for silicon),
n is a constant ($\approx$1.5 for double diffused silicon transistors).

$$V_{BEO} = \frac{kT_0}{q} \ln \frac{I_N}{I_{ES}(T_0)} \tag{34}$$

and $I_{ES}(T_0)$ is the intercept current at reference temperature T_0. When $V_{be} = 0$, $I_N = I_{ES}(T)$, the intercept current at temperature T. Substituting equation (34) in equation (33) for the above condition gives:

$$I_{ES}(T) = I_{ES}(T_0) \frac{T}{T_0} \exp \left[\left(\frac{T}{T_0} - 1\right)\left(\frac{qV_{go}}{kT} + n - 1\right)\right]. \tag{35}$$

This has been found to be in excellent agreement with experimental results. Equations (32) and (35) then give the statistical description for the intercept current including temperature effects.

6.3.7 *The Dynamic Parameters*

The preceding sections have described the techniques used to generate integrated circuit device parameters consistent with available measured data. These results can only be regarded as temporary. Not

only will processing techniques change but it is hoped that, as appropriate measured data become available, interdependencies will be observed which were expected but could not be detected with existing data.

Similar comments apply to the capacitance and characteristic time parameters which are also expected to show some correlation with each other and with other device parameters.

Referring to base resistivity as the controlling variable, it might be expected that base width variations would affect the current gains, the intercept current, the base resistance, and the transit times. Changes in base width arising from variations in emitter diffusion depths affect the profile slopes and hence the junction capacitances. It is not unreasonable, then, to expect some interrelationship at least between B_N, I_{ES}, R_B, T_{CN}, T_{CI} and C_{ej}. The nature of this can only be determined from measurements. C_{cj} on the other hand is determined by the base diffusion rather than the emitter diffusion and may be expected to show no dependence on the base width. Thus C_{cj} may be assumed to be independent of the above six interrelated parameters.

Although the interdependence is not known, the variability of the capacitance parameters is reasonably well documented. The space charge capacitances C_{ej} and C_{cj} are found to have global distributions which are gaussian with 3σ points of ± 20 percent. This figure presumably applies also to the substrate capacitance.

The temperature dependence of the junction capacitance results predominantly from the reduction in contact potential, which implies that temperature changes in capacitance are significant only in forward bias and for low reverse bias voltages. Even at zero applied voltage, the junction capacitance typically changes by ten percent or less over the temperature range—40°C to 80°C. To a first order, such a change can be ignored in comparison with the production variability.

The characteristic time parameters T_{CN} and T_{CI} have not been determined for a large enough sample of any one device type to be able to quote variational bounds at the present time. Likewise, the specific details of the temperature dependence have not been characterized. It is known,[23] however, that both parameters increase with temperature.

VII. CONCLUSIONS

The results of any Monte Carlo study are only as accurate as the characterization of the manufacturing and temperature variations of device model parameters. Thus, the objective in modeling for sta-

tistical design is to give an adequate description of the electrical behavior of devices, consistent with the accuracy of the available parameter data. In general, the availability of parameter data is directly proportional to the ease of measurements and the device model to be favored is one with parameters obtained directly from routine production measurements. The model must be sufficiently simple that parameters can be determined uniquely, since the alternative of optimization to find a "best fit" is impractical for large quantities of data from a production environment.

It was shown for transistors that one of the two forms of model in common use is to be preferred for both measurement simplicity and model accuracy. This model was expanded to account for output resistance by a simple yet efficient technique within the framework of existing computer analysis programs. At that point the important device effects were considered to have been taken into account.

The method of representing the variability of the "dc" model parameters for use in Monte Carlo analysis was outlined, with no pretense to mathematical rigor. Rather, forms were assumed and coefficients estimated such that the calculated parameters, spreads, and correlations "matched" existing measurement data and were consistent with the expectations of device designers. The same approach is being extended to the "dynamic" device parameters such that Monte Carlo techniques can be applied in a meaningful way to computer simulation at higher frequencies.

To determine statistical correlation, it is obviously essential to group measurement data for all parameters related to one device. This is not always possible in production where tests are performed on a go/no-go basis, or statistics on each individual test are recorded rather than data logging the information relating to identifiable devices. In planning for future statistical analysis support, every effort should be made to measure this type of consistent data.

The usual question in sensitivity analysis is to determine those items on which a given design may be particularly dependent. The studies for which the characterization of this article is intended, are sufficiently complicated that the question has to be turned around; given certain parameter spreads and correlations in production, what will be the yield of a circuit design in terms of some performance criteria? This is a very real problem faced in practice and simulation should be able to predict the performance. At the same time, analysis of the results should indicate paths to take to improve any given situation.

It should be noted that all the comments made in this article regarding modeling and characterization for statistical design apply to devices made by the Bell System standard process. Behavior of other devices is expected to be qualitatively the same but obviously the specifics will have to be verified before the techniques are widely applied.

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APPENDIX A

A.1 *Estimation of Incremental Current Gain β from Tabular Data of B_N vs I_N*

For transistors, linear interpolation of B_N as a function of $\ln I_N$ generally gives reasonable estimates of B_N at intermediate values of I_N.

If B_{Ni} and $B_{N(i+1)}$ are the values of current gain at I_{Ni} and $I_{N(i+1)}$ where $I_{Ni} < I_N < I_{N(i+1)}$, then

$$B_N = R + S \ln I_N$$

where R is a constant, and

$$S = [B_{N(i+1)} - B_{Ni}]/\ln (I_{N(i+1)}/I_{Ni}). \tag{36}$$

The incremental current gain is

$$\beta = \frac{dI_N}{dI_B} = \frac{d}{dI_B}(B_N I_B) = B_N + I_B \frac{dB_N}{dI_B},$$

$$= B_N + I_B \frac{d}{dI_N}(R + S \ln I_N) \frac{dI_N}{dI_B}.$$

So

$$\beta = \frac{B_N}{1 - \dfrac{SI_B}{I_N}},$$

$$= \frac{B_N}{1 - \dfrac{S}{B_N}}.$$

APPENDIX B

B.1 *Estimation of* R_{be}

From Section 4.2,

$$\frac{1}{R_{be}} = \frac{dI_B}{dV_{be}} = \frac{d}{dV_{be}}(I_N/B_N),$$

$$= \frac{1}{B_N}\frac{dI_N}{dV_{be}} - \frac{I_N}{(B_N)^2}\frac{dB_N}{dV_{be}},$$

$$\frac{dI_N}{dV_{be}} = \theta_N I_{ES} \exp(\theta_N V_{be}),$$

$$\approx \theta_N I_N .$$

(dB_N/dV_{be}) may be estimated from $(\Delta B_N/\Delta V_{be})$ where,

$$\frac{\Delta B_N}{\Delta V_{be}} = [B_{N(i+1)} - B_{Ni}]/[V_{be(i+1)} - V_{bei}],$$

$$= \theta_N[B_{N(i+1)} - B_{Ni}]/\ln(I_{(i+1)}/I_i),$$

$$= \theta_N S, \qquad \text{where } S \text{ is defined in equation (36).}$$

So

$$\frac{1}{R_{be}} = \frac{\theta_N I_N}{B_N} - \frac{I_N}{(B_N)^2}\theta_N S,$$

$$= \frac{\theta_N I_N}{B_N}\left(1 - \frac{S}{B_N}\right) = \frac{\theta_N I_N}{\beta}.$$

Thus

$$R_{be} = \frac{\beta}{\theta_N I_N}.$$

APPENDIX C

C.1 *Derivation of Output Resistance* R_o

At low frequencies

$$R_0 = \left.\frac{dV_{ce}}{dI_N}\right|_{I_N/B_N = I_B,\ a\ \text{constant}}$$

So

$$I_N = B_N I_B = [\beta_N + V_{cb}/V_N]I_B$$

and

$$\frac{dI_N}{dV_{ce}} = \frac{d}{dV_{ce}}\{[\beta_N + (V_{ce} - V_{be})/V_N]I_B\},$$

$$= \frac{I_B}{V_N}, \quad \text{neglecting any small changes in } V_{be} \text{ which may result from changes in } V_{ce}.$$

So

$$R_0 = \frac{V_N}{I_B},$$

$$= \frac{B_N V_N}{I_N}.$$

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