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Statistical Circuit Design:

Confirmation of Design Using Computer-Controlled Test Sets

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The ability to evaluate the performance of linear network elements used in complex systems is vital to effective optimization and verification of the system design.

Measuring systems controlled by digital computers provide a new capability for linking the steps of network design, breadboard development and characterization, and factory test in such a way that the networks produced will more nearly meet the requirements of the systems in which they are used. This linkage is effected by incorporating in the measuring system the algorithms relating the measured quantities to the system performance parameters used during the design stage.

Output of the system performance parameters in real time provides a powerful aid for debugging development models and a more valid basis for accepting or rejecting product in factory tests. Statistical analysis is used as an aid in setting test limits by evaluating the relationships between component tolerances, measurement errors and the calculated system performance parameter.

I. INTRODUCTION

Communication systems, both analog and digital, often use linear networks to which system performance is highly sensitive. In cases where the relationship between network characteristics and system performance are complex, computers are being increasingly used for network and systems design. Examples of such designs are given in other papers in this issue. The design process is not completed until the design intent is verified, first by measurements of the breadboard models and finally by measurements of the manufactured networks.

When a physical network is to be evaluated, direct measurement of its effect on system performance requires having a system available

as a test instrument. To be a satisfactory test, one would also require that the physical system represent all necessary worst cases. This approach has been used, but it has inherent difficulties such as the difficulty in obtaining a nominal or worst-case system, the difficulty in maintaining the system, and the lack of information on a network that has failed a test.

These difficulties are largely overcome with the test method described in this paper. Using this method, the network is measured on a general purpose test set controlled by a computer. From these measurements of the network, parameters are calculated which predict the performance of the network in a system and which provide direct information about the network. The sections which follow give examples of such tests and the steps necessary to implement the tests and establish their validity.

II. IMPLEMENTATION OF TESTS

With the general purpose computer operated test set, we evaluate the linear network parameters from insertion loss and phase data produced by the network when measured in a suitable connection. In many cases, the linear parameter used for network synthesis can be directly measured. In other cases, a transformation of the insertion loss and phase data is required.[1]

As suggested in the introduction, the relationship between loss and phase measurements and system performance with the network inserted can be quite complex. In fact, examples exist where setting limits on insertion loss and phase (based on component tolerances) rather than system performance causes "good" networks to be rejected and "bad" networks to be accepted. Output of the system performance in real time provides a more valid basis for accepting or rejecting networks in factory tests and provides a powerful aid for debugging breadboard models during development.

What is needed to implement the system performance test then is a computational link between system performance and network loss and phase. Fortunately, this link has essentially been established in those cases where network synthesis, optimization, or tolerance analysis were done on a computer using system performance as the design goal. What remains is to extract the required computation section of the design program, put it on the test set computer, and couple it to the measurement program through a common set of parameters.

After the system performance test is implemented, we must establish

its validity. A lack of exact correspondence between the on-line measurements and actual system performance with the network inserted is caused by:

(*i*) uncertainties in the linear measurement, and
(*ii*) error multiplication in the system parameter calculation.

Uncertainties in the linear measurement are a function of such quantities as test frequency, insertion loss, and measurement averaging time. These uncertainties can be reliably predicted. Errors in the system parameter calculation could in theory be determined by experiment (measurement) but this would be very time consuming and worst-case values would be difficult to obtain. The framework used in the Tolerance Analysis Program is a convenient tool for providing a statistical model of the relationship between measured system performance and actual system performance. This is discussed in more detail in Section V.

The next section will describe, in some detail, the implementation of a test for digital (D2) channel bank filter.

III. D2 CHANNEL BANK FILTER TEST

The D2 Channel Bank is used for time division multiplexing and demultiplexing in a pulse code modulation transmission system.[2] The two filters being tested are linear networks operating in series with a periodically operated switch. In the design stage, filter component values were optimized to meet requirements imposed on the tandem combination of filter and switch, i.e., "switched transfer function." Historically, acceptance of the filter would be based on measurements of insertion loss under continuous excitation. However, computer studies by E. M. Butler[3] point to the possibility of passing bad product (i.e., failed STF test) and rejecting good product (i.e., passed STF test) when using the insertion loss test. Figure 1 shows the results

INSERTION LOSS:	SWITCHED TRANSFER FUNCTION	
	PASS	FAIL
PASS	88.5%	0
FAIL	9.5%	2.0%

2% TOLERANCES

INSERTION LOSS:	SWITCHED TRANSFER FUNCTION	
	PASS	FAIL
PASS	66.5%	1%
FAIL	19.5%	13%

3% TOLERANCES

Fig. 1—Comparisons between switched transfer function and insertion loss tests.

of Butler's studies for the demultiplex filter when all network elements are deviated from nominal with uniform distributions of ±2 percent and ±3 percent. Note that in the 2 percent case, 9.5 percent of the good product fails the insertion loss test. In the 3 percent case, 1 percent of the bad product passes the insertion loss test. Even though the correspondence between the two tests improves for the tighter tolerances actually used in the system, the conclusion is reached that a proper filter acceptance test must be based directly on the switched transfer function (STF).

3.1 *General Approach*

Figure 2 shows the configuration of the switched filters used in the D2 system. Two different approaches are available for calculating the STF of the filters. The state variable method of F. R. Mastromonaco and M. L. Liou[4,5] can give us exact solutions but require exact knowledge of the network topology and element values including all parasitic elements. The other approach, used by W. R. Bennett,[6] C. A. Desoer,[7] T. H. Crowley,[8] M. R. Aaron,[9] and P. E. Fleischer,[10] expresses the STF as a function of z parameters of the network. Z parameters can be easily derived from loss and phase measurements at the terminals of the network. The value of a capacitor in the network is also required, but this too is readily obtained.

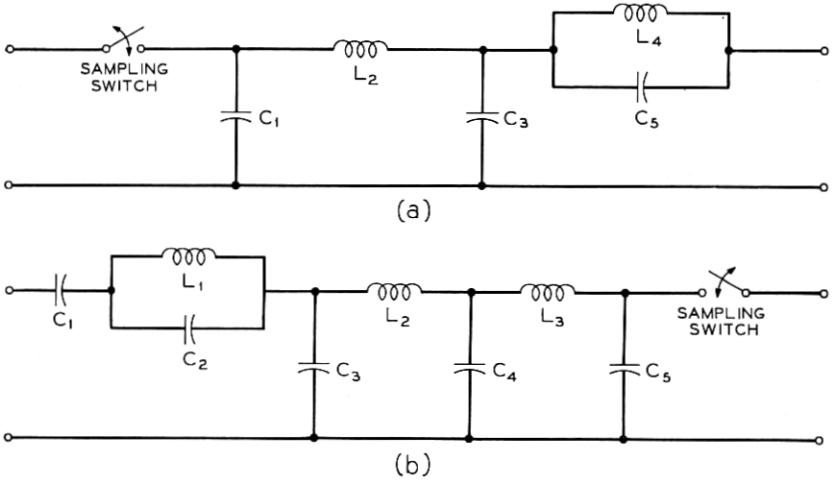

Fig. 2—Switched filters for pulse code modulation transmission system. (a) Demultiplex network. (b) Multiplex network.

The STF of the demultiplex filter, $H_d(j\omega)$, and the STF of the multiplex filter, $H_m(j\omega)$, are expressed by Fleischer as:

$$H_d(j\omega) = \frac{H_m(j\omega)}{\frac{T}{RC}} = \frac{z_{12}(j\omega)}{\frac{T}{2C} + \sum_{k=-\infty}^{+\infty} z_{11}\left(j\omega + jk\frac{2\pi}{T}\right)} \tag{1}$$

where: T = period of switching frequency,
C = input capacitance, and
R = source impedance of multiplexer.

An approximation to the equation above is given by Fleischer as:

$$H_d(j\omega) = \frac{H_m(j\omega)}{\frac{T}{RC}}$$

$$\doteq \frac{z_{12}(j\omega)}{\frac{T}{2C} + \sum_{k=-1}^{+1} z_{11}\left(j\omega + jk\frac{2\pi}{T}\right) + j\frac{0.645T}{\pi C}\left(\frac{\omega T}{2\pi}\right)\left[1+0.127\left(\frac{\omega T}{2\pi}\right)^2\right]}. \tag{2}$$

Since the STF formulation used for the filter test [equation (2)] gives only approximate results, it was important to confirm the accuracy of the approximation. Results from equations (1) and (2) were compared with results of calculations using the state variable method of M. L. Liou. This comparison between the three methods showed a maximum discrepancy of 0.0049 dB in the passband and 0.029 dB in the reject band.

3.2 *Measurement Method*

To perform the calculation indicated by equation (2), three values of z_{11} and one value of z_{12} are required for each frequency at which STF is to be calculated. Referring to Fig. 3 and for the case where $I_2 = 0$,

$$V_1 = z_{11}I_1 ,$$

$$V_2 = z_{12}I_1 .$$

Hence:

$$z_{12} = \frac{V_2}{V_1} z_{11} ,$$

also,

$$\frac{V_1}{E_0} = \frac{z_{11}}{z_{11} + R_1}$$

and

$$z_{11} = R_1 \frac{V_1/E_0}{1 - V_1/E_0}.$$

The value of capacitance C_1 (Fig. 2a) must also be known. This is determined by measuring z_{11} as just described at a frequency where the series inductance L2 is in resonance with its distributed capacity so that the remainder of the circuit is virtually disconnected. At the resonant frequency, ω_r,

$$C_1 = \frac{1}{j\omega_r z_{11}(\omega_r)} = \frac{1 - (V_1/E_0)}{j\omega_r R_1 V_1/E_0}.$$

The measurements of C_1, z_{12}, and z_{11} are implemented by automatically switching a high impedance probe to measure V_1/E_0 and V_2/V_1 at the appropriate frequencies.

3.3 *Validation of STF Test*

The STF test is validated by reviewing the factors contributing to error in the STF measurement and performing tests to gain assurance that the net error is small.

3.3.1 *Determination of Capacitance*

The value of capacitance obtained by measuring $z_{11}(\omega)$ is shown on Fig. 4 together with the values obtained from measurements on an admittance bridge. The discrepancy in the two values was less than 0.2 percent and perturbs the STF by less than 0.008 dB in the passband. The reproducibility of the measurement of C_1 is better than 0.5 percent.

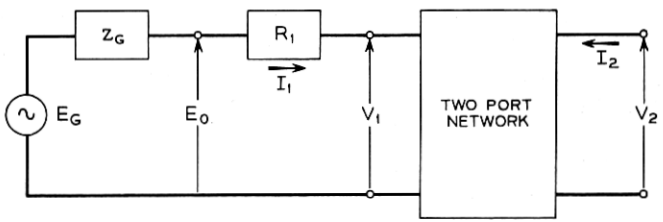

Fig. 3—Basic test configuration.

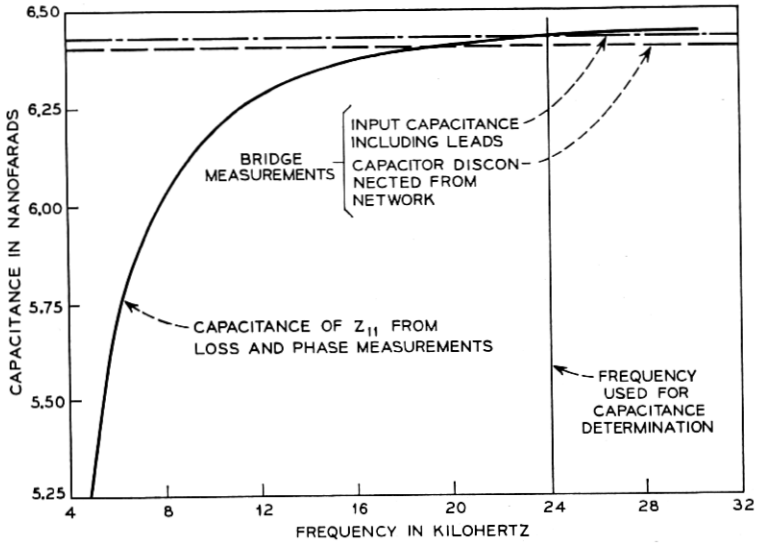

Fig. 4—Determination of filter input capacitance.

3.3.2 *Probe Errors*

After optimizing levels for the best tradeoff between probe noise and linearity, the linearity errors in the probe were measured to be less than 0.01 dB and errors from probe noise were less than 0.1 dB in the STF reject band. Loading errors from the finite probe input impedance were considered and were estimated to introduce less than 0.01 dB error in the STF passband.

3.3.3 *Accuracy of z_{11} and z_{12} Measurements*

Admittance measurements were made on a demultiplex filter using an admittance bridge capable of ± 0.1 percent accuracy. From these measurements z_{11} and z_{12} were evaluated and compared with values obtained from loss and phase measurements and agreement is within 0.4 percent. When bridge measurements are made directly on the individual components of the filter and STF is calculated, the discrepancy with the STF obtained from loss and phase measurements is as large as 0.05 dB in the passband. Much of this difference is due to errors in the circuit model used in calculating z parameters.

3.4 *Sensitivity of STF to Loss and Phase Measurement Errors*

The Tolerance Analysis Program (TAP)[11] was used to determine the "amplification" of measurement errors inherent in the computation of STF from loss and phase data. Figure 5 gives the results for a

demultiplex filter in which errors in each measurement (V_1/E_0, V_2/V_1 in Fig. 3) were assumed to be 0.03 dB and 0.2° with the sign of the error randomly chosen. This run included 17,500 cases and virtually 100 percent of the STF loss values lie within ±0.1 dB of the correct value. We also note that a 0.3 percent error in loss and phase (0.03 dB, 0.2°) has been amplified to a 1 percent error in STF. In a second run, loss and phase errors 1/3 as great produced errors in STF 1/3 as great. Similar results were obtained at other passband frequencies where TAP runs were made. Slightly greater spreads were observed in the filter reject region, but the differences were not significant.

3.5 *Summary of D2 Test*

The STF test on the computer operated test set provides a more valid acceptance test of the D2 multiplex and demultiplex filters than the insertion loss tests commonly used for filters of this type. The STF

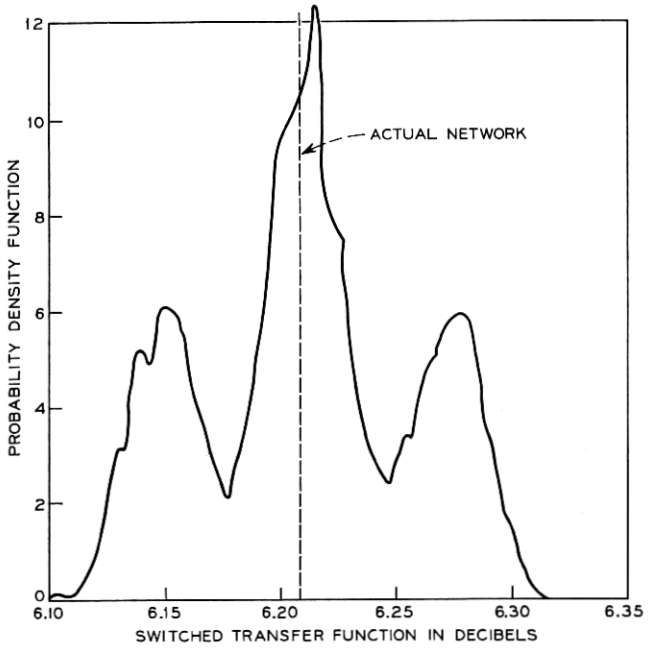

Fig. 5—Distribution of STF loss measurements for 0.3 percent errors in loss and phase. (17,500 samples; measurement error, ±0.03 dB and ±0.2°; frequency, 2.2 kHz.)

is measured with a passband error of less than 0.05 dB and an error of less than 0.2 dB in the reject band. Using computer controlled relays for switching the measuring probe, the STF measurement at 1, 2, 3, 4, and 5 kHz is obtained in 14 seconds.

IV. T2 DIGITAL SYSTEM EQUALIZER TEST

The design evolution of the T2 equalizer is covered elsewhere in this issue.[12] This digital system network provides a potent example of design criteria having a very complex relationship to loss and phase measurements. In the T2 equalizer test used during development, insertion loss and phase measurements were transformed to pulse response, eye opening, and error rate for a system section having varying cable lengths and varying cable temperature. The program to effect this transformation was essentially the same program used for the equalizer design. In the T2 factory test, eye opening was chosen as the test parameter, and the original program was modified somewhat to reduce the program size and running time.

The results of a TAP analysis on the eye opening measurement and some verification by analytical techniques show that, for a nominal network, errors of ± 0.1 percent in loss and phase cause a variation of ± 0.3 percent in the eye pattern. In the test program used, measurement precision is controlled to ± 0.1 percent or better and the eye pattern is evaluated for 3 cases of cable length and temperature in about 1.5 minutes.

V. SETTING LIMITS ON FACTORY TESTS

In the two TAP analyses previously described, the effects of measurement errors on the calculated STF and eye opening were considered for the nominal network only. In the actual factory environment, we also have the statistical variation of the networks themselves resulting from component variations. To establish the limits of acceptance in the factory test, a two-stage TAP analysis is used.

In the first step, network components are varied according to expected statistical distributions and the maximum and minimum of the system performance parameter is determined. The output from this step is the loss and phase values associated with the nominal network and with the networks producing the upper and lower limits of the system performance parameter.

In the second step, 3 TAP runs are made using the appropriate statistical variations in measured loss and phase (these depend on net-

work loss). The output here is three distributions of system performance parameter. Figure 6 gives the results for the D2 demultiplex filter. This analysis provides a model of the distribution of measurements to be expected in the factory with the assumed design and shows the relationship between design limits and test limits. Note that a requirement of 100 percent yield on the network would mean that these limits must lie within the system requirements.

There is one tradeoff that should be mentioned. If one is concerned with a minimum cost network, the cost of testing with higher or lower accuracy must be compared with the cost of decreasing or increasing the component tolerances. Two possible conditions are indicated in Fig. 7.

VI. DISCUSSION AND SUMMARY

In the past, test requirements on networks used in systems have not necessarily been optimum from the standpoint of system per-

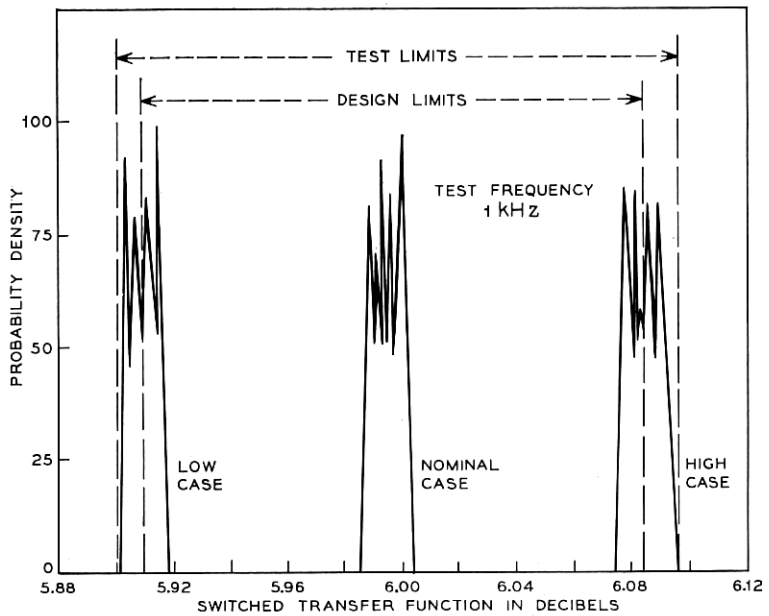

Fig. 6—Distribution of STF loss measurements for D2 filters with lowest loss, nominal loss, and highest loss.

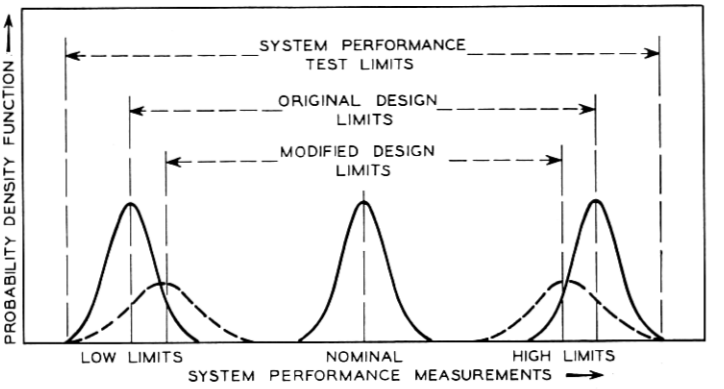

Fig. 7—Relation between measurement accuracy and design limits. (_____ original measurement accuracy; _ _ _ _ lower measurement accuracy.)

formance or network cost. The test requirements have depended on such things as the availability of test equipment and the confidence in the knowledge of relationships between network characteristics and system performance. Analysis tools to determine yield or tradeoffs between component and test costs were not available. If special test equipment was needed, delays for development of test equipment were incurred and development tests and factory tests were often different.

The test method described in this paper provides a flexible and accurate method of evaluating linear networks on general purpose test sets in terms of parameters that are meaningful to the system designer. The approach fits in conveniently with techniques used during the design phase and makes use of software developed in that phase. This makes possible, in cases where the designer and the manufacturer have compatible measuring sets, very rapid startup of factory tests and convenient intercomparison of data. The TAP analysis used to set test set limits provides an analytical tool for use in comparing costs related to components, testing, and yield.

VII. ACKNOWLEDGMENT

The authors are indebted to Mr. E. M. Butler whose work in statistical design techniques pinpointed the shortcomings of insertion loss tests for characterizing switched filters and whose TAP computer program greatly expedited the task of verifying the filter tests described in Section III.

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