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TH-3 Microwave Radio System:

The IF Main Amplifier

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The IF main amplifier is the output amplifier for the TH-3 microwave radio receiver. The amplifier provides a 3- to 49-dB gain range under control of an associated AGC circuit to compensate for radio signal fading. It was designed to operate with a carrier frequency of 70 MHz with extremely flat transmission characteristics over a 53- to 87-MHz band.

I. INTRODUCTION

The TH-3 IF main amplifier* provides an output of +1 dBm and normally operates at a gain of 9 dB. Under control of an AGC circuit, this gain can be increased to 49 dB or decreased to less than 3 dB. The amplifier uses ten silicon transistors in five gain stages and six silicon transistors in the AGC circuit. Figure 1 shows the block schematic of the amplifier. There are five gain stages in tandem to provide the 49-dB maximum gain. The three intermediate stages are variable gain to provide the 46-dB gain range.

The design objective for the amplifier was a flat transmission and delay characteristic over the 53- to 87-MHz band. Gain deviations of less than 0.03 dB and delay deviations of less than 0.2 ns were desired. In order to meet these objectives a basic gain stage was needed having a very stable broadband transmission characteristic. Other desired characteristics were: (*i*) use of feedback to obtain gain stability, (*ii*) automatic gain control capabilities with the use of a single variable element, and (*iii*) negligible interaction between stages to facilitate cascading. The use of transformers was to be avoided due to the variability of ferrites at these frequencies. This basic gain stage could then be used throughout the radio repeater where IF amplification was required.

* This amplifier is also used in current production of transmitter-receiver bays for the TD-3 system.

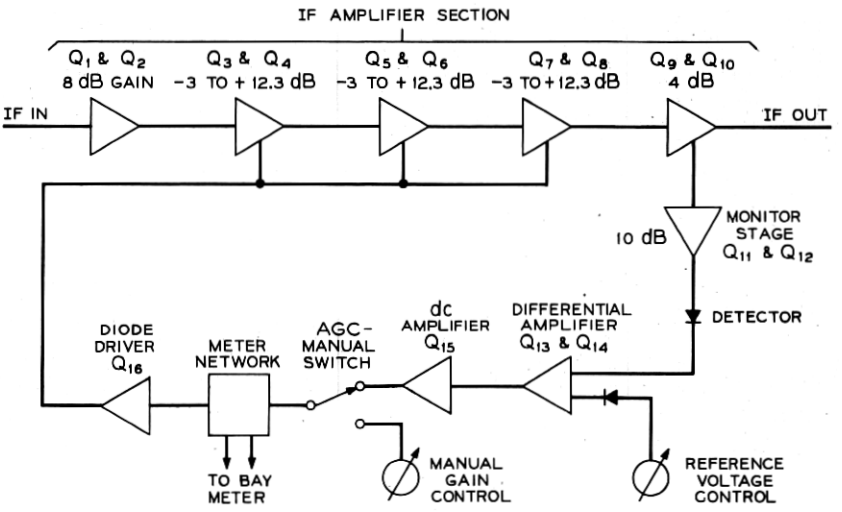

Fig. 1—Block schematic of IF main amplifier.

II. BASIC GAIN STAGE

The basic gain stages developed are shown in Figs. 2 and 3. They are series-shunt feedback pairs having a low input impedance and employing both ac and dc feedback to maintain gain and bias stability. The load may be connected to either the emitter, as shown in Fig. 2, or the collector as shown in Fig. 3. Each connection has a preferred area of usefulness. The emitter-coupled load connection was selected for the IF amplifier section because of its better linearity. The output impedance under this condition is very low due to the shunt feedback. The collector-coupled load connection was selected

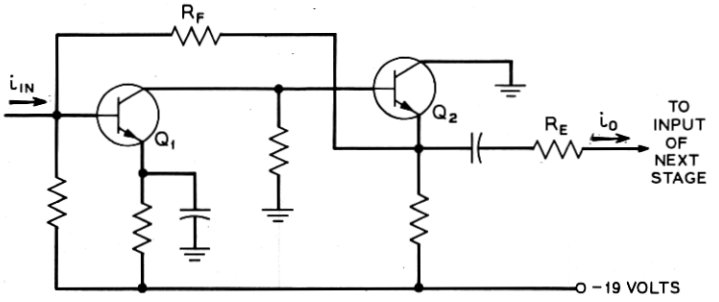

Fig. 2—Emitter-coupled basic gain stage.

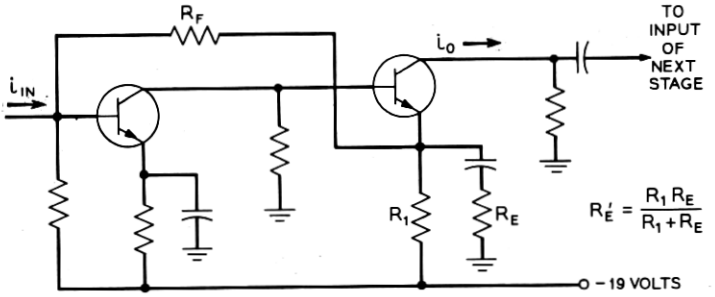

Fig. 3—Collector-coupled basic gain stage.

for the monitor stage because of its greater isolation between input and output. The output impedance under this condition is very large due to the series feedback. Other circuits which use this basic gain stage are the limiter amplifier, the squelch initiator,[1] and the 4A FM terminals.[2]

The transmission response of either the emitter-coupled or the collector-coupled stage is given by a quadratic equation of the form

$$\frac{i_o}{i_{in}} = \frac{k}{s^2 + a_1 s + a_2} \tag{1}$$

where s is complex frequency and k, a_1, and a_2 are constants which depend on the circuit parameters. When $R_F = \infty$, the two open loop poles are real and are located on the negative real axis as shown in Fig. 4. As R_F is decreased the poles move along the axis, finally meet, and then form complex conjugate pairs. Further motion is along a line parallel with the $j\omega$ axis as indicated. When the poles reach points such

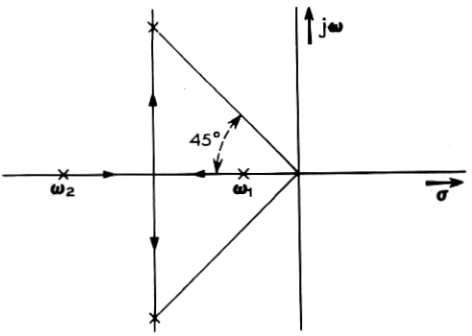

Fig. 4—Root locus plot.

that lines extended to the origin form 45-degree angles with the real axis, a maximally-flat-magnitude response results. If the presence of coupling and bypassing capacitors is ignored, the amplifier is a low-pass structure having a bandwidth equal to the distance between a pole and the origin. For the existing circuit parameters this bandwidth is greater than 200 MHz. Some differences in bandwidth occur between an emitter-coupled and a collector-coupled stage depending on the magnitude of the collector load impedance due to the Miller capacitance effect. These differences, however, are small if the collector load impedance is small, as would be the case in cascaded stages.

Assuming the open-loop gain is large, the closed loop gain for the emitter-coupled stage is

$$\frac{i_o}{i_{in}} = \frac{R_F}{R_E}. \tag{2}$$

Since the collector current contains the shunt feedback current the closed-loop gain for the collector-coupled stage is

$$\frac{i_o}{i_{in}} = 1 + \frac{R_F}{R_E'}. \tag{3}$$

For both circuits R_F is selected for a flat transmission characteristic and R_E is selected for the desired gain. Since the emitter of Q2 is very nearly a zero-impedance point due to the shunt feedback, R_E may be varied without changing the value of the feedback current significantly. This allows variation in gain without affecting the transmission response. R_E may be a fixed resistor for a fixed gain stage or a diode for a voltage-controlled variable gain stage. Thus the basic gain stage has built-in automatic gain control capabilities with the use of a single variable element.

The diode selected for the variable gain stages is the WE474A PIN diode.[3] This diode differs from the standard PN junction diode by a layer of intrinsic silicon between the P and N type silicon. The resistance of the I-layer is controlled by the direct current flowing through it by the process of conductivity modulation, and is independent of the instantaneous variations of the IF signal due to the long transit time and long life time of the injected carriers. Therefore at frequencies above which the junction impedance (which is frequency dependent) is small compared to the I-layer impedance, the PIN diode acts as a frequency independent linear resistance whose value is controlled by the direct current. Figures 5 and 6 show the overall transmission characteristic and the schematic diagram of the

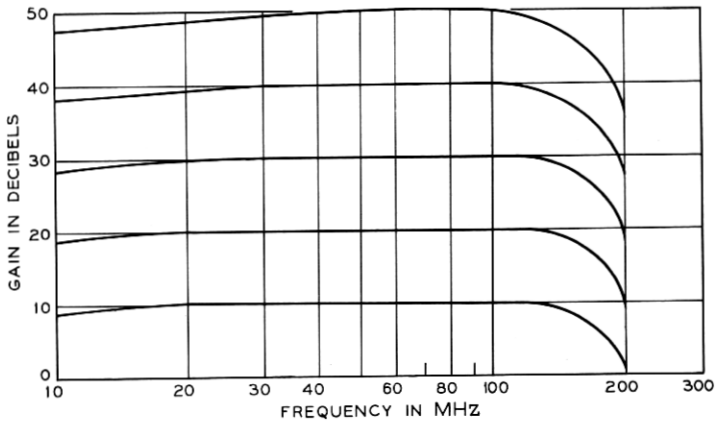

Fig. 5—Transmission characteristic of IF main amplifier.

main amplifier section using the emitter-coupled basic gain stage. Two PIN diodes are used in series for each variable gain stage to minimize the effect of the diode shunt capacitance.

Input and output impedances of 75 ohms are obtained by using a series resistor and shunt capacitor as shown in Fig. 6. The input stage has an additional resistor in series with the capacitor to form a constant resistance network which results in a slightly better return loss. Return losses greater than 30 dB are achieved using this type of matching. Since the emitter impedance of the output stage is fixed by the return loss requirement, the desired gain is obtained by proper selection of the feedback resistor. The value required to obtain 4 dB of gain results in a positive slope across the IF band. An adjustable series R-C network is provided at the input to the stage, as shown in Fig. 6, to correct for this slope and to correct for minor transmission variations in the remainder of the amplifier. With these adjustments the transmission characteristic can be adjusted to be flat within 0.01 dB over the 53- to 87-MHz IF band. The delay is essentially flat (within measuring accuracy of 0.1 ns) over the band with a value of 10.5 ns at normal gain. The delay increases to about 12 ns at 49 dB gain.

The signal levels throughout the amplifier are selected as a compromise between noise figure, AM/PM conversion, and harmonic distortion. For best thermal noise performance the signal levels within the amplifier should be as high as possible. Conversely, AM/PM and harmonic distortion are minimum for low signal levels. For this reason, only a small amount of gain (8 dB) is used ahead of the first variable

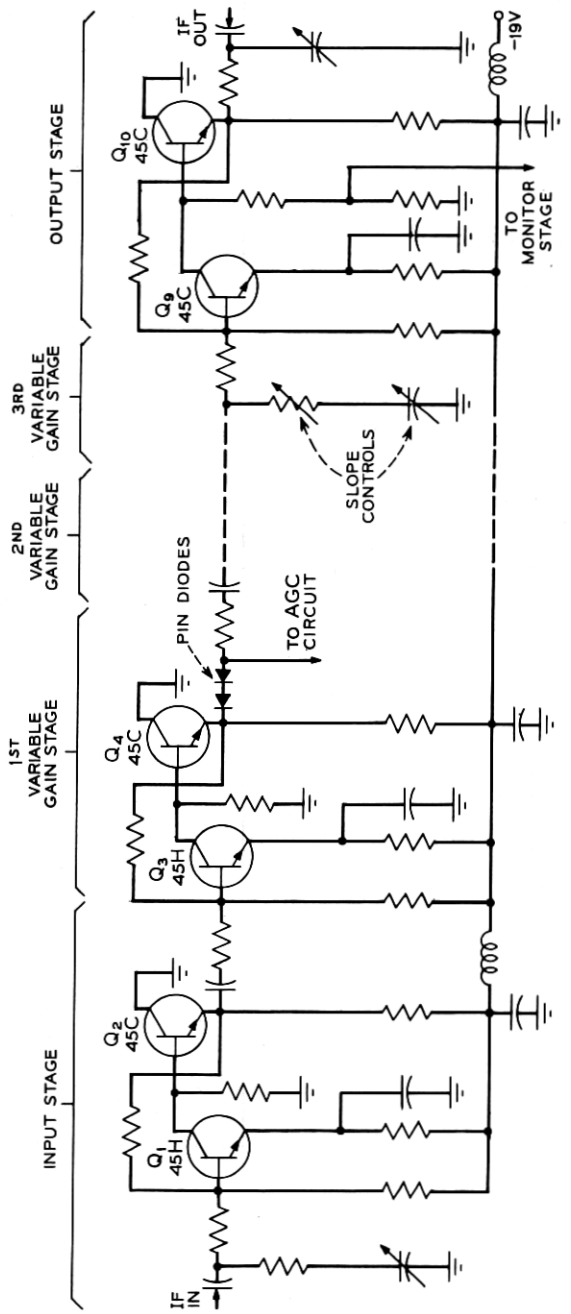

Fig. 6—Schematic of IF amplifier section.

gain stage. This results in an overall noise figure of about 12 dB when the amplifier is operating at normal gain (9 dB). A plot of noise figure versus gain is shown in Fig. 7. Also shown in Fig. 7 is the AM/PM conversion and the second and third harmonic distortion at an output power of +1 dBm. Harmonics cause cross-modulation noise in FM systems by combining in a following nonlinearity to form a delayed fundamental similar to an IF echo. Amplitude modulation, created by previous transmission deviations, causes cross-modulation noise and baseband amplitude distortion when converted to PM by an AM/PM conversion.[4] Design objectives for these parameters were harmonic-to-fundamental power ratios less than −35 dB and AM/PM conversion of less than 0.4 degree/dB measured at normal gain and output power. To meet these objectives for the given signal level conditions, the first and second transistors of each feedback pair were biased at 9 volts, 15 ma and 6 volts, 32 ma respectively.

The 45B, C, and H transistors which are used are part of a family of high-frequency planar, epitaxial, NPN silicon transistors which are characterized by a 1-GHz gain bandwidth product.[3] The 45H is simi-

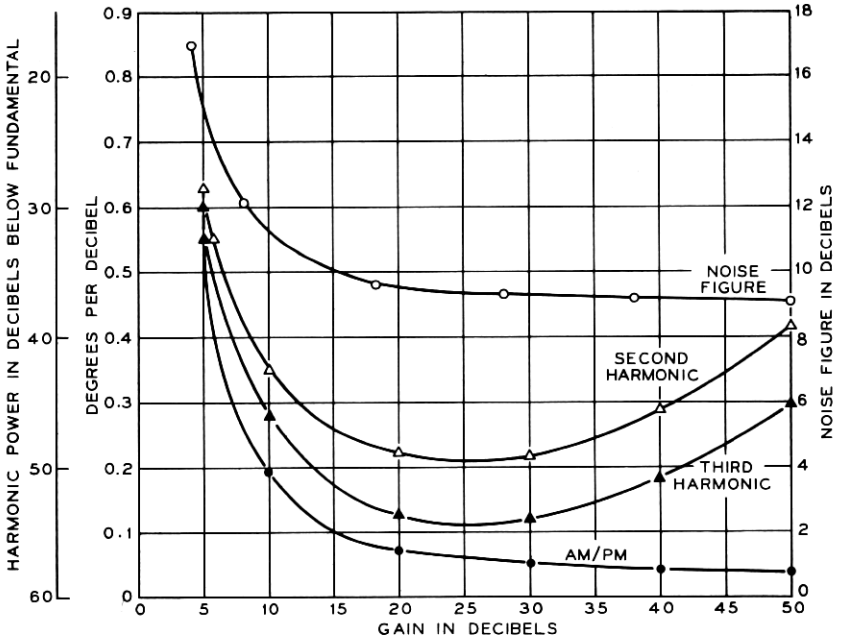

Fig. 7—AM/PM conversion and harmonic distortion of IF main amplifier.

lar to the 45C except for a smaller base resistance which results in a lower noise figure. This transistor is used as the first transistor of the first three feedback pairs to help meet the noise figure objective.

III. AGC CIRCUIT

A schematic of the AGC circuit is shown in Fig. 8. Except for the monitor stage (Q11 and Q12) and the absence of an IF filter, this amplifier is similar to the AGC amplifier described in Ref. 5. The system bandpass filter ahead of the IF main amplifier is relied upon to prevent unwanted tones from affecting the AGC regulation.

The monitor stage is a collector-coupled series-shunt feedback pair. This stage isolates the detector diode from the IF output stage and provides 10 dB of amplification. The IF signal is detected by the detector diode and amplified by a three-stage differential dc amplifier. The IF level control located in the base of Q14 is used to set the output power of the amplifier by adjusting the reference voltage. A diode identical to the detector diode is also used to provide temperature compensation. The metering network at the output of the dc amplifier is used to indicate received signal level. Transistor Q16 provides a high-impedance source with which to drive the PIN diodes. As shown in Fig. 9, the loop gain is large enough to restrict the output level variation over the 40-dB fade range to 0.5 dB. Switch S1 opens the dc feedback loop to allow manual gain adjustment for sweep testing purposes.

Figure 10 shows a photograph of the main amplifier and AGC circuit housed in an aluminum casting, $1\frac{1}{2} \times 2\frac{1}{2} \times 20$ inches.* Three separate printed circuit boards are used for the IF amplifier, AGC circuit and meter network, and supply voltage filter.

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* The mechanical design was done by R. M. Wheatley.

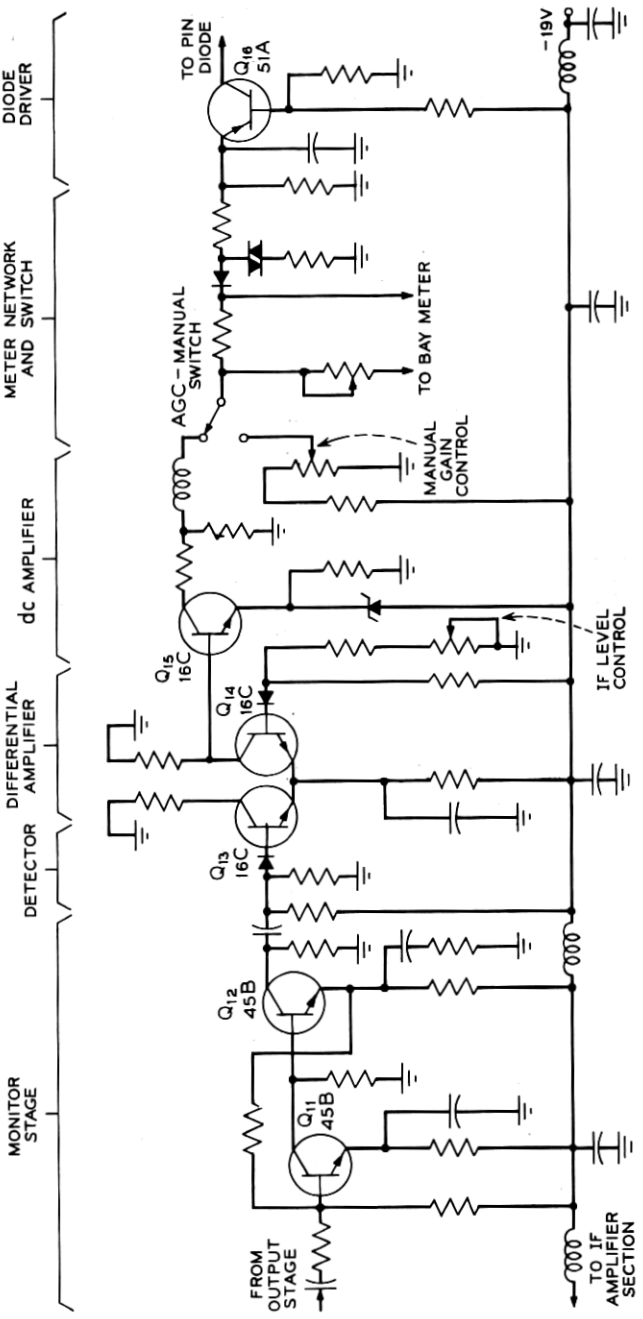

Fig. 8—Schematic of AGC circuit.

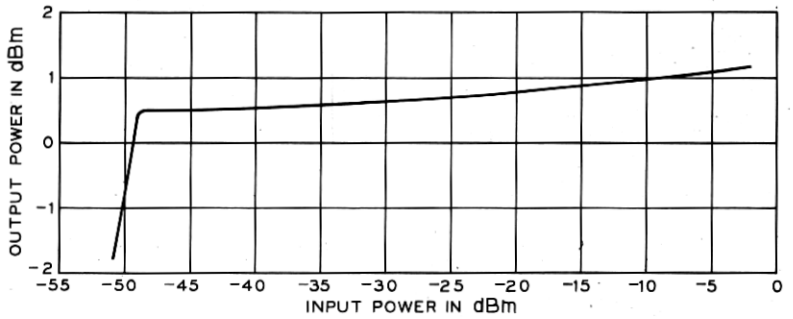

Fig. 9—AGC regulation of IF main amplifier.

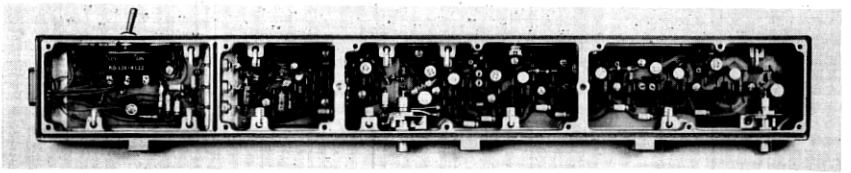

Fig. 10—IF main amplifier.