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Fabrication and Performance Considerations of Charge-Transfer Dynamic Shift Registers

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Two similar dynamic shift register schemes have recently been proposed, the insulated-gate-field-effect transistor (IGFET) version of the bucket-brigade register and the charge-coupled device (CCD). These charge-transfer dynamic shift registers show great promise for many digital and analog applications because of their small size and simplicity. In this paper the fabrication, performance, and drive characteristics of the registers are considered in detail to bring out common and comparative capabilities, the discussion being supplemented with presently available experimental data. In order to be specific in comparing the two devices, we assume 10-micrometer metallization tolerances and emphasize digital rather than analog operation of the registers. In addition, a refractory gate technology with two levels of metallization has been assumed so that the devices can be compared using similar technologies. With respect to the common capabilities, it is found that the registers have several significant advantages over other existing shift register schemes—a minimum of processing steps leading to areas of under 3 mil^2 per bit, with the possibility of areas down to 1.1 mil^2 per bit using a refractory gate technology; operation up to frequencies of 10 MHz p-channel or 50 MHz n-channel; and power requirements under 5 μW per bit at a clock frequency of 1 MHz, power varying approximately linearly with clock frequency. From a comparative point of view, it is found that the charge-coupled device and the IGFET bucket brigade are so similar that area limitations, voltage, current, and power requirements, and high- and low-frequency operating limitations arise from the same mechanisms and hence are essentially the same within less than a factor of two. There appear to be only two major differences. First, the fabrication requirements are somewhat different. The CCD requires no diffusions in its active region and may be less sensitive to mask realignment when two levels of metallization are available. However,

under the restrictions of a single level of metallization and 10 μm tolerances, only bucket-brigade registers have presently been successfully fabricated. Second, at intermediate frequencies of operation both registers are capable of transfer efficiencies in excess of 99.9 percent. The residual inefficiency in the bucket-brigade register is due to the nonzero IGFET dynamic drain conductance; the CCD has no analogous limitation so its intermediate frequency performance, limited only by interface state trapping of mobile carriers, has the potential for more efficient charge transfer.

I. INTRODUCTION

There has been a renewed interest recently in the use of charge storage on p-n junctions or capacitors for memory and shift register applications.[1-3] Because leakage currents gradually degrade the stored information, the memories require periodic refreshing, but the simplicity, speed, small size, and modest power requirements of many schemes and their compatibility with silicon technology can often offset the disadvantage of the regeneration requirement. This class of memories can be divided into two general groups—those which are designed for random access, and those which are inherently dynamic shift registers and can only be accessed serially. This article is particularly concerned with the dynamic shift register.

Several dynamic shift registers have been proposed which use charge storage on metal-oxide semiconductor (MOS) capacitors[3-6] and at least one of these is presently available commerically.[6] Two of the most promising are the CCD first described by Boyle and Smith,[3] and the IGFET bucket-brigade shift register reported by Sangster and Teer.[4,5] These two register schemes are similar in many respects, and we shall refer to both of them as charge-transfer shift registers. The purpose of this paper is to describe in detail the operation, fabrication, and performance of these two MOS charge-transfer shift registers, with particular emphasis on digital applications, and to bring out both their similarities and differences. In order to provide a basis for comparison, we assume 10 μm metallization photolithographic tolerances. It should be recognized that such an assumption, while it simplifies the comparison, greatly restricts the possible fabrication schemes. Hence our results and conclusions may change if a different set of ground rules is defined, and care must be taken in extrapolating the results to improved or different fabrication capabilities.

In the next section, a qualitative description of charge-transfer shift register operation is given, and the points where the two registers differ are identified; in the third section, the fabrication requirements

and techniques are outlined and the ultimate size limitations described; in the fourth section, some experimental and theoretical results on performance limitations are discussed; and in the final section the common and comparative capabilities of charge-transfer shift registers are summarized.

II. DESCRIPTION OF CHARGE-TRANSFER SHIFT REGISTERS

This description of the two dynamic charge-transfer shift registers the IGFET bucket brigade and the CCD, will proceed for convenience on the assumption that both devices are fabricated on n-type silicon substrates. Both operate on the basic principle of moving holes from position to position along the silicon surface by making the potential of the forward position more negative (hence attractive to holes) while the trailing position is made less negative. The devices differ in the mechanisms used to establish unidirectional information transfer, and this difference is reflected in the device construction.

The bucket-brigade concept has been described by Janssen[7] and by Hannan, et al.,[8] and the operation of the IGFET version has been described by Sangster[5] and by Berglund and Boll.[9] By its nature, the bucket brigade is a two-phase device although extension to multiphase operation is straightforward. This means that each element or half-bit has an asymmetry which insures that propagation will occur only in the forward direction. In the MOS bucket brigade, the half-bit consists of a p-region covered with SiO_2 and coupled capacitatively to a metal clock electrode which is arranged to induce a field-effect transistor (FET) channel between the p-region and that associated with the preceding half-bit. The structure which will accomplish this is diagrammed in Fig. 1 which shows a four-bit MOS bucket-brigade shift register. The two-phase clocking is accomplished by driving all the odd gates with a periodic signal $\varphi_1(t)$ and the evens with $\varphi_2(t)$; these signals are ordinarily the same but displaced in time by one-half period.

The unloaded state of the bucket brigade is that state where all the p-islands are strongly reverse biased with respect to the substrate; this means they have a deficiency of holes. A signal would be introduced by adding some holes to the first p-island, and this reduces its negative potential. Information transfer is effected by driving φ_2 to a negative value and at the same time driving φ_1 toward a more positive potential. The p-island coupled to φ_2 now becomes the drain of an IGFET which has its channel coupled to the φ_2 gate, and the p-island coupled to φ_1 is the source. If the source is carrying some signal charge, a channel will be induced between the two p-islands, and the charge will flow

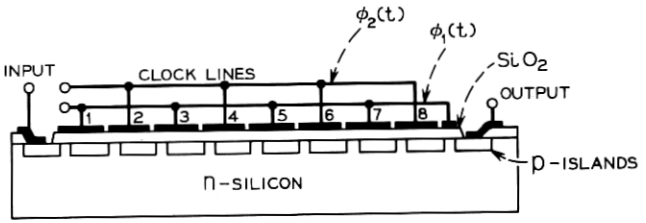

Fig. 1—Simple four-bit IGFET bucket-brigade shift register.

forward into the drain until the potential on the source p-island is reduced to the point where the difference between the source voltage and the gate voltage equals the threshold voltage; then there is no more channel. As clock signals φ_1 and φ_2 reverse their phases, the *evens* become sources and the *odds* drains, and the entire cycle is repeated. By this means, information is advanced two p-islands (one bit) for each cycle of the clock. Transfer in the reverse direction does not occur because the voltage on the gate over the channel is always more positive than the voltage on the p-island capacitatively coupled to that gate, so that the reverse channel never turns on.

The CCD concept was first described by Boyle and Smith.[3] The device consists of a series of MOS capacitors placed very close together and driven by two, three, or more clock signals. In its unloaded state, all the capacitors are driven into deep depletion (a transient state) and no minority carriers are present at the surface. Information would be represented as a controlled number of minority carriers trapped under one or more of the plates. In its simplest realization, diagrammed in Fig. 2, three electrodes are used per bit, and the device is driven by three sequential periodic signals $\varphi_1(t)$, $\varphi_2(t)$, and $\varphi_3(t)$. In this case the holes representing a signal would be injected into the device when the first phase is most negative, and the holes are trapped under the first electrode. Transfer is effected when φ_2 becomes more negative than φ_1 ; then the holes move from the first electrode to the second by a combination of drift and diffusion. The sequential application of the clock potentials moves the information through the device, and reverse transfer does not occur because φ_1 , φ_2 , and φ_3 occur in a sequence which assures that when the electrode ahead of the charge is becoming more negative, the one behind is becoming more positive. Thus, the electrostatic attraction is always in the forward direction.

If two-phase drive is desired for CCD operation, the simple structure shown in Fig. 2 will not suffice. The charge transfer mechanism has no inherent directionality, so each half-bit must be designed to inhibit

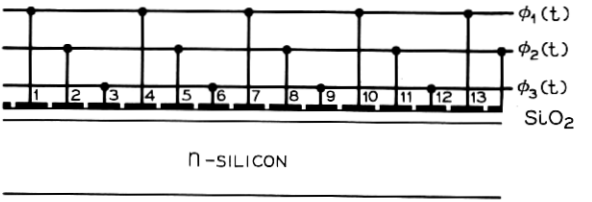

Fig. 2—Simple three-phase charge-coupled device.

propagation in the reverse direction. This can be achieved, for example, by arranging a periodic alteration in the channel threshold voltage—such as by using two different oxide thicknesses, or two different doping levels at the surface.[10] Such devices will be described in the next section.

III. FABRICATION CONSIDERATIONS

3.1 *IGFET Bucket Brigade*

3.1.1 *Description*

The basic steps required for fabrication of an IGFET bucket-brigade shift register (two-phase) using conventional diffusion and metallization technology are listed in Table I and illustrated by the cutaway view

TABLE I—TWO TYPES OF BUCKET-BRIGADE FABRICATION

Bucket-Brigade Elements (Regenerator Elements)	Conventional Processing	Refractory Gate Processing
1. Field Oxide (~1 μm)	Oxidation Photomasking Etching	Oxidation Photomasking Etching
2. Diffused Islands (Sources and Drains)	Photomasking Etching Diffusion	
3. Gate Insulation	Oxidation CVD Insulator	Oxidation CVD Insulator (Optional)
4. Refractory Metallization	No	Deposition from Chemical Vapor Deposition of Insulator Photomasking Etching Diffusion (Ion Implantation Optional)
5. Refractory Gate Definition (Gates)	No	
6. Sealing Insulation	No	Sputtered or CVD Insulator
7. Contact Holes	Photomasking Etching	Photomasking Etching
8. Metallization	Evaporation Photomasking Plating (Optional) Etching	Evaporation Photomasking Plating (Optional) Etching

in Fig. 3. An experimental register chip fabricated this way is shown in Fig. 4.[9] There are no critical steps or photolithography tolerances beyond those normally encountered in IGFET processing. Apart from input and output, the operation of the register is self-compensating for variations in IGFET threshold,[9] and since somewhat heavier channel doping than for most IGFET applications will normally be used, the register should have less stringent requirements on stability, interface state density, and reproducibility than other IGFET circuits.

For comparison to CCD registers, it is also of interest to examine the fabrication of an IGFET bucket-brigade shift register assuming that a refractory gate (either silicon or refractory metal) technology is available. The basic fabrication steps in this case are also listed in Table I assuming silicon gates as a specific example, and they can be followed by referring to the cutaway view in Fig. 5. Even though bucket-brigade registers can be fabricated without a two-level metallization, the fabricational advantages of such a technology should be emphasized at this point. First, a self-aligned gate is achieved so that undesirable capacitance from one gate to the preceding p-island is minimized without a critical alignment step; second, the p-islands are also self-aligned with respect to the thin oxide; third, a second level of metallization is available for associated circuitry on the chip; and finally, these advantages are all achieved with, at most, an increase of only one mask, depending on the particular fabrication scheme.

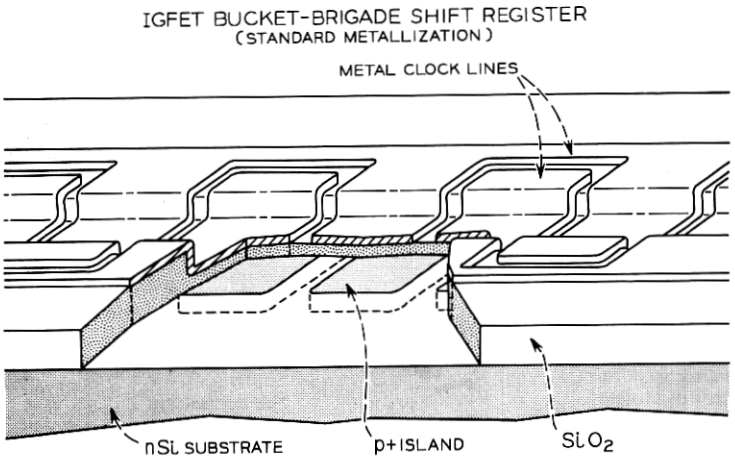

Fig. 3—Cutaway view of integrated bucket-brigade register—standard metallization.

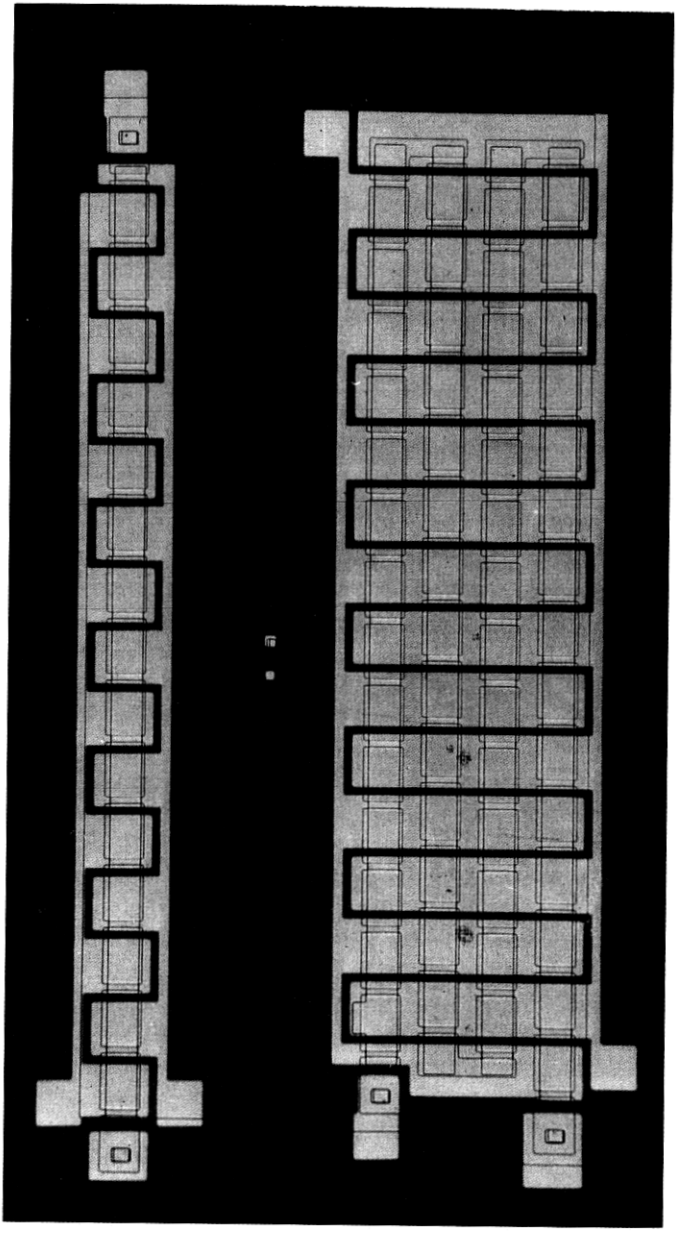

Fig. 4—Photograph of experimental bucket-brigade register chip showing an 8-bit string and a 31-bit string. Metal clock lines are approximately 3 mils wide.

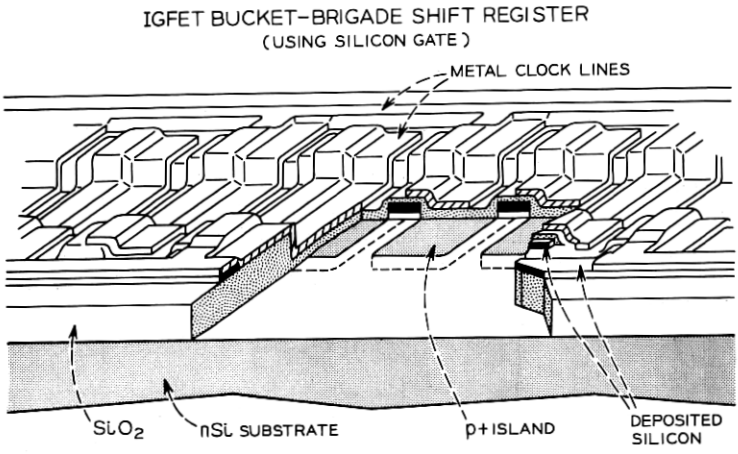

Fig. 5—Cutaway view of integrated bucket-brigade register—silicon gate technology.

3.1.2 *Shift Register Size and Tolerance Limitations*

In the shift register fabrication which we have described, we have restricted ourselves to the basic processing steps and ignored the extra steps associated with channel-stop diffusions, second insulator deposition, and beam-lead processing which may be necessary for any particular application. These have not been included because of the large number of alternatives available to the designer. Similarly, we have not discussed input, regeneration, and output circuitry and their compatibility with the register, including any restriction they may place on the geometry, operating voltages, and minimum charge that must be transferred (i.e., minimum size of the shift register). For these reasons, an estimate of the minimum area per bit in the register obtained only from the basic processing steps restricted by photolithographic tolerances will be somewhat optimistic. Nevertheless, such an estimate does provide a basis for comparison of similar shift register schemes, and it is some measure of processing simplicity.

In this paper we shall estimate the minimum shift register area by arbitrarily assuming the following tolerances in the device fabrication: minimum metallization etching tolerance, 10 μm; mask realignment tolerance, 4 μm; and minimum oxide etching tolerance, 7.5 μm. Under these restrictions, an IGFET bucket-brigade register fabricated using standard metallization according to Table I must have a length per bit (along the direction of charge transfer) which corresponds to two p-islands and two IGFET gates. The gates can be 7.5 μm long, but

the p-islands must be large enough to allow a 4 μm metal overlap with the preceding metal gate, 10 μm metallization spacing, and at least 18 μm for the intentional overlap capacitance. This last figure is derived from the requirement that the desired overlap must exceed the unavoidable overlap with the previous p-island even under worst case misalignment. Hence, the minimum bit length for such a shift register is 79 μm. The width of each bit must include p-regions of at least 15.5 μm, 8 μm due to mask realignment, and 7.5 μm for the oxide etch tolerance, plus an additional 7.5 μm for spacing between adjacent shift register strings. Hence, the minimum bit width is 23 μm and the minimum bit area is 1.8×10^3 square micrometers (2.8 mils^2).

If we now assume the register is to be fabricated using refractory gate technology according to Table I and Fig. 5, the minimum length per bit will include two 10 μm self-aligned gates, and two p-islands, each of which must include 4 μm for spacing between the metallization and the silicon gate and a minimum of 10 μm for p-island overlap capacitance. This gives a total bit length of 48 μm. The minimum width per bit, however, is not as easily calculated when using refractory gates since it is determined by the nature of the signal flow in a shift register array. Figure 6 illustrates two principal types of signal flow—parallel and serpentine. In parallel flow, the signal in every string moves in the same direction as might be useful, for example, in a multichannel or multiplexed register or in an imaging device. The serpentine signal flow is that type of flow which will be most prevalent in digital circulating memory applications. Here, the signal reverses itself from left to right as it goes through the array (Fig. 4). For parallel flow, the minimum bit width will be simply two oxide etch tolerances 15 μm,

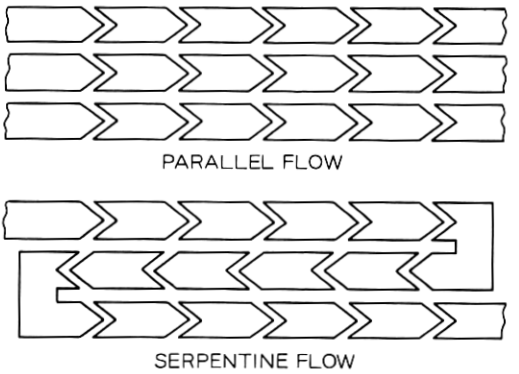

Fig. 6—Illustration of shift register layout for serpentine or parallel signal flow.

one for the p-island and one for the spacing to the next string. Hence, the minimum bit area will be 0.72×10^3 square micrometers (1.1 mils^2). However, for serpentine flow the refractory gate lines and metal lines must crisscross from string to string and additional area will be required. For example, even if the gate length is increased from 10 μm to 14 μm, photolithographic tolerances can only be maintained using a p-island width of 7.5 μm as before but increasing the spacing between strings to 10 μm. Under these conditions the minimum bit length will be 56 μm and minimum bit width will be 17.5 μm for a minimum bit area of 0.98×10^3 square microns (1.5 mils^2). An illustration of the layouts for two-phase arrays for both serpentine and parallel flow using refractory gates is shown in Fig. 7.

3.2 *Charge-Coupled Device*

3.2.1 *Description*

While the conceptual charge-coupled device, a series of MOS capacitors, would appear from its elegant simplicity to be easy to fabricate, there are a number of complicating factors which alter this conclusion. First, for digital applications, it is virtually a necessity to include diffused regions and associated contact holes either for the input, output, and regeneration, or because of the polyphase clock requirement. The eight-bit register of Tompsett, Amelio, and Smith[11] is representative of this simplest class of device, fabricated using conventional metallization techniques. Because it is a three-phase register, it has been necessary to provide diffused crossunders at the expense of area and complexity. This fabrication approach is also limited because the thin channel oxide is exposed, thus making the device performance prone to gross alterations of its operating characteristics when ionic contamination reaches this sensitive surface. The simple expedient of subsequent passivating insulator deposition over the device may reduce the device performance instabilities, but in many cases this will not be a satisfactory solution. Even if the instability were eliminated, experimental and theoretical studies[12] indicate that while CCD operation is possible with wide gaps between metal plates, best operation, particularly with p-channel, is normally achieved when the gaps are smaller than approximately three micrometers, a spacing smaller than the allowable photolithographic tolerances that we have assumed.

In the long run the best fabrication procedure will probably involve the use of two levels of metallization such as that available from re-

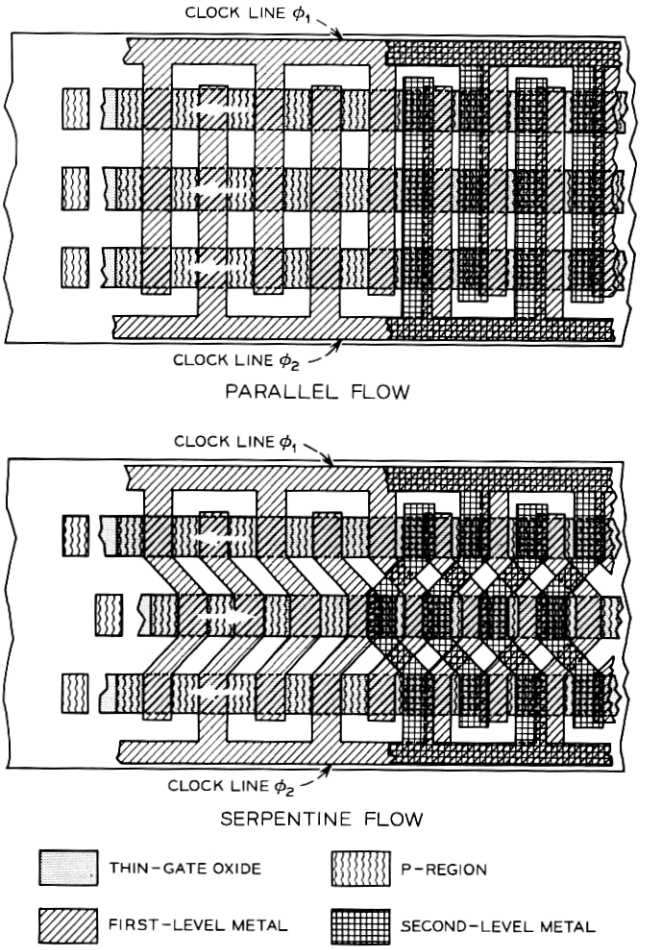

Fig. 7—Layout for serpentine and parallel flow arrays assuming a two-level metal technology for a bucket brigade.

fractory gate technology since the problem of the spacing between adjacent plates can be solved without requiring more stringent photolithographic tolerances. Within this context, it is natural to make two-phase or four-phase[13] rather than three-phase devices primarily because of the difficulty in laying out serpentine signal flow in three-phase. Four-phase CCD's may have some performance advantages and be more versatile, while two-phase registers may be smaller and easier to lay out in arrays. In this article we restrict ourselves to CCD's

made using two-level metallization and we ignore schemes for fabricating CCD's using conventional metallization. Figure 8 is a sectional drawing of a multilevel CCD. It is clear that the problems associated with the gaps between adjacent capacitor plates has been eliminated because the gaps are reduced to the oxide thickness; further, the channel is entirely sealed by metallization to prevent ionic contamination of the oxide. For two-phase operation, directionality may be incorporated in the half-bits by providing two levels of oxide thickness, or by differential surface doping.[10]

Conventional CCD operation will be most efficient when the silicon substrate doping is relatively light. This is in contrast to the relatively heavy channel doping required for the IGFET bucket-brigade register. As a result, it may be necessary to provide channel-stop doping to inhibit the inversion of the surface outside the CCD channel.

3.2.2 *Shift Register Size and Tolerance Limitations*

For comparison with Fig. 7, arrays with serpentine and parallel layouts of two- or four-phase CCD's using refractory gate technology according to Table II are shown in Fig. 9. An estimate of minimum bit size will be obtained only for these registers for comparison to the IGFET bucket-brigade registers.

Applying the same fabrication tolerances as previously described, the minimum length per bit must include four metallization tolerances

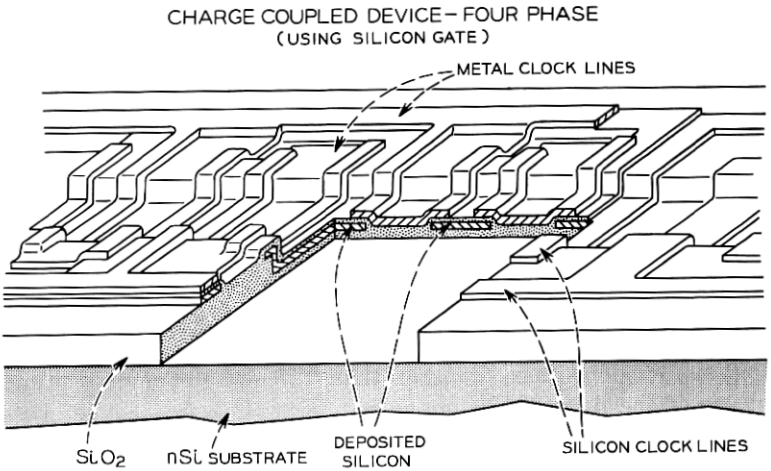

Fig. 8—Sectional drawing of a multilevel charge-coupled device.

TABLE II—REFRACTORY GATE PROCESSING OF CHARGE-COUPLED DEVICES

CCD Elements (Regenerator Elements)	Processing
1. Field Oxide	Oxidation Photomasking Etching
2. Gate Insulation	Oxidation CVD Insulators (Optional)
3. Refractory Metallization	Deposition from Chemical Vapor Deposition of Insulator
4. Input and Output Diffusions (Sources and Drains)	Photomasking Etching Diffusion (Ion Implantation Optional)
5. Refractory CCD Plates Definition (Gates)	Photomasking Etching
6. Sealing Insulation	Oxidation CVD Insulator Optional
7. Contact Holes	Photomasking Etching
8. Metallization	Evaporation Photomasking Plating (Optional) Etching

for a total of 40 μm. However, because of the overlap requirement between the two metallization levels, the refractory metallization must be increased by two realignment tolerances per half-bit, or a total of 16 μm. For two-phase operation, then, the minimum bit length will be 56 μm, and for four-phase operation where the plates would usually be the same size, the minimum bit length will be 72 μm. For parallel strings, the minimum bit width will be the same as for the IGFET bucket-brigade register, 15 μm. Hence, the minimum bit area of a CCD will be 0.84×10^3 square microns (1.3 mils^2) and 1.08×10^3 square microns (1.7 mils^2) for two- and four-phase operation respectively. For serpentine arrays, there again must be an increase in area per bit because of the crisscrossing of the two metallization levels. While there are several compromises available, for comparison with the bucket-brigade register we will increase the minimum length per bit on the CCD to allow the same minimum width of 17.5 μm for the serpentine array. This requires an increase in bit length to 76 μm for the two-phase register and 92 μm for the four-phase register. Hence, for serpentine signal flow the minimum CCD bit area will be 1.33×10^3 square microns (2.0 mils^2) and 1.61×10^3 square microns (2.5 mils^2) for two- and four-phase operation respectively.

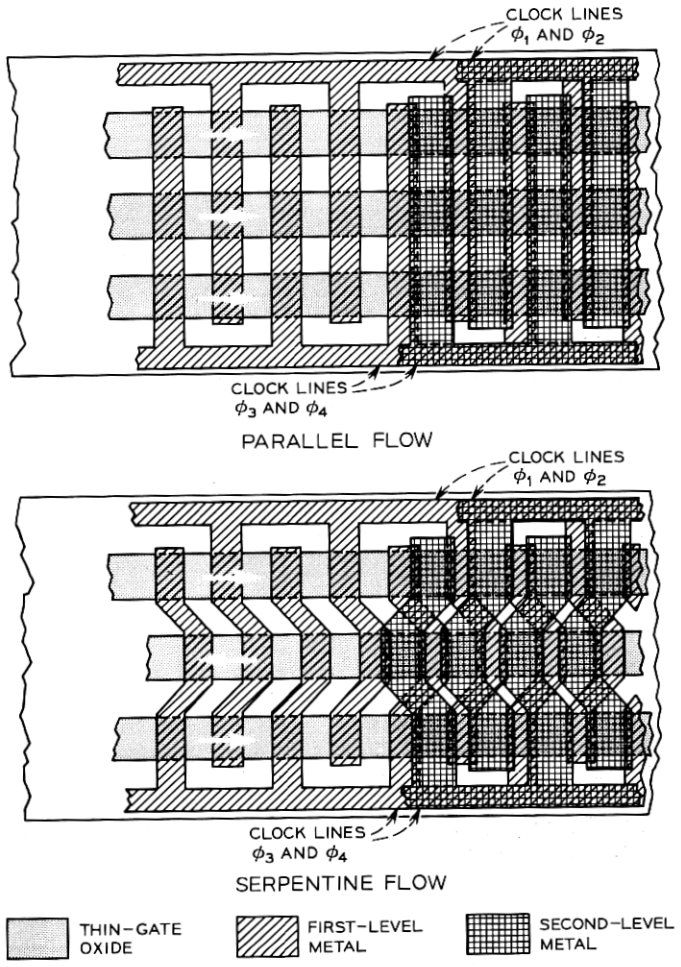

Fig. 9—Layout for serpentine and parallel flow arrays assuming a two-level metal technology for charge-coupled devices.

3.3 *Regeneration and Output Circuitry*

When a shift register is to be used for digital applications, periodic regeneration of the pulses will be required. This will be the case even if the shift register has a perfect transfer characteristic because of generation currents in the reverse-biased p-islands of the IGFET bucket-brigade register or in the depletion layers of the CCD. Regeneration of the pulse train can, in principle, be accomplished off the

chip if a sufficiently low leakage current and high transfer efficiency can be achieved so that hundreds of bits can be allowed before regeneration. However, in general the charge transferred in a register is so small that some amplification and output circuitry is always required on the chip in order to obtain usable impedance and signal levels off the chip. Since the processing steps necessary for regeneration are the same as those required for this amplification and output circuitry, there will often be no fabricational advantage to attempting regeneration off the chip. If this is the case, the extra area required to put regenerators every 10 bits, for example, rather than every 100 bits may be negligible when considered together with the improved margins and less severe performance requirements that accompany more closely spaced regenerators. Depending on the complexity of the regenerator, some compromise spacing will be found, and it will probably be of the order of 5 to 50 bits.

Since for digital applications some output circuitry will always be required on the chip and regenerators may be required every 5 to 50 bits, the compatibility between the extra circuitry and the basic shift register properties and fabrication requirements may become rather important. For example, because of the shift register simplicity, the fabrication steps required for the basic register may be a subset of the steps required for the output and regeneration circuitry. In this case, the fabrication complexity of the output and regeneration circuitry would determine the fabrication complexity of the register chip. Similarly, the speed of the regenerator or output circuit may be the important limitation to the speed of the register operation, and the minimum signal required to drive the regenerator or output circuitry may provide a more important limitation to the size of the register than photolithography tolerances. In this way, it is possible that the output and regeneration circuitry could provide important factors in determining many of the fabricational and operational limitations of charge-transfer shift registers.

IV. SHIFT REGISTER PERFORMANCE

The performance of both the bucket brigade and the charge-coupled device as shift registers must be described in terms of two rather different but interrelated properties, signal transmission and drive requirements. It will be shown that the signal degradation properties of these registers depend very strongly on signal amplitude, and as a consequence, device performance is invariably enhanced if information is represented by rather large quantities of charge and by assuming that all cells are

never totally devoid of charge during operation. The charge-carrying ability of a register is roughly proportional to the drive voltage. On the other hand, the drive power increases with the drive voltage. Hence, there will always be a close link between signal transmission characteristics and drive power.

While the practical limitations to overall performance of a register may often be determined by the input, regeneration, and output circuitry, the inherent limitations of the register itself are of great importance. These must arise from the characteristics of the step-by-step charge transfer operation within the register. In each step the charge is moved forward by one element, but invariably some of the charge lags behind. This effect will always provide a limit to the number of bits in a register before unacceptable signal degradation occurs. The less time available for charge transfer, as at increased clock frequencies, the more charge is left behind in each transfer. Ultimately this will result in a high-frequency limitation to shift register operation for any given number of bits.

At low frequencies, another limitation arises. Generation centers in the depleted regions of the semiconductor and states at the interface give rise to thermal generation currents; and these tend to fill the potential wells which have been intentionally left partially empty. This provides a general shift to higher charge levels in all bits and will eventually lead to unacceptable signal degradation as the register begins to be overloaded. Depending on the temperature of operation, generation currents will thus impose a low frequency limit for operation.

To simplify the discussion which follows, the important charge transfer and drive characteristics of the bucket brigade and charge-coupled device will be discussed separately but in a parallel fashion. Then those general characteristics which are common to the two registers, such as low-frequency limitations and waveform and signal level effects, will be described. The discussion of signal transmission characteristics of charge transfer shift registers, however, is complicated not only by the fact that the signal degradation is extremely nonlinear but also by the fact that the amount of degradation depends on the nature of the signal;[14] i.e., in a digital context it depends on the bit sequence. This means that the exact relationship between the performance of a given shift register and the charge transfer characteristics of each stage is very complex. One approach to simplifying this problem is to linearize the transfer characteristics by making a small-signal approximation.[14] In this way an estimate of the dependence of shift register performance on the nature of the signal can be made in terms

of an incomplete transfer parameter characteristic of each stage of charge transfer.[14,15] Another approach is to assume a worst case situation, a signal which is an alternating series of ONE's and ZERO's, and assume the fractional signal degradation of all stages in the register is the same as that of the first stage.[16] In this way the nonlinearity of the incomplete transfer can be illustrated by varying the magnitudes of the ONE and the ZERO. Both approaches will be used here, but it should be emphasized that both are approximations and are intended only to give an indication of the limitations of charge transfer shift registers.

In the paragraphs that follow, for convenience, the particular devices analyzed theoretically will be those cited as the minimum size devices in the previous section; and they both assume the same design rules and a two-level metallization technology. Because the field of charge-transfer devices is still evolving, some of the theoretical expressions represent approximations which are in the process of being refined. Consequently, the estimated performance represents, in each case, the application of the best theoretical work currently in hand. These best estimates will be subject to further refinement both by improved analysis and subsequent experimental work.

4.1 *Bucket-Brigade Performance*

4.1.1 *Transfer Characteristics*

It is possible to consider the operation of the bucket brigade as a sequence of capacitor discharges, where the discharging current path is an insulated gate field effect transistor with finite nonlinear transconductance, and the current sink is another identical capacitor C. Using this approach, Berglund and Boll have determined the charge Q_r left behind in the course of a single transfer, assuming a square-wave drive.[9] The result is an algebraic function of the signal level and transfer time t:

$$\frac{V_r}{V_i} = \frac{1}{1 + KV_i t}, \tag{1}$$

where V_i is the voltage associated with the initial charge Q_i stored in the capacitor C, V_r is the voltage associated with Q_r, Q_r/C, and K is a normalizing factor which is a function of device parameters and capacitance C. The behavior of V_r for two specific signal levels, V_i of 2 volts and 10 volts, is shown in Fig. 10 where time has been arbitrarily normalized in units of K^{-1}. Note that for times beyond $t' = 1$, the

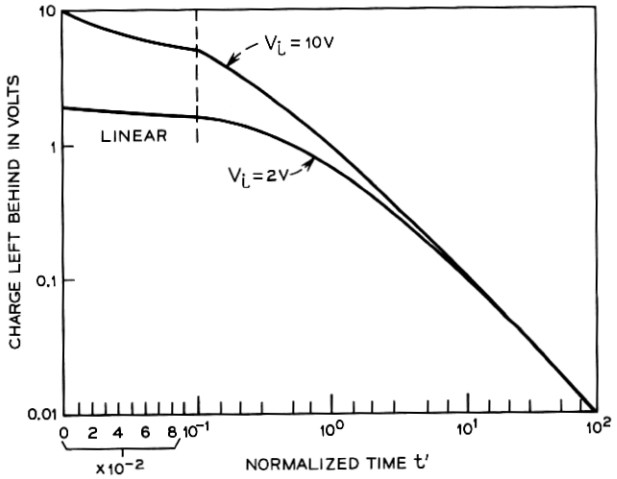

Fig. 10—Charge remaining on a bucket-brigade capacitor versus normalized time for two initial values of charge.

amount of charge remaining, V_r , becomes relatively independent of the initial charge. For this reason signal degradation should be reduced by assuring that relatively large quantities of charge are always transferring through the register.[9]

This effect can be made more evident by defining a large signal digital degradation factor Γ. This is the fractional change in the difference between an adjacent ONE and ZERO in a sequence of alternating ONE's and ZERO's on transferring through the first stage of a shift register.

$$\Gamma = 2p \frac{(Q_{r1} - Q_{r0})}{(Q_{i1} - Q_{i0})}. \tag{2}$$

The factor 2 comes from the fact that the charge lost by a ONE is added to the ZERO, and the p, representing the number of phases in the register, is the number of charge transfers per stage. Figure 11 shows the variation of Γ with the ratio Q_0/Q_1 for a register with the previously described minimum dimensions operating at 10 MHz. The abscissa is the ratio of the amplitude of a ZERO to that of a ONE, keeping the ONE constant at 5 volts, and curves are presented for n-channel (mobility, μ = 500 cm^2/V-sec) and p-channel (μ = 150 cm^2/V-sec) devices. Three points are evident from this plot. First is the advantage gained by having the higher mobility of n-channel devices (at large values of Q_0 , Γ varies approximately as μ^{-2}); second

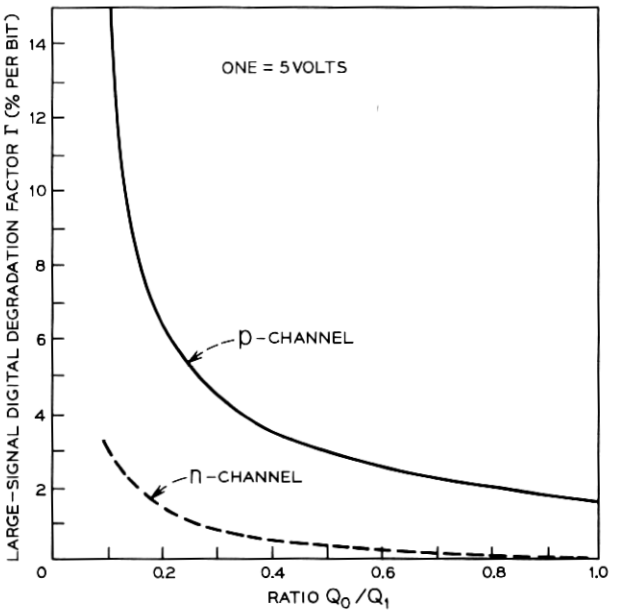

Fig. 11—Variation of signal degradation with size of the ZERO in a bucket brigade.

is the steady diminution of Γ with increasing size of the ZERO; third is the tendency for Γ to decrease less rapidly as the size of the ZERO increases.

Several other features of charge transfer in bucket-brigade shift registers can be conveniently illustrated by using the small-signal incomplete transfer parameter α defined by Berglund.[14]

$$\alpha = \frac{dQ_r}{dQ_i}. \tag{3}$$

This is the differential charge left behind after a single transfer due to a differential change in the charge being transferred. Thornber[17] has proposed that since α is usually quite small, the various contributions to incomplete transfer can be described by writing

$$\alpha = \frac{\partial Q_r}{\partial Q_i} + \sum_i \frac{\partial Q_r}{\partial X_i}\frac{dX_i}{dQ_i}. \tag{4}$$

In this expression, X_i might be any one of the parameters associated with the transfer, like the times of initiation and completion of transfer or the channel length, which had been assumed constant in calculating Q_r but which in fact depends somewhat on Q_i .

The first term in equation (4) is the intrinsic term α_i and has been analyzed by Berglund and Boll[9] for square-wave clock drive and by Thornber[17] for arbitrary clock waveform. Thornber concludes that this term can be made exponentially small with respect to the sum of the terms in equation (4) provided that the quantity (Cf_c/AV_a) is much smaller than unity. In this expression, C is the capacitance in which the signal charge is stored (typically it will consist primarily of the metal gate overlap with the p-islands, but it will also include the effects of gate-to-channel capacitance and the p-island-to-substrate capacitance), f_c is the clock frequency, V_a can be considered to a first approximation to be the voltage associated with the average signal charge $Q_a(Q_a \cong CV_a)$, and A is the parameter which relates drain current I_D to source-gate voltage V_{SG} in an ideal IGFET through

$$I_D = A(V_{SG} - V_T)^2, \tag{5}$$

where V_T is the IGFET threshold voltage. Figure 12 illustrates the clock frequency dependence of the intrinsic contribution to incomplete transfer, α_i , by the dashed lines as calculated by Thornber for the specific case of sine-wave drive. In this calculation the previously described minimum dimensions and a signal voltage V_a of 5 volts have been assumed. Note that this contribution to the total α represented

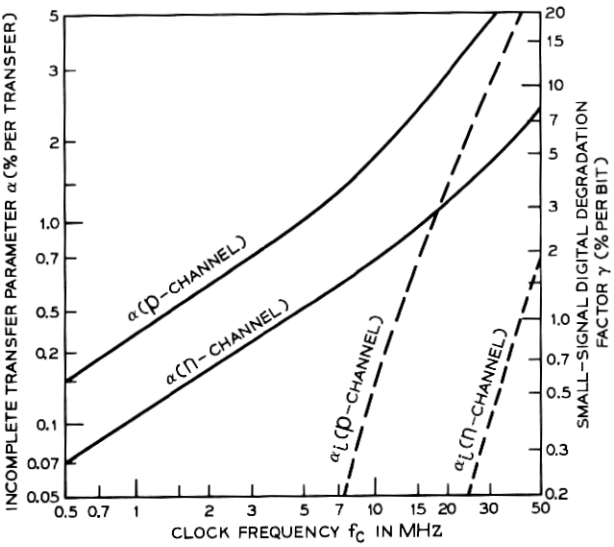

Fig. 12—Theoretical incomplete transfer parameter versus clock frequency for minimum size bucket-brigade shift register.

by the solid lines is modest even to frequencies as high as 50 MHz, and decreases exponentially as the frequency decreases.

In the previous discussion, it was pointed out that α_i varies exponentially with the quantity Cf_c/AV_a . In all other analyses performed to date on incomplete transfer including that leading to Fig. 10, the clock frequency always appears in the product Cf_c/AV where the voltage V is a voltage associated with the signal or drive level, or some combination of the two. Since the signal and the drive voltages are typically within a factor of two, it is useful to define the quantity C/AV_a as the characteristic bucket-brigade time constant τ_B . Also, since AV_a is the IGFET transconductance at a source-gate bias of $V_a/2$, τ_B is the time constant for charging the capacitor C through the IGFET transconductance at source-gate bias $V_a/2$. Alternately, for comparison to charge-coupled devices, τ_B can be written in terms of geometrical and materials properties as

$$\tau_B = \frac{L_G L_O}{\mu V_a}, \tag{6}$$

where μ is the field effect mobility, L_G is the channel length, and L_O is the effective gate overlap length defined as that required to make the overlap oxide capacitance equal to C. Because of the contributions of gate and p-island capacitances, L_O will always be somewhat larger than the actual overlap.

As α_i decreases with decreasing clock frequencies, other contributions to α begin to dominate. One of the most important terms in equation (4) has been found to be that associated with the IGFET dynamic drain conductance.[9,17] Since the transfer characteristic is dependent not only on the source-to-gate voltage but also weakly on the drain voltage, and since the drain voltage depends on the charge transferred, nonzero dynamic drain conductance introduces an additional dependence of Q_r on Q_i . Assuming that this effect is entirely due to channel length modulation, Thornber has calculated this contribution to α, α_D , for sinusoidal clock waveform, and his results can be sumsumarized by the approximate expression

$$\alpha_D \cong \frac{0.3}{L_G} (f_c \tau_B)^{\frac{2}{3}} \left(\frac{V_a}{N_c}\right)^{\frac{1}{3}}, \tag{7}$$

where L_G is the channel length in microns, V_a is the signal voltage in volts, and N_c is the channel doping density in units of 10^{16} cm^{-3}. This contribution has been included in Fig. 12 to yield the solid curves assuming N_c equal to 10^{16} cm^{-3}.

It should be noted that if the actual dependence of τ_B on L_G is included in equation (7), there is an optimum channel-length-to-overlap-length ratio which minimizes α_D . Depending on channel doping, this minimum is rather broad and is centered approximately near L_G equal to the actual overlap length. The minimum value of α_D decreases as L_G decreases.

Interface states in the channel region also make a contribution to α. However, they typically add less than 0.1 percent even when the interface state density is in the 10^{11} states/cm^2-eV range and nonoptimum clock waveforms are assumed. For this reason and because interface state effects will be described in detail in the section on charge-coupled devices, no additional discussion will be included here.

While experimental data on bucket-brigade registers is relatively sparse, most of the qualitative features of incomplete transfer described above have been experimentally observed. The large signal effects illustrated in Fig. 11 have been demonstrated using a register constructed from discrete components, and experimental data from integrated registers in the 1 to 10 MHz range have verified the frequency, clock waveform, and voltage magnitude effects predicted in the discussion of equation (4). Figure 13 shows measured values of α as a function of clock frequency for a register using a distorted trapezoidal waveform. Also included for comparison are theoretical curves for the dimensions and device parameters used assuming sine and ideal trapezoidal clock waveforms. Over the measured frequency range, the channel length modulation effect dominates α and can be seen to explain both the approximate magnitudes and the frequency dependence of the data. Additional measurements on registers in which the channel doping was intentionally increased have verified that α_D is the major contribution to α under most conditions. By such a technique it appears that values of α smaller than 10^{-3} at 1 MHz can be achieved. Figure 14 shows the measured dependence of α at 1 MHz on the amplitude of the clock waveform for a signal level chosen to give optimum results. The main features of the experimental data are quite accurately reproduced; namely, the rapid increase in α at the smaller clock voltages as the intrinsic contribution to α becomes important, and the tendency for the measured α to saturate at higher clock voltages as the dynamic drain conductance term dominates. While the data indicate that shift register operation at frequencies up to and exceeding 10 MHz with α less than 0.01 should be easily attainable, it is possible that other terms in equation (4) not considered here may become important as the frequency increases. For this reason no estimate of the ultimate

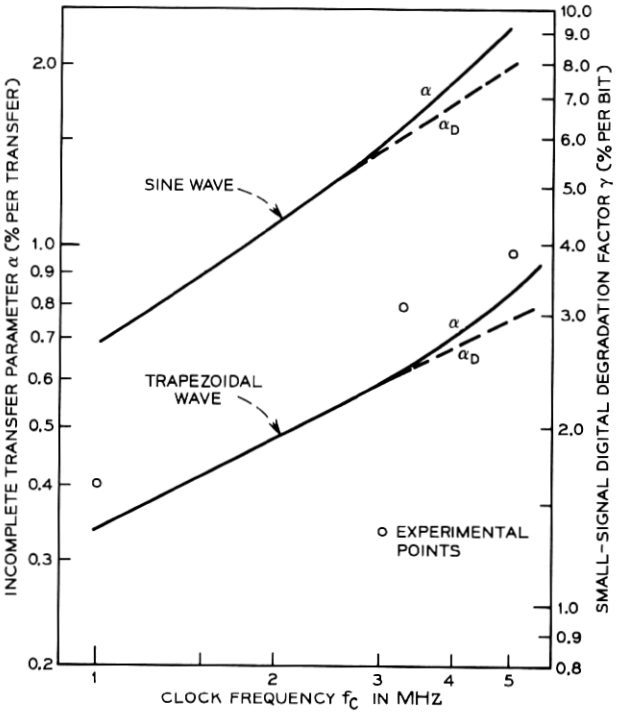

Fig. 13—Comparison of experimental and theoretical incomplete transfer parameter as a function of clock frequency for a bucket brigade.

high-frequency limit for IGFET bucket-brigade operation is available.

4.1.2 *Drive Characteristics*

The drive characteristics of a bucket-brigade register must include the voltage and current requirements on the clock power supply and the power dissipated on the chip. These characteristics are all clock waveform dependent, and hence difficult to describe exactly for the general case. However, clock power supply requirements of major interest are the peak values of current and voltage rather than the detailed time dependences, and these peak values as well as the power dissipated on the chip can be estimated in a relatively simple way. The clock waveform effects will be discussed in a separate section.

The minimum voltage levels required by the IGFET bucket-brigade shift register and the relationship between these voltages and the maximum charge that can be transferred have been briefly discussed by Berglund and Boll.[9] The values are best illustrated by assuming

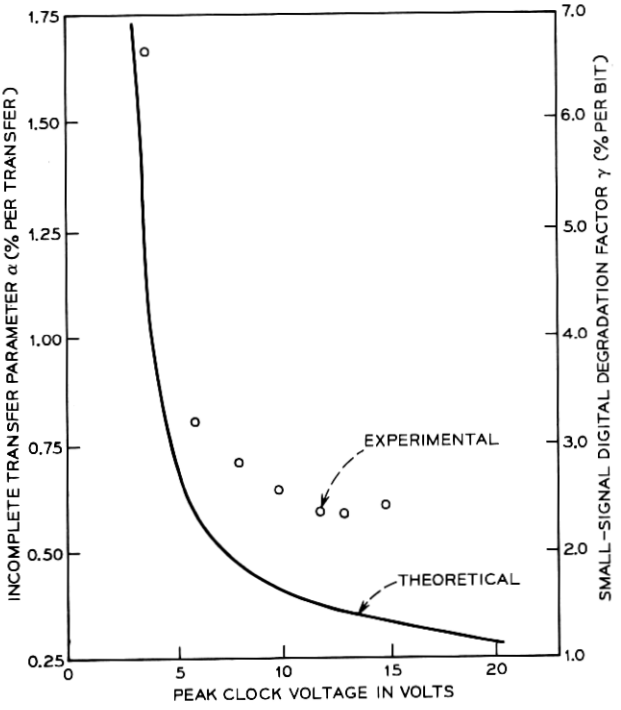

Fig. 14—Comparison of experimental and theoretical incomplete transfer parameter as a function of peak clock voltage for a bucket brigade.

that we are dealing with a p-channel register and that the capacitance C is entirely made up of oxide overlap capacitance. Then if V_n and V_p are the most negative and most positive values of clock voltage respectively, each p-island in the register under the no charge transfer condition will vary in potential from a most positive value of $V_n - V_T$ to a most negative value of $2V_n - V_p - V_T$ where V_T is the IGFET threshold voltage. Since each p-island must always be negatively biased, V_n must at least be sufficiently negative that $V_n - V_T$ is a negative voltage. This condition defines the minimum allowable negative excursion of the clock voltage. Also, since the maximum charge that can be transferred is $Q_M = C(V_p - V_n)$, and since the register performance has been shown to be very sensitive to the magnitude of charge transferred, the minimum difference between V_p and V_n can be defined given the performance requirements of the register. Hence, the most positive and most negative values of the clock voltage for any application are rather simply defined by the IGFET threshold

voltage under operating conditions and the desired register characteristics. Because of back gate bias, it should be noted that the IGFET threshold voltage will be different from that when source is shorted to the substrate.

The peak current that will flow in a clock line will consist of two contributions. One term will be due to the substrate capacitive loading on the clock lines and will include the displacement current to the substrate through this capacitance. Generally, registers will be designed to minimize this capacitive loading such that this term will be negligible. The other term will be the current which flows from one clock line to the other due to the charge transfer itself. Its value will depend on the quantity of charge being transferred in each bit. In any given charge transfer event the peak value of this current will typically occur approximately τ_B after initiation of charge transfer where τ_B is given by equation (6), and at this time the peak current contributed by that bit of the register will be given approximately by

$$I_p = C \frac{dV_{cc}}{dt}, \tag{8}$$

where V_{cc} is the voltage between clock lines. The peak current required from the clock power supply will be given by equation (8) multiplied by the number of bits in the register. Figure 15 illustrates the values of I_p per bit assuming sinusoidal clock voltages of 10 volts peak-to-peak for a register fabricated with the previously defined minimum dimensions.

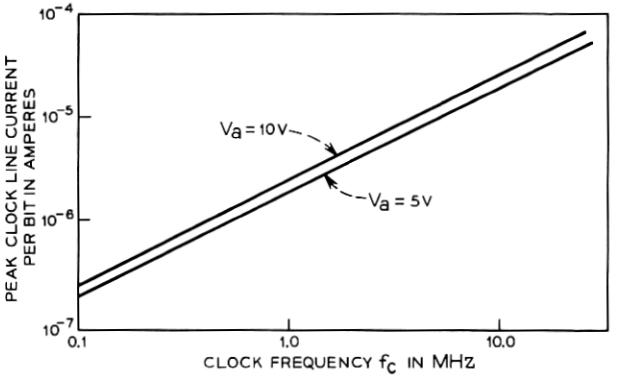

Fig. 15—Theoretical peak clock current required per bit as a function of clock frequency for a bucket brigade.

The average power dissipation on the chip, like the peak current and voltage requirements on the clock supply, is dependent on clock waveform. However, a relatively simple expression can be derived in which the detailed dependence on clock waveform can be lumped into one term. This term will often be negligible under practical operating conditions.

Assuming series resistance of the substrate is negligible, the major power loss on the chip is associated with charge transfer from one capacitor C to the next. Suppose that the capacitance C is entirely due to the oxide overlap capacitance and that a periodic clock voltage $V_c(t)$ with peak-to-peak magnitude V_{pp} is applied to the two clock lines, one delayed one-half a clock period with respect to the other. Then during transfer the source-to-drain voltage magnitude is given by

$$V_{SD} = 2V_c(t) + \frac{2Q}{C} - \frac{Q_a}{C}, \tag{9}$$

where Q is the instantaneous charge remaining on the source capacitance and Q_a is the total charge to be transferred. The power dissipation per bit, P_{DISS}, is given by the energy loss per cycle multiplied by the number of transfers per clock period and by the clock frequency f_c.

$$\begin{aligned} P_{\text{DISS}} &= 2f_c \int_0^{Q_a} \left[2V_c(t) + \frac{2Q}{C} - \frac{Q_a}{C} \right] dQ \\ &= 2f_c \int_0^{Q_a} 2V_c(t)\, dQ. \end{aligned} \tag{10}$$

From equation (5), $V_c(t)$ is related to Q by

$$I = \frac{dQ}{dt} = A\left[2V_c(t) - V_{pp} + \frac{Q}{C} \right]^2. \tag{11}$$

Hence, from equations (10) and (11)

$$P_{\text{DISS}} = 2f_c \left[V_{pp}Q_a - \frac{Q_a^2}{2C} + \int_0^{Q_a} \sqrt{\frac{I}{A}}\, dQ \right]. \tag{12}$$

The last integral in equation (12) is the only term dependent on the details of the clock waveform, and can be recognized as the integral over a clock period of the IGFET source-gate voltage above threshold. Defining this integral as $V_{av}Q_a$ where V_{av} is some average source-gate voltage above threshold during transfer of Q_a, equation (12) becomes

$$P_{\text{DISS}} = 2Q_a f_c \left[V_{pp} + V_{av} - \frac{Q_a}{2C} \right]. \tag{13}$$

Note that V_{av} will tend to zero in the limit of low frequencies and will

probably never be comparable to V_{pp} in normal operation. For this reason, depending on the clock waveform, V_{av} can probably be neglected compared to V_{pp} in order to obtain estimates of P_{DISS} . This means that a first-order estimate of power dissipation in a two-phase bucket-brigade register is independent of the details of the clock waveform but dependent only on Q_a , f_c , and the peak-to-peak clock voltage V_{pp} .

Figure 16 illustrates the 1-MHz power dissipation per bit as a function of charge being transferred, assuming the previously defined minimum dimensions. While the previous discussion has centered on the power dissipated on the substrate of the charge transfer shift register, the driving supply must provide the current (e.g., Fig. 15) necessary to both move the charge, and establish the pattern of stored energy associated with the new charge distribution. Figure 16 has been prepared assuming an ideal sine wave voltage driver, so the power to move the charge is the real power, while the modifications of stored energy can be considered to be reflected in the reactive power. The reactive power is simply the product of the sine wave clock voltage and the quadrature Fourier component of the current. Both power components rise with increasing charge, and the real power starts linearly from zero, while the reactive power is fairly large for zero charge because of the capacitative loading of the substrate (assumed to be doped to 10^{16} carriers/cm^3). This component can be lowered by using nonuniform doping profiles. The total power (since this is a sine wave analysis) is the phasor sum of the real and reactive powers.

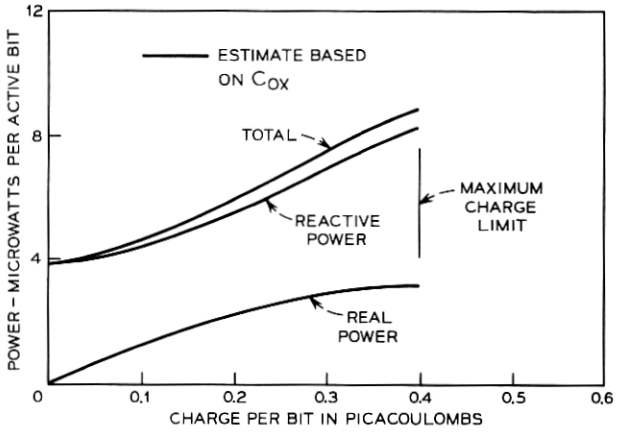

Fig. 16—Theoretical power requirements per bit versus signal charge at 1 MHz for a bucket brigade: peak-to-peak clock voltage of 10 volts.

Figure 17 shows the frequency dependence of the total power dissipation for a bucket brigade loaded to approximately half its absolute maximum value. This figure also illustrates the fact that the drive power varies roughly as the square of the drive voltage. At higher frequencies, the drive power will tend to rise more rapidly than linearly, because the importance of V_{ss} increases when more charge is left behind.

4.2 *Charge-Coupled Device Performance*

4.2.1 *Transfer Characteristics*

Difficult as the analysis of a bucket brigade is, the charge-coupled device presents even more formidable difficulties. In the general case, charge motion in CCD's is governed by a nonlinear relative of the diffusion equation, with driving forces coming from external fields, electrostatic repulsion of the mobile charges, and density gradients. Numerical solutions of this equation have been obtained in specific cases, but in the absence of general solutions, many approximations have been employed to reach reasonable estimates of CCD performance.

In charge-coupled devices with relatively large plates, there is negligible penetration of fringing fields under the plates, and the charge transport is governed by this approximate equation:[16]

$$\frac{\partial q}{\partial t} = \frac{\mu}{C}\left(\frac{\partial q}{\partial x}\right)^2 + \mu\left(\frac{q}{C} + \frac{kT}{e}\right)\frac{\partial^2 q}{\partial x^2}, \tag{14}$$

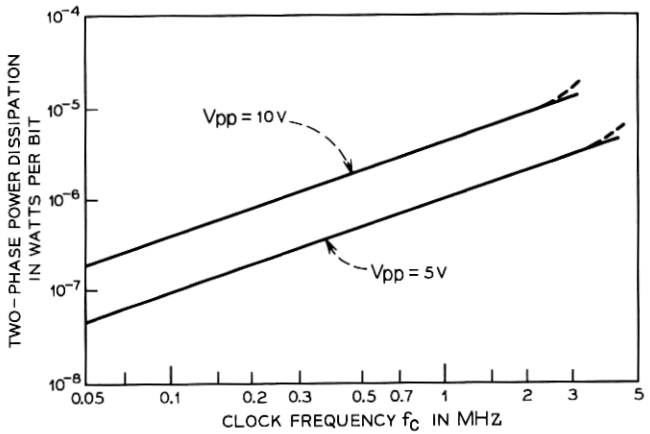

Fig. 17—Theoretical power dissipation per bit versus clock frequency for a bucket brigade.

where q is the mobile surface charge density, n is the surface mobility, C is the capacitance per unit area, approximately equal to the oxide capacitance ϵ_o/δ, but modified by space charge repulsion and depletion layer loading. The other symbols have their usual meanings. The assumption of negligible fringing fields is analogous to the "gradual channel" approximation in IGFET theory.

In solving this problem, it is found that time scales naturally against τ_o defined as

$$\tau_o = \frac{L_p^2}{\mu V_o}, \tag{15}$$

where L_p is the length of a CCD plate and V_o is arbitrarily taken to be one volt. Also, the total charge is most readily described by a voltage $V_a = \int q\, dx/CL$. The results[16] of a numerical solution of equation (14), presented as the amount of charge remaining under the plate as a function of time normalized to τ_o, in analogy to the similar calculation [equation (1) and Fig. 10] for bucket brigade, appear in Fig. 18. Note that for normalized times exceeding one, the charge quickly becomes independent of the initial charge. While time in Fig. 18 is normalized

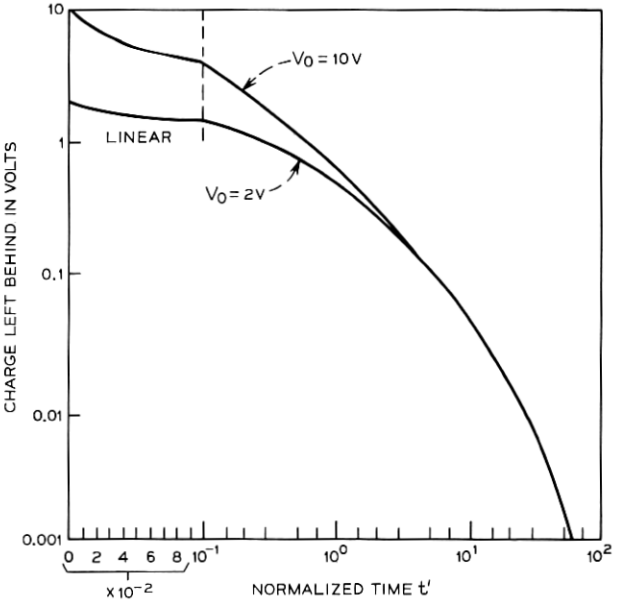

Fig. 18—Charge remaining on a CCD capacitor versus normalized time for two initial values of charge.

to τ_a as defined by equation (15), it is useful to also define a characteristic time for the CCD $\tau_c = L^2/\mu V_a$ for direct comparison to the bucket brigade τ_B in equation (6). As long as V_a is much greater than kT/e, it is found that the transport as determined by solving equation (14) scales with τ_c in much the same way that bucket-brigade transport scales with τ_B .

In Fig. 18 the advantage of a "fat" ZERO in digital charge-coupled devices is strongly suggested,[18] and it becomes clearer in Fig. 19. The large-signal digital degradation factor Γ is shown for a 5-volt ONE at 10 MHz, again in analogy with the bucket-brigade results (Fig. 11), with the ZERO varying from completely empty to nearly equal to the ONE. Equation (2) has been applied to the specific four-phase charge-coupled device described earlier, with four 18-μm plates formed by two levels of metallization. While the loss drops to the order of one percent in n-channel devices, the p-channel devices have a much higher percentage of loss at this operating frequency.

The loss associated with the finite rate of charge transport, illustrated by the calculated curves in Figs. 18 and 19, is similar to the intrinsic contribution to the incomplete transfer parameter, α_i , in bucket brigade. As is the case with the bucket-brigade register, this effect

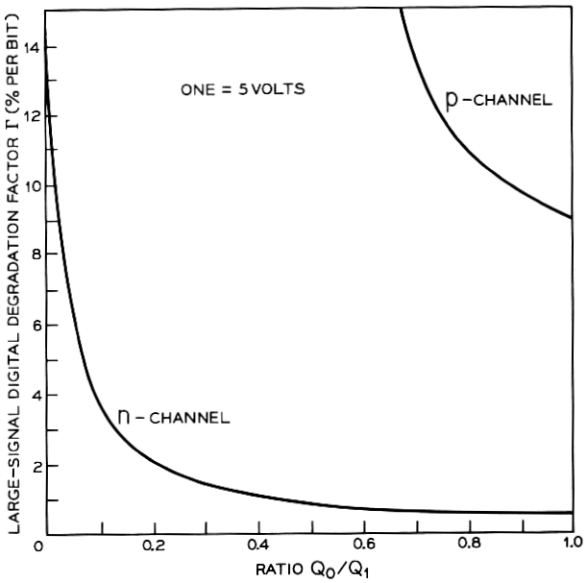

Fig. 19—Variation of signal degradation with size of the ZERO in a charge-coupled device.

becomes dominant at high frequencies and ultimately provides the high-frequency limitation for operation. The dashed curves in Fig. 20 show the frequency dependence of $\partial Q_r/\partial Q_i$ as calculated using equation (14) assuming a four-phase CCD with the previously defined minimum dimensions. To make it easier to include interface-state effects later, we have plotted the small-signal equivalent γ of the digital degradation factor Γ defined in equation (2),

$$\gamma = \lim_{Q_0 \to Q_1} \Gamma, \tag{16}$$

rather than the incomplete transfer parameter α. The two are simply related by

$$\gamma = 2p\alpha \tag{17}$$

so the bucket brigade results have been plotted using both parameters in order to simplify comparisons. Note that this intrinsic contribution to incomplete transfer decreases exponentially as the clock frequency decreases (as is the case with the bucket-brigade register), and that it becomes important at a somewhat lower frequency. The latter is due

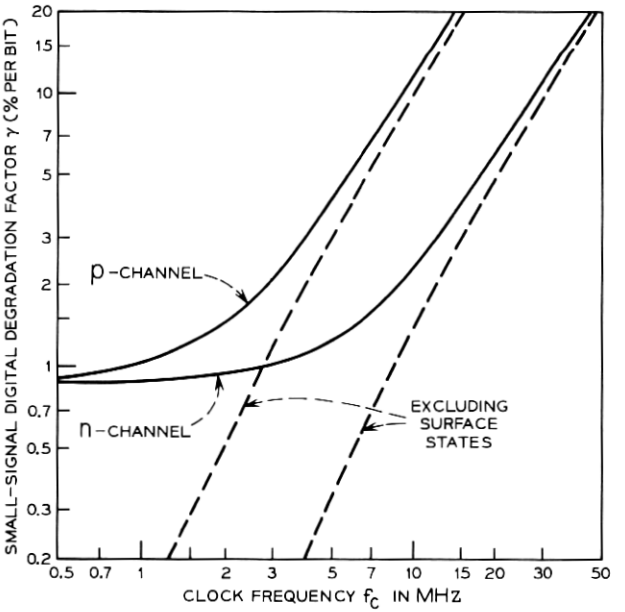

Fig. 20—Theoretical digital degradation factor versus clock frequency for minimum size four-phase CCD.

partly to the fact that the minimum register dimensions over which minority carrier transport occurs are somewhat larger for the CCD and partly to the four-phase mode of operation.

As the frequency of operation decreases, other contributions to incomplete transfer must begin to dominate. However, the CCD has no contribution analogous to the dynamic drain conductance term in the bucket brigade. Since it is believed that interface states will make a significant contribution to incomplete transfer at the lower frequencies, it is this term which will be considered next.

There are three principal ways for the interface states to interact with the information transport. The first interaction occurs through the generation of minority carriers at the surface, the second is by acting as a recombination site, and the third and most serious is their ability to retard mobile carriers, leading both to attenuation and distortion of the information. The generation of minority carriers at the surface adds to the bulk generation in depleted areas, and acts to limit low-frequency operation, as discussed separately in a later section. The recombination process only assumes importance if, at some time during the charge transfer cycle, a portion of the surface is drawn into accumulation. When this happens, majority carriers are trapped in states across a considerable portion of the bandgap, and when information in the form of minority carriers reaches this surface, recombination effects attenuation of the signal. This difficulty is readily eliminated in both charge transfer shift registers by assuring that no surface is ever drawn into accumulation.

Incomplete charge transfer due to interface-state trapping, on the other hand, is a more serious effect, and can be illustrated by using the formulation introduced in equation (4). If we define the charge left behind in interface states as Q_r' and the interface-state contribution to incomplete transfer as α_{ss}, we can write

$$\alpha_{ss} = \frac{dQ_r'}{dQ_i}. \tag{18}$$

Now suppose there is a time τ following transfer of the signal charge beyond which charges still trapped in interface states will be left behind. Then equation (18) can be written

$$\alpha_{ss} = \frac{\partial Q_r'}{\partial Q_i} + \frac{\partial Q_r'}{\partial \tau}\frac{d\tau}{dQ_i}. \tag{19}$$

Since interface-state emission times vary exponentially with energy, after time τ essentially all the interface states below some energy

ϵ_1 corresponding to an emission time τ will be filled and all those above will be empty. Hence, the first term in equation (19) can be made exponentially small by making Q_i large enough to fill the interface states to a level above ϵ_1 on each cycle; i.e., the use of "fat" ZERO's will make the first term in equation (19) negligibly small. The second term, however, reflects the difference in total emission time available to interface states as a function of signal level, and will be very dependent on clock waveform.

The interface-state effects have been analyzed for CCD operation using an idealized traveling wave model,[18] and the results have been used to yield the solid curves in Fig. 20 assuming a sinusoidal clock voltage with 10 volts peak-to-peak. In this model, the optimum transfer characteristics occur when the signal charge is 5 volts. An interface-state density of 10^{11} states/cm^2/eV was assumed in preparing the data. The interface-state contribution to incomplete transfer leads to the tendency for γ to saturate as the clock frequency decreases as shown in Fig. 20. Further, the value to which the γ tends is independent of the type of carrier. Hence, when interface states dominate as at low frequencies, CCD operation will be relatively independent of whether it is fabricated on n- or p-type substrates.

In the preceding discussion of CCD transfer characteristics we have analyzed, for simplicity, the performance of four-phase registers. Two-phase CCD operation, while probably very similar to that of a four-phase CCD, will depend in detail on the scheme used to achieve directionality, but three-phase operation can be predicted with only a minor change in the four-phase theoretical treatment. This has been done to compare the theory to existing experimental data in Fig. 21. The experimental points were obtained from an 8-bit, three-phase, p-channel register with 50 μm plates operating with a sawtooth clock voltage varying between -1.5 volts and -10 volts.[19] Also shown for comparison are results from a two-phase p-channel register made using silicon-gate technology with 50 μm plates operating with a square-wave clock voltage between -2 volts and -8 volts.[20] Two-phase operation was achieved by using two thicknesses of oxide. The reasonable agreement between theory and experiment and the strong frequency dependence of Γ indicates that the intrinsic transfer rate is limiting the performance of both CCD's, and that the theory of Strain and Schryer[16] represents a reasonable theoretical approximation to this limitation. On the other hand, greatly improved performance over that shown in Fig. 21 will result by going to smaller sizes. In fact, transfer efficiencies in excess of 99.9 percent at 1 MHz have already been reported.[19]

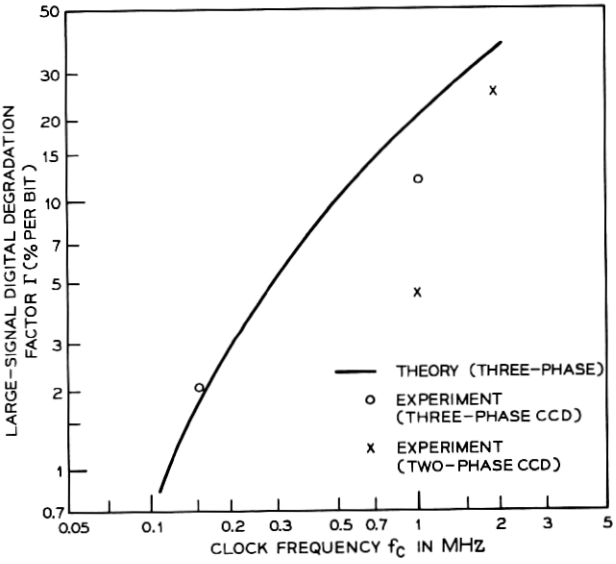

Fig. 21—Comparison of experimental and theoretical digital degradation factor as a function of clock frequency for a charge-coupled device.

4.2.2 *Drive Characteristics*

The operating voltage requirements of the CCD will also vary depending on the clock waveform, but in general they can be determined by considerations similar to those used for the bucket-brigade register. Assuming a p-channel register, the most positive voltage V_p on any clock line must not allow accumulation of majority carriers at the interface because of the loss that would be introduced through interface states. Hence, if the most negative flat-band voltage in the active region of the CCD is V_{FB} , V_p must be more negative than V_{FB} .

The minimum peak-to-peak clock voltage swing, V_{pp} , will be determined, as is the case for the bucket brigade, by the desired operating frequency and required transfer characteristics. Since the signal degradation is reduced as the charge being transferred is increased, and since the maximum charge that can be transferred is directly proportional to V_{pp} , the clock voltage requirements are rather simply defined by the flat-band voltage and the performance requirements of the register.

The peak current required from the clock power supply will be made up of the same two components existing in the bucket-brigade register—the displacement current to the substrate through the capacitive loading and the current between adjacent clock lines associated with

the charge transfer. The substrate current will generally be small, so the current associated with the transfer will usually dominate. Its peak value will occur approximately τ_c after initiation of transfer where τ_c is given by equation (15), and it too will be given approximately by equation (8) with C equal to the CCD plate capacitance and V_{cc} representing the voltage between adjacent clock lines. Thus, as a first approximation, the peak current required from a CCD clock supply is independent of the number of phases, given that the storage capacitance C_p is fixed, and is essentially identical to that required by a bucket-brigade register with the same storage capacitance.

The power dissipated on the chip of a two-phase CCD register can be calculated in the same way as that of the bucket-brigade register. However, in this case the dissipation will be dependent on the height of the potential barrier V_s introduced to achieve the two-phase operation as well as on the charge transferred and clock frequency. An analysis similar to that resulting in equation (12) yields

$$P_{\text{DISS}} = 2Q_a f_c \left[V_s + V_{av} - \frac{Q_a}{2C_p} \right], \tag{20}$$

where Q_a is the signal charge, C_p is defined by the half-bit area less the barrier area, and V_{av} here is the average excess voltage above the potential barrier through which the charge moves during transfer.

The power dissipated for polyphase operation can be considerably less than that given by equation (20) for two-phase operation. The major difference comes from the fact that directionality in the register is achieved by proper phasing of the clock lines rather than by building in a potential step. This means that the charge transfer is achieved by moving the carriers through a smaller potential gradient, resulting in less dissipation. A general analysis of this dissipation has not been carried out because of its mathematical complexity and dependence on clock waveform. However, a lower bound of its magnitude can be obtained from the sinusoidal traveling-wave CCD model described by Strain[18] in which the average power dissipation per bit was derived to be

$$P_{\text{DISS}} = Q_a \frac{16 L_p^2 f_c^2}{\mu}. \tag{21}$$

Figure 22 shows this power as a function of frequency for the particular case of $Q_a = 0.5$ picacoulomb. The dissipation can be seen to be very modest over the entire frequency range of interest. Even though equation (21) may provide a somewhat low estimate, it can be concluded

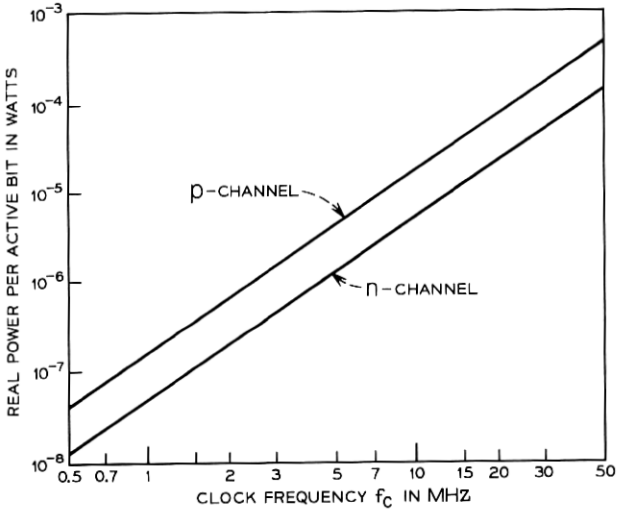

Fig. 22—Theoretical power dissipation per bit versus clock frequency for a polyphase charge-coupled device.

that the power dissipation of a polyphase CCD can be made to be considerably less than that of a two-phase CCD or bucket-brigade register. On the other hand, a polyphase CCD presents a significant reactive load to its driver. Since there is no advantage to using a highly doped substrate for a charge-coupled device, the substrate loading contributes very little to the reactive power required for a CCD, as Fig. 23 indicates. In the traveling-wave model, the reactive power rises to $\frac{1}{2}\omega C_{ox}V^2$ when the device is carrying the maximum possible charge. Optimum operation occurs with approximately one-third that charge, and there the power is just under half that predicted from C_{ox} . So far as the driving source is concerned, the loading is totally reactive; substrate dissipation contributes negligibly.

4.3 *General Considerations*

4.3.1 *Low-Frequency Limitations*

When a charge-transfer shift register is operated at low frequencies, or if the register operation is stopped for some time interval between regenerations, there are two problems which must be considered. First, generation currents due to interface states or bulk generating centers in the space-charge regions of the registers will contribute excess charge to both the ONE's and the ZERO's. Ultimately this

effect will overdrive the register, providing a lower frequency limit for operation and a limit on the maximum number of stages between regenerators. Second, any output and regeneration circuitry must be designed with the realization that only a small, finite amount of charge is available, and any shunt conductance may render the device inoperative at low frequencies. This effect may become very important as the register size is reduced, but since it depends on the detailed design of the regenerator, it will not be considered further here.

Using the usual carrier generation statistics, it can be shown that the generation current density due to interface states J_G is

$$J_G = \frac{\pi}{2} kTn_i v_{th} N_{ss} , \tag{22}$$

where kT is thermal energy, v_{th} is the mean carrier thermal velocity, n_i is the intrinsic carrier density, and N_{ss} is the interface state density near midgap. In the bucket-brigade register, only those interface states in the gate region contribute to J_G and then only for that part of a clock cycle during which the gate region is not transferring charge. In the CCD, the entire surface over which charge is not being transferred

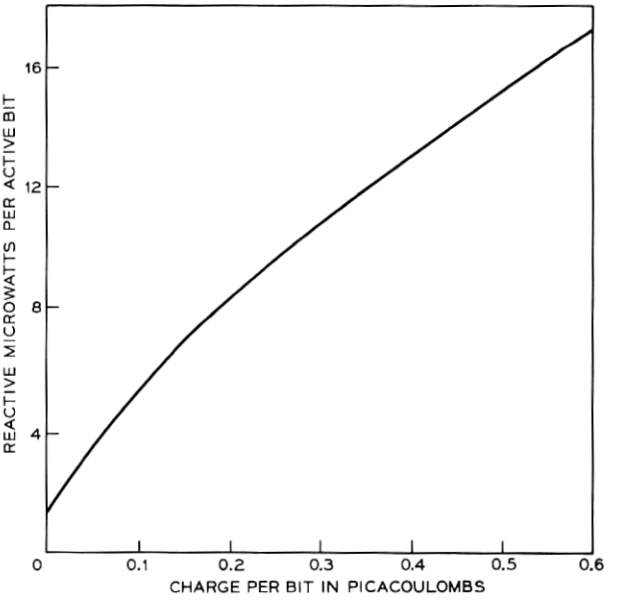

Fig. 23—Theoretical reactive power per bit versus signal charge for four-phase CCD for sinusoidal clock drive.

is active so interface state generation currents will be somewhat more important. Since charge will accumulate in proportion to the time a bit spends in residence in the shift register, Fig. 24 presents an estimate from equation (22) of the ratio of the charge accumulated per microsecond of residence to the nominal charge in a bit, using the minimum shift register sizes that appear throughout the paper and assuming $N_{ss} \cong 5 \times 10^{10}/\text{cm}^2\text{eV}$. The independent variable is temperature and the activation energy is that associated with n_i . Since charging due to bulk centers is likely to be negligible, they have been neglected in preparing Fig. 24.

The compromise between interface state generation currents and charge transfer efficiency can be summarized by relating the various signal degradation parameters to the maximum length of a single-string shift register between regenerators. This has been done in Figs. 25 and 26 which present the maximum length as a function of operating clock frequency assuming the following two limits apply: (*i*) $\Gamma n \leqq 1$ where n is the number of stages in the register, and (*ii*) the fractional increase in the signal charge due to interface state generation current

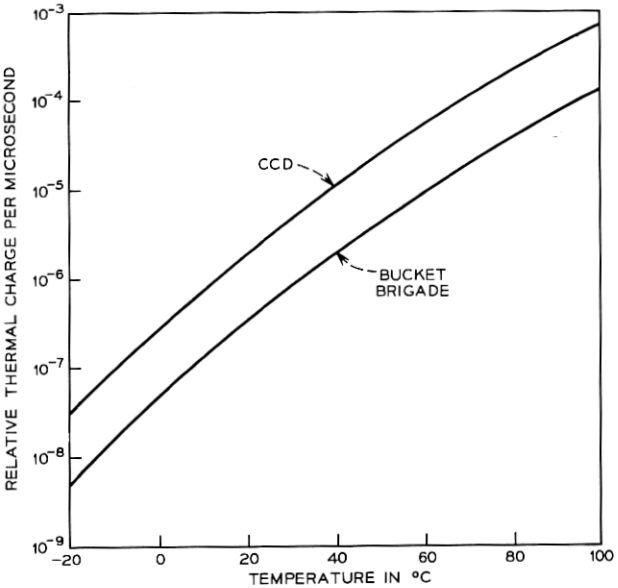

Fig. 24—Ratio of thermal generation charge accumulated per microsecond to signal charge as a function of operating temperature for bucket brigade and charge coupled devices. Only interface states are assumed to contribute to thermal generation.

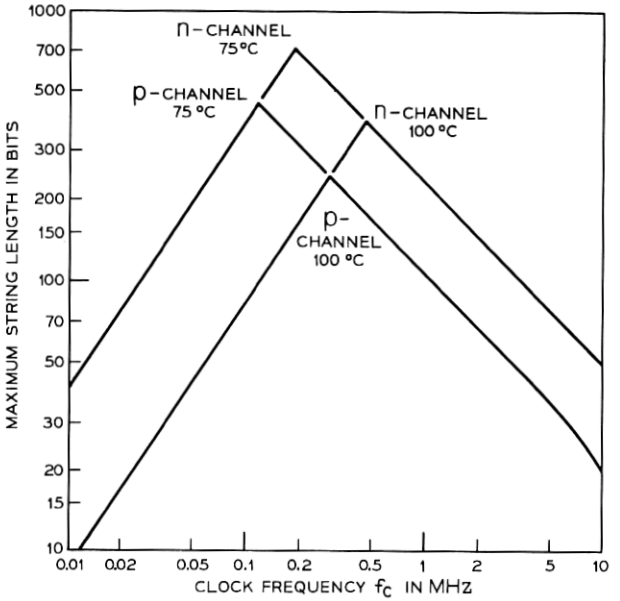

Fig. 25—Maximum length of single shift register string versus clock frequency as limited by thermal generation and incomplete transfer in a bucket brigade.

$\leqq 0.1$. The positive slope portions of the curves represent the limitation due to thermal generation currents; whereas, the negative slope portions represent the limitations of incomplete transfer effects. It is evident that for frequencies above approximately 0.7 MHz, generation currents are not expected to significantly affect charge transfer shift register operation even at 100°C. Further, bit strings up to 50 bits long appear feasible at approximately 2 MHz in p-channel and 10 MHz in n-channel for both CCD's and bucket-brigade registers.

4.3.2 *Clock Waveform and Signal Level Effects*

In the previous sections a dependence of shift register characteristics on both signal level and clock waveform was pointed out and several examples were given. However, because of its importance, it is felt that a separate section describing the effects in more detail is warrented.

The dependence of incomplete transfer effects on the signal charge Q_a reflects the nonlinear transfer characteristics inherent in both register schemes, and without exception all contributions to incomplete transfer which have been considered here decrease as the drive voltage, and consequently the signal charge, is made larger. Assuming this is a

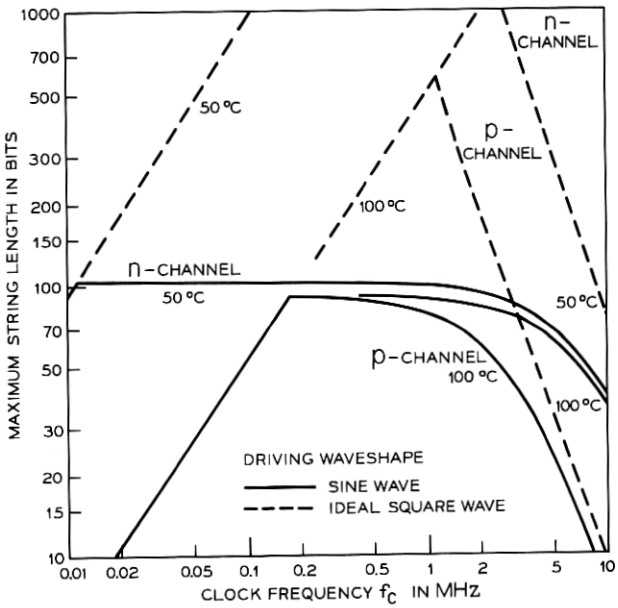

Fig. 26—Maximum length of single shift register string versus clock frequency as limited by thermal generation and incomplete transfer in a charge-coupled device. The dotted lines represent the maximum length if it is assumed interface states do not contribute to incomplete transfer.

general result, it can be concluded that best register operation will occur when the largest possible clock voltages are used and when the optimum fraction of that voltage is used for the signal. For digital applications this means that for fixed clock voltages, for example, a ONE should be represented by something near or greater than one-half the absolute maximum charge that can be transferred and a ZERO by some smaller but still reasonably large quantity of charge; for analog applications this means that the signal should be superimposed on a dc background. In the latter case it is important to recognize the noise disadvantage and the necessity for compromise between transfer efficiency and reduced nonlinear distortion, and signal-to-noise ratio.

The dependence of the various contributions to incomplete transfer on clock waveform differs depending on the particular contribution so that no ideal waveform can be defined. However, all of the contributions for the charge-transfer dynamic registers will either be decreased somewhat or, at worst, remain unchanged by choosing a

clock waveform with both a short rise time and a short fall time. Also, a waveform should be chosen which makes the time interval over which transfer current flows as long as possible. While precautions of this kind can decrease signal degradation, at the same time they place more stringent requirements on the clock power supply. With this in mind it is important to note that either register will operate quite satisfactorily even with sinusoidal clock voltages, and that the frequency characteristics presented in the figures of the previous sections were often calculated assuming sinusoidal clocks and always measured using waveforms with rather poor rise and fall characteristics.

Ignoring for a moment the disadvantages associated with different clock voltage waveforms, it is instructive to illustrate the dependence of the theoretical incomplete transfer effects on the waveform. Figures 27 and 28 show the calculated values for p-channel bucket-brigade and CCD registers respectively, keeping the signal charge and peak-to-peak clock voltage constant but varying the waveform. A channel doping of 10^{16} cm^{-3} has been assumed. Note that bucket-brigade performance is best at high frequencies using trapezoidal waveforms but best at low frequencies using square waves. The crossover comes about as a result of different magnitudes and frequency dependencies

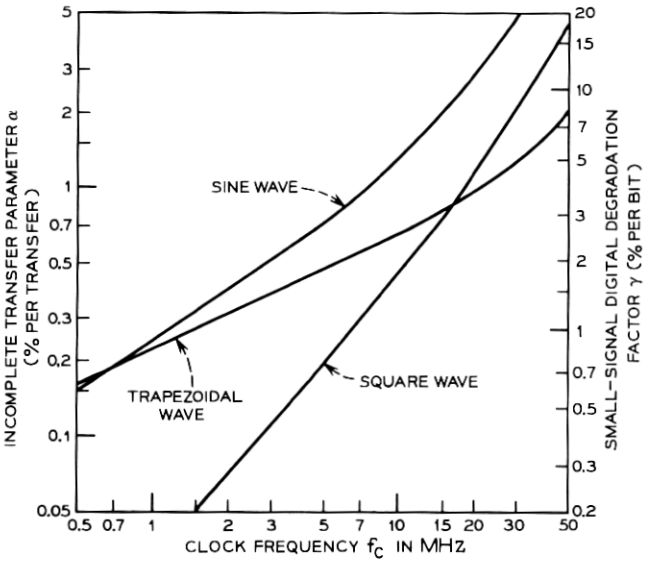

Fig. 27—Illustration of clock waveform dependence of incomplete transfer in a bucket brigade.

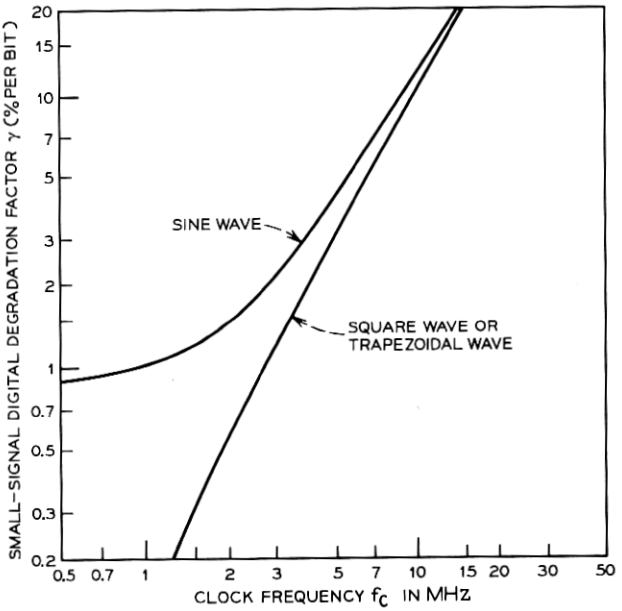

Fig. 28—Illustration of clock waveform dependence of incomplete transfer in a charge-coupled device.

of the intrinsic and drain conductance contributions to α. Note also that degradation due to interface states in the CCD is effectively reduced to zero by using clock waveforms with negligible rise and fall times. This can be explained using equation (19). The first term is α_{ss} is made exponentially small by using a large signal charge, and the second term becomes zero since $d\tau/dQ_i$ is zero.

There is another performance-limiting effect in addition to the increased clock current requirements associated with very short rise and fall times in the clock waveform. To illustrate this effect, suppose that the time required to change a clock line voltage from its most negative value to its most positive value is negligible compared to the time for most of the charge to transfer from one capacitor to the next. Then if a relatively large quantity of charge was present on a capacitor, the surface potential in the case of the CCD or the p-island potential in the case of the IGFET bucket-brigade register could be driven positive with respect to the substrate for a short period of time. If this occurred, some of the holes representing the signal would be injected into the semiconductor bulk where they would be lost to recombination. This injection effect can seriously limit the maximum

charge that can be transferred, thus limiting the transfer efficiency and the maximum frequency of operation. To eliminate this additional signal degradation contribution, one can either include an appropriate dc offset of the clock drive, or limit the clock waveform rise and fall times to at least several τ_B in the case of the bucket brigade and several τ_c in the case of the CCD.

V. SUMMARY

The detailed considerations of the preceding pages can be summarized and the major conclusions stated. Because of the large number of considerations involved, we will subdivide the summary into four sections: size and fabrication considerations, performance limitations and characteristics, drive and power requirements, and regeneration and output requirements.

5.1 *Size and Fabrication Considerations*

If it is assumed that charge-transfer shift register size is limited only by 10 μm photolithographic tolerances, minimum sizes of the two registers, fabricated in serpentine geometry using such tolerances, are indicated below:

	Conventional Metal	Refractory Gate Technology
Bucket Brigade	1.8×10^3 μm^2 (2.8 $mils^2$)	10^3 μm^2 (1.5 $mils^2$)
Two-Phase CCD	not considered	1.3×10^3 μm^2 (2 $mils^2$)
Four-Phase CCD	not considered	1.6×10^3 μm^2 (2.5 $mils^2$)

While factors other than photolithographic tolerances may often be more important in limiting shift register size, these results show that charge-transfer shift registers have the potential for significantly smaller size than other existing shift register schemes.

The fabrication of CCD's using conventional metallization has not been considered because of the difficulty in defining a practical scheme within the restrictions of a 10 μm metallization tolerance. While some novel technology may lead to simplified fabrication schemes for either or both charge transfer registers, the aim here was to consider a practical but relatively simple technology for CCD fabrication within the assumed tolerance restrictions which would allow comparisons with bucket-

brigade registers yet be compatible with additional circuitry on a register chip. This was the reason for choosing a two-level metallization scheme. Assuming such a technology, it can be concluded that the bucket-brigade register can be made slightly smaller than either CCD register. This conclusion comes about because there is no necessity to guarantee metal overlap between adjacent half-bits of the bucket brigade register. On the other hand, the CCD may be less sensitive to the precision of alignment between the two metal levels. With these fabrication differences, it is evident that significant reduction in photolithography tolerances may alter this comparison by making it possible to fabricate practical CCD's using a single level of metallization and by simultaneously emphasizing the realignment problem for bucket brigades.

Approximately the same number of processing steps and masks are required for fabrication of both charge transfer shift registers. However, both registers are so simple and include such a small number of steps than if a two-level metallization is available, the steps will inevitably be included in the processing steps required for the input, output, and regeneration circuitry. The same conclusion applies to the bucket brigade with conventional metallization. Hence, it will be the fabrication complexity of the associated circuitry rather than that of the shift register which will often determine the fabrication complexity of a register chip.

5.2 *Performance Limitations*

Charge-transfer shift register performance becomes limited when the signal transferring through the register is unacceptably degraded. For digital operation this will occur when the difference between ONE's and ZERO's is significantly reduced or becomes noticeably dependent on the bit sequence. Since most signal degradation mechanisms in these shift registers are cumulative, for operation at a given frequency an upper limit to the number of stages will result, while for operation with a given number of stages, a minimum and maximum allowable clock frequency will be defined.

Both charge-transfer shift registers will be limited similarly at low frequencies by generation currents. These currents will come partially from bulk generation in the space-charge regions and partially from interface states in the channel regions of the bucket brigade and over the active surface of the CCD. The difference in area over which interface states can contribute represents the major low-frequency difference between the two registers. If too long a period of time is left between

regeneration of the signal in the register, the generation currents will add to the signal charge and tend to overload the register. With presently available technology it should be possible to operate 50-bit p-channel charge transfer shift registers at frequencies as low as 100 KHz even at temperatures of 100°C; i.e., periods approaching a millisecond between regenerations should be achievable.

At high frequencies, register performance will be limited by the intrinsic rate at which charge can transfer from one capacitor to the next. This leads to a characteristic time constant for transfer which is $L_p^2/\mu V_a$ for the CCD and $L_G L_O/\mu V_a$ for the IGFET bucket brigade, where μ is the field effect mobility, V_a is approximately the voltage associated with the signal charge, L_p is the CCD capacitor plate length, L_G is the IGFET channel length, and L_O is the effective p-island overlap length in the bucket brigade. Because the signal degradation due to this effect varies exponentially with clock frequency, it provides a high-frequency operating limit, but it is inconsequential for operation at lower frequencies. Using the minimum dimensions assumed throughout the paper, it is found that the bucket-brigade register should operate to somewhat higher frequencies than the CCD. However, for both registers it should be possible to operate p-channel up to approximately 10 MHz and n-channel up to approximately 50 MHz even with the assumed 10 μm photolithographic tolerances. With improved tolerances the gradual channel approximation used here for both registers will cease to be valid as fringing fields become important, so that a simple extrapolation of the results using smaller dimensions may be somewhat pessimistic.

At intermediate frequencies both generation current and intrinsic transfer rate effects will be negligible, and other mechanisms will lead to performance limitations of charge transfer shift registers. For the bucket brigade, the most important mechanism in this range is due to the IGFET dynamic drain conductance. Primarily due to channel length modulation, it gives rise to an incomplete charge-transfer contribution which varies slowly with clock frequency. However, the limitation is not serious for most applications since by appropriate doping of the channel region charge transfer efficiencies in excess of 99.9 percent at 1 MHz can be achieved.

For the CCD, there is no contribution to incomplete transfer analogous to the dynamic drain conductance effect in the bucket brigade. However, there is a larger area over which interface states are active. For these reasons interface state effects, which were ignored in the bucket brigade, will probably provide the important limitation to CCD

performance at intermediate frequencies. It is found that their contribution to incomplete transfer is relatively independent of clock frequency and carrier type, but very dependent on the details of the clock voltage waveform. As an example, an interface state density of 10^{11} states per cm^2 per eV will limit transfer efficiency at intermediate frequencies to less than 99.9 percent if the clock waveform is sinusoidal. However, interface states will introduce no limitation at all if the clock waveform is an ideal square wave. Hence, it may be possible to achieve extremely high transfer efficiencies at intermediate frequencies with the CCD by using clock voltages with very short rise and fall times. As will be pointed out later, such operation will be limited by the peak current capabilities of the clock power supply, but in most cases it should be possible to achieve more efficient mid-frequency transfer than with the bucket-brigade register.

All contributions to incomplete transfer in both registers are nonlinear. The nonlinearity is such that best performance is achieved when rather large quantities of charge are transferring through the register at all times. For digital applications, for example, this means that a ONE should be represented by a large quantity of charge and a ZERO should be represented by a slightly smaller, nonzero quantity of charge.

5.3 *Drive Characteristics*

The drive characteristics of charge-transfer shift registers can be described in terms of three related properties: power dissipation on the register chip per bit, clock voltage magnitudes and waveform, and peak current requirements from the clock supply. For two-phase operation, the power dissipation of both charge-transfer shift registers is approximately linear with clock frequency and is a maximum when the largest quantities of charge are being transferred. This maximum power is relatively independent of clock waveform but varies as the square of the peak-to-peak clock voltage. Typical values at 1 MHz for the previously described minimum dimensions will be in the 1-to-5-microwatt-per-bit range assuming a peak-to-peak clock voltage of 10 volts, and will be approximately the same for both the CCD and the bucket brigade. Polyphase CCD's may dissipate considerably less power depending on the details of the clock waveform, perhaps up to one or two orders of magnitude less at 1 MHz. Since directionality is achieved by proper phasing of the clock lines, the charge does not have to transfer through as great a potential difference at each step for polyphase operation.

While the dc level of the clock voltage is an important factor to some of the operating conditions of a register, it is only the peak-to-peak clock voltage magnitude which enters into power dissipation and limits the maximum charge that can be transferred. Because of their nonlinearity, all of the incomplete transfer effects considered here are reduced as the peak-to-peak clock voltage, hence the peak signal charge carried in the register is increased. In this way, the performance requirements of the register place a minimum on the peak-to-peak clock voltage which, for a given storage capacitance, is essentially the same for both charge transfer registers.

There is some performance advantage to shaping the clock voltage waveform, especially by reducing the rise and fall times. However, the peak current from the clock power supply, being essentially displacement current through a capacitance, increases as the rise and fall times are reduced. Since peak current values of the order of one microampere per bit are found to be required for 10-volt operation of minimum size registers at 1 MHz even under sinusoidal operation, the current requirements of a register chip might become completely unrealistic if the rise and fall times are required to be too short. In addition, for some operating conditions, charge injection effects into the semiconductor bulk will limit the maximum charge that can be transferred as the rise and fall times are reduced.

5.4 *Regeneration and Output Circuitry*

In the preceding sections the minimum sizes and optimum performance characteristics of the basic charge-transfer register have been described. Because of the small quantities of charge transferred and small capacitance in which the charge is stored, all register chips will probably have additional circuitry for amplification on the chip. For digital applications, the finite generation currents and incomplete transfer effects will make periodic threshold regeneration necessary in a register string, and this regeneration will most often be performed by circuitry on the register chip itself. This additional output and regeneration circuitry on a register chip may impose serious limitations to both fabrication and performance. The fact that fabrication complexity of the additional circuitry will often determine completely the fabrication complexity of a register chip has already been pointed out. In a similar way the speed of the regeneration or output circuitry may be the important limitation to the speed of the register operation, and the minimum signal required to drive the circuitry may provide a more important size limitation than photolithography tolerances.

In these ways it is possible that output and regeneration circuitry may provide the more important fabrication, size, and performance limitations to charge-transfer shift register chips.

In devices which are designed for production, margins must be taken into considerations; this has not been done in this article, in part because the inputs to a margin analysis are very intimately associated with the input, output, and regeneration circuitry and with the details of device manufacture. Because of the importance of margin considerations, however, some general comments are in order. In the size range discussed in this paper, margin limitations and requirements will probably be very similar for the two registers, particularly since input, output, and regeneration circuitry are likely to be essentially the same. Differences will arise primarily because of the fact that the charge in the bucket brigade register is stored in diffused regions; but they will be modest unless metallization dimensions approach diffusion depths either through improved photolithography or through extended diffusion times.

In the final analysis, one of the most important comparative features of these devices will be fabrication yield. The major fabrication difference is associated with the addition of a diffusion at each storage site in the bucket-brigade register, but no detailed information concerning yield is presently available.

REFERENCES

1. Note, for example, Smits, F. M., "Charge Storage Semiconductor Devices," presented at the European Semiconductor Device Research Conference, Munich, March, 1971.
2. Waaben, S., Digest of Technical Papers, ISSCC, Philadelphia, 1970, p. 46.
3. Boyle, W. S., and Smith, G. E., "Charge Coupled Semiconductor Devices," B.S.T.J. *47*, No. 4 (April 1970), pp. 587–593.
4. Sangster, F. L. J., and Teer, K., IEEE Journal of Solid State Circuits, *SC-1*, p. 131 (1969).
5. Sangster, F. L. J., presented at the International Solid State Circuits Conference, Philadelphia, February 18–20, 1970.
6. Intel, Electronics, *43*, No. 12, p. 56 (June 8, 1970). Motorola, *Microelectronics Data Book* (Supplement 2 to 2nd Ed), (September 1970).
7. Janssen, J. M. L., Nature, *4291*, (149) January 26, 1952.
8. Hannan, W. J., Schanne, J. F., and Woywood, D. J., IEEE Trans. Milt. Elec., p. 246, July–October, 1965.
9. Berglund, C. N. and Boll, H. J., talk presented at the International Electron Device Meeting, Washington, D. C., October 1970.
10. Walden, R. H., Strain, R. J., and Krambeck, R. H., unpublished work.
11. Tompsett, M. F., Amelio, G. F., and Smith, G. E., Appl. Phys. Letters *17*, p. 111 (1970).
12. Krambeck, R. H., unpublished work.
13. Strain, R. J., presented at the International Electron Device Meeting, Washington, D. C., October 1970.
14. Berglund, C. N., IEEE Trans. Solid State Circuits, *SC-6*, p. 391 (1971).

15. Joyce, W. B., and Bertram, W. J., "Linearized Dispersion Relation and Green's Function for Discrete-Charge-Transfer Devices with Incomplete Transfer," B.S.T.J. *50*, No 6 (July–August 1971), pp. 1741–59.
16. Strain, R. J., and Schryer, N. L., "A Nonlinear Diffusion Analysis of Charge-Coupled-Device Transfer," B.S.T.J. *50*, No. 6 (July–August 1971), pp. 1721–40.
17. Thornber, K. K., IEEE Trans. Electron Devices, *ED-18*, pp. 941–50 (1971).
18. Strain, R. J., unpublished work.
19. Boyle, W. S., and Smith, G. E., Spectrum, *7*, (July 1971), p. 18.
20. Powell, R. J., private communication.