B. S. T. J. BRIEF

The Buried Channel Charge Coupled Device

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The charge-coupled device, as described originally by Boyle and Smith,[1] operates by moving minority carriers along the surface of a semiconductor with voltage pulses applied to metal electrodes which are separated from the semiconductor by an insulating layer. The transit from one electrode to the next is determined by the minority carrier transport under the influence of their own potential, fringing fields, and diffusion, and by the trapping properties of interface states. The transport limitations are largely determined by device geometry;[2] for 10-μm electrodes, thermal diffusion is predominantly responsible for transferring the last small amounts of charge forward and limits efficient operation to clock frequencies below 10 MHz. Surface state trapping is much less dispersive, and even at low frequencies 10^{11} states/cm^2 eV can impose the requirement for regeneration after as few as 100 transfers.[3,4] In order to circumvent these problems, Boyle and Smith[5] have proposed a modified CCD structure in which the charges do not flow at the semiconductor surface; instead they are confined to a channel which lies beneath the surface. This buried channel device has the potential of eliminating surface state trapping. (Bulk trapping should be several orders of magnitude less important as a CCD loss mechanism.) Calculations show that this modification will give rise to increased fringing fields under the CCD electrodes. Diffusion is replaced as an important factor in the intrinsic transfer process by the more powerful field-aided transfer. This leads to fast, efficient transport even when very little charge remains to be transferred. In addition to these advantages, the higher mobility found in the bulk of the semiconductor should further enhance the speed of the device.[2]

The proposed buried channel structure is shown in Fig. 1 as a three-phase, p-channel CCD. It consists of a p-type layer of Si on an n-type Si substrate with p^+ contacts at either end of the channel. The structure is completed with an SiO_2 film and metal electrodes. The thickness of the p-layer is a few μm and the acceptor concentration is 10–20 times the donor density of the substrate. In order to form a buried channel,

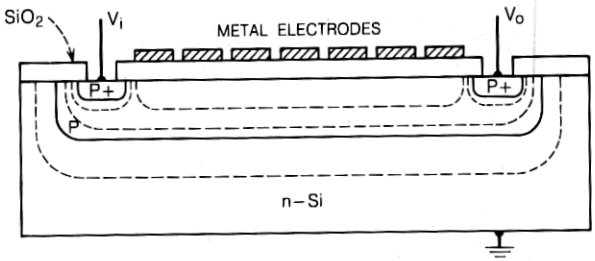

Fig. 1—Cross-sectional view of buried channel CCD.

it is necessary to completely deplete the p-type layer and part of the adjacent n-region. This is accomplished by putting the output diode at a voltage V_0, a reverse bias strong enough to drain all of the holes out of the p-layer (a total charge of the order of 10^{12} cm^{-2}). A solution of the one-dimensional Poisson's equation for this depleted condition is shown in Fig. 2, where it was assumed that the p-layer has a uniform concentration of 2×10^{15} cm^{-3} and is 5 μm thick, and the SiO_2 is 1000 Å thick. The substrate is taken to be uniformly doped to 1×10^{14} cm^{-3}. The graph shows negative potential plotted upward as a function of distance away from the Si-SiO_2 interface for an applied gate voltage of 0 V. The peak at -37 V in the curve represents a potential minimum for holes, and its position, about 4 μm from the interface, is the buried channel. This value of peak voltage also gives some idea of the potential that must be applied to the output diode in order to deplete the p-layer.

The charge-carrying capability of this structure has been estimated to be about 4×10^{-8} C/cm^2 and the effect of this charge on the potential is shown in Fig. 2. A surface device would accommodate a charge load of about 3×10^{-7} C/cm^2, almost an order of magnitude more, and this is one of the penalties of using a buried channel structure, a reduced charge capacity.

In order to ascertain the fringing fields in the channel, two-dimensional potential calculations[6] have been made numerically using the buried channel structure. The first structure considered for this calculation, corresponding to the experimental device described below, is shown in Fig. 3 and consisted of 45-μm-wide plates with 5-μm interelectrode gaps. The channel potential curve in Fig. 3 shows a rather disturbing feature, i.e., the existence of potential wells under the interelectrode spaces. It is understandable that such wells will exist since the floating region between the plates would go to -800 V without the influence of fringing fields from the grounded plates. These wells will, of course, fill with

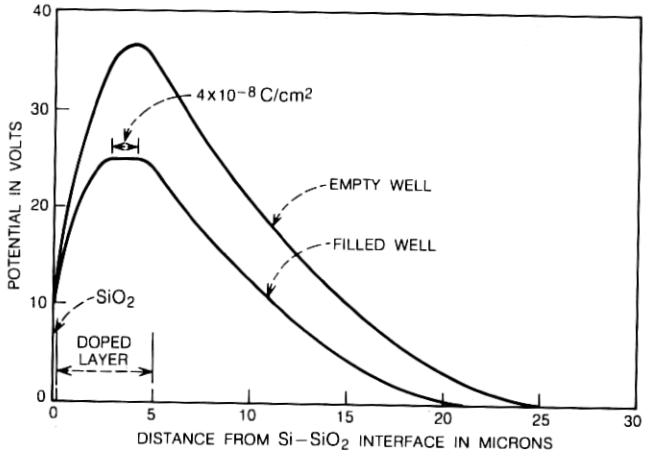

Fig. 2—Potential as a function of distance into the silicon showing an empty and a filled well.

mobile charge, but the amount contained in each is going to depend on the potentials of the spaces under the neighboring CCD plates. This means that the wells can exchange charge with any signal that might be present, leading to a severe loss. It would be desirable then to have the interelectrode potential vary monotonically across the gap; one way

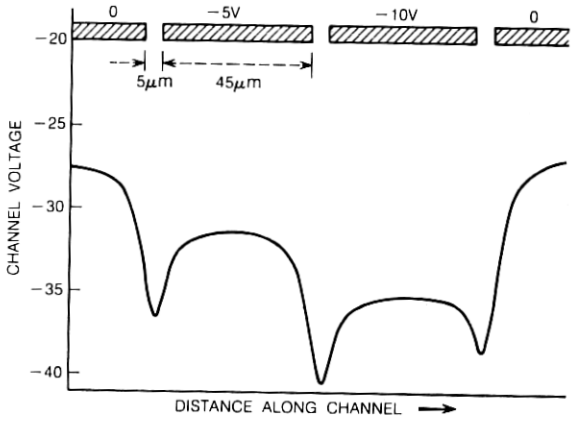

Fig. 3—Two-dimensional calculation of potential along the buried channel. The finite interelectrode gaps give rise to the potential minima.

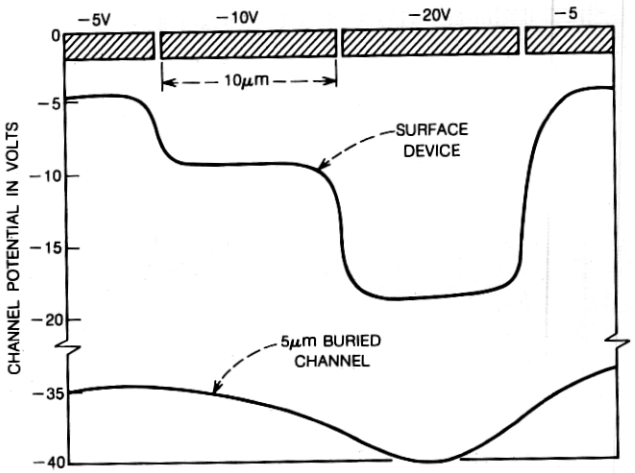

Fig. 4—Two-dimensional calculation of potential along the buried channel for the case of zero spacing. Also shown is potential plot for a surface device for comparison.

to do this would be to let the spacing go to zero. The potential calculation was repeated for the configuration shown in Fig. 4 for a plate length of 10 μm and for a zero spacing between metals. Two curves are shown, one for the buried channel CCD and one for a surface device for comparison. Here, the undesirable charge pockets are clearly missing and there is a significant amount of tilt in the potential under the plate at -10 V (the one where charge would be transferred from). The surface device, on the other hand, shows a relatively flat potential. The field under the -10-V plate for the buried channel is at least 3×10^3 V/cm, while the minimum field for the surface device is about 10 times smaller. Transport calculations, using this field value and the indicated plate length, show that only 10^{-7} of the charge will remain behind after 1 ns. Thus operation of the shift register at a clock frequency of several hundred MHz should be possible.

In order to examine these ideas experimentally, some test structures were fabricated. The p-layer was formed by a shallow ion implantation of 10^{12} boron atoms/cm^2 followed by a 7-hour diffusion at 1200°C. It was estimated that the final junction depth was 5–7 μm. The substrate had a doping density of 1×10^{14} cm^{-3} and 1000 Å of SiO_2 was employed as the insulator. Aluminum metallizations were defined using standard photoresist techniques to yield the CCD plate structure shown in Fig. 3, i.e., 45-μm plates and 5-μm spaces. These devices failed to operate as

CCD's because of the gap problem which was subsequently understood as a result of the calculation. However, the existence of a buried channel was verified by operating the device as an IGFET. This test was made by tying all of the electrodes to a single gate voltage. The channel conductance was then measured as a function of the source and drain voltages. This experiment was repeated at a series of different gate voltages and the resulting cutoff voltages are plotted against gate voltage in Fig. 5. The solid curve was obtained by means of the same potential calculation that was used for Fig. 3 and the agreement between theory and experiment is good.

In conclusion, a buried channel CCD has been described which offers the advantages of improved high-frequency response relative to surface devices because of stronger fringe-field-aided transfer and also because carrier mobilities have higher values in bulk Si than at the $Si-SiO_2$ interface. Further, the transfer efficiency should also be better at lower frequencies since surface state losses are eliminated. One significant design criterion has been established: the interelectrode potential in the channel of a polyphase device must vary monotonically across the gap. This can be achieved by making the gap very narrow, e.g., by using an overlapping metallization structure[7,8] or by undercut isolation techniques.[9] Once the gap problem is alleviated, the major remaining disadvantage of the buried channel device is its reduced charge-carrying capability. It is possible, however, to trade some degree of fringe-field-aided transfer for charge capacity by moving the channel closer to the semiconductor surface.

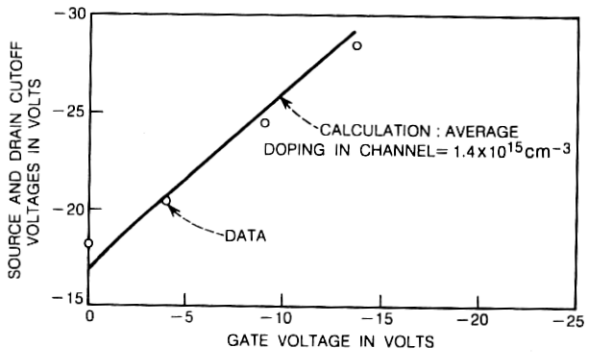

Fig. 5—Experimental plot of channel cutoff voltage as a function of gate voltage. Also shown is a theoretical curve for an average doping density in the p-layer of 1.4×10^{15} cm^{-3}.

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