THE BELL SYSTEM TECHNICAL JOURNAL
Vol. 53, No. 9, November 1974
Printed in U.S.A.

Interfacial Dopants for Dual-Dielectric, Charge-Storage Cells

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(Manuscript received February 19, 1974)

When a suitable interfacial dopant, such as W, is introduced at the interface between the dielectrics of a DDC cell, the write-erase characteristics of the cell are greatly improved. The useful range of the dopant concentration is determined to lie between about 10^{14} to 10^{15} atoms/cm^2. The interfacial dopant allows the fabrication of a DDC cell with relatively thick SiO_2 layers (>50 Å). The result is a substantially permanent memory cell that can still be subjected to electrical write-erase at reasonable gate-voltage conditions.

I. INTRODUCTION

There has been an increasing interest in recent months in the dual dielectric metal insulator semiconductor (MIS) cell as a nonvolatile semiconductor memory element. A true nonvolatile semiconductor memory could replace the omnipresent magnetic memory because associated with it one also expects fast access capability as well as interface compatibility with other semiconductor logic circuits. Key features in such a semiconductor memory cell, then, are: true nonvolatility, high-speed access capability, and ease of write-erase operations. The development of the dual-dielectric charge-storage (DDC) cells have followed two parallel paths, both enjoying a limited success yielding commercial products. The first centers around the concept of the *floating gate*,[1] an artificially created metallic charge-storage site located at the dual dielectric interface. The second uses the naturally occurring interfacial states existing at the dual-dielectric interface as the charge storage sites, as in metal-nitride-oxide-semiconductor (MNOS) memory transistors.[2] The advantages and disadvantages of these two approaches to the realization of DDC cells is reviewed

briefly. And then the concept of the interfacial dopants, the heart of this paper, emerges as a particularly beneficial compromise between these two concepts, resulting in an optimum DDC cell, with true nonvolatility, yet with undemanding write-erase conditions.

1.1 Floating-gate concept

The early DDC cells were built around a floating gate introduced as the charge-storage site located between the two dissimilar dielectric layers. The charge exchange between the floating gate and Si in this structure was achieved via electron tunnelling through a thin SiO_2 layer grown on the Si substrate. The advantage in the floating-gate concept lies in that the potential well can be tailored to the write-erase needs. In practice, a difficulty was encountered in achieving true nonvolatility in these cells, at least in large-volume-memory situations, because any single shorting path between the floating gate and either the Si substrate or the external gate was sufficient to cause rapid loss of the entire charge on the floating gate. It has been suggested[3] that this shortcoming may be overcome by replacing the continuous-metal floating gate with mutually isolated small metal islands separated by distances shorter than the Debye length at the Si surface. Since then, attempts have been made[4] to fabricate and characterize dual-dielectric MIS cells with metal islands at the dielectric-layer interface. In general, the nonvolatility has not been exceptionally good (the retention time being on the order of several hours) presumably because the existence of the metal islands have degraded the quality of the dielectric layers, leading to higher leakage. The metal islands are also expected to give rise to a field-enhancement effect, causing more rapid stored-charge decay.

A more successful approach[5] to achieve true nonvolatility has been to insert a continuous floating gate between thick (approximately 1000 Å) SiO_2 layers. However, due to its large oxide thickness, this structure would require prohibitively large gate voltages to effect write-erase if tunnelling were to be used. Thus, injection of electrons from Si into the floating gate is accomplished by use of hot electrons created by biasing a nearby pn junction into avalanche.[6] This approach, although it gives rise to excellent nonvolatility, suffers from the lack of a ready electrical means to eject electrons from the floating gate. The erase operation is only possible either by thermal means or by ultraviolet irradiation, thus severely limiting the versatility of these devices. Although some arrangements which permit electrical erasing have been proposed and tested,[7] they usually require increased com-

plexity in the cell structure as well as high gate voltages, and therefore do not appear practical at present.

1.2 MNOS cells

Another DDC cell structure uses the naturally occurring interface states at the dividing planes of the two dissimilar dielectric layers. The structure commonly referred to as the MNOS cell is the outgrowth of Si_3N_4-SiO_2-Si MIS studies carried out initially by Szedon et al.[8] Since then, there has been a considerable amount of work done in this area in the past few years, culminating in experimental memories as large as 2048 bits.[9] It has been well established that ease of write-erase operations in these devices requires use of very thin (a little less than 30 Å) SiO_2 layers on Si so that the charge exchange between the interfacial storage sites and Si may proceed via direct tunnelling across the SiO_2 layers.

Figure 1a, a schematic energy-band diagram of an MNOS structure under bias, illustrates the direct tunnelling mechanism. Electrons from the Si conduction band tunnel through the energy barrier associated with the thin oxide layer to final states at the oxide-nitride interface. Some of these electrons may further penetrate into the nitride layer by hopping along the bulk traps. However, the majority of them are expected to reside at or near the dual-dielectric interface. If the oxide thickness is larger than about 30 Å, an appreciable current flow is possible only when the electrons originating from the Si conduction band tunnel to the conduction band of the oxide and then proceed to the dual-dielectric interface (as in the Fowler-Nordheim tunnelling in Fig. 1b). In this case, however, most of the electrons reach the nitride as hot electrons and only a small fraction of them are captured by the interface states. Since the Fowler-Nordheim tunnelling probability is significantly smaller than the direct tunnelling case at a given field, a higher field must be applied to induce a comparable current density. This would raise the field in the nitride and further impede electron trapping in the nitride. It is clear from the above that the conventional MNOS cells are expected to work well only with thin oxide layers. A similar argument is expected to hold true in the case of hole tunnelling in MNOS structures, although the discussion so far has been given in terms of electron tunnelling for simplicity.

A major drawback in the MOS cells is, however, a direct consequence of the thin SiO_2 layer. The nonvolatility is limited by charge leakage through the thin SiO_2 layer by direct back-tunnelling. Although some claims have been made that nonvolatility of 10 to 100 years is possible

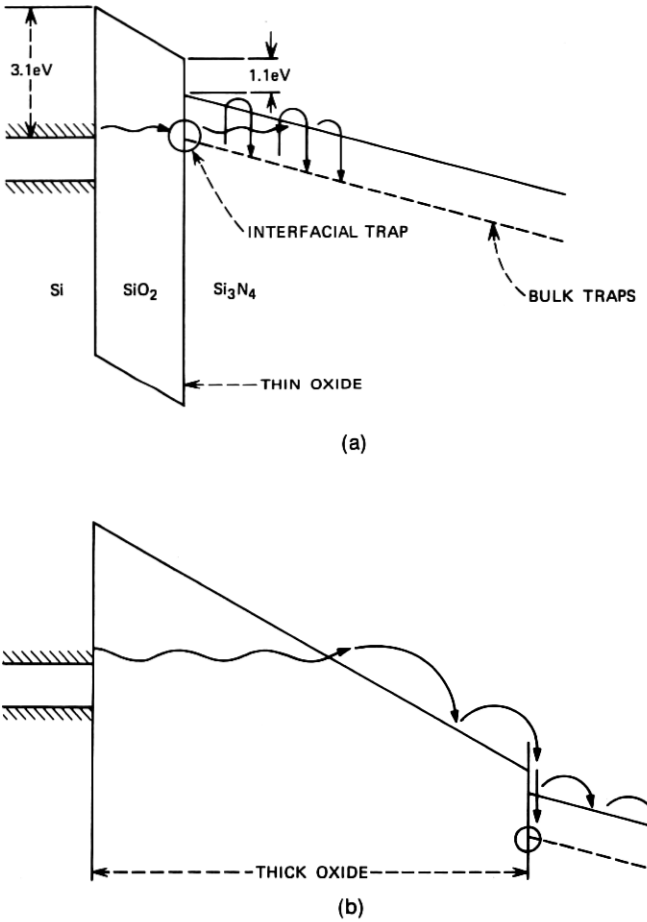

Fig. 1—Energy-band diagram of charging of the dual dielectric interfacial region. (a) Direct tunnelling of electrons. (b) Fowler-Nordheim tunnelling of electrons.

with MNOS structures, it appears that this feat is only achievable by use of thicker SiO_2 layers with the ensuing penalty in write-erase gate-voltage pulse both in height and width. The MNOS structures operable with a short write-erase time, say in 1-μs range, appear to have a non-volatility usually considerably less than 1 year.

Outer dielectric layers other than Si_3N_4 have also been used in dual-dielectric charge-storage cells. A notable example is the use of Al_2O_3. In 1970, Nakanuma et al.,[10] for example, showed that Al_2O_3 is a suitable outer layer. The nonvolatility of these cells is again critically dependent on SiO_2 layer thickness. Cells with SiO_2 layers about 100 Å in thickness

were fabricated and showed good charge retention. However, their write-erase gate voltages had to be 50 volts or more and of 1 ms or so in duration. Also, the ejection of electrons from the interfacial states during the erase operation appears to be rather sluggish, possibly because the density of states is not high enough and/or the barrier height appears to be too high. Some attempts to increase the interfacial state density by, for example, varying the Al_2O_3 deposition conditions appear to result in a lack of reproducibility and/or loss of good nonvolatility.

1.3 Interfacial dopants

It is apparent from the foregoing that while a true nonvolatility in a dual-dielectric cell can only be expected with a structure utilizing relatively thick (greater than 50 Å) SiO_2 layers, this has led to write-erase operations requiring high voltage and/or long pulses. These problems have arisen from the fact that the naturally occurring interfacial states are not really ideal for the various roles they have to play. Attempts to increase their density, which allows shorter time for write-erase, usually result in lossy outer dielectric layers. Although no specific description is available in the literature, past attempts in this regard appear to be comprised of variations in outer-layer-deposition conditions to achieve a certain degree of off-stoichiometric outer layers, at least in the vicinity of the interface.

It is reasonable to expect that if a method for controlling interfacial states without degrading the dielectric properties of the dual-dielectric layers were available, one might overcome the aforementioned difficulties. We wish to show in this paper that, indeed, such a means has been found. Interfacial states induced by certain dopants deliberately located at the interface do have beneficial effects such that considerable improvement in write-erase operations have resulted in conjunction with the use of relatively thick (greater than 50 Å) SiO_2 layers, which are essential for nonvolatility.

Interfacial dopant-induced states of a sufficient density will increase the capture probability of the incoming electrons. This is schematically illustrated in Fig. 2. Furthermore, the energy levels associated with these dopant-induced states will depend on the choice of the dopant. This would allow a suitable condition for the erase operation. The energy levels should not be excessively deep, since this would require a prohibitively high field for ejection of stored electrons. The energy levels should not be too shallow, since the stored charge might easily decay through thermal activation. The naturally occurring interfacial

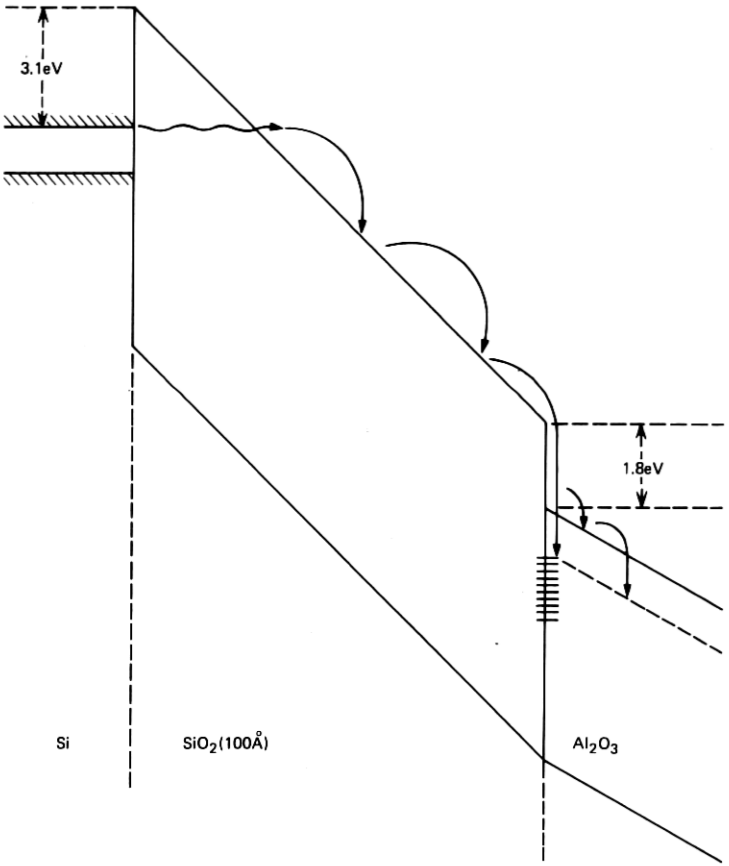

Fig. 2—Energy-band diagram of dopant-induced interfacial states. These states efficiently capture electrons arriving at the dual-dielectric interface following Fowler-Nordheim tunnelling through a relatively thick energy barrier.

states clearly do not possess a comparable versatility as charge-storage sites.

We find that there exists a range of dopant concentration which gives rise to optimum benefits. The upper limit of this range is dictated by the considerations that island formation by the dopant, either during its deposition or during the subsequent outer-layer deposition, is not really desirable since the dielectric property of the dual-dielectric layers is usually degraded. Furthermore, the initial deposition of the outer layers is strongly influenced by the presence of nonuniformity and may result in lossy layers. The upper limit also depends on the choice

of an outer layer and a dopant. Thus, Al_2O_3 with a nonoxidizing dopant such as Ir appears to limit the dopant concentration below $1 \times 10^{15}/cm^2$. On the other hand, Si_3N_4 with W may tolerate up to $5 \times 10^{15}/cm^2$. The lower limit is naturally dictated by the ease of write-erase operations and appears to lie at around $1 \times 10^{14}/cm^2$.

1.4 Selection of dopants

It is desirable that the dopants selected be physically confined at the dual-dielectric-layer interface. This means that both during dopant deposition and during subsequent outer-layer deposition, any migration of the dopant is undesirable. The preferred method for depositing the dopant on the surface of the SiO_2 layer is thermal evaporation. Since good-quality outer layers are, at present, only obtainable through chemical vapor deposition (CVD) techniques at somewhat elevated temperatures of about 900°C, it is important that the deposited dopant does not diffuse into the SiO_2 layer and the outer layer at these temperatures. It is equally important that the deposited dopant does not evaporate away during the first phase of the outer layer growth. The vapor pressures of W, Pt, Ir, Ta, and Nb at 900°C are all lower than 10^{-11} torr.[11] On the other hand, Al has a vapor pressure of 1.5×10^{-5} torr;[11] thus, considerable amounts of Al could be lost. At any rate, control of the final dopant concentration may be more difficult in the case of Al.

The vapor pressures of the dopant oxide may also be an important quantity to consider especially when the outer layer is an oxide layer. For example, tungsten oxide has a vapor pressure of approximately 2×10^{-6} torr.[12] The diffusion constant of Pt into SiO_2 at 900°C is reported[13] to be 7.3×10^{-17} cm²/sec. Compare this with the diffusion constant of Al into SiO_2 at 990°C of 8.2×10^{-14} cm²/sec[14] and that of P into SiO_2 at 900°C of 9×10^{-15} cm²/sec.[15]

It is evident from the above that indeed the suitable dopants available are quite limited in number from the thermodynamic properties alone. The dopant-induced interfacial states should also possess suitable properties. This might narrow the choice down further. We discuss this aspect in more detail when we examine the electrical behavior of these cells, since it is in this aspect that the dopant-induced states come into strong play.

II. CELL FABRICATION

Our experimental vehicles have been capacitors and IGFETs built on an Si substrate about 5-ohm-cm n- or p-type, oriented ⟨111⟩ or

⟨100⟩. The usual mechanical-chemical polish was given before the first thin SiO_2 layer growth was carried out in dilute O_2 in He at about 1100°C. Prior to this important thin-SiO_2-growth step, the wafers were oxidized in 100 percent O_2 to a thickness of about 1000 Å. This initial oxide was kept until the wafer was ready to receive the treatment for the thin oxide layer when this thick oxide layer was stripped in a buffered HF and thoroughly rinsed in deionized water. The thin-oxide-growth time was kept at 10 minutes. The partial pressure of O_2 was varied to give rise to the desired first SiO_2 layer thickness of 50 Å to 150 Å. The dielectric breakdown strengths of the thin-oxide layers were usually 7 to 8 $\times$ 10^6 V/cm defined as the dc field at which the current density reaches 5 $\times$ 10^{-8} A/cm^2.

The dopant evaporation was performed with an E-gun. A quartz oscillator monitor was located about 5 cm away from the source and the samples were located at various distances away from the source depending on the amount of dopant desired. A shutter was employed to initiate the dopant flux as well as to shut it off. An exposure time of 2 minutes was generally used. The monitor had a capability of measuring 5 $\times$ 10^{16}/cm^2 of deposited dopant to within 50-percent accuracy. A dopant concentration of 5 $\times$ 10^{14}/cm^2 could easily be obtained on the sample surface when the sample was located at about 50 cm away from the source.

The dopant-covered samples were then ready for the outer-dielectric-layer deposition, which was either an Al_2O_3 deposition using the well-known techniques of $AlCl_3$-CO_2-H_2 CVD or an Si_3N_4 deposition via SiH_4-NH_3 CVD. A ratio of SiH_4 to NH_3 of about 0.01 was used to obtain Si_3N_4 layers of least conductance.[16] We feel that freedom in choosing CVD conditions for optimum results in outer layers, such as low conductance and/or high-dielectric constant, need not be surrendered in our case since the interfacial states configuration is more or less independent of the chemical nature of the outer layer when the interfacial dopants are employed. This is important because a true nonvolatility requires not only relatively thick SiO_2 layers but also good insulating outer layers. Outer-layer thickness in the 300-Å to 700-Å range were investigated in this study.

Some of the doped and undoped dual-dielectric layers were subjected to Rutherford back-scattering experiments[17] to ascertain dopant location and its concentration. The dopant concentration was within a factor of two of the estimated values from the indication on the monitor. The dopant location is judged to be at the dielectric interface, to the degree that this type of probe can be used to certify this.

The dual-dielectric layers were finally contacted with Al by evaporation from a devitrified carbon crucible through masks defining 15-mil-diameter circular areas for test capacitors. In addition, we have fabricated IGFETs with the dual-dielectric gate insulator for examination, more or less following a standard procedure. Again Al was used as the gate electrode.

III. MEMORY CHARACTERISTICS

IGFET threshold voltages are the most convenient parameter to assess memory behavior of the dual-dielectric charge-storage cells. Figure 3 shows write characteristics of a cell with interfacial dopant W

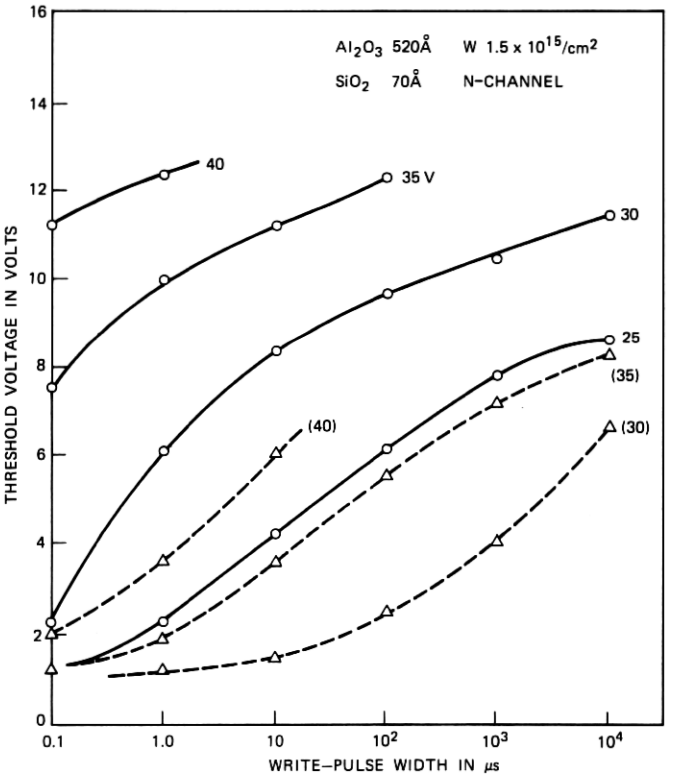

Fig. 3—Shifts in threshold voltage in n-channel IGFETs with dual-dielectric gate insulation consisting of 70-Å-thick SiO_2 and 520-Å-thick Al_2O_3 after application of positive-gate-voltage pulses. Solid lines apply to structures containing 1.5×10^{15}/cm² of W at dual-dielectric interface; dashed lines apply to structures with no interfacial dopant. The initial threshold voltages were at 1 volt.

of $1.5 \times 10^{15}/cm^2$ in concentration. The n-channel IGFET threshold voltages attained after positive-gate-voltage pulses (with respect to the Si substrate) were applied are plotted as a function of pulse width. The threshold voltage was initially at about 1 V. After each pulsing, the threshold voltage shifted to a larger positive value as one might expect since the pulsing resulted in electron injection from the Si substrate into the storage states. The SiO_2-layer thickness was about 70 Å and the Al_2O_3-outer-layer thickness was about 520 Å. It is evident that this structure allows shifts in threshold voltages of as much as 7 V with only a 35-V, 100-ns pulse. A similar shift can be obtained with a 30-V pulse when the pulse width is increased to 100 μs. For comparison, plots are shown obtained with cells located on the same wafer identical to those discussed above, except that the W dopant was not present. These curves are shown in Fig. 3 in dashed lines. With 35 volts, it is necessary to use a 10-ms pulse width to produce a similar shift in threshold voltages.

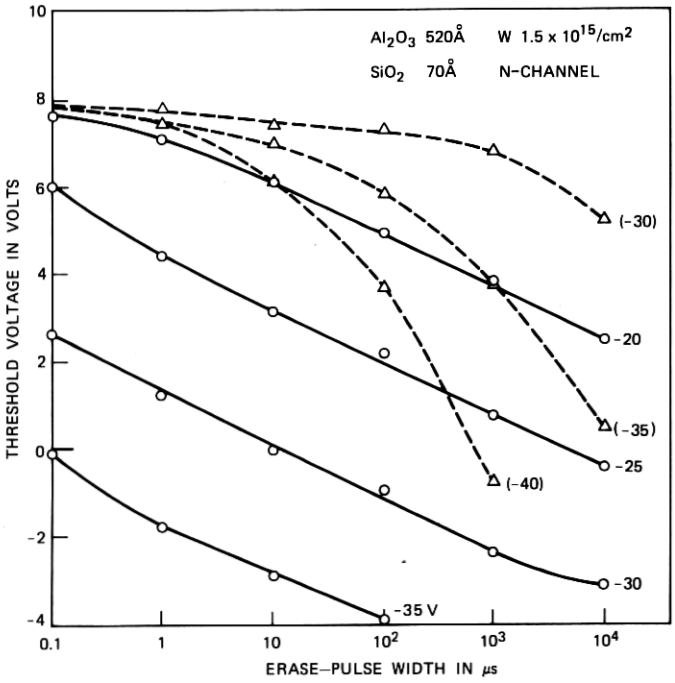

Fig. 4—Shifts in threshold voltage, initially at 8 V, after application of negative-gate-voltage pulses to the IGFETs described in Fig. 1.

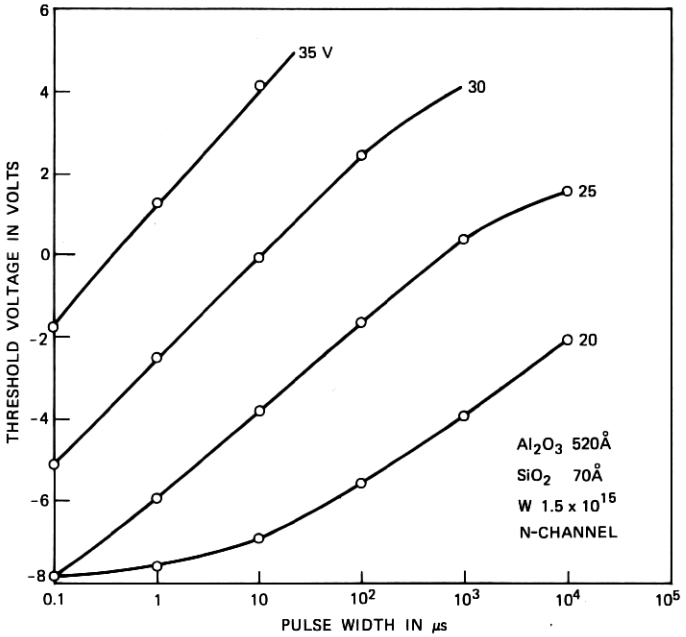

Fig. 5—Shifts in threshold voltages, initially at −8 V, after application of positive-gate-voltage pulses to the IGFETs described in Fig. 1.

Even more spectacular differences between memory cells with and without the interfacial dopant are evident when one examines the erase characteristics shown in Fig. 4. The initial threshold voltage was at 8 V prior to application of erase-voltage pulses. The usual sluggish erase behavior of an Al_2O_3-SiO_2-Si structure has clearly disappeared with similar structures with W as the interfacial dopant. An important additional feature of cells with interfacial dopant W is the fact that Al_2O_3-SiO_2-Si structures allow *positive* charging as well, which is usually not the case without the interfacial dopant. Figure 5 shows the erase characteristics after positive charging to the extent of −8 V in threshold voltage.

Dual-dielectric charge-storage cells with thicker insulator layers show similar improvements when the interfacial dopants are used. Figure 6 shows the erase characteristics of cells with a 100-Å-thick SiO_2 layer and 570-Å-thick Al_2O_3 layer. Again curves pertaining to cells with and without interfacial dopant W are shown for comparison. As expected, the pulse voltages required to induce comparable threshold-voltage shifts are increased from the values needed with thinner structures

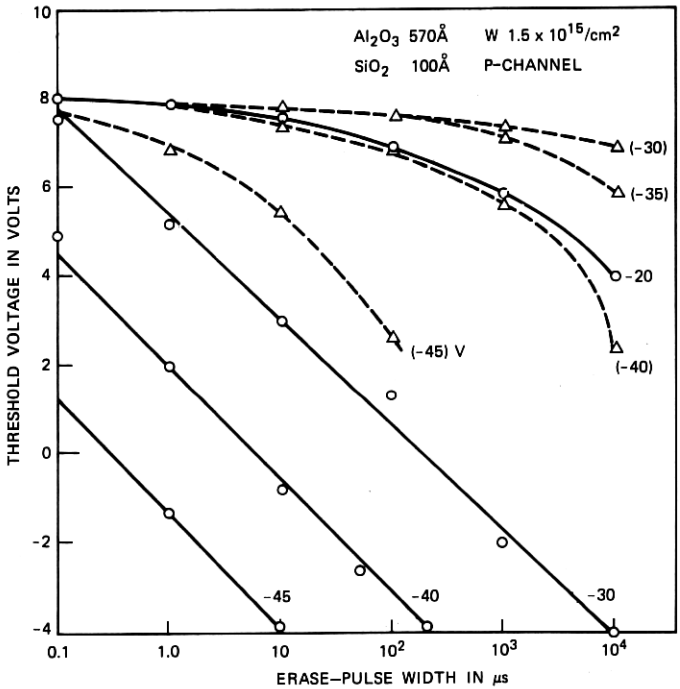

Fig. 6—Shifts in threshold voltage, initially at 8 V, after application of negative-gate-voltage pulses to p-channel IGFETs with dual-dielectric gate insulation consisting of 100-Å-thick SiO_2 and 570-Å-thick Al_2O_3. Solid lines apply to structures containing $1.5 \times 10^{15}/cm^2$ of W at dual-dielectric interface; dashed lines apply to structures with no interfacial dopant.

(Fig. 4). However, dramatic improvements in erase characteristics in structures with the interfacial dopant are clearly evident. Here again, the initial threshold voltage of 8 V was used prior to the erase operation. The write characteristic also shows similar improvements.

One does not expect a strong dependence of the erase characteristics on the initial amount of charge in storage (although the self-induced field is linearly super-imposed on the externally applied field) because the induced field is very small compared to the externally applied field. This is shown in Fig. 7 where the threshold voltages after application of the erase pulse are plotted as a function of pulse height with the initial threshold voltages as a parameter. A pulse width of 200 μs was used for this experiment. As can be seen, the erase curves quickly converge with each other. For a −30-V pulse, the resulting threshold voltages are identical for all practical purposes. This is a useful feature

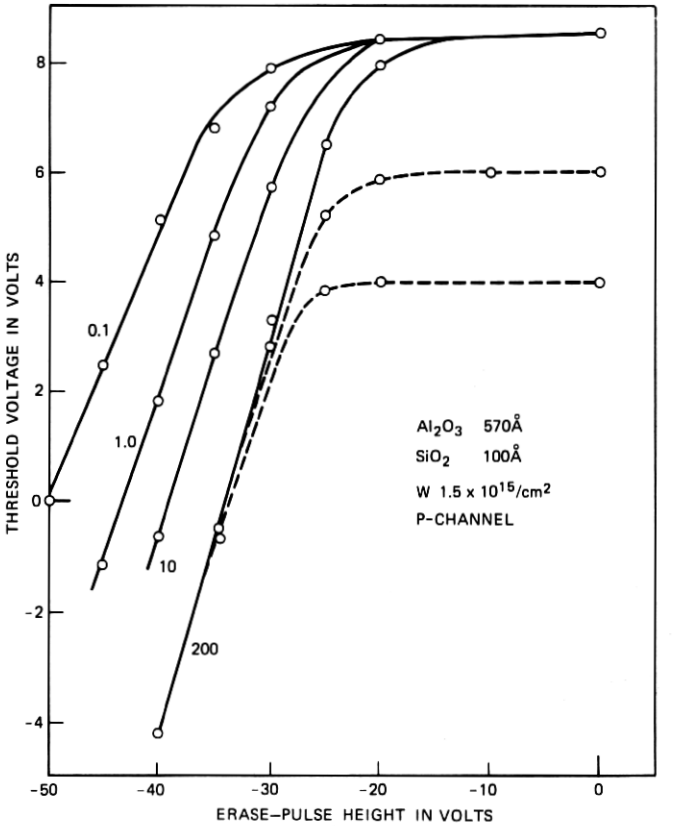

Fig. 7—Shifts in threshold voltages, initially at three different values, in IGFETs described in Fig. 4 after application of negative-gate-voltage pulses of 200-μs duration and various pulse heights. Also shown are shifts in threshold voltages, initially at 8 V, after application of pulses of 10 μs, 1.0 μs, and 0.1 μs in duration.

in that the various initial threshold voltages may represent cells that have gone through various amounts of information storage time after the simultaneous write operation. Figure 7 also shows erase curves using shorter pulse widths for comparison.

The interfacial-dopant concentration is expected to have a lower limit for which the beneficial aspect of the interfacial dopant is not so evident. This lower limit is established to be about 1×10^{14}/cm^2, as can be seen from Fig. 8. Here the amount of interfacial dopant W is 1.5×10^{14}/cm^2. When compared to the mate cell with no interfacial dopant, the erase curves show some effect, but it is not as pronounced

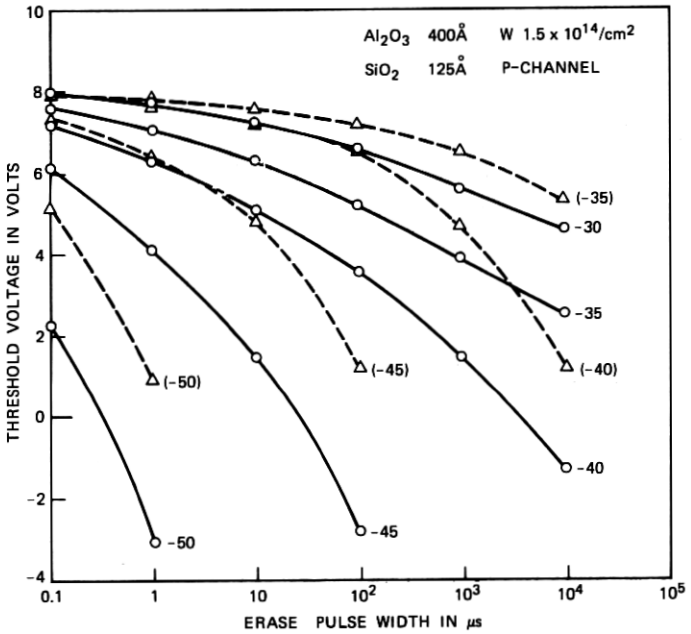

Fig. 8—Shifts in threshold voltage, initially at 8 V, after application of negative-gate-voltage pulses in p-channel IGFETs with dual-dielectric gate insulation of 125-Å-thick SiO_2, 400-Å-thick Al_2O_3. Solid lines apply to structure with $1.5 \times 10^{14}/cm^2$ of W at dual-dielectric interface; dashed lines apply to structures with no interfacial dopant.

as in earlier comparisons with interfacial-dopant concentration at a larger value.

It is well known that MNOS cells do not function well when the SiO_2 layer thickness is larger than 50 Å. This is not the case when the interfacial dopant is introduced. Figure 9 shows write-erase characteristics of MNOS cells with a 500-Å-thick Si_3N_4 layer and a 100-Å-thick SiO_2 layer. Not only does this cell function well with $1.5 \times 10^{15}/cm^2$ of W interfacial dopant but it also shows negative charging. It is virtually impossible to charge MNOS cells negative with any SiO_2 layer thickness when no interfacial dopants are present. The mate cell with no interfacial dopant (see Fig. 9) shows some charging with positive charges. However, it is not possible to erase this cell before a catastrophic breakdown sets in. In Fig. 9, an initial value of 8 V in threshold voltage is again used for erase curves and 1 V for the write curves. For cells with no interfacial dopant, the initial threshold voltage was near zero.

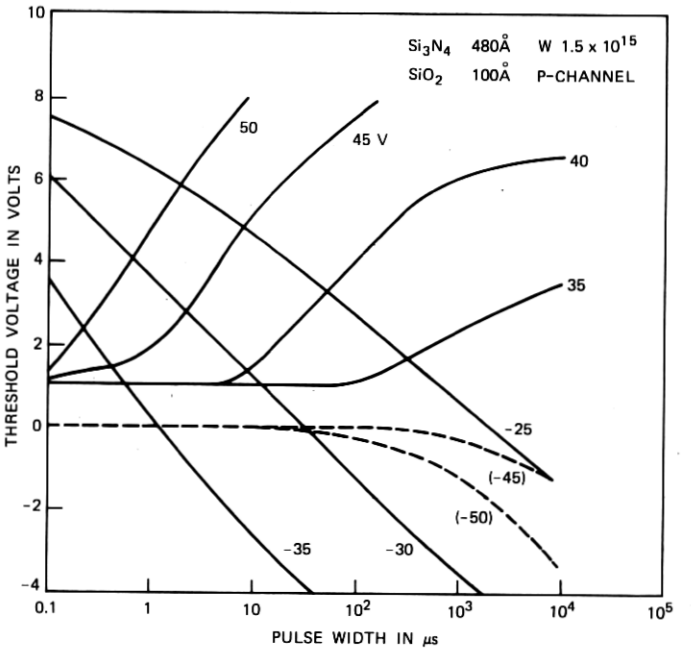

Fig. 9—Shifts in threshold voltages—initially at 1 V after application of positive-gate-voltage pulses, and initially at 8 V after application of negative-gate-voltage pulses—in IGFETs with dual-dielectric gate insulation consisting of 100-Å-thick SiO_2 and 480-Å-thick Si_3N_4 and containing $1.5 \times 10^{15}/cm^2$ of W at dual-dielectric interface. Dashed lines show shifts in threshold voltages, initially at 0 V, after application of negative-gate-voltage pulses in same IGFETs but with no interfacial dopant.

We have also examined dual-dielectric charge-storage cells with interfacial dopants other than W. Ta induces storage states with a behavior indicative of two distinct energy levels for electron trapping. The shallower level can be filled with electrons and emptied as well. However, the second deeper level can only be filled, or at least it was impossible to completely empty this level. This behavior was observed for both Si_3N_4 and Al_2SO_3 outer layers. We do not understand the behavior of Ta-induced states well enough at present to warrant further discussion at this time.

We have also examined Ir-induced interfacial states. Their behavior is fairly close to that of W-induced states. Exact comparison, however, requires a further study. It could be conjectured that the dopant-induced states may show in their behavior marked correlation with the relative oxygen affinity of the dopant employed. Ir and W more or less

lack the ability to steal oxygen from SiO_2 or Al_2O_3 in our thermodynamic environment, while Ta is expected to be oxidized.

IV. SUMMARY AND CONCLUSION

It is shown in this paper that when suitable interfacial dopants such as W are introduced in a well-defined concentration range, the write-erase characteristics of dual-dielectric charge-storage cells are enormously improved. The upper limit of the dopant is dictated by its influence on the dielectric properties of the outer layer and is determined to lie at about $10^{15}/cm^2$ for Al_2O_3. Cells with $5 \times 10^{15}/cm^2$ interfacial dopants showed marked increase in charge leakage. The lower limit is determined to lie at about $10^{14}/cm^2$ by comparison with cells with no interfacial dopants.

The improvement in write-erase characteristics of these cells is of such a magnitude as to allow using relatively thick SiO_2 layers (greater than 50 Å) in these cells, which is mandatory for long memory-retention time (longer than 20 years at 100°C). (Detailed studies of retention time will be published separately.[18]) This study indicates that cells with thinner outer layers (approximately 300 Å of outer layer and approximately 60 Å of SiO_2) that would operate at gate-pulse voltages in the 25-V, 1-μs range, should be feasible.

V. ACKNOWLEDGMENTS

The authors are grateful to R. C. Beairsto for evaporation of impurities, to L. D. Molnar for Al_2O_3 depositions, and to W. R. Costello and F. V. Burckbuchler for Si_3N_4 depositions. We also wish to thank T. Buck for the Rutherford back-scattering experiments for quantitative analysis of the interfacial dopants and C. C. Chang for impurity analysis using Auger spectroscopy.

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