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Bias-Temperature-Stress Studies of Charge Retention in Dual-Dielectric, Charge-Storage Cells

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We present a simple, relatively efficient method to predict the nonvolatility of dual-dielectric, charge-storage cells. Using this method, charge-retention times of several hundred years can be predicted unambiguously from experiments of several days' duration made at elevated temperatures and with externally applied, accelerating fields. The method is first presented in the context of a simple, physically reasonable model of the bias and temperature dependence of the characteristic relaxation time of the device. It is then used to analyze a particular device structure. At 80°C, we predict that this device can maintain a flatband-voltage shift in excess of 4 volts for approximately 500 years. Our analysis suggests that this method can be applied to a variety of dual-dielectric, charge-storage cells to predict their nonvolatilities.

I. INTRODUCTION

The retention time[1–9] of charge in dual-dielectric, charge-storage cells[10–12] (DDC's) is of central importance in evaluating and comparing these devices. An ideal device would hold its charge at a constant level indefinitely. While, of course, such an ideal device is physically impossible, nonideal, charge-storage memory cells have been fabricated that are expected to have minimum charge-retention times on the order of tens of years. And, as such devices are improved, even longer retention times can be expected. The question that naturally arises is how to evaluate such devices in a few days to predict their charge-retention times.

The primary purpose of this paper is to describe a method of bias-temperature stressing in which the decay of the stored charge is greatly enhanced and, as a result, from which one can predict the charge-

retention time of the device under normal operating conditions (zero bias and room, or somewhat higher, temperature). We stress at the outset, moreover, that our primary concern is charge retentivity and *not* device reliability. Bias-temperature-stress methods are often used to good advantage in reliability studies to artificially reduce the lifetime of the device. Here, we are using similar methods to artificially reduce the retention time of charge stored on the device. For reliability studies, one makes use of models in which the device lifetime is governed by temperature and applied bias. Owing to the complexity of the aging, however, these models are often quite tentative. Here we use a well-defined model in which the rate of decay of the stored charge is governed by temperature and bias. As in reliability studies, experimental results are used to determine the parameters of the model. While the bias dependence of the rate of decay of stored charge has been noted previously,[7] the work we report on here is the first in which bias and temperature stressing have been used simultaneously to predict charge retention under normal operating conditions. We feel obligated, therefore, to elaborate our approach and findings in some detail.

At the heart of our method of prediction are the observations (*i*) that there exists an "envelope" function that sets an upper bound on the total stored charge that can be present in the device at any given time, independent of initial conditions, (*ii*) that this envelope function is determined primarily by the characteristic relaxation of the device, and (*iii*) that this relaxation is a strong function of temperature and electric field. By focusing attention on the envelope function, which properly indicates the long-time decay of the stored charge, we avoid incorrect predictions of decay time based on extrapolations of the initial portion of the charge-decay curve. (If the charge decay is plotted versus log time, such predictions are overoptimistic; if it is plotted versus time, such predictions are overpessimistic.) From measured values of the characteristic relaxation obtained at elevated temperatures and under applied bias, relaxation times of interest at room temperature and under zero bias can be predicted. Owing to the nonlinearities inherent in the charge decay, these zero-bias, room-temperature relaxation times are functions of the initial stored charge; the larger the initial stored charge, the smaller the relaxation time. For example, for one version of our device[13] we find that, for an initial charge corresponding to a flatband voltage of 10 V, a relaxation time of $3 \cdot 10^4$ years is predicted; for 7 V, we predict $6 \cdot 10^4$ years. Using our results, predictions of relaxation times can also be made for devices

operated under bias and at other than room temperature. For example, at 80°C under zero bias we predict for 10 V a relaxation time of 100 years and for 7 V 300 years. Linear extrapolations of the initial portion ($t \ll \tau_{relax}$) of the charge-decay curve would result in misleading estimates of charge-retention times on the order of 10^{20} years.

It is important at the outset to stress that we are concerned in this paper with devices[10] with "thick" oxide layers; that is, with oxide layers between the semiconductor and the charge-storage sites sufficiently thick that the rate of decay of charge via back-tunneling through the oxide layer is small compared to the rate of decay of charge through the insulator layer between the storage sites and the gate. While one can accelerate the back-tunneling charge decay of thin-oxide devices[7] by applying an electric field, we believe that, unless one has an exceptionally good means of characterizing the specific tunneling processes of interest, such information is of little direct value in estimating the decay in the absence of such field, i.e., under normal operating conditions. The applied voltage, of course, can accelerate or decelerate decay through the oxide layer or the insulator layer, depending upon its polarity. If electrons are stored, a positive gate voltage enhances the decay in thick-oxide devices because the decay is through the insulator, whereas the same voltage reduces the decay in thin-oxide devices[7] where the primary decay is back through the oxide. One reason for studying thick-oxide devices is to determine the limits on the retention time of charge-storage devices imposed by charge decay through the insulator layer. Such limits are of considerable interest, especially for devices whose back-tunneling decay is sufficiently low that, based on this decay mechanism alone, one might exaggerate the device's charge-storage capabilities.

In this paper we first discuss in general terms the physical processes that lead to the decay of the stored charge. A relatively thick oxide layer is used so that the primary discharging current is through the insulator layer. This current through the insulator is found to be characterizable as a thermally activated flow of charge via defects with a very low, but strongly field-dependent, mobility. We then discuss how this strong temperature and electric-field dependence of the decay current can be used to controllably accelerate the discharging of the DDC. A simple, physically reasonable, empirical model is introduced to explain the experimentally measured decay of the flatband-voltage shift in time with temperature and externally applied bias as parameters. The mathematical expression for the decay current is sufficiently simple that all quantities of interest, particularly device relaxation

times, can be calculated analytically. From the high-temperature, high-accelerating-field results, it is possible to predict low-temperature, zero-bias behavior. We can thus unambiguously determine nonvolatility on the order of tens or hundreds of years on the basis of experiments performed in several days or weeks.

Before proceeding, it must be emphasized that the method of bias-temperature stressing that we develop here is not limited to devices which behave according to our simple empirical model. Indeed, as we point out in Appendix A, the central ideas at the heart of the method are valid, within certain limits, to a variety of models: the method is, within certain bounds, insensitive to the details of the actual decay process. We discuss the physical processes that we believe are operative in our devices first, however, because this will permit the reader to familiarize himself with the actual devices to which our method is then applied. Although our results indicate the general features of a particular, detailed decay model, we emphasize that we are not primarily concerned with establishing the existence of such a model.

II. PHYSICAL PROCESSES

The structure and fabrication of the memory devices studied here have been described in detail elsewhere.[13] For our purposes here, it suffices to note that a typical device consists of the following layers (see Fig. 1): a metallic contact (taken fixed at zero voltage), n- (or p-) type silicon, 70 to 200 Å of SiO_2 (referred to as the oxide layer, or simply the oxide), a set of suitable dopant-induced storage states (referred to as the storage states), 400 to 500 Å of Al_2O_3 or Si_3N_4 (referred to as the insulating layer, or simply the insulator), and a metallic contact (referred to as the gate). Inclusion of the specific states, which are the interfacial dopant-induced states, makes it possible to store either electrons or holes, whichever is desired, as well as to provide very well-defined storage sites for the elementary charges. The oxide and the insulator are sufficiently thick that tunneling from one side of either to the other side can be neglected.

The device can be charged either negative or positive as follows. Negative charge can be stored by driving the gate to a high positive voltage (≈ 50 V) for a short period of time (≈ 100 μs). Some electrons in the Si tunnel into the conduction band of the oxide, traverse the oxide, and then are trapped in the storage states or pass completely through the device to the gate electrode. Positive charge is stored by driving the gate negative to force electrons out of the storage states, through the oxide, and into the semiconductor.

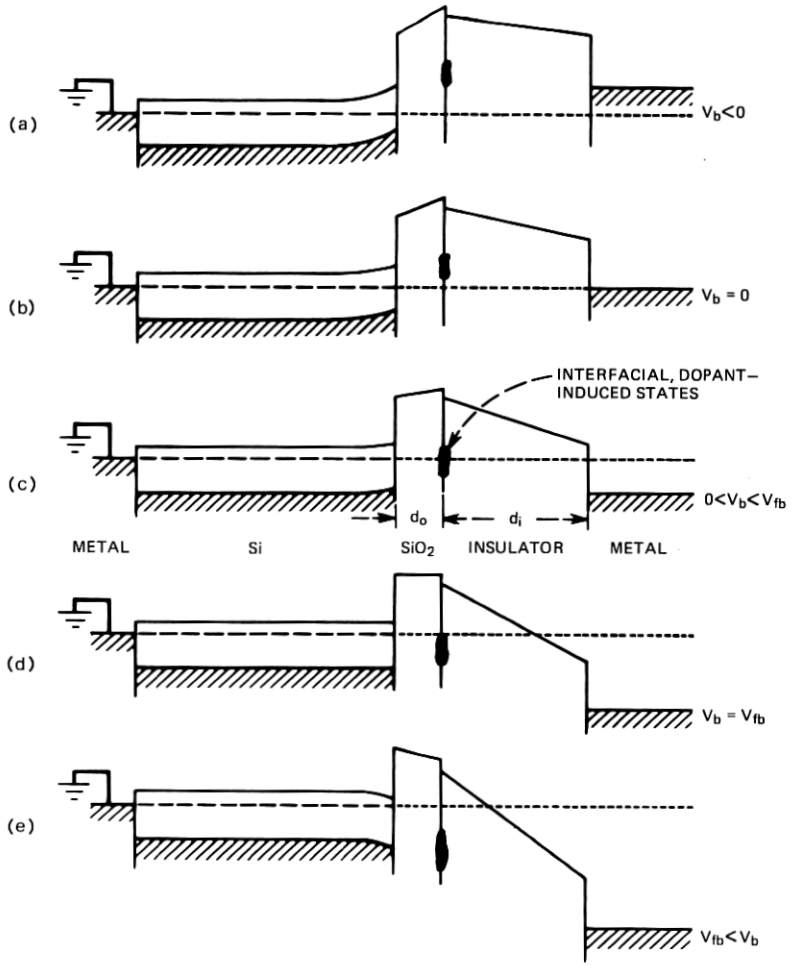

Fig. 1—Schematic of the structure of the MIOS memory device under five different, applied-bias conditions. The location of the interfacial, dopant-induced, charge-storage states is indicated. They are assumed to be charged negative.

Our experimental results indicate that these multilayered memory devices discharge as follows. (Refer to Fig. 1 in which a device is shown under five different biases. Note, in particular, Fig. 1a, in which the semiconductor is inverted near the SiO_2.) The (negative) stored charge produces large electric fields in both the oxide and the insulator. In the first few hundred milliseconds, some fraction of the charge is lost through thermionic emission or tunneling into the conduction bands of

the oxide and/or the insulator. For most of the stored charge, however, the trapping levels are sufficiently deep that these processes are very improbable. Charge can tunnel into traps in the insulator, and through such imperfections a discharging current can pass into the conduction band of the insulator and flow to the gate. Some charge can also pass completely through the insulator in the forbidden band by means of these traps. In addition, in a similar manner, a discharging current can be present in the oxide and flow to the Si.

The size of the discharging current is expected to be strongly field dependent.[1–9] In addition, we note that increasing the (positive) gate voltage enhances the electric field in the insulator and decreases this field in the oxide. The manyfold increase in the decay current which occurs when a positive voltage is applied to the gate thus implies that the primary discharging current is passing through the insulator. Inversely, when a negative voltage is applied to the gate, a decrease in the decay current is observed. In this case, the change in the applied fields is such as to increase the current through the oxide and decrease the current through the insulator. A detailed study of the reverse gate-bias decay was not undertaken because of the long time intervals required even at high temperatures. For the present, it is sufficient to note that the total decay current increases with positive voltage and decreases with negative voltage applied to the gate.

The physical details of the transport of the charge within the insulator can be narrowed down as follows. The strong temperature enhancement of the decay of the charge indicates that thermal activation rather than tunneling plays the dominant role in enabling charge to be transferred toward the gate. The question of whether the charge passes through the insulator to the gate entirely within the forbidden band, or partially in the conduction band, is more difficult. The relatively low thermal activation energies observed (≈ 0.6 eV) suggest that the rate limiting portion of the transport is not associated with the conduction band. If it were, much higher decay currents would be expected. We infer, therefore, that the current is controlled by the traps in the bulk of the insulator.

For charge transport from one trap to the next, one might expect the current to be proportional to $\exp[(E_o + q\mathcal{E}a/2)/kT]$, according to Poole's law.[14] (Here E_o is an ionization energy, $\mathcal{E}$ is the electric field in the insulator, and a is the intertrap spacing.) However, Poole's law, or its extension and modification by Frenkel[15,16] and others[17–19] include only the thermal excitation of carriers and do not include velocity-versus-field effects connected with the transport from one site

to the next.[20] Current density is proportional to qnv, where n is the number of charges per unit volume and v is the carrier velocity. One expects n to be thermally activated; however, in an insulator, v can be a rapidly varying function of applied fields,[21–23] whether electron transport is in the conduction band or in a defect "band," as seems to be the case here. Thus, whereas for pure Frenkel-Poole behavior the excitation of electrons is the rate-limiting, field- and temperature-modulated process, for our devices both n and v are so modulated.

Our experimental results indicate that the discharging current is proportional to the empirical expression

$$\mathcal{E}_o(T) \exp(-E_a/kT) \exp[+\mathcal{E}/\mathcal{E}_o(T)], \tag{1}$$

where $\mathcal{E}_o(T)$ is a very slowly varying, *decreasing* function of the temperature T. To the accuracy of the experiments, the activation energy E_a is independent of the applied field. The decrease of $\mathcal{E}_o(T)$ with temperature could be due to an increased overlap between polarized electronic states because of increased lattice vibrations. The electric field dependence can in general be expected to be more complicated than that given in eq. (1). Fortunately, eq. (1) suffices for our purposes, partially because the decay curves are relatively independent of the detailed dependence of the discharging current on electric field. See Appendix A for a discussion of more complicated field dependences.

One final point should be made regarding the decay current. As part of the assumption that the rate-limiting process controlling the charge decay is the trap-controlled current within the bulk of the insulator, we have assumed that the number of carriers in transit is independent of time. In other words, as a trap in close proximity to the storage states loses its charge to a trap somewhat closer to the gate, the emptied trap is quickly refilled with a charge from a storage state. Thus, the average time for a charge to pass from a storage state to an empty trap is much less than the average time for a charge to pass from one trap to the next. This results from the high density of storage states, and makes the effective number of carriers available for transit independent of the magnitude of the stored charge and hence independent of time. This is reasonable throughout most of the decay owing to the large number of stored electrons. Near the end of the decay, however, when the amount of stored charge is much less than its initial value, the rate-limiting process may become the transfer of charge from the storage states into the insulator. We ignore this effect, since, by the time it becomes important, the fundamental relaxation time of the device will be well determined.

From the foregoing discussion, it is evident that we can artificially enhance the decay greatly by increasing the temperature and the electric field in the insulator. In so doing, however, we must be very careful that we do not excessively enhance charge-transport mechanisms that under normal operating conditions would play no significant role. For example, by applying too large a potential at the gate, the field in the oxide will be enhanced to such an extent that the storage layer will be slowly charged by electrons tunneling from the Si into the conduction band of the oxide. Excessive temperatures, on the other hand, may enhance decay into the insulator's conduction band, exaggerating this mode of charge transport. These effects are often easily detected experimentally, and they give rise to upper limits on the increases in temperature and electric field possible to enhance charge decay for measurement purposes.

Although the decay of charge from the storage states can be enhanced by increasing either the temperature or the insulator electric field, the enhancement from either is insufficient to bring the decay times into the range of days. However, this can be achieved by combining higher temperature with higher fields. Of course, we again must be careful to avoid introducing decay processes that under normal conditions would be insignificant. (An example of this would be Schottky emission.) Nonetheless, we find that we can obtain the entire charge decay curve within a few days (at most) without introducing extraneous decay mechanisms. From these curves, we can predict the normal decay curve and hence the charge-retention time of the memory element. In this way we avoid having to determine this retention time by extrapolating the initial portion of the time dependence of the charge decay. In the next section we see how the nonlinear dependence of the rate of decay on the quantity of stored charge leads to characteristic, charge-decay curves from which one can predict the nonvolatility of DDC's.

In those cases where certain alternative conduction mechanisms are activated, this method may or may not work. In some devices, the charge decay is via Fowler-Nordheim tunneling from the storage states into the conduction band of the oxide or the insulator, or it is via direct tunneling from these states into the semiconductor. Neither of these decay currents will be affected by changes in the temperature; however, both such currents will be strongly modulated by applied bias. In the case of Fowler-Nordheim tunneling, our method is directly applicable. For direct tunneling, however, in which the primary decay is via Si-SiO_2 interfacial states, we must be very careful as we increase

the bias not to enhance the tunneling into semiconductor states in the valence or conduction band, which under normal conditions would play no important role in the discharging of the DDC. Perhaps one can modulate the decay by altering the thickness through which the electrons tunnel, either by physically squeezing the sample or by constructing samples of varying thicknesses.

III. EMPIRICAL MODEL AND MEASUREMENT TECHNIQUE

Let us assume that we have some (negative) charge stored in the interfacial, dopant-induced states. The quantity of charge stored in these states is proportional to the measurable flatband voltage V_{fb}. Also proportional to V_{fb} is the field in the insulator under zero-bias conditions. In the presence of a finite bias voltage V_b, an additional field proportional to the bias voltage will be linearly superimposed on the zero-bias field (with a *different* constant of proportionality). Thus, using expression (1) and expressing fields in terms of voltages, we write for the time rate of change of V_{fb}, the flatband voltage,

$$\frac{dV_{fb}}{dt} = -\frac{V_s(T)}{\tau(T)} \exp\left[\frac{V_{fb} + bV_b}{V_s(T)}\right], \tag{2}$$

where V_s and τ are experimentally determined functions of temperature only and b is a relative constant of proportionality (see Appendix B). Equation (2) presumes decay via the insulator; for decay through the oxide, one would have the factor $(V_{fb} - V_b)$ in place of the factor $(V_{fb} + bV_b)$. This empirically satisfactory expression is reasonable physically, as explained in Section II. It also permits a simple, analytic treatment of all significant features of the decay. Should the flatband voltage decay according to a relation other than (2), one can still employ bias-temperature stressing. This is indicated in Appendix A.

Before solving eq. (2), we should clarify two points. (*i*) We do not require eq. (2) to be valid for $t < 1$ minute. It may be valid there but, being interested in the long-time decay of the charge, all we need to do is to integrate eq. (2) from some time t_1, on the order of minutes after charging, when the experiments are begun. (*ii*) Since dV_{fb}/dt does not vanish as $(V_{fb} + bV_b) \to 0$, eq. (2) is clearly not valid as $t \to \infty$. As remarked in Section II, this difficulty results from assuming that there are always a large number of stored charges, whereas in fact near the end of the decay this number becomes small. Again, this difficulty need not concern us, since we do not have to consider the leakage after the bulk of the stored charge has decayed away. (See Appendix A for a

more general treatment.) With these limitations in mind, we proceed to solve eq. (2).

The solution to eq. (2) follows at once after a separation of variables and an integration from (t_1, V_1) to (t, V_{fb}). The resulting $V_{fb}(t)$ for the decay of the flatband voltage as a function of time t at temperature T and applied bias V_b is given by

$$V_{fb}(t) = V_s(T) \log_e \{(\exp [-V_1/V_s(T)] + [(t - t_1)/\tau(T)] \cdot \exp [bV_b/V_s(T)])^{-1}\}. \quad (3)$$

For a single value of T, this function is sketched in Fig. 2 as a function of $\log_{10} (t/t_1)$ for several V_b and for hypothetical, illustrative values of V_s, τ, and b. The purpose of plotting as a function of $\log_{10} (t/t_1)$ is to call attention to the *actual* long-time behavior of $V_{fb}(t)$. For $t_1 < t \ll \tau(T) \exp [-(V_1 + bV_b)/V_s(T)]$, $V_{fb}(t)$ is relatively flat. However, for $t \gg \tau(T) \exp [-(V_1 + bV_b)/V_s(T)]$, $V_{fb}(t)$ is given approximately by $V_e(t)$ where, if $\dot{t}_1$ is any convenient scale factor,

$$V_e(t) = V_s(T) \log_e [\tau(T)/\dot{t}_1] - bV_b - V_s(T) \log_e (t/\dot{t}_1). \quad (4)$$

The function $V_e(t)$ is the previously mentioned envelope function for each T and V_b. It is shown dashed in Fig. 2. (Note $\log_e x = \log_{10} x / \log_{10} e$.) Although $\dot{t}_1$ may be assigned the same value as t_1, the two

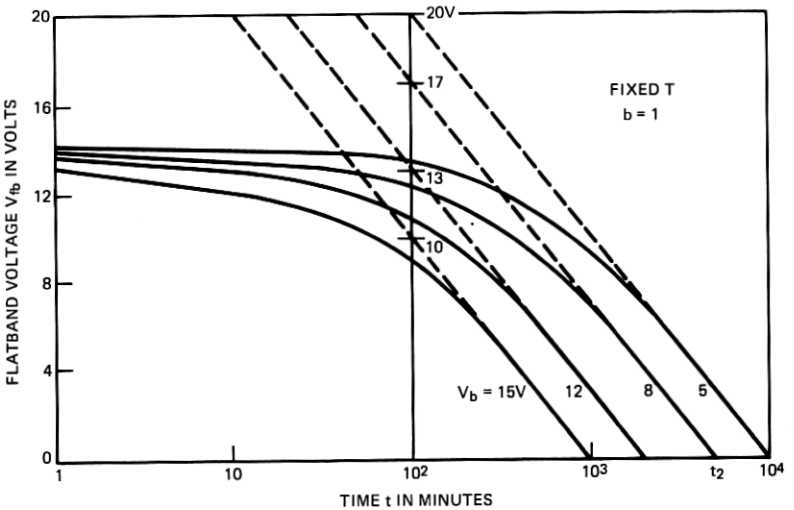

Fig. 2—Schematic illustrating a possible decay of the flatband voltage $V_{fb}(t)$ as a function of $\log_{10} (t/t_1)$ in a hypothetical device for four different applied biases V_b at a fixed temperature T. For simplicity, we set $b = 1$. Also shown are the envelope functions $V_e(t)$ associated with each V_b.

must be distinguished. Our t_1 refers to an initial condition, while $V_e(t)$ is independent of the initial conditions, t_1 and V_1, and satisfies $V_{fb}(t) < V_e(t)$ (see Appendix C) and

$$V_{fb}(t) \approx V_e(t), \quad t \gg \tau \exp\left[-(V_1 + bV_b)/V_s\right]. \tag{5}$$

When $V_e(t)$ is plotted versus $\log_{10}(t/t_1)$, V_s is the slope and τ is the intercept $[V_e(\tau) = 0]$ for zero bias ($V_b = 0$). From the experimental $V_{fb}(t)$ curves obtained for several V_b at a given T, it is possible to readily determine $\tau(T)$, $V_s(T)$, and b, the three parameters in eq. (4). From the envelope function $V_e(t)$ drawn tangent to $V_{fb}(t)$ as shown in Fig. 2, we obtain $V_s(T)$ from the slope of $V_e(t)$, b from the difference between $V_e(t)$ (for fixed t) at different V_b, and $\tau(T)$ from the value t_2 of t where $V_e(t) = 0$:

$$\log_e\left[\tau(T)/t_1\right] = \log_e\left(\frac{t_2}{t_1}\right) + \frac{bV_b}{V_s(T)}. \tag{6}$$

In Fig. 2, t_2 for $V_b = 8$ V is shown ($t_2 = 5 \cdot 10^{+3}$ minutes). It is a test of the form of eq. (2) that $V_s(T)$, b, and $\tau(T)$ be independent of V_b to within experimental accuracy. That this is indeed the case is discussed in Section IV. We now repeat the above for other temperatures in the range $150°C \leqq T \leqq 300°C$. We find that both $\tau(T)$ and $V_s(T)$ appear to be "thermally activated":

$$\tau(T) = \tau_o \exp(E_a/kT), \quad V_s(T) = V_{so} \exp(E_s/kT). \tag{7}$$

Since the slope V_s may arise from a combination of physical processes, identifying it with a thermally activated process may be somewhat misleading. (The parameter b is a weakly decreasing function of T. Since we are interested only in predicting zero bias ($V_b = 0$) behavior, we need not concern ourselves further with extrapolating b to room temperature. In other words, we can for each temperature use the b measured at that temperature to extrapolate to zero bias. Once we know the zero-bias result, we can extrapolate to the desired temperature. Since b enters only as bV_b and V_b is zero, this latter extrapolation can be performed without knowledge of b.) The quantities τ_o, E_a, V_{so}, and E_s are obtained from the usual $(1/T)$ plots. We assume, and indeed from our discussion in Section II it is not unrealistic to expect, that we may extrapolate τ and V_s to room temperature using (7). We must now relate these quantities to the characteristic relaxation time τ_{relax}, the charge retention time, of the storage device.

In Fig. 3 we define $\tau_{\text{relax}}(\tau_r)$ graphically, again for hypothetical device parameters. It is simply the "roll-off" time of $V_{fb}(t)$: $V_e(\tau_{\text{relax}}) = V_1$, where $V_1 = V_{fb}(t_1)$. [As shown in Appendix C, $V_1 \approx V_{fb}(0)$

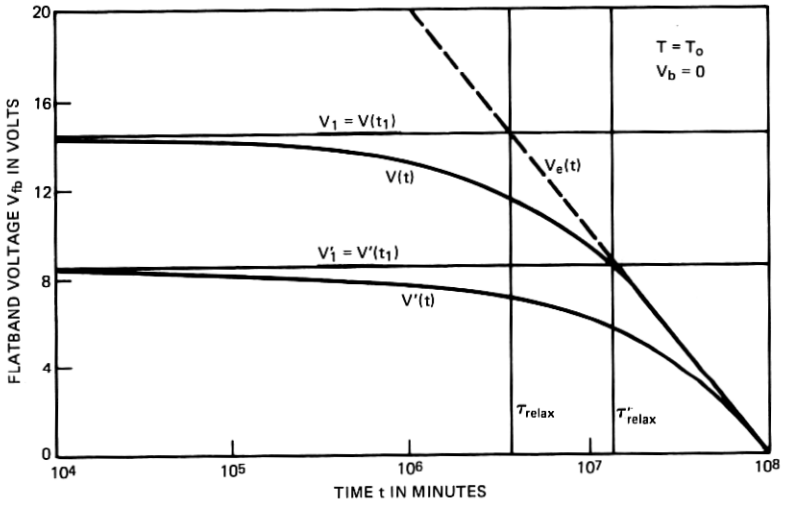

Fig. 3—Schematic illustrating a possible decay of the flatband voltage $V(t)$ in a hypothetical device for room temperature ($T = T_o$) and zero applied bias ($V_b = 0$) for two different quantities of stored charge, V_1 and V_1'. The size of the characteristic relaxation time τ_{relax} is indicated for both cases. Note that $V_1 - V_1^o = V_1' - V_1'^o = 0.69\ V_s$.

for $t_1 \ll \tau_{relax}$.] Solving (4) for τ_{relax} at room temperature T_o for $V_b = 0$, we obtain

$$\tau_{relax} = \tau(T_o) \exp\left[-V_1/V_s(T_o)\right]. \tag{8}$$

Indicative of the nonlinearities inherent in the charge-decay process, τ_{relax} is a function of the initial stored charge, and hence the initial flatband voltage V_1, increasing as V_1 decreases. (Compare τ_{relax} and τ'_{relax} corresponding to different amounts of initial stored charge V_1 and V_1', respectively, in Fig. 3.) Again we emphasize that τ_{relax} cannot be obtained from (linearly) extrapolating $V(t)$ based on its behavior for $t \ll \tau_{relax}$. Since τ_{relax} is on the order of 10^4 years at room temperature for devices reported on here, it is doubtful whether room-temperature, zero-bias experiments alone will be able to predict τ_{relax}.

Although τ_{relax} provides a measure of the charge retention time of the device, we must, in addition, know how far V_{fb} has decayed below V_1 by the time τ_{relax} before full significance can be attached to this definition of characteristic decay time. Returning to eq. (3) and letting $t_1 = 0$, $V_1 = V_1^o$, $V_b = 0$, we obtain for $V_{fb}(t)$ under zero bias

$$V_{fb}(t) = V_s \log_e \left[e^{+V_1^o/V_s} \left(1 + \frac{t}{\tau_{relax}}\right)^{-1} \right]. \tag{9}$$

In arriving at eq. (9), we have used eq. (8). Thus,

$$\begin{aligned} V_{fb}(\tau_{\text{relax}}) &= V_1^0 - V_s \log_e 2 \\ &= V_1^0 - 0.69 V_s. \end{aligned} \tag{10}$$

We thus obtain the very important result that, at the roll-off time τ_{relax}, V_{fb} has dropped $0.69V_s$ volts below its initial value. This amount is independent of V_1^0, the initial flatband voltage. Of course, $V_{fb}(\tau_{\text{relax}})$ must be several volts positive so that eq. (2) will still be valid. In addition, $0.69V_s$ thus defines the decay that must be taken into account when including this device in circuits. In determining V_s from the envelope of a decay curve, one must be careful to convert from $\log_{10}$ to $\log_e$:

$$V_s = \frac{V_e(t_1) - V_e(t_2)}{\log_{10}(t_2/t_1)} \times 0.434,$$

where $0.434 = \log_{10} e$.

Another characteristic decay time is the time at which the flatband voltage drops below a certain margin voltage V_m. We refer to this time as the margin time, τ_{margin}, or simply τ_m. It follows at once from eq. (9) that τ_m as a function of V_m and V_1 is given by

$$\tau_m = \tau(T)\{\exp[-V_m/V_s(T)] - \exp[-V_1/V_s(T)]\} \tag{11}$$

as a function of T under zero bias conditions. A plot of τ_{margin} is presented in the next section.

IV. EXPERIMENTAL RESULTS

Bias-temperature-enhanced, charge-relaxation experiments were carried out on the recently devised dual-dielectric, charge-storage cells.[13] Aluminum oxide (Al_2O_3, $\epsilon = 9$) was used as the insulator. The thickness d_o of the SiO_2 ($\epsilon = 4$) was 125 Å, and that of the Al_2O_3, d_i, 550 Å. Thus, $b = C_o/C_i$ [see eq. (25)] is predicted to be given by

$$b = \frac{C_o}{C_i} = \frac{\epsilon_{SiO_2} A}{d_o} \frac{d_i}{\epsilon_{Al_2O_3} A} = 2.0.$$

Experimental values for b ranging from 0.8 to 1.2 were obtained over the temperature range of $150°C \leqq T \leqq 300°C$. The reason for this discrepancy is not known. Some possible explanations are discussed in Appendix D. The area of the devices was about $1 \cdot 10^5$ μm^2, and the doping of the n-type silicon was about $6 \cdot 10^{15}$ per cm^3. Tungsten of a density of about 2 to $3 \cdot 10^{14}$ per cm^2 was used to produce the interfacial storage sites.

Table I

Sample*	T (°C)	$1/T \cdot 10^3$	V_b (volts)	V_e (volts)	t_2 (minutes)	b	$\tau(T)$ (minutes)
H15-4	150	2.36	15	2.44	$2.6 \cdot 10^4$	1.2†	$3.75 \cdot 10^7$
H15-1	200	2.11	10	1.93	$1.3 \cdot 10^4$	1.12	$4.3 \cdot 10^6$
H15-1			15	1.92	$7.7 \cdot 10^2$		
H15-4	250	1.91	7	1.76	$2.7 \cdot 10^4$	1.03	$1.7 \cdot 10^6$
H15-4			10	1.76	$4.7 \cdot 10^3$		
H15-1	300	1.74	5	1.53	$4.6 \cdot 10^3$	0.8	$6.2 \cdot 10^5$
H15-1			10	1.52	$3.3 \cdot 10^2$		

* H15 is the wafer label and 1 or 4 is the chip label.
† Estimated value.

Table I presents a summary of the experimental results which we have analyzed most carefully. Four representative charge decay curves are plotted in Fig. 4. The envelope function $V_e(t)$ associated with each curve is shown as well. From the $V_e(t)$ we obtain the data given in Table I. One might do better by attempting to fit the actual experimental curves with eq. (3), but we have found $V_e(t)$ adequate for our purposes.

In studying Fig. 4 one may wonder why the slope of the decay curves seem to diminish at higher temperatures. In fact, as is clear from eqs.

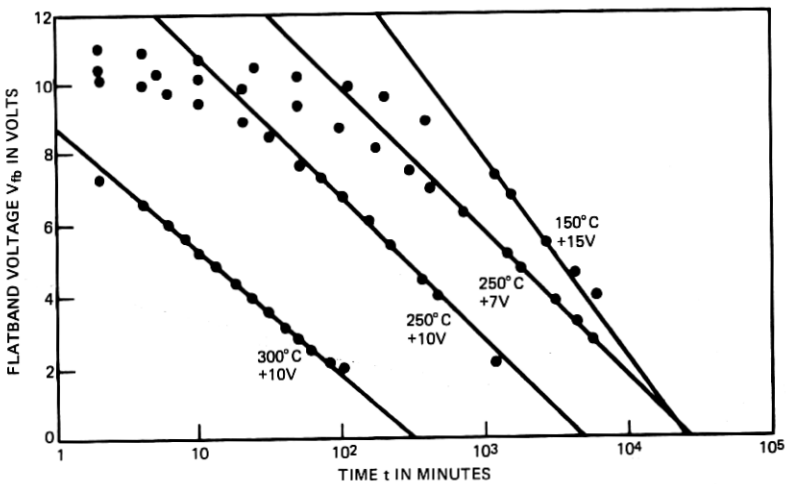

Fig. 4—Experimental results under four different conditions: T = 150°C, V_b = 15 V; 250°C, 7 V; 250°C, 10 V; 300°C, 10 V. In each case, the element was charged by setting V_b = 50 V for 100 μs.

(2) and (7), $|dV_{fb}/dt|$ increases as T increases, as one would expect. One must remember that we are plotting $V_{fb}(t)$ versus $\log_{10}(t/t_1)$. Thus, the enhanced decay has shifted $V_{fb}(t)$ to lower t, reducing the apparent decay of V_{fb} when plotted on a $\log_{10} t$ scale. The authors must admit to having expended some effort themselves getting used to plotting V_{fb} versus $\log t$ rather than $\log V_{fb}$ versus t, as is common in many decay problems.

By plotting the values of τ and V_s given in Table I as functions of $1/T$, the activation energies $E_a = 0.61$ eV for τ and $E_s = 0.065$ eV for V_s can be determined [see Fig. 5 and eq. (7)]. From Fig. 5 we can also calculate τ_o and V_{so} [eq. (7)]: $\tau_o = 2.0$ minutes and $V_{so} = 0.41$ V. Using the E_a, τ_o, E_s, V_{so} so determined, we use eq. (7) to extrapolate $\tau(T_o)$ and $V_s(T_o)$, where T_o is room temperature (290°K, 17°C). We find $\tau(T_o) = 7.7 \times 10^{10}$ minutes and $V_s(T_o) = 5.5$ V. With these values, we can predict the room-temperature, zero-bias relaxation times using eq. (8).

The activation energy E_a of 0.61 eV is comparable to activation energies ranging from 0.4 to 1.2 eV reported for Frenkel-Poole conduction through oxide layers.[24–28] We conclude, therefore, that E_a may be interpreted as being associated with an activation process. Although E_s is relatively small, being on the order of several kT's, its existence does result in an appreciable variation of V_s with T (as observed experimentally). We do not have a simple independent quantitative explanation of its magnitude and caution the reader against interpreting E_s as being associated with a simple, thermally activated process.

As discussed in Section III, the charge-retention time of our dual-dielectric, charge-storage cell is well-characterized by the device "roll-off," or relaxation time, as defined in Fig. 3. Owing to the nonlinear dependence inherent in the charge decay, τ_{relax} depends upon the "initially" stored charge, which we denote in terms of flatband voltages by $V_1 = V_{fb}(t_1)$. In Fig. 6 we plot τ_{relax} as a function of V_1 for several temperatures of interest. For room temperature and a V_1 of 10 V, τ_{relax} is $3 \cdot 10^4$ years; for 7 V, $6 \cdot 10^4$ years. That τ_{relax} is a function of stored charge should be carefully noted. Lastly, we note that, for room temperature at τ_{relax}, V_{fb} has dropped $(0.69)(5.5) = 3.8$ V below V_1. At 80°C the drop is only 2.4 V owing to the reduced value, of V_s (=3.4 V at 80°C). However, now τ_{relax} for 10 V is only 100 years, and for 7 V, 300 years.

In Fig. 7 we plot τ_{margin} as a function of V_1 for zero bias and for the same temperature used in Fig. 6. As is obvious physically, the larger

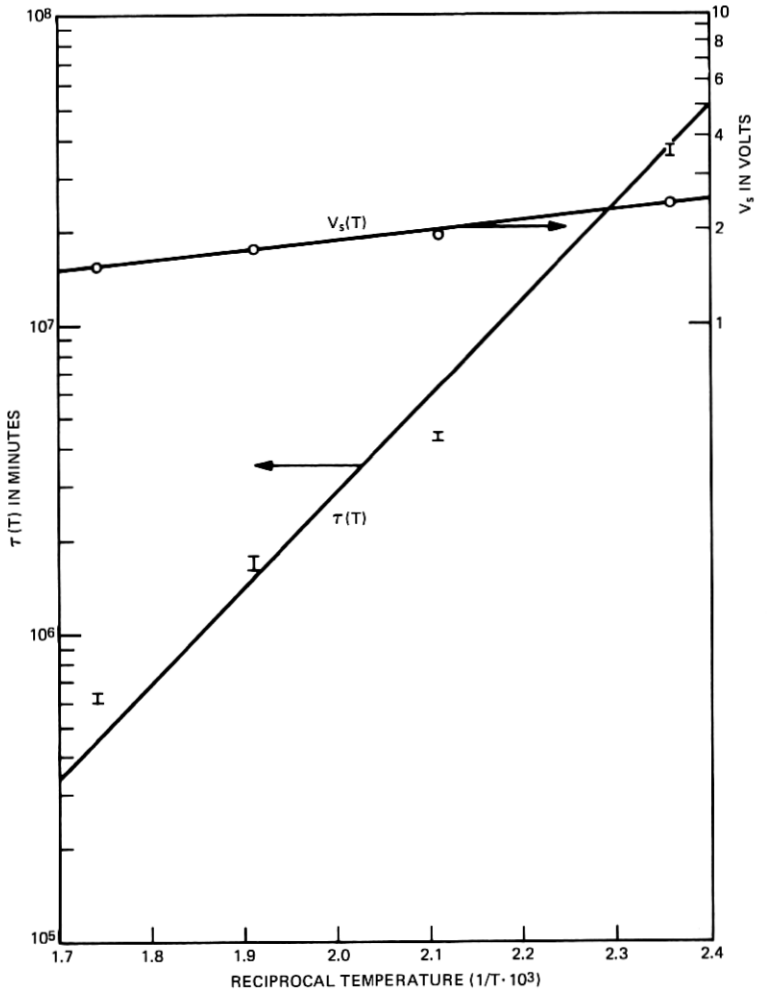

Fig. 5—Experimentally determined parameters τ and V_s plotted versus $1/T$ to determine the activation energies E_a and E_s.

the initial stored charge (initial flatband voltage V_1), the longer the time required for the flatband voltage to drop to the margin voltage V_m, here taken to be 4 V. The horizontal lines give the upper limit or largest possible τ_{margin} for the given temperature. For V_1 between 4 and 5 V, τ_m goes rapidly to zero, as is clear from Fig. 3. For V_1 less than 4 V, τ_m is obviously meaningless.

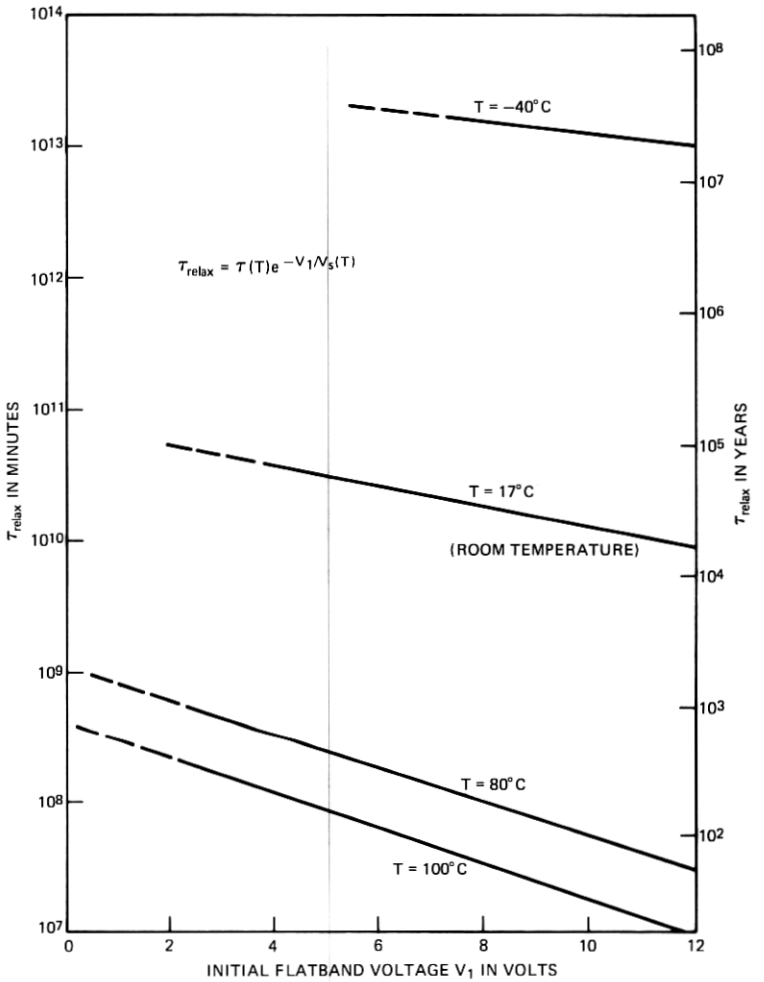

Fig. 6—The predicted roll-off or device relaxation time for zero-applied bias ($V_b = 0$) and temperatures of −40°C, 17°C, 80°C, and 100°C plotted as a function of "initial" flatband voltage $V_1 = V(t_1)$, where $t_1 = 1$ minute.

V. CONCLUSION

In this paper we have discussed a method of predicting the retention time of charge in dual-dielectric, charge-storage cells. The method is based on the realization that an envelope function $V_e(t)$ exists, that this function is determined primarily by the characteristic relaxation of the device, and that this relaxation is a strong function of tempera-

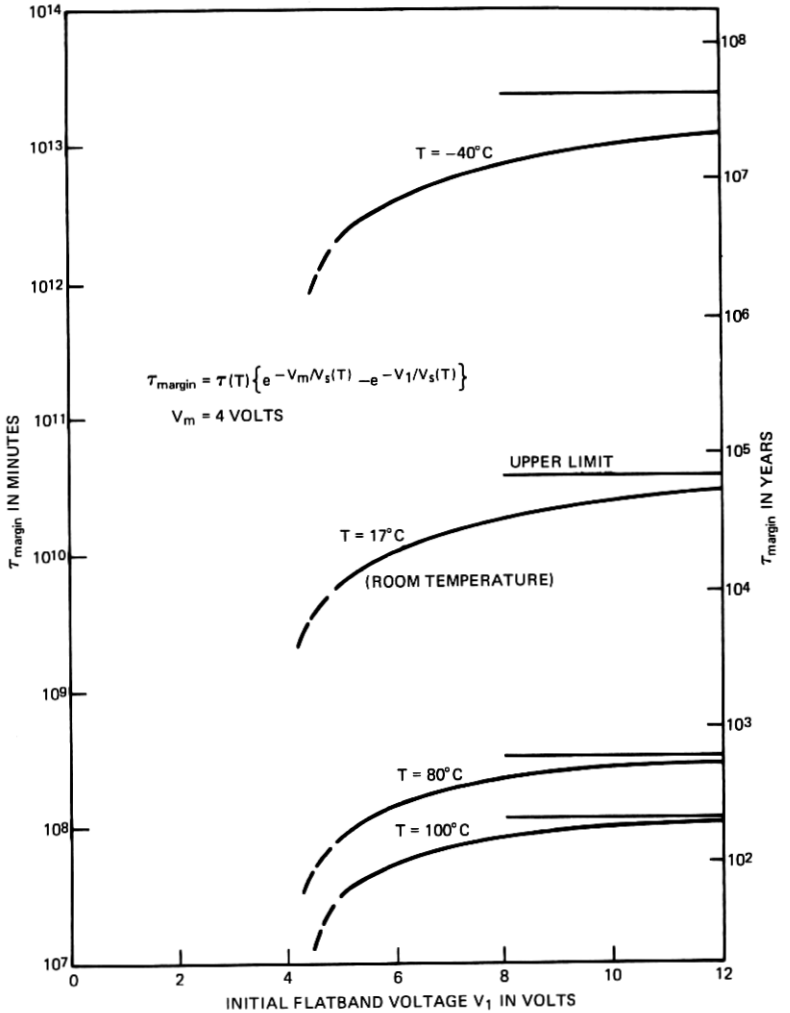

Fig. 7—The predicted margin time for zero-applied bias ($V_b = 0$) and temperatures of −40°C, 17°C, 80°C, and 100°C plotted as a function of "initial" flatband voltage $V_1 = V(t)$, where $t_1 = 1$ minute. The horizontal line above each curve is the upper limit for τ_{margin} as V_1 is taken larger and larger.

ture and applied bias. By choosing an appropriate function to represent the dependence of the discharging current on the applied bias and stored charge, it is possible to discuss all the interesting features of the time-dependent charge decay in terms of simple mathematical expressions. We were thereby able to predict, on the basis of experimental

data obtained under bias-temperature stressing of representative devices, the time dependence of the shift in the flatband voltage at zero bias and operational temperatures (room temperature to 80°C). In particular, we can characterize the nonvolatility of the DDC's in terms of a roll-off or relaxation time τ_r and a margin time τ_m, both dependent on the level of initial charging. Although these times are on the order of 10^4 years, they were determined from experimental data taken over a period of only a few weeks. This was possible because our method of bias-temperature stressing greatly enhances the dominant discharging processes, speeding up the charge decay without introducing significant decay from otherwise insignificant decay modes. Because of this, we feel that our method will greatly facilitate the realistic prediction of the nonvolatility of DDC's.

VI. ACKNOWLEDGMENTS

We wish to thank D. M. Boulin for his assistance in preparing and charging the devices studied and W. J. Sundburg for his measurements of insulator and oxide layer thicknesses.

APPENDIX A

Equations (1) and (2) in the text are admittedly oversimplified, despite the ease they render in interpreting the data. Nonetheless, the characteristic decay $V(t)$ discussed in the text is approximately obtained in a variety of cases, e.g., tunneling or Frenkel-Poole, even when it is known that the rate of decay is proportional to more complicated voltage dependences than exp (V/V_s). It is the purpose of this appendix to outline why this is so. For simplicity, we assume that conditions are such that only one decay mode is important.

Usually we can write the decay of the stored charge, or, equivalently, that of the flatband voltage V, in the following form,

$$\frac{dV}{dt} = -[f(V + bV_b) - f(0)], \tag{12}$$

where, in turn,

$$f(V') = Ae^{g(V')}, \quad V' = V + bV_b, \tag{13}$$

A being a dimensional constant and $g(V')$ a function of temperature and applied bias as well as of various powers of V' (and possibly of $\log_e V'$). The point of writing $f(V')$ in the form given in (13) is to focus primary attention on the exponential nature of the functional depen-

dence of $f(V')$ on V. Thus, $f(V')$ can be approximated over a wider range of V by a Taylor expansion of $g(V')$ in (13) than by a Taylor expansion of $f(V')$ directly.

Suppose at $t_1 \ll \tau_{\text{relax}}$, $V = V_1$. Then, assuming $f(0) \ll f(V')$ for V of interest, we can readily integrate (12) if we approximate $g(V')$ by $g(V_i') + \gamma(V - V_1)$, where γ may be chosen in various ways ($V_i' = V_i + bV_b$). For example, we may desire upper and lower bounds for $V(t)$, in which case we can use upper and lower bounds for $g(V')$. In some cases, $\gamma = g'(V_1')$ or $\gamma = [g(V_1') - g(V_2')]/(V_1 - V_2)$ give such bounds. In all cases, we obtain the characteristic decay of which eq. (3) is one example.

A somewhat more appealing approach that avoids approximating quantities in exponents is the following.[28,29] Again, assume $f(0) \ll f(V')$ to write the integral of (12) in the form

$$t_2 - t_1 = -\int_{V_1}^{V_2} \frac{dV}{f(V')} = -\frac{1}{A}\int_{V_1}^{V_2} \frac{dVe^{-g(V')}g'(V')}{g'(V')}. \tag{14}$$

According to the intermediate-value theorem, this becomes

$$\begin{aligned} t_2 - t_1 &= -\frac{1}{A}\frac{1}{g'(V_3')}\int_{V_1}^{V_2} dVe^{-g(V')}g'(V') \\ &= \frac{1}{A}\frac{1}{g'(V_3')}[e^{-g(V_2')} - e^{-g(V_1')}], \end{aligned} \tag{15}$$

where $V_2 < V_3 < V_1$. (Physically, we must have $g'(V') > 0$.) Thus, given V_1 and t_1, for each V_2 of interest, t_2 follows from (15) to within the uncertainty of choosing $g'(V_3')$. (This will normally be, at most, a factor of 2 for $V_2 \approx 1/2V_1$.) The envelope function $V_e(t)$ follows at once from (15) by setting t_1 and $\exp[-g(V_1')]$ to zero.

$$t = e^{-g(V_e')}/Ag'(V_3'). \tag{16}$$

If we note that $V_e'(t) = V_e(t) + bV_b$, differentiating (16) with respect to V_b at fixed t and assuming that $g'(V_3')$ is only weakly dependent on V_b, it follows at once that

$$\frac{dV_e}{dV_b} = -b.$$

Under these conditions, the vertical separation between envelope functions $V_e(t)$ corresponding to two different applied biases V_b^1 and V_b^2 (at the same temperature) will be $b(V_b^1 - V_b^2)$, even when these

envelope functions are not straight lines, but are given in general by (16).

Equation (15) may be rewritten in the characteristic form as

$$g(V_2') - g(V_1') = -\log_e [1 + Ae^{g(V_1')}g'(V_3')(t_2 - t_1)], \qquad (17)$$

where we may write

$$g(V_2') - g(V_1') \approx g'(V_4')(V_2 - V_1). \qquad (18)$$

Equation (18) follows from the mean-value theorem ($V_2 < V_4 < V_1$). Thus, while it is clear that the exact solution will in general not be precisely given by (17) and (18), such a solution will still show the same general features as the above for physically reasonable $g(V)$. It should be noted that, since $g'(V_3')$ and $g'(V_4')$ actually represent averaged quantities, and since $g(V_1')$ is simply an initial condition, the results given in (17) and (18) are rather insensitive to the detailed dependence of $g(V')$ on V.

One final point should be noted. For V sufficiently small and $V_b = 0$, we may write

$$\frac{dV}{dt} \approx -f'(0)V. \qquad (19)$$

The solution to (19) is the common exponential decay {exp $(-t/t_o)$, $\tau_o = [f'(0)]^{-1}$} now with voltage V an exponential rather than a logarithmic function of time t. For $t \gg \tau_{\text{relax}}$, clearly $V(t)$ will be of this form. But this is well beyond the region in time of the primary decay of the charge, and it is this primary decay governed approximately by (17) to (18), which is of crucial importance for evaluating charge storage devices.

APPENDIX B

B.1 Decay through the insulator

Section II indicated that the electric field $\mathcal{E}$ in the insulator drives the charge-decay current [see eq. (1)]. This electric field arises from the stored charge and the applied bias. The purpose of this appendix is to express $\mathcal{E}$ in terms of two measurable voltages, the flatband voltage, which measures the stored charge, and the applied-bias voltage.

Let C_o be the capacitance of the oxide in series with the semiconductor, and let C_i be the capacitance of the insulator. We assume C_o (as well as C_i) is independent of voltage. (We thus ignore the bias dependence of the semiconductor capacitance.) Simple capacitative

division implies that, if V_b is applied to the gate and there is no stored charge, then the voltage $\bar{V}_b$ dropped across C_i is given by

$$\bar{V}_b = V_b \frac{1/C_i}{1/C_i + 1/C_o}. \tag{20}$$

On the other hand, if a charge Q is stored and $V_b = 0$, then the voltage $\bar{V}_a$ across C_i is given by

$$\bar{V}_a = Q(C_i + C_o)^{-1}. \tag{21}$$

See Fig. 1b. But Q is related to the flatband voltage V_{fb} by the relation

$$Q = C_i V_{fb}. \tag{22}$$

See Fig. 1d. Thus,

$$\bar{V}_a = V_{fb} \frac{1/C_o}{1/C_i + 1/C_o}. \tag{23}$$

The total voltage drop V_T across C_i, which produces $\mathcal{E}$, will in general be a superposition of the two; thus,

$$V_T = \bar{V}_a = \bar{V}_b \frac{1/C_o}{1/C_i + 1/C_o} (V_{fb} + bV_b), \tag{24}$$

where

$$b = C_o/C_i. \tag{25}$$

In passing from eq. (1) to eq. (2) in the text, we have let $V_s(T)$ absorb the prefactor (24). Thus, $V_s(T)$ depends both on the physical processes of the decay and on the geometry of the device.

It is important to note that b can be greater than as well as less than unity. In principle, b can be computed from knowledge of C_o and C_i. It is more easily obtained from the measured decay curves, a more reliable method. Its slight temperature variation is somewhat of a puzzle. If at higher temperatures additional capacitances C_i' and C_o' arose in series with C_i and C_o, respectively, then b would become b' given by

$$b' = \frac{C_o}{C_i}\left(\frac{1 + C_i/C_i'}{1 + C_o/C_o'}\right). \tag{26}$$

One expects the semiconductor portion of the device C_o to be more susceptible to degradation than the insulator side C_i. If $C_i' = \infty$ and $C_o' < \infty$, then $b' < b$, as observed. For lower temperatures, b is close to its value predicted by (25). Fortunately, b is determined within experimental error at a given temperature to be independent of V_b. Thus, at each temperature we can predict zero-bias behavior. We can

then predict room temperature, zero-bias behavior from higher temperature, and zero-bias behavior *without* knowledge of b. This is because only the factor bV_b enters eq. (2), and $V_b = 0$ for zero bias.

B.2 Decay through the oxide

If the primary discharging current is through the oxide (rather than through the insulator, as assumed throughout this paper), then the electric field that produces this current must be calculated from the voltage across the oxide. Using the notation introduced above, we note that the portion $\bar{V}_b'$ of the bias voltage V_b dropped across the oxide is

$$\bar{V}_b' = V_b \frac{1/C_o}{1/C_i + 1/C_o}. \tag{27}$$

On the other hand, it is clear from Fig. 1b that the contribution $\bar{V}_a'$ of the voltage resulting from the stored charge is just $\bar{V}_a$ given by (23). Thus, the total voltage drop V_T' across C_o is given by

$$V_T' = \bar{V}_a' - \bar{V}_b' = \frac{1/C_o}{1/C_i + 1/C_o}(V - V_b). \tag{28}$$

Thus, unlike the case of V_T (24), no geometrical factor analogous to b enters.

APPENDIX C

In this appendix, we derive two minor results used in the text.

(*i*) To show that $V_{fb}(t) < V_e(t)$, we need only compare the argument of the $\log_e$ in eq. (3) with $t_1 = 0$ and $V_1 = V_1^0$ with that of eq. (4) when written

$$V_e(t) = V_s \log_e \left[\left(0 + \frac{t}{\tau} e^{bV_b/V_s} \right)^{-1} \right]. \tag{29}$$

From (3), we have

$$V_{fb}(t) = V_s \log_e \left[\left(e^{-V_1/V_s} + \frac{t}{\tau} e^{bV_s/V_s} \right)^{-1} \right]. \tag{30}$$

As the argument of the $\log_e$ in (30) is less than that in (29), it follows at once that

$$V_{fb}(t) < V_e(t). \tag{31}$$

[Additional decay mechanisms important for very short times (<1 minute), which are not included in (30), will, of course, reduce V_{fb}

even further.] It may be noted that V_1 and t_1 may be chosen so that $V_{fb}(t)$ given in (3) exceeds $V_s(t)$ and V_{fb} approaches V_s from above. Such unphysical behavior would result if one mistakenly chose a value of t_1 too large; that is, if, after completing the charging of the device ($t = 0$), one recorded V_1 at t_1 using a clock that read a time sufficiently larger than 0 at $t = 0$.

(*ii*) To show that $V_1 \approx V_1^o$ when $t_1 \ll \tau_{\text{relax}}$, we calculate V_1 from eq. (3), in which we set $V_1 = V_1^o$, $t_1 = 0$, and $V_b = 0$. Then it follows that

$$V_1 = V_s \log_e \left[e^{V_1^o/V_s} \left(1 + \frac{t_1}{\tau_{\text{relax}}} \right)^{-1} \right]. \tag{32}$$

If now $t_1 \ll \tau_{\text{relax}}$ (the usual case), then

$$V_1 \approx V_1^o - \frac{t_1}{\tau_{\text{relax}}} V_s. \tag{33}$$

Since $V_s < V_1^o$ and $t_1 \approx 10^{-2}\tau_{\text{relax}}$ at most (for room temperature and zero bias 10^{-7} is typical), we may use $V_1 \approx V_1^o$ to a very good degree of approximation. The actual, initial, flatband voltage may be larger than V_1^o, owing to other decay mechanisms which may be important for $t < 1$ minute. It is V_1 [or V_1^o obtained from V_1 using eq. (3)], however, with which we are concerned.

APPENDIX D

The "b-Factor"

The disagreement between the predicted b-factor (25) of 2.0 and the much smaller measured b-factor (Table I) of 0.8 to 1.2, which we shall call b', calls into question our assumption that the electric field in the insulator is spatially constant. This follows because, if the field is spatially constant (and if the current per carrier depends only on the electric field, as is physically reasonable), then the measured and predicted b-factors, b' and b, would agree. Since, in fact, they do not agree, we conclude that the field is not spatially constant, a result, perhaps, of charge stored in the insulator. It is the purpose of this appendix to investigate some consequences of charge stored in the insulator (in addition to charge stored at the oxide-insulator interface) on the decay of the flatband voltage V_{fb}.

Let us begin by asking what information our flatband-voltage measurements tell us in light of the possibility of having charge storage in the insulator. Referring to our empirical result (2), we note that, at a fixed temperature, the rate of decay of $V_{fb}(t)$ is a function of

$[V_{fb}(t) + b'V_b]$. Thus, whatever electric field governs the decay of $V_{fb}(t)$, it too must depend on V_{fb} and V_b in the form $[V_{fb}(t) + b'V_b]$.

The next step is to express the various fields and voltages of interest in terms of the stored charge. Let $Q_s(t)$ be the charge stored at the oxide-insulator interface at time t, $\rho_i(x, t)$ the density of charge stored in the insulator, ϵ_i the dielectric constant of the insulator, and ϵ_o that of the oxide. It follows (see Fig. 1d) that the flatband voltage is given by

$$V_{fb}(t) = \frac{Q_s(t)}{C_i} + \int_0^{d_i} \frac{\rho_i(x, t)}{\epsilon_i} (d_i - x)dx \tag{34}$$

$$\equiv V_s(t) + V_m(t) \tag{35}$$

$$= \int_0^{d_i} \frac{\rho_T(x, t)}{\epsilon_i} (d_i - x)dx \tag{36}$$

$$\equiv V_T(t), \tag{37}$$

where

$$\rho_T = \rho_i + (Q_s/A)\delta(x). \tag{38}$$

Here A is the cross-sectional area of the device, d_i is the thickness of the insulator, $\delta(x)$ is the usual delta function, V_s is the contribution of Q_s to V_{fb}, and V_m (the m referring to moment of charge) is the contribution of the charge stored in the insulator to V_{fb}. (Throughout our discussion, we are assuming that *no* charge is stored in the oxide.) A straightforward but more involved calculation leads to the electric field in the insulator, $0 < x < d_i$, under general charging and applied-bias conditions:

$$E(x, t) = (1 + b)^{-1}\left[\frac{Q_s(t)/d_i}{C_i} + b\frac{V_b}{d_i} + \int_0^x dx' \frac{\rho_i(x', t)}{\epsilon_i}\left(1 + b\frac{x'}{d_i}\right) - \int_x^{d_i} dx' \frac{\rho_i(x', t)}{\epsilon_i} b\left(1 - \frac{x'}{d_i}\right)\right] \tag{39}$$

$$= (1 + b)^{-1}\left[b\frac{V_b}{d_i} + \int_0^x dx' \frac{\rho_T(x', t)}{\epsilon_i}\left(1 + b\frac{x'}{d_i}\right) - \int_x^{d_i} dx' \frac{\rho_T(x', t)}{\epsilon_i} b\left(1 - \frac{x'}{d_i}\right)\right]. \tag{40}$$

If we integrate (39) or (40) over the insulator, we obtain the average field times d_i, the voltage drop across the insulator $V_d(t)$ given by

$$V_d(t) = (1 + b)^{-1}[V_s(t) + V_m(t) + bV_b] = (1 + b)^{-1}[V_{fb}(t) + bV_b]. \tag{41}$$

Using these results, we can discuss what physical effects can and cannot lead to the observed behavior ($b' < b$).

Owing to the presence of charge in the insulator, the electric field at the oxide-insulator interface will be reduced from its value in the absence of such charge. If $E(0^+, t)$ controls the decay, perhaps this reduction can lead to a reduced b-factor. Unfortunately, this effect would result in ($b' > b$) rather than ($b' < b$). To see this, we note from (39) that

$$\begin{aligned} E(0^+, t) &= (1 + b)^{-1} d_i^{-1} [V_s(t) + bV_b - bV_m(t)] \\ &= \frac{b/b'}{(1 + b)d_i} \left[\frac{b'}{b} V_s(t) - b'V_m(t) + b'V_b \right]. \end{aligned} \tag{42}$$

If this expression is to be a function of $[V_{fb}(t) + b'V_b]$, it is necessary that

$$V_{fb}(t) = (b'/b)V_s(t) - b'V_m(t). \tag{43}$$

To satisfy both (35) and (43), it is necessary to have

$$V_m(t) = \frac{1/b - 1/b'}{1/b + 1} V_{fb}(t) \tag{44}$$

and

$$V_s(t) = \frac{1 + 1/b'}{1/b + 1} V_{fb}(t). \tag{45}$$

However, if $b' < b$, then $1/b < 1/b'$, and the coefficient of $V_{fb}(t)$ in (44) is negative. This is rather disturbing since, as a result of the initial charging and subsequent decay of the charge through the insulator, one would expect $V_m(t)$, as defined in (35), to be positive. In addition, (44) implies that, as V_{fb} decreases during charge decay, V_m must increase algebraically. This can occur only if charge stored at the oxide-insulator interface becomes trapped in the insulator neutralizing the charge trapped there. This effect would be enhanced if more charge were neutralized near the interface ($x = 0$) than in the middle of the insulator. Although this may be the source of ($b' < b$), the origin seems physically unreasonable of the bulk trapped charge of sign opposite the stored charge which, although not neutralized by the charging current, is neutralized by the decay current. We conclude that, if ($b' < b$), then the field at the interface probably does *not* control the charge decay.

We note in passing that, since the voltage drop $V_d(t)$ across the insulator (41) is already a function of $[V_{fb}(t) + bV_b]$, it also cannot

be the average field in the insulator which is controlling the decay. This hardly requires further elaboration.

One effect that charge stored in the insulator has on the decay is to enhance the electric field near gate ($x = d_i$) relative to the field near the interface ($x = 0$). This enhancement may be sufficient to remove charge stored in the region $x_o < x < d_i$ of the insulator during the initial portion of the decay, leaving significant stored charge only in the region $0 < x < x_o$ of the insulator and at the interface. If, during the remainder of the decay, the decay rate is governed by the electric field at x_o, we then expect to observe ($b' < b$). Let us see how this comes about.

If $\rho_i(x, t) = 0$ for $x > x_o$, then the electric field at $x = x_o$ is, according to (39), given by

$$E(x_o, t) = \frac{b/b'}{(1 + b)d_i} \left\{ \frac{b'}{b} V_s(t) + b'V_b + \frac{b'}{b}\left[(b + 1) \frac{Q_i(t)}{c_i} - bV_m(t) \right] \right\}, \quad (46)$$

where

$$Q_i(t) \equiv A \int_0^{d_i} dx' \rho_i(x', t) \quad (47)$$

$$= A \int_0^{x_o} dx' \rho_i(x', t), \quad (47a)$$

the size of the stored charge in the insulator. Alternatively, using (40) for the field, we obtain

$$E(x_o, t) = \frac{b/b'}{(1 + b)d_i} \left[-b'V_T(t) + \frac{b'}{b} (1 + b) \frac{Q(t)}{c_i} + b'V_b \right], \quad (48)$$

where $Q(t)$ is the total stored charge defined by

$$Q(t) \equiv Q_s(t) + Q_i(t). \quad (49)$$

For $E(x_o, t)$ to be a function of $(V_{fb} + b'V_b)$, it is necessary that [using (37)]

$$V_T = -b'V_T + \frac{b'}{b} (1 + b) \frac{Q(t)}{C_i} \quad (50)$$

or that

$$V_T(t) = \frac{1 + 1/b}{1 + 1/b'} \frac{Q(t)}{C_i}. \quad (51)$$

Now ($b' < b$) implies that $C_i V_T(t) < Q(t)$, which means in turn that some charge is stored in the insulator, a consistent result.

Having seen how a measured b-factor (b') can arise which is less than the computed b-factor (b), we must inquire as to whether the effect is sufficient to explain the measured results. For simplicity, let us assume that ρ_i is uniform for $0 < x < x_o$. Then it follows that

$$V_T = \frac{Q_s}{C_i} + \frac{Q_t}{C_i}(1 - x_o/2d_i). \tag{52}$$

It then follows from (48), (51), and (52) that

$$\frac{Q/C_i}{V_T} = \frac{1 + Q_t/Q_s}{1 + (Q_t/Q_s)(1 - x_o/2d_i)} = \frac{1 + 1/b'}{1 + 1/b}. \tag{53}$$

If we consider the case at hand where $b = 2.0$ and b' is essentially 1, then (53) implies that x_o must be at least $0.50 \times d_i$, that is, that the stored charge in the insulator must extend at least 50 percent of the distance from the interface to the gate. If Q_t/Q_s is 1.0, then $x_o = d_i$. Thus, Q_t/Q_s must be at least 1.0 for, if it were smaller, then $x_o > d_i$, which is not possible. Therefore, if the charge stored in the insulator is uniform between $x = 0$ and $x = x_o$, then it is necessary to understand the observed b' that $0.50 < x_o/d_i < 1$ and $1.0 < Q_t/Q_s$, the latter implying that more charge must be stored in the bulk at the insulator than at the interface.

In the preceding paragraph, we have assumed that the stored charge was uniformly distributed in the region $0 < x < x_o$. In fact, we expect the charge to be more dense near the interface ($x = 0$) where the field is lowest than near $x = x_o$. To satisfy (51), this would require larger values of Q_t/Q_s and of x_o than for the uniform case. We have also assumed that it is the electric field at x_o that controls the decay. It is possible that $E(x, t)$ for $x < x_o$ in fact performs this function. This would further increase the values of Q_t/Q_s and x_o required to achieve ($b' < b$). One's lattitude here is rather limited, however, for, as we have seen, if it is $E(0^+, t)$ which controls the decay, then Q_t/Q_s becomes negative. We offer the above, therefore, as possibilities only.

Another source of the ($b' < b$) effect is that the charge may be extraction-limited, that is, controlled by the field at $x = d_i$. If we put $x_o = d_i$ in eqs. (46) and (47a), then we again obtain (51) relating the total stored charge to its first moment. We noted above that we could understand the measured b-factor for $x_o = d_i$ and a uniform, stored, insulator charge if $Q_t/Q_s = 1.0$, a reasonable but perhaps somewhat

large value. However, if the current is extraction-limited, then we expect that the charge would be more dense near $x = d_i$ than in the bulk of the insulator. As a hypothetical example, suppose that the stored, insulator charge is uniform for $x_1 < x < d_i$ and zero for $0 < x < x_1$. Then from (37) we obtain

$$V_T = \frac{Q_s}{C_i} + \frac{Q_t}{C_i}\frac{1}{2}\left(1 - \frac{x_1}{d_i}\right). \tag{54}$$

It then follows from (49) and (51) that

$$\frac{Q/C_i}{V_T} = \frac{1 + Q_t/Q_s}{1 + (Q_t/Q_s)(1 - x_1/d_i)/2} = \frac{1 + 1/b'}{1 + 1/b}. \tag{55}$$

This relation provides a much greater possibility for obtaining ($b' < b$) than (53). For example, if $Q_t \gg Q_s$, then

$$b' \leqq (1 + 2/b)^{-1} < b/2. \tag{56}$$

Or, if $x_1 \approx d_i$, then

$$b' = b[(1 + b)Q_t/Q_s + 1]^{-1}, \tag{57}$$

from which $b' = 1$ would follow for $b = 2.0$ if $Q_t/Q_s = 0.333$, a very reasonable value. For $x_1 < d_i$, somewhat larger Q_t/Q_s would be required to satisfy (55). However, in most cases Q_t/Q_s would be smaller than that in the previous example (53), in which the stored charge was assumed near the oxide-insulator interface. We conclude that, while we have indicated the possibility of how ($b' < b$) can come about, further work is required to really pin down and calculate the measured b-factor b'.

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