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Monolithic Electronic Devices Based on Domain Wall Motion in a Ferroelectric Crystal

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Ferroelectric domain wall motion can provide the basis for monolithic electronic devices which are able to gate, amplify, perform digital logic, read out permanent analog messages, provide digital shift register storage, and scan optical images. No use of ferroelectric coercivity is made in these devices. Most of the functions have been experimentally demonstrated in simple form. The basic operating principles of these devices are explained, and their material requirements are discussed. The specific operation of five categories of devices is described.

I. INTRODUCTION

A variety of electronic functions can be accomplished in a novel way by taking advantage of the properties of domain wall motion in ferroelectric single crystals. Using lead germanate, an elementary gating/amplifying device and a simple analog read-only memory have been demonstrated.[1] Using gadolinium molybdate, a much more complicated analog read-only memory capable of storing four seconds of speech waveforms has been produced.[2] The theory of several other wall motion devices, including image scanners and logic gates, has been investigated. These latter devices have not been demonstrated but rely on the same principles as those which have. The purposes of this paper are (*i*) to summarize the basic concepts common to all the above devices, (*ii*) to discuss material problems and requirements as they relate to improving the devices already demonstrated and to realizing the undemonstrated ones, and (*iii*) to describe specific device configurations using presently available materials and to show configurations achievable with improved materials.

II. BASIC PRINCIPLES OF THE DEVICES

The devices discussed here employ ferroelectric crystals which permit only two anti-parallel polarization states. The crystals used are in

the form of thin slabs with the polarization axis generally normal to the broad faces of the slab, as in Fig. 1. In this configuration, domain walls can be moved sideways by applying a potential between electrodes on opposite sides of the slab. Coherent wall motion of this type (as opposed to nucleation of new domains) will be assumed to be the only mode of domain switching to occur during device operation.

Depending on the type of ferroelectric material used, the domain's configuration and motion may either be arbitrary, as in Fig. 1, or rigidly anisotropic. A domain like the inner one in the figure (i.e., with downward directed P vector) will be termed a positive-favoring domain because it expands in response to a positive potential applied to the top of the crystal. Domains with upward directed P vector exhibit the opposite behavior and will be termed negative-favoring.

As the domain advances across the electrode, the sign of the spontaneous polarization, and hence the compensating conduction charge on the electrodes, must change. This requires a flow of current in the electrode leads. Presuming intimate electrode contact to the ferroelectric surface, the induced wall motion current is

$$I = 2P_s \frac{dS}{dt}, \tag{1}$$

where P_s is spontaneous polarization and S is the area of the positive-favoring domain lying under the electrode.

The monolithic electronic devices described here function by employing two ferroelectric effects: wall motion and induced currents.

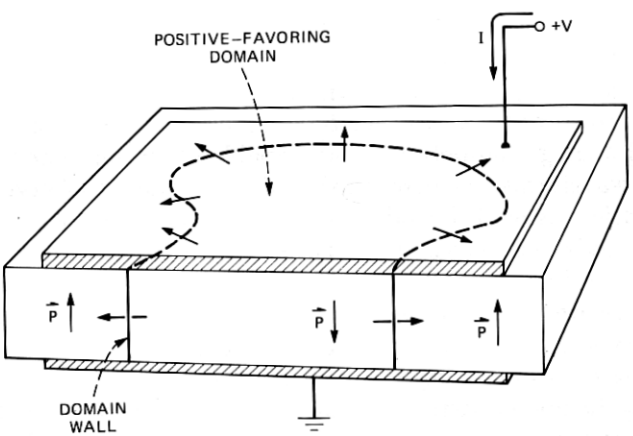

Fig. 1—Ferroelectric single crystal shown in perspective and cross section. Voltages applied to electrodes on opposite faces of the crystal slab produce an electric field parallel to the ferroelectric polarization axis. The wall of the arbitrarily shaped domain propagates outward under the influence of this field. As the wall moves, it induces a current I in the leads of the electrodes. Since the domain of the polarity shown expands in response to the positive voltage applied to the upper electrode, it is called a positive-favoring domain.

When suitable voltages are applied to appropriate configurations of electrodes, domains can be gated, shifted sequentially from place to place, made to perform scanning motions, or kept isolated from each other. Currents induced by wall motion can be used directly as outputs, digital or analog. Since the domains need no power to maintain their existence, the devices can have nonvolatile properties. Most importantly, currents due to wall motion can be fed to other parts of the crystal to control further wall motion. The specific configurations of a number of devices are presented in Section IV.

Superficially, such devices might appear to be the ferroelectric analogs of magnetic bubble devices, but in fact they differ in two important ways. The more important difference derives from the incompleteness of the analogy between electrical and magnetic phenomena. Electric field lines can terminate on electrical charges. It is the rearrangement of the terminating charges that accompanies wall motion which gives rise to the induced ferroelectric current. Since no analogous magnetic charge exists, this phenomenon has no direct analog in bubble devices.

A second distinction is that magnetic bubbles are ferromagnetic domains of a special character, ones which represent a minimum energy configuration created by the presence of an opposing field. The ferroelectric materials used, however, do not exhibit analogous "electric bubbles." Instead, they support conventional domains whose dimensions are determined by the configuration of the electrodes.

Past efforts to apply ferroelectric phenomena to electronic devices have been based on the concept of ferroelectric coercivity. These devices used the coercive strength as a threshold and were in many ways analogous to magnetic square-loop core devices such as ferrite core memories or magnetic amplifiers. Unfortunately, coercivity does not appear to be a fundamental property of ferroelectrics. Despite much experimentation, true coercivity is not observed in ferroelectric materials.[3] Ferroelectric wall motion devices, on the other hand, do not utilize threshold principles. While they have their own material requirements and constraints, they employ only properties believed to be fundamental to ferroelectricity.

III. DEVICE REALIZATION

3.1 Materials

The ideal ferroelectric material for use in wall motion devices should have a Curie temperature well above room temperature, be mechanically stable, and possess only two domain states (preferably optically distinguishable, as a diagnostic). It must switch only by rapid, consistent wall motion, not by nucleation of new domains. It is desirable that the material permit domains of arbitrary shape (as in Fig. 1).

The central materials problem of the wall motion devices is that no single material has yet been found that has all these ideal properties. The working experimental devices demonstrated to date[1,2] have been made using either gadolinium molybdate or lead germanate. Gadolinium molybdate satisfies every property above except that its domains can only assume a restricted planar shape. Lead germanate satisfies all conditions except that, in all samples tested to date, it permits nucleation to occur at all but very low fields. The properties and applicability of these materials are summarized below.

Gadolinium molybdate,[4] $Gd_2(MoO_4)_3$, is orthorhombic below its Curie temperature of 159°C and has a room temperature spontaneous polarization of 0.17 $\mu C/cm^2$. It is ferroelastic as well as ferroelectric. When a wall sweeps across the crystal, the a and b axes (which differ in lattice spacing by about 0.3 percent) are exchanged. Thus the change of electrical polarization is accompanied by a slight change in the shape of the crystal. Since the a and b axes are optically dissimilar, the domains may be easily viewed by polarized light microscopy.

To make the slightly different strain of adjacent domains compatible, the domain walls must take the form of planes stretching across the whole crystal and must be oriented at a 45-degree angle to the a and b axes. Strain compatibility also requires that the walls do not intersect. These constraints mean that the domains must stack up like parallel plates across the crystal slab. Hence, one can at best deal only with a one-dimensional array of domains.

On the other hand, it is probable that these same strain compatibility effects are also responsible for making gadolinium molybdate so resistant to the nucleation of new domains. Walls can be moved back and forth across the crystal at velocities of several m/s without danger of nucleation.[5] This is true in spite of polishing damage, saw-cut edges, inclusions, or scratches.

Recent electron microscopic investigations of wall in gadolinium molybdate indicate that, for very thin samples (around 1000Å), strain compatibility effects may no longer restrict domain shape.[6-8] The micrographs actually show numerous closed domains with right-angle bends in the walls. Under these circumstances, gadolinium molybdate would appear to satisfy every condition for an ideal material for application to the devices proposed. Neither device fabrication on samples of this type nor investigation of the possibility of closed domains in thicker samples has yet been tried.

Lead germanate,[9,10] $Pb_5Ge_3O_{11}$, is a trigonal ferroelectric below its Curie temperature of 176°C and has a room temperature spontaneous polarization of 4.6 $\mu C/cm^2$. The two permitted domain states are enantiomorphic and because of their optical activity can be observed by polarized light microscopy. Domain shape in lead germanate is observed to be quite arbitrary, and the demonstrated devices employ-

ing it have made use of this property. A small wall velocity anistropy exists, however, imparting a rounded hexagonal shape to domains which grow outward from a point and are unrestricted by electrode geometry.

The ease with which new domains nucleate in lead germanate is the primary drawback to the use of this substance in practical wall motion devices. Theoretical studies of ideal ferroelectrics show that a very large increment of energy, on the order of 10^8 kT for barium titanate, for example, is necessary to produce the nucleus of a new domain capable of further expansion.[11] Similar studies of wall motion in barium titanate[12] show that the minimum energy to initiate wall motion is on the order of 10 kT. This large ratio of nucleation and wall motion thresholds should be typical of ferroelectrics. Consequently, there appears to be no fundamental reason why a wall motion device cannot operate without causing nucleation of new domains. Unfortunately, presently available samples of lead germanate do not even approach these limits of nucleation immunity. It is hypothesized that nucleation may occur with anomalous ease due to crystal flaws, flaws in electrode coatings, or tiny unswitched domains left behind by a propagating wall.

3.2 Substrate fabrication

The devices described here require a single crystal substrate with a thickness on the order of a few microns to a few tens of microns. Both sides of the substrate must be accessible for electroding, though only one side carries patterned electrodes in most of the devices. This paper is basically concerned with what can be done with such substrates, rather than how than can be fabricated. However, we can list some techniques which could be employed.

(*i*) Hetero-epitaxy on a crystal substrate which is then selectively dissolved away so that the back surface can be electroded.

(*ii*) Hetero-epitaxy on a substrate crystal which has sufficient electrical conductivity to serve as a back-surface electrode.

(*iii*) Careful etching of saw-cut crystal wafers. Techniques of this kind[13] when applied to silicon can produce a crystal as thin as around 25 μm with a thicker rim for support.

(*iv*) Conventional polishing of saw-cut wafers. Reduction of thickness to a few mils can be practical.

3.3 The use of a resistive layer

In nearly all the devices described in this paper, domain walls are required to propagate across gaps separating adjacent electrodes. The surface polarization charge of the ferroelectric is always fully compensated for by conduction charge where an electrode is present, but the polarization charge in the interelectrode gaps has no direct source of

compensating charge. Thus, when a wall attempts to cross a gap, a strong depolarizing field will be set up (see Fig. 2a). This field can hinder wall motion or stop it completely.

A layer of resistive material in intimate contact with the crystal surface can alleviate this effect by providing a source of compensating charge as shown in Fig. 2b. The layer should be conductive enough to allow rapid wall motion, but not so conductive that it causes needless power dissipation when the electrodes are at differing potentials or causes excessive loss of currents intended as outputs. The layer may be deposited before the electrodes are formed as in the figure, or it can be deposited into the gaps after the patterning of the electrodes. It may also be possible to produce a resistive layer by doping the surface of the ferroelectric crystal itself.

Experience with devices made from lead germanate shows that the use of a resistive layer is necessary to the crossing of electrode gaps by domain walls in this substance. This held true for gaps of all the widths

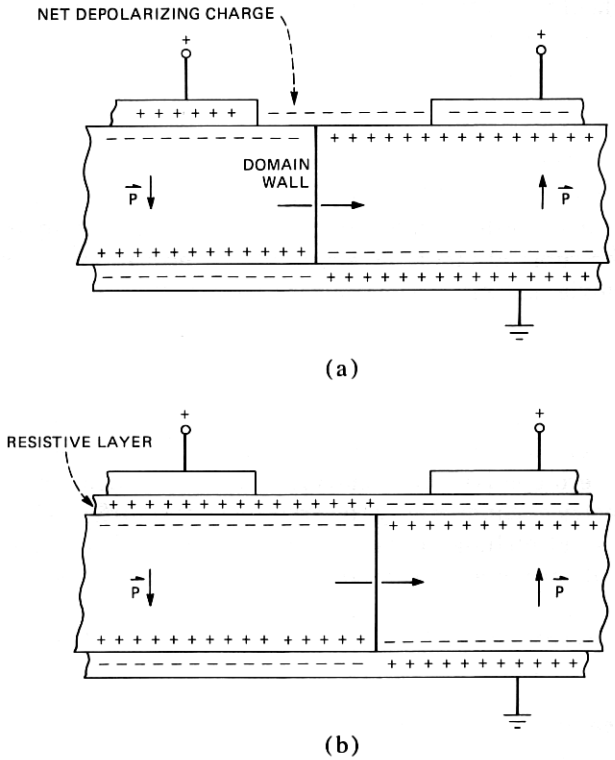

Fig. 2—(a) Cross-section view showing a domain wall attempting to cross an inter-electrode gap. The surface polarization charge of the ferroelectric changes as the wall advances, but the surface conduction charge remains fixed because the ferroelectric is a near-insulator. This creates a net depolarizing charge which can slow or stop the wall. (b) With a resistive layer in contact with the ferroelectric surface, charge compensation is maintained and the wall can cross the gap easily.

employed, including the narrowest of about 5 μm. In gadolinium molybdate, however, gaps as large as 10 μm can be crossed by the wall, on the condition that the gap extends along only a relatively small part of the length of the wall, the remaining wall length residing beneath unbroken electrodes.

IV. SPECIFIC DEVICE CONFIGURATIONS

In the remainder of this paper, the specific configurations of five device types are presented. The descriptions center on the more general versions made possible by an ideal material permitting arbitrary domain shapes. Specialization of these devices to planar domain geometry (i.e., gadolinium molybdate) are made where appropriate.

4.1 Gating device

This device permits one current to control another and is capable of amplification. Its operation illustrates many principles employed in the other devices. An experimental gating device has been demonstrated in lead germanate.[1]

The basic wall-motion gating principle is reviewed in Figs. 3a to 3d. A positive-favoring domain, permanently residing under an origin electrode, can propagate under the detector electrode if the intervening trigger electrode is positive. If the trigger is kept negative, the detector's domain state cannot change from negative-favoring to positive-favoring (in spite of a positive detector voltage) because no positive-favoring domain is available to the detector electrode. A negative confiner electrode is employed to ensure that the trigger provides the sole access of positive-favoring domain to the detector. Since the motion of a domain wall under the detector induces a current in the detector lead, the detector current is therefore gated by the trigger voltage. The device must operate in a pulsed mode: detector current ceases when the wall traverses the detector, and both trigger and detector voltage must be made negative to restore the device for a new gating cycle. The crossing of the interelectrode gaps is aided by a resistive layer if necessary. A similar device can be made using a planar-wall material by simply deleting the confiner electrode.

It can be shown that the ferroelectric gating device is capable of gain of various sorts. First note that the trigger draws a current of its own when traversed by the domain wall. By integrating eq. (1), it is clear that the total charge in the current pulses of both detector and trigger is proportional to the electrode areas. Hence by making the detector arbitrarily larger than the trigger, any desired charge gain can be obtained:

$$G_{\text{charge}} = \frac{S_d}{S_t}, \tag{2}$$

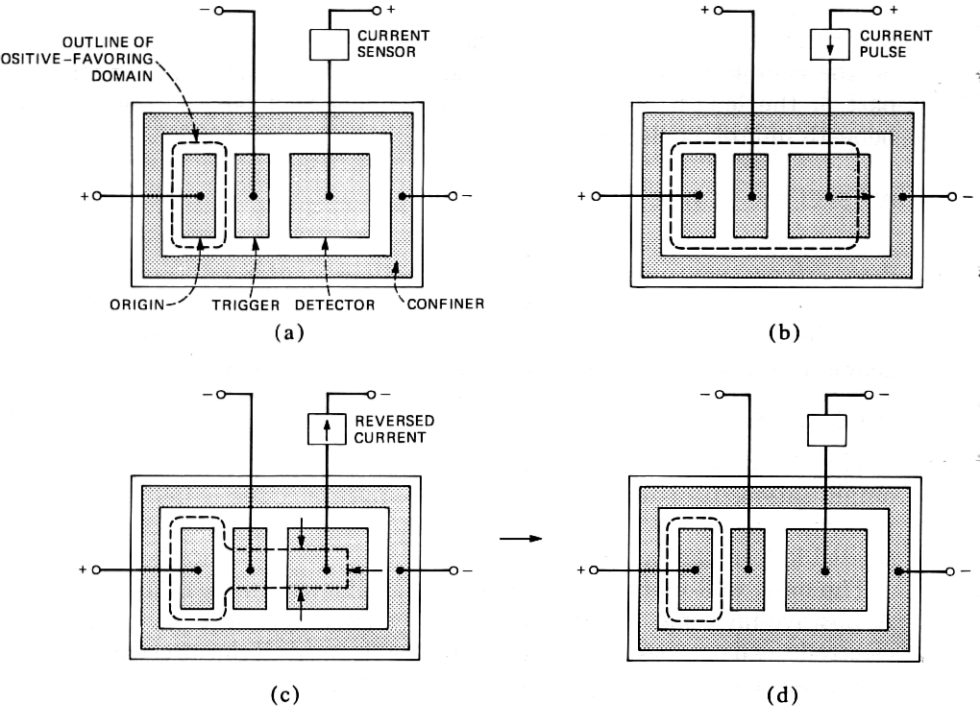

Fig. 3—Top view illustrating the operation of a ferroelectric gating device capable of gain. The trigger electrode serves to control the detector electrode's access to the positive-favoring domain beneath the origin electrode. (a) When a negative trigger voltage blocks this domain, the detector domain cannot change polarity because no domain wall is present and because nucleation cannot occur. Therefore, no current is sensed. (b) When the trigger is positive, a wall motion current is induced in the current sensor. By making trigger and detector supplies negative, the device is restored to its original state (c and d).

where S_d and S_t are detector and trigger areas. For a crystal of a given thickness, wall velocity is a function of applied voltage, $V(v)$. By applying a greater voltage to the detector than to the trigger, the detector wall velocity can be made larger than that of the trigger, yielding a current gain. Assuming the width of the detector, trigger, and origin to be identical (as in Fig. 3),

$$G_{\text{current}} = \frac{V(v_d)}{V(v_t)}, \tag{3}$$

where v_d and v_t are the detector and trigger voltages.

Suppose a resistor is placed in the detector lead to yield an output voltage, and suppose the trigger voltage is taken as the input voltage. To analyze this case in general requires the trial-and-error solution of

a functional equation involving $V(v)$, an experimental curve. We will therefore consider a convenient special case in which v_{ds}, the detector supply voltage, is set so that wall velocity is the same under trigger and detector. For this case,

$$G_{\text{voltage}} = \frac{v_{ds}}{v_t} - 1 \tag{4}$$

so that gain greater than 1 is achieved when $v_{ds} > 2v_t$. The value of v_{ds} required to make the trigger and detector wall velocities equal is given by

$$v_{ds} = v_t + 2P_s WRV(v_t), \tag{5}$$

where W is the width of origin, trigger, and detector and R is the load resistance. This implies that voltage gain greater than 1 results when

$$2P_s WR > \frac{v_t}{V(v_t)}. \tag{6}$$

Hence, voltage gain exceeding 1 is always attainable simply by designing the gating device to have W and R satisfying eq. (6).

The conditions of equal wall velocity and equal electrode width imply that trigger current and detector current are also equal. If we define instantaneous power gain as the ratio of power dissipated in resistor R to the power input to the trigger lead, then

$$G_{\text{power}} = \frac{v_{ds}}{v_t} - 1 \tag{7}$$

for conditions of eq. (5). Instantaneous power gain will exceed 1 when the device is designed so that eq. (6) is also satisfied. Finally, we may define energy gain as the ratio of total energy dissipated in R to the total energy input into the trigger lead. Since we are analyzing the special case of equal trigger and detector velocities, the duration of input and output power pulses will have the same ratio as the lengths of trigger and detector electrodes measured in the direction of wall motion, ℓ_t and ℓ_d. Hence,

$$G_{\text{energy}} = \frac{\ell_d}{\ell_t}\left(\frac{v_{ds}}{v_t} - 1\right) \tag{8}$$

for conditions of eq. (5). Energy gain will exceed 1 when, for instance, the design fulfills eq. (6) and $\ell_d > \ell_t$.

The behavior of the gating device has been analyzed without taking into account the interelectrode current leakage which will result if a resistive layer is employed. This leakage can be reduced by making appropriate compromises in the design of the resistive layer. Leakage can be avoided by placing the output device (current sensor or load

resistor) in the lead of the underside grounded electrode. The output will then be the trigger's plus the detector's current, yielding a greater gain. Alternatively, the detector electrode may be surrounded by a guard ring electrode connected to the detector supply, thus blocking leakage to the detector.

4.2 Analog read-only memories

The ferroelectric analog read-only memory provides a function not provided by any other monolithic technique: the direct readout of permanently stored continuous analog waveforms. A simple analog readout device made using lead germanate has been demonstrated.[1] Application to speech waveforms is especially appropriate. A gadolinium molybdate device which can read out either of two 2-second sentences has been demonstrated.[2]

Ferroelectric analog readout devices in general operate by allowing a domain wall to scan down a long detector whose shape varies in accordance with the intended output. A multiple track version of the device is shown in Fig. 4, as it would be configured for use with a material supporting arbitrarily shaped domains. To read out a track, the wall of the origin domain is gated by the trigger and is allowed to propagate down the detector. The wall is restricted to follow the outline of the detector by the negative confiner. The detector's width is a function $W(x)$, where x is the distance down the long axis of the detector. If the advancing wall has the form of a straight line oriented

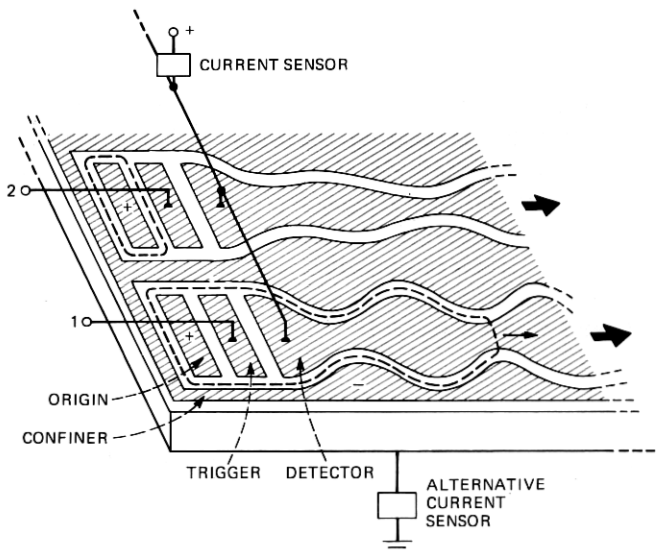

Fig. 4—Multiple-track analog readout device using one detector per track and employing arbitrarily shaped domains. Separate triggers are used to select the desired track. The output detected by the common current sensor is proportional to the width of the wall moving down the selected track.

perpendicular to its direction of advance, then the wall will sweep out surface area of the crystal at a rate of

$$\frac{dS}{dt} = v_0 W(x_0) = v_0 W(v_0 t), \tag{9}$$

where v_0 is the constant wall velocity and x_0 is the wall position. By eq. (1), this will cause a current to flow both in the detector lead and in the lead of the underside ground electrode:

$$I = 2P_s v_0 W(v_0 t). \tag{10}$$

Hence, the time variation of the output will be directly proportional to the spatial variation of the selected detector's width. If the thickness of the crystal does not vary, constant velocity can be maintained simply by applying a fixed voltage to the detector. Otherwise, a feedback circuit is employed to control the detector supply voltage in such a way as to maintain the time-averaged detector current at a desired fixed value.

Analog read-only memories with data tracks oriented parallel to each other may be made using planar wall materials such as gadolinium molybdate.[2] A differential, multiple-track version of such a device is seen in Fig. 5. The total width of the two detectors which constitute a

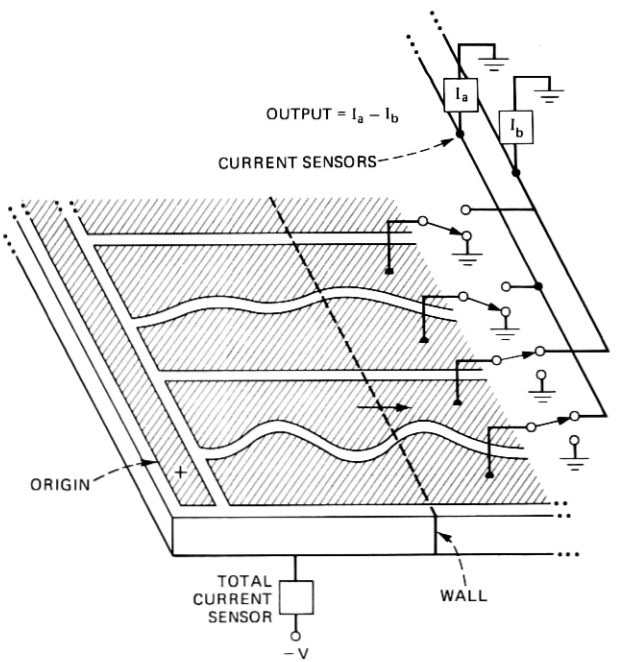

Fig. 5—Multiple-track differential analog readout device utilizing a planar wall material. External switches are used to connect the desired track to the current sensors. All unselected tracks are switched to ground.

track is constant, but the difference of their widths is equal to the desired function $W(x)$. The output may therefore be obtained as the difference of the two detector currents:

$$I_2 - I_1 = 2P_s v_0 W(v_0 t). \tag{11}$$

The sum of the two currents is directly proportional to wall velocity and can be conveniently utilized by a feedback system to regulate wall velocity.

Because the wall extends across the entire crystal, all tracks are necessarily scanned at once, and no common connection to all detectors can be used. Separate leads are therefore brought out, two per track in the differential version. The current in the lead of the desired track is selected by external circuitry, and all other leads are connected to a common potential.

4.3 Optical image scanners

In this section, optical area and line scanners are described which employ ferroelectric domain wall motion as the scanning mechanism. Though such devices have not yet been experimentally demonstrated, their operation depends on the same ferroelectric phenomena as the devices which have been demonstrated.

Figure 6 shows the structure of an optical area scanner employing a material permitting arbitrary domain shapes. The electrode geometry consists of numerous scanning electrodes interleaved with confiners. All the scanning electrodes are connected to one common terminal, and the confiners are connected to another common terminal. A ferroelectric shift register (see Section 4.4) lying along the left-hand end of the scanned area transports a single positive-favoring origin domain from one detector electrode to the next. When the detectors are made positive, the origin domain in the shift register crosses over to the adjacent scanning electrode and propagates down it. After the domain reaches the end, the common lead is made negative, rapidly restoring the scanning electrode by a motion of the walls inward toward the axis of the scanning electrode. Repeating this process for each scanning electrode in sequence generates a domain wall scan of the whole area of the chip.

The scanning action of the domains is used to sense resistivity changes in a photoconductive layer applied to the bottom surface of the ferroelectric crystal. Figure 7 shows this layer in a cross-section view taken through one scanning electrode. Electrical contact is made to the surface of the photoconductor by a thin transparent electrode. The image to be scanned is focused on the photoconductor from below by an optical system. Induced ferroelectric currents originate specifically from the line where the moving domain wall intersects the surface of the crystal, since that is where the polarization surface charge changes its sign as the wall moves. Thus a scanning domain wall acts

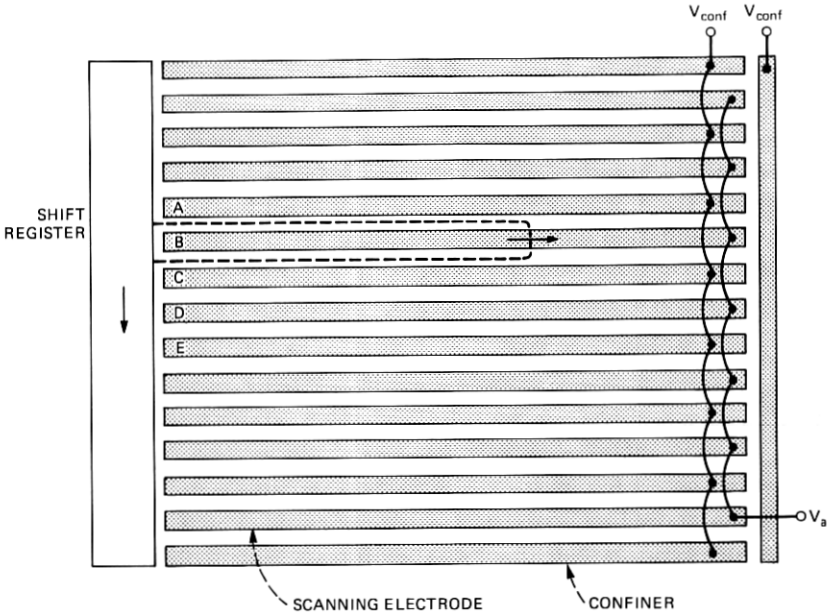

Fig. 6—Top view of electrode geometry used for area image scanner. A single positive-favoring domain held in the shift register at the left is used to initiate domain wall scans along the strip electrodes. The scanning domain is confined to one electrode by the interleaved confiner strips. When the scanning of one electrode is completed, it is restored by a brief negative pulse and the shift register is incremented to the next scanning electrode.

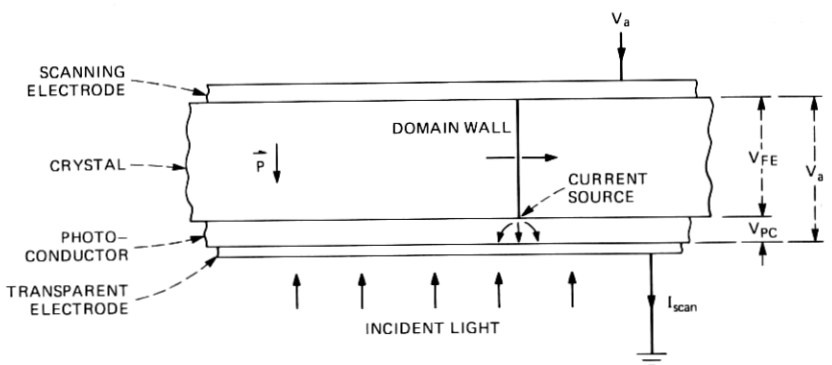

Fig. 7—Detection principle of the image scanner shown in cross section. The scanning wall acts as a moving current source. This localized current passes through a photoconductive layer whose conductivity is dependent on the intensity of the local illumination. The value of applied voltage V_a required to keep the scanning rate constant (i.e., to keep V_{FE} constant) varies in accordance with the conductivity of the photoconductive layer.

as a moving current source. The current from this source passes downward through the photoconductive layer and exits through the transparent electrode. If we apply a fixed voltage to the scanning electrode, the wall will not travel at a constant velocity, but rather will

speed up when passing places where the photoconductor has high conductivity and slow down when passing places of low conductivity. The current exiting through the transparent electrode, I_{scan}, is directly proportional to the scanning wall velocity. Under these conditions, the ferroelectric scanning system yields an external current indicative of the illumination present at the position of the advancing wall.

The illumination data conveyed by I_{scan} are obtained at the price of a varying scanning rate. By regulating the wall velocity through a simple feedback system, a constant scanning rate can be obtained while still generating a signal indicative of the conductivity of the photoconductive layer. A block diagram of this system is seen in Fig. 8. A differential amplifier senses the difference between I_{scan} and a fixed reference signal. The amplifier's output is applied directly to the common scanning electrode lead. The applied voltage, V_a, is thus varied in just such a way as to keep I_{scan} equal to a desired constant. V_a can be viewed as a sum of two components: V_{FE}, the drop across the ferroelectric crystal, and V_{PC}, the drop across the photoconductive layer:

$$V_a = V_{FE} + V_{PC}. \tag{12}$$

Because wall velocity is held constant, it follows that V_{FE} is constant (assuming the ferroelectric crystal to be of constant thickness). This is so because, at a given crystal thickness, wall velocity is solely dependent on applied voltage. Consequently, any fluctuation of V_a must be due entirely to the fluctuation of V_{PC}:

$$\Delta V_a = \Delta V_{PC}. \tag{13}$$

Since I_{scan} is held constant, ΔV_{PC} will be proportional to $\Delta \rho_{PC}$, the resistivity of the photoconductive layer at the point of scanning. Thus

$$\Delta V_a \propto \Delta \rho_{PC}. \tag{14}$$

That is, the fluctuation of the feedback voltage itself constitutes the light signal output of the image scanner.

In the scanning electrode geometry shown in Fig. 6, it can be seen that the scanning electrodes and confiners are interchangeable. By alternately switching the role played by the two sets of electrodes, a doubling of the scanning density can be obtained.

A striking feature of the scanning electrode geometry is the fact that it is free of structure in the direction of scanning. Present silicon image scanners, by way of comparison, consist of two-dimensional arrays of individual light sensors. Each sensor has a structure of its own, that is, a configuration of diffusions, windows and metalized areas. In the ferroelectric scanner, each single scanning electrode performs the function of an entire row of structured light sensors. Figure 9 shows the "resolution cell," or picture element of a ferroelectric scanner.

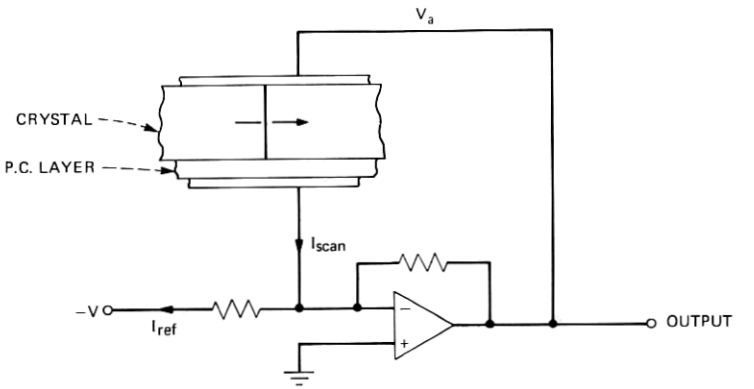

Fig. 8—Feedback circuit used to maintain constant wall velocity in the image scanner. The wall current I_{scan}, which is proportional to wall velocity, is compared with a reference current I_{ref} so as to generate a feedback signal V_a. This signal is used to drive the scanning electrodes and constitutes the output signal as well.

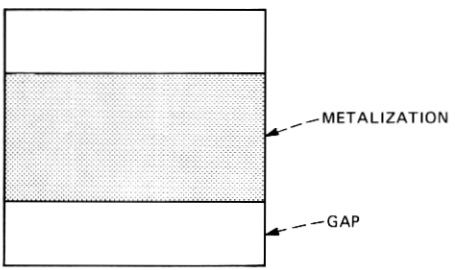

Fig. 9—Resolution cell of the area scanner for the case where scanning and confiner electrodes are exchanged on alternate scans. The cell is notable for its simplicity.

Though the resolution of the scanner in the horizontal direction is greater than in the vertical direction, the cell has been drawn conservatively as a square. The cell consists of a metal strip with two half gaps to either side. It is hard to imagine a solid-state area scanner with a simpler resolution cell than this.

A color scanner can be made by overlapping the photoconductive layer with an array of narrow parallel red, blue, and green filters oriented perpendicular to the direction of scanning (see Fig. 10). An output will be produced which represents the detected amounts of the different color components in a rapidly repeating sequence. External circuitry employing a phase-locked loop is used to sort out the different color indications into three separate parallel outputs. A narrow transparent strip interposed between each group of color filters provides a phase reference for the separation of the three color signals. Such a scheme involves a substantial reduction of resolution in the direction of scanning, but since the resolution of ferroelectric scanners should be high to begin with, the compromise is especially appropriate.

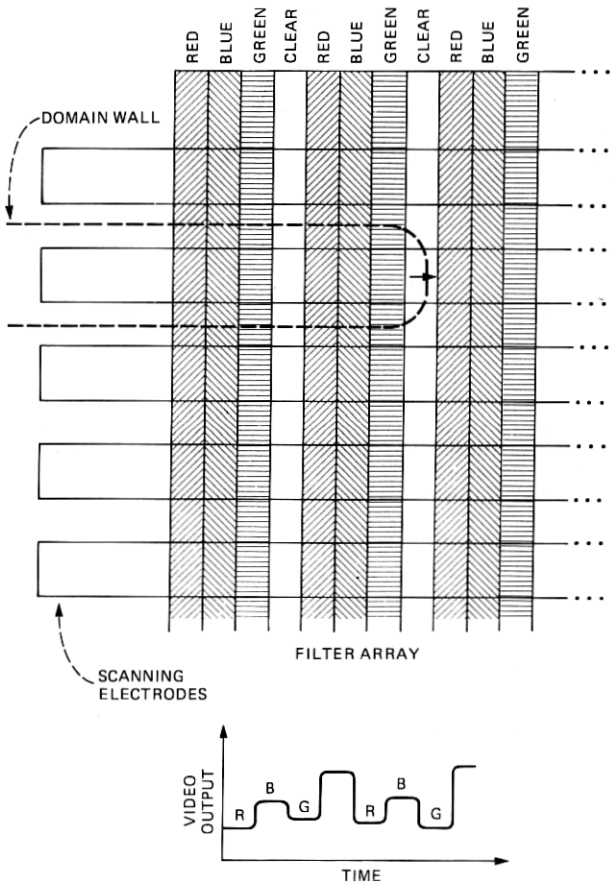

Fig. 10—Area scanner geometry with superimposed strip filter array for color applications. An example of the resulting output is seen at the bottom. External electronics are employed to separate out the three color signals into three parallel analog channels. Sync for doing this is provided by the interposed clear filters which are recognizable by their greater magnitude in the output signal. Note that no precise alignment of the filter array in position or angle is required.

A line scanner of very simple design can be made using a planar domain ferroelectric. The structure of such a device is shown in Fig. 11. The operating principle is the same as in the area scanner, but now a single domain wall extending across the width of the crystal is used for scanning. The only electrodes used are the origin, the scanning electrode, and the negative stop electrode which prevents the wall from being lost at the end of the crystal.

Ideally, one would want the crystal to be very narrow so that only a thin strip of the incident image would be scanned. Unfortunately, this leads to chip proportions which may be impractical. Instead, one can employ an optical system which itself defines the strip to be scanned and projects it on a crystal which has as narrow a shape as

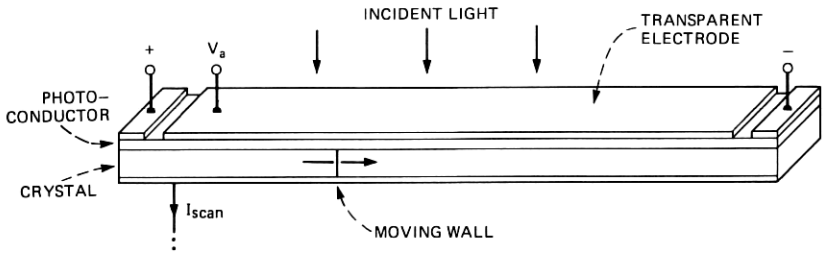

Fig. 11—Line scanner employing a planar wall ferroelectric. The principle of operation is the same as in the area scanner except that the wall extends across the full width of the crystal.

possible. This image is then defocused by a weak cylindrical lens to spread it out in a direction parallel to the domain wall. Thus the whole extent of the wall, all of which is sensitive to illumination, is illuminated by the same part of the image at a given time.

At first, it may appear that an area scanner may be obtained by dividing the top or bottom electrode of a planar wall scanner into numerous strips. This scheme will not work because the planar domain wall must scan all such strips simultaneously and would therefore be sensitive to the conductivity of the photoconductive layer associated with each of the strips at the point of scanning. This cannot be remedied by disconnecting all strips except that desired to be sensed, because the ferroelectric current from those strips would have nowhere to go, and wall motion would therefore cease. Even if the strips other than the one being sensed were connected to a voltage source (as was done in the planar wall analog readout device, Fig. 5), the wall's motion would still be influenced equally by conductivity changes anywhere along the wall.

4.4 Nonvolatile shift register memories

Static, nonvolatile, digital shift register memories can be made which employ ferroelectric domain wall motion phenomena. An experimental 4-bit shift register using lead germanate has been demonstrated.*

The basic shift register consists of a series of shifting electrodes preceded by an origin and trigger and completely surrounded by a confiner† (see Fig. 12). The shifting electrodes are connected in repeating sequence to voltage sources V_1, V_2, and V_3, as shown. By

* Unpublished experimental demonstration by the author. Origin, trigger, confiner, and shifting electrodes were all formed by small wires positioned close to the surface of a thin lead germanate crystal. The crystal was immersed in a slightly conductive fluid which established electrical contact between the wires and the crystal surface and served as a resistive layer. Domains could be introduced at will by the trigger and shifted along by the shifting electrodes. The moving domains could be observed in polarized light.

† A device for shifting domains in gadolinium molybdate was independently discovered by J. E. Geusic, T. J. Nelson, and D. P. Schinke (U.S. Patent 3,701,122). Domain detection was optical in this invention, however, and no use was made of the induced ferroelectric current.

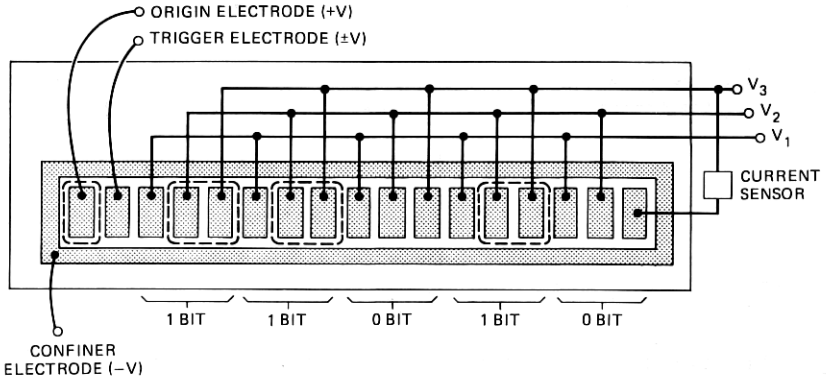

Fig. 12—Top view of a ferroelectric shift register memory. Domains introduced by the trigger are swept along by an array of 3-phase shifting electrodes. A "1" bit is represented by the presence of a positive-favoring domain in a 3-electrode cell, a "0" bit by the absence of such a domain. The arrival of a domain at the end of the register is sensed by means of the induced ferroelectric current in the last electrode.

allowing these voltages to go through the cycle of alternations shown in the waveforms of Fig. 13, positive-favoring domains introduced by the trigger can be shifted from electrode to electrode. A full shifting cycle has six stages or time periods as illustrated in the cross-section views of Fig. 13. It can be seen that each domain advances by expanding forward when the electrode ahead of it is made positive, and by pulling up from the rear when the electrode behind it changes negative. The surrounding confiner denies the shifting electrodes access to positive-favoring domains from any other part of the chip. The domains will therefore propagate down the shift register as isolated positive-favoring islands, one for each set of three shifting electrodes. The presence of such a domain represents a "1" bit and its absence of an "0" bit. The arrival of a domain at the end of the shift register is detected by the induced ferroelectric current generated in the lead of the last electrode. With suitable design, this current is adequate to drive external silicon devices directly.

Ferroelectrics generally exhibit a significant field threshold for wall motion. With supply power removed from the shift register, all electrode voltages go to zero, thus making wall motion impossible. Pyroelectric and piezoelectric effects can generate tiny voltages in the absence of supply power but, with appropriate design (e.g., finite shunt resistance between power supply terminals and ground), these will fall far below the threshold. Thus nonvolatile memory should be obtainable with ferroelectric shift registers.

4.5 Logic gates

Modifications to the prototype geometry can yield ferroelectric logic gates. Figure 14a shows an AND gate produced by interposing two

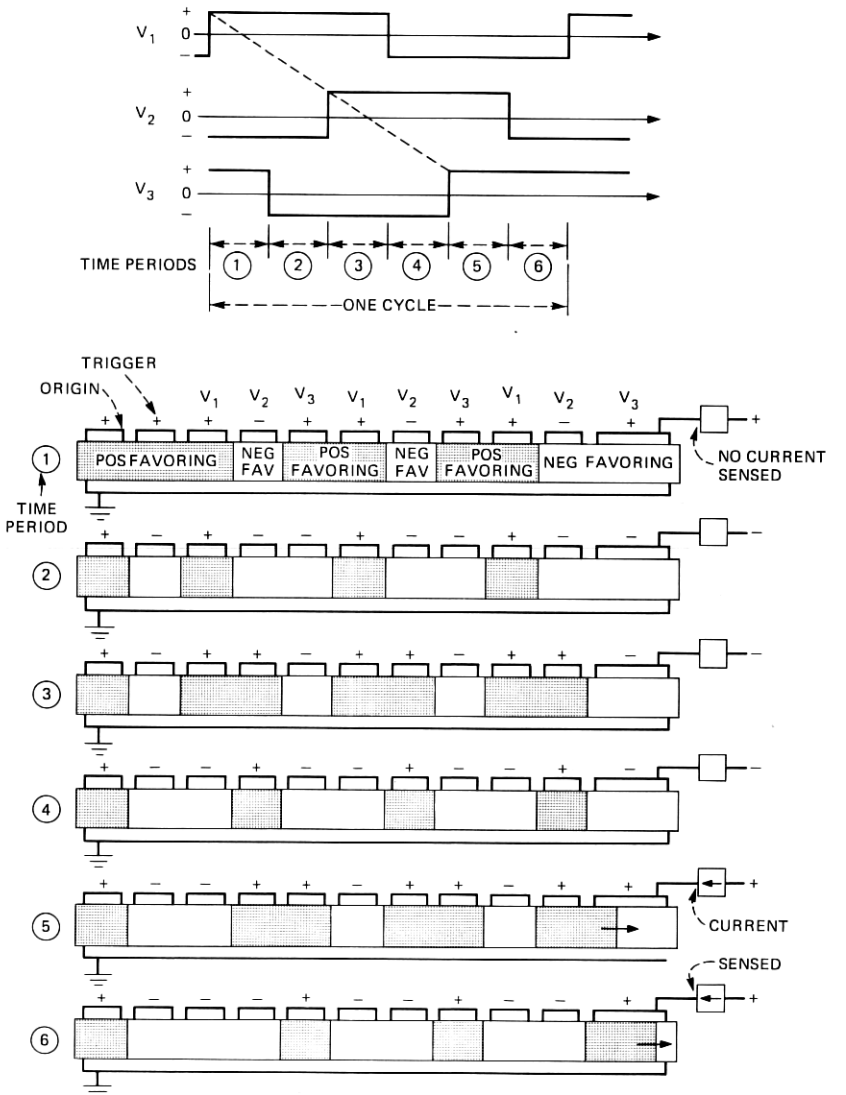

Fig. 13—Details of operation of the ferroelectric shift register. The six time periods making up a full shifting cycle are shown above, and an example illustrating the domain state of the register for each time period is seen below.

triggers between the origin and detector. A logic "1" input to the triggers is represented by a positive voltage during the first half of an operating cycle (the active period) and by a negative voltage during the second half (the restoring period) of the cycle. A logic "0" input is represented by a zero voltage throughout the full operating cycle. The detector is always supplied with a positive voltage during the active

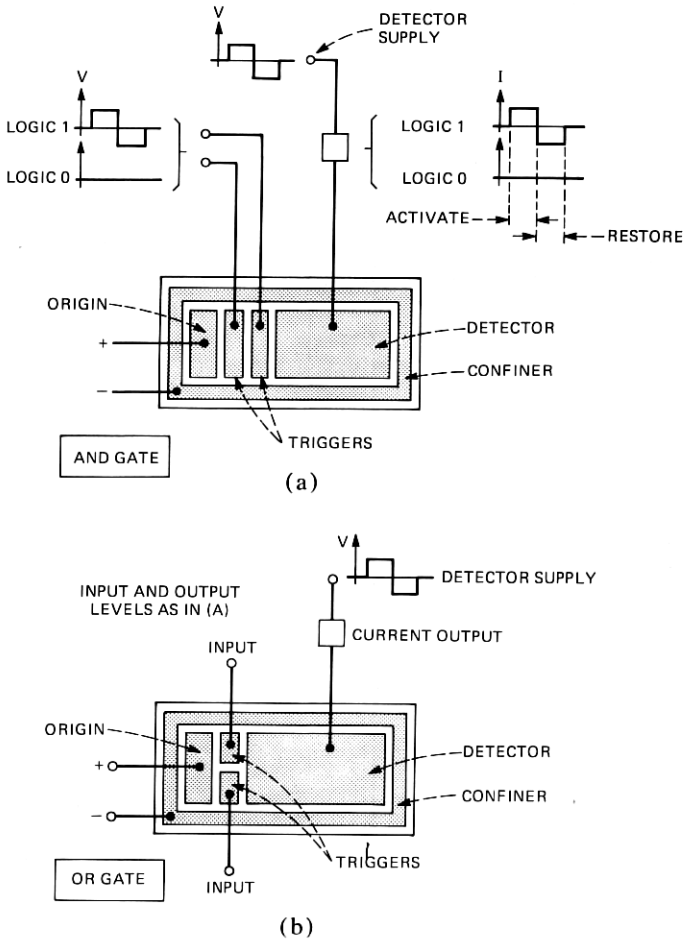

Fig. 14—Top view of simple ferroelectric logic gates. (a) AND gate made by interposing two triggers in sequence between detector and origin. Both triggers must be activated to obtain an output. (b) OR gate made by placing the triggers side by side so that either may cause an output.

period and with a negative voltage in the restoring period. Clearly, a logic "1" input to both triggers is required to produce an output current in the detector lead. A second detector current of opposite polarity will then flow during the restoring period. Should a logic "0" be applied to either trigger, no current will flow in the detector lead during either the active or restoring periods. Thus, an AND function is obtained with voltage inputs and current output. Note that the same logic level definitions used for the inputs also apply to the output: positive and negative half cycles = "1," no signals = "0."

An OR gate may be obtained if the triggers are arranged side by side,

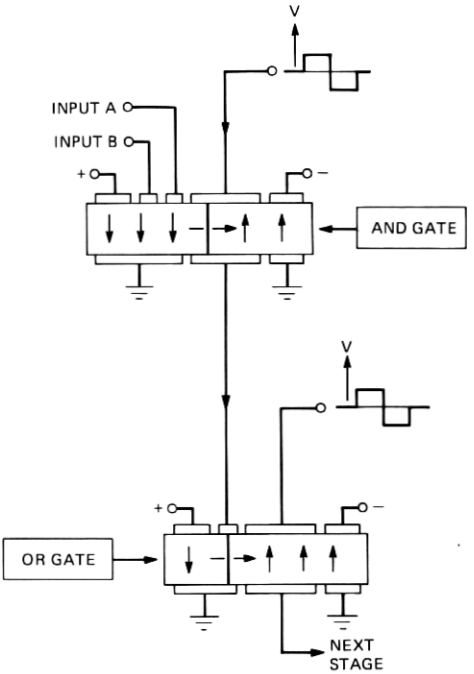

Fig. 15—Series-coupling of an AND gate output to one input of an OR gate. Both gates are seen in cross section and are schematically depicted as though they were on separate ferroelectric crystals. The wall motion current from the AND gate is fed to the OR gate trigger so that both walls must advance together. The wall motion current of the OR gate's detector can be fed to a third gate in a similar way.

as in Fig. 14b. The operation is identical to that of the AND gate except that either trigger alone may cause a 1 output. Both AND and OR gates may be made with any number of inputs in sequence or side by side.

If the above logic gates are to be of substantial utility, a means must be found to couple the output of one gate to the input of another. This can be done by series coupling. Figure 15 shows this scheme as applied to the coupling of an AND gate output to input of an OR gate. The AND gate (seen in cross section) is of conventional design except that its underside metallization has been patterned to isolate that portion of the ground electrode which lies under the detector. Wall motion currents to this electrode are fed to one trigger of an OR gate. For clarity, this is depicted as though the OR gate were on a second crystal. The series connection of detector and trigger implies that a domain wall can move under the trigger electrode if and only if a domain wall also moves under the detector electrode. If the logic condition is satisfied for the first gate, domain walls will move simultaneously in both its own detector and in the trigger of the next gate. During the restoring period, the domain walls in both gates return to their original

positions, again by a series flow of current. In practice, the two gates of Fig. 15 would be on the same chip, with the OR gate turned upside down. This configuration makes it unnecessary for leads to pass through the crystal.

Series coupling may be viewed as a means of electrically transporting a domain from one part of the crystal to another. The output detector of a shift register, for example, could be series-coupled to the input trigger of the same shift register. Thus, a continuous data loop could be created without the design constraint of actually forming a physical loop.

The ability to perform logical inversion is fundamentally necessary for generation of the full range of logic functions. The output of a series-coupled ferroelectric gate can be inverted by a subtraction scheme as illustrated in Fig. 16. The figure shows a conventional AND gate connected in series with a gate with no trigger (an "inverter") which is connected to a polarity reversed version of the usual detector square wave supply. Suppose that the logic condition of the AND gate is satisfied, so that a domain wall is allowed to travel under the AND gate's detector. When viewed from a point on the series connection lead (point A in Fig. 16), this condition is symmetrical: point A is connected through mobile domain walls to both normal and inverted power supplies. Hence, the voltage at point A will be zero during both the active and restoring periods. Point A constitutes the inverted output of the first gate and is connected to a trigger input of a succeeding gate. Since point A remains at zero volts, no current flows in this connection, and the succeeding gate's trigger will not be activated.

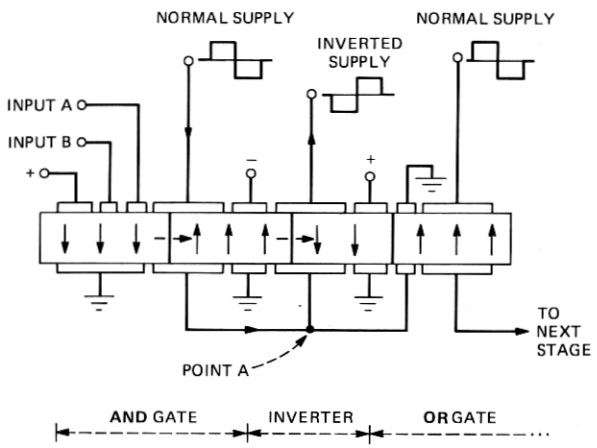

Fig. 16—Cross-section view showing an AND gate's output being inverted and series coupled to an OR gate input.

When the logic condition of the AND gate is not satisfied, no ferroelectric current will be provided to point A from the AND gate's square wave supply. However, the detector of the triggerless inverter gate always has access to a domain wall and will provide current to point A from the reversed polarity square wave supply. This current will activate the trigger of the succeeding gate. Thus the desired NAND logic function is accomplished. Since its trigger is activated from a reversed polarity source, all other aspects of the succeeding gate must be reversed in polarity also.

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