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The Nature and Use of Limit Cycles in Determining the Behavior of Certain Semideterminate Systems

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For some well-known systems such as speech encoders or digital filters, the excursions of the input are so dramatic and so loosely correlated that the system performance itself appears indeterminate. For these systems we present a technique of determining the system behavior by feeding a set of coherent frequency signals. For the analog inputs of any such system, we derive these inputs from coherent frequency synthesizers all synchronized to a common signaling frequency. For digital inputs into the system, we derive these inputs from a single master clock and set of logic functions to yield the desired bit patterns at different input ports. We present experimental evidence of the existence and utilization of these limit cycles for systems with some initial knowledge about the configuration and interconnections of components. The techniques presented here do not apply to systems for which complete initial ignorance is asserted.

I. INTRODUCTION

In the context of this paper, a limit cycle is defined as the periodic output into which the behavior of a system is forced by controlling one or several periodic inputs. The conditions which lead to an operation under a limit cycle vary from system to system. A perfectly linear system may exhibit a level-insensitive, limit-cycle condition whenever the input frequencies bear integral relationship(s) with respect to each other. A highly nonlinear system may exhibit several level-sensitive limit-cycle operations for each integral relationship(s) between the input signal frequencies. General techniques for using these limit cycles to evaluate and categorize system behaviors are presented. However, it is up to the ingenuity of the experimentalist to use the techniques to obtain the information sought about the system.

The coherence of the input signals is the fundamental concept behind the generation of limit cycles. For example, consider a network with several input ports. A set of input signals to the system would not produce a periodic response unless the inputs were mutually coherent, as well as individually periodic. The availability of stable frequency synthesizers and jitter-free digital signal generators has an immense effect on the stability of limit cycles and thus upon the design of experiments for evaluating the system behavior. In a sense, the technique is an extension of the single-input, single-output analysis which probes the system by changing the frequency and amplitude of the input signal. With multiport systems, the concept is expanded by using *coherent, periodic, and jitter-free* signals at the inputs. Phase jitter of analog signals and timing jitters of digital signals have detrimental effects on the stability of the limit cycles.

The determination of the behavior of semideterminate systems is often sought by exciting it with a given input signal and measuring the output response. Such techniques are potentially made difficult by variations in the initial state of the system when excited and the brevity of the measurement duration. The more suitable technique would be to excite the system in such a manner that a periodic response is generated. Furthermore, if a variety of input excitation exists which generate a variety of periodic responses, several aspects of system behavior can be probed. The basic condition for the generation of such periodic responses is that all input signals to the system be coherent. The condition of coherence is often difficult to achieve in real systems since random effects typically occur within the system. The random effects which cause variations in the functions performed by the system components are generally negligible. However, the additive random signals due to noise generation, etc. are usually not negligible and prevent fully coherent system signals.

Many systems exhibit the phenomenon of limit-cycle* behavior, however. Limit-cycle behavior is basically generation of a periodic output response with the application of a given set of periodic input signals despite the random, aperiodic noise effects. The limit-cycle behavior therefore allows coherent periodic input signals to be used to generate periodic output responses in a real system contaminated by random effects. The excitation of a limit cycle requires that a specified and well-controlled set of inputs be provided to the system. A somewhat stronger definition of limit-cycle behavior is used here to allow characterization of the overall system in terms of the behavior of

* Limit cycles generally degrade the system performance and for this reason they have been routinely eliminated, suppressed, or controlled (see the IEEE Trans. on Circuits and Systems, *CAS 24*, No. 6 (June 1977), p. 291 or 300). However, under specific conditions they provide an insight into the behavior of complex systems.

individual components. In particular, a stable limit cycle is defined as the condition in which the terminal voltages and currents for each component of the system are periodic, when random noise and circuit element parameter variations are included. Limit-cycle hopping occurs when the random effects are sufficient to disrupt a given limit cycle and trigger a new limit cycle with the same set of coherent signals applied. Limit-cycle hopping may occur since there may be more than one stable limit cycle associated with a given set of coherent input signals.

The discussion below characterizes some properties of limit-cycle behavior and presents examples of the use of limit cycles in determining the behavior of systems compatible with such an approach. In presenting limit cycles as a potential probe of system behavior, an important consideration is the variety of limit cycles which can be excited upon variation of the input signals. Examples of changes in the system inputs which may lead to different limit cycles are presented.

The most common method of visual and experimental observation of the system behavior is by synchronizing the oscilloscopic sweep with the frequency of input variation into the system. However, for a multi-input system consisting of both digital and analog inputs, the principle may be extended by ascertaining that the periodic repetition of all the inputs is derived from a common source frequency. Many such standard common source frequencies (e.g., Cesium clock, 64-kHz and 8-kHz standard signals, or any one of the overall Bell System synchronization[1] network frequencies at central offices) are available within the telephone network.

The nonlinearities within the system generally cause the system behavior to be level-sensitive after the synchronization of inputs has been achieved. However, if hysteresis and jump effects are tentatively ignored, then a finite set of input levels may often be achieved,* which will force perfectly repetitive behavior from the system. The number of components and the interaction of the nonlinearity of the various components also influence the level at which the system would reach a "limit cycle."

II. CHARACTERISTICS OF A LIMIT CYCLE

2.1 Modality of the limit cycle

When a set of coherent frequencies are present at the input to a system, then its reaction would tend, for certain parameter values, to

* In some "systems," limit cycle will never be achieved. For instance, take the case of an unbounded system or the case where the input is open-circuited and the output is connected to a source of arbitrary frequency or a case where the system has an infinite memory with variable initial conditions.

stabilize itself repeatedly during that minimum duration which can accommodate an integral number of cycles of each input frequency. For instance, when a linear delta modulator has a clock frequency of 24 kHz and the audio frequency (generated coherently from the 24 kHz) is 1.8 kHz, then the binary pattern generated would be perfectly repetitive every 1⅔ ms, thereby constituting three of 1.8-kHz cycles and 40 of 24-kHz cycles, and so on. Further, an oscilloscopic sweep should be able to display the voltages and currents at each component of the encoder and decoder as a stationary pattern. The nonlinearity of the adaptive delta modulation (ADM) introduces another dimension into the problem. Whereas the binary patterns, voltages, and currents, may be stable for selected values of the audio frequency input to a delta modulator without any memory effects, a further restriction of voltage levels for a limit cycle occurs for an adaptive delta modulator, because of the multiple weighted memory effects from the past bits. These tend to alter the final values of the currents and voltages of each of the components of the encoder and decoder from their initial values exactly 1⅔ ms earlier. Hence, the stability of the limit cycle, by definition, is that the voltages and currents for each component of the system do not violate the boundary condition every 1⅔ ms, or some integral multiple, which constitutes the duration of a limit cycle. Section A1 in the appendix describes the ADM codec operation[2] and Section A2 discusses the generation and experimental existence of such limit cycles for the ADM codecs.

The relative phases of the inputs also influence the existence of a stable limit cycle. When three coherent inputs A, B, and C, are forced at the inputs of a system, then the boundary conditions for various values of the phase relations between A, B, and C, would all be different. Such a condition influences the input levels for which the system would reach a limit cycle, especially if the former has nonlinear feedback. Under these conditions, the phase relations between the inputs offer another parameter to control the stability of the limit cycle if it is difficult to achieve by level adjustment alone.

2.2 Advantages of operation under limit cycle conditions

When the performance of a system and its components must be critically evaluated, then the limit cycle functioning presents a repeated picture of all the parameters within the system. Further, since a large number of limit cycles can be generated, the observer can obtain the parameters under a diversity of conditions, thus having an opportunity to "freeze" the performance of the components by synchronizing the inputs. Such a "frozen" picture would depict the component performance under a given set of conditions which would otherwise exist only as transients. (See Section A3 in the appendix.)

During early developmental steps of a system, these limit cycles offer an invaluable tool in critically deriving the component values and ascertaining their accurate performance.

These limit cycles can be used to characterize the system performance and the component values. Further, when uncertainty of performance* has to be eliminated, the inputs may be synchronized to study the effect on performance. The concept applies to both linear and nonlinear systems. For hybrid systems, both coherent analog and digital inputs may be derived from frequency synthesizers which also trigger pulse generators. While testing the coherence of a system in the time domain, the limit cycle still offers a means of validating the correct functioning. Coherent inputs under specific conditions produce a coherent output from determinate systems. This principle has been exploited to test the interfacing of a minicomputer from an ADM voice encoder. The computer clock, the ADM clock, and the audio frequency input are coherently derived with respect to a predefined frequency synthesizer. The received binary data within the memory must form a repetitious pattern repeating at the limit cycle frequency. When the sequence is permitted to accumulate over several seconds or minutes, the memory core locations at which the binary pattern repeats yields any malfunctioning of the interfacing. In addition, the exact input conditions which caused the error can be traced by the break in the limit cycle. This principle is further explained and utilized in Section A4 in the appendix.

III. STABILIZATION OF AN *n* INPUT SYSTEM

3.1 Analog system

Consider the n inputs into a system to be at $f_1, f_2, \cdots f_n$ Hz. The limit cycle would have a duration of t seconds, which is the lowest common multiple of $t_1, t_2 \cdots t_n$ seconds at the respective frequencies of $f_1, f_2, \ldots f_n$ Hz. If the frequencies are adjusted to have no phase jitter with respect to one another, then the initial boundary conditions at the start of the limit cycle are such as to lead to identical final boundary conditions at the conclusion of the limit cycle. Unless this criterion is satisfied, there is no limit cycle every t seconds. However, it is sometimes possible to meet these boundary conditions every $2t$, $3t$ seconds, etc. Under these circumstances, the limit cycle would form not at the lowest common multiple of $t_1, t_2 \ldots t_n$, but at its multiple values. When the number of inputs and the complexity increases, then

* We have successfully used this principle (Ref. 3) to eliminate the idle channel noise (which becomes worse as the clock rate diminishes) of an ADM decoder by forcing a bit pattern of 0101 $\cdots$, 00110011, 01001101, etc. (derived from the master clock) during silence periods.

it becomes more and more frequent to see the limit cycle* itself hopping from one period to another (say, from $2t$ to $3t$ seconds and so on). Stabilization of an n input system thus becomes progressively more difficult as n increases considerably.

When the wave shapes of various inputs are not sinusoidal, the response of the system contains transient or higher frequency effects. The overall criterion, even though identical to the one described earlier, is influenced by multiple n' frequency effects† superimposed by n'' sinusoidal responses. Under these conditions of mixed inputs, the existence of the stability is not evident, especially in the presence of intrinsically nonlinear feedback effects within the system. However, for experimental investigation, the control parameters (i.e., the levels of inputs and the phase relationships), if judiciously used, may lead to a stable limit cycle at t or multiple t second periods.

3.2 Digital systems

The n digital input signals may be coherently derived from a single master clock and a series of n logic circuits. When the input patterns repeat, an input cycle is created even though the bit values could vary in any order within this input cycle. The n inputs so derived would correspond to the n inputs of analog systems and the entire discussion of the periodicity and stability of the limit cycle applies for digital systems as well.

However, since far greater transients are imposed upon the system unless it is a perfect digital system, the system is unlikely to achieve the limit cycle within the lowest period t. Once the digital system is functioning perfectly synchronously, out of transients, it must achieve its limit cycle within the period t, and this test may be critically employed to test the overall functioning of the system and to localize any malfunctions. Hybrid systems, on the other hand, face all the uncertainties that a perfectly analog system would face with nonsinusoidal inputs, and the input flexibility available for the analog system does not exist for the n digital input hybrid system. However, the experimentalist does have a control of the bit patterns within the input cycle, and it may be controlled to yield a limit cycle. This principle may be extended to study the transient behavior of a system. For instance, when the transient response of an ADM compander is to be determined, a data pattern of a sequence of 0's or 1's followed by a sequence of 0 to 1 (which is coherent with the clock frequency) excites

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* The existence of these "quasi-limit cycles" is analogous to the existence of instantaneous frequency. These quasi-limit cycles occur when the stability of two or more limit cycles becomes equally likely.

† n' is the number of the nonsinusoidal inputs and $n'' = n - n'$.

the decoder. The audio frequency output (or the voltage at the output capacitor) contains the nature and extent of the transient response when the binary data changes from a sequence of 0 and 1 to a long sequence of 0's or 1's, and vice versa. The details are presented in Section A4 of the appendix.

IV. DEGREE OF CHARACTERIZATION AND NUMBER OF INTERMEDIATE POINTS

Multi-input systems are generally too complex to have the overall system performance analyzed by a single output study. Hence, a series of intermediate points can be selected to determine the characteristics of the elements constituting the system. Under limit cycle conditions, the propagation of the input at each port is influenced by the character of the input at all the other ports by a determined amount and at a repeated interval.

If the effect of the inputs is also experimentally determined (by studying the intermediate points limit-cycle conditions), then the behavior of each element can be uniquely described to make up for the overall system performance. Hence, the choice of intermediate points and the study of the circuits and voltages at these points is critical in determining an overall system performance. For instance, if the characterization of an ADM codec[2] is necessary, the decoder, consisting of a four-bit shift register, a compander circuit, a current generator, a polarity selector, and an integrator capacitor, can be modeled by (*i*) forcing a series of synchronous binary bit patterns at the input and by (*ii*) recording the following:

(*i*) Compander functioning (to relate the shift register pattern and compander action).

(*ii*) The compander capacitor voltage (to relate the compander function with the extent of the change in compander capacitor voltage).

(*iii*) The generated step current (to relate the compander capacitor voltage and the size of the current).

(*iv*) The integrator capacitor voltage (to relate the change in audio frequency output and the size of the step current).

If it is not already known that the polarity reverses with the binary bit, it would also be necessary to record the polarity selector function. These principles, used together under various limit-cycle conditions, have led to the development of an ADM decoder model.

V. CONCLUSIONS

Limit cycles are useful in (*i*) characterizing a system function in a time domain, (*ii*) "freezing" the transient response of systems and their components especially if there are two or more inputs, and (*iii*) debugging and testing a multi-input system operation.

System coherence is the fundamental concept behind the technique of generating and stabilizing limit cycles.

Inputs are most easily obtained by synchronous frequency synthesizers and/or triggered pulse generators for the analog, hybrid, and/or digital systems. The method has proven satisfactory for a complex ADM system and can be valuable for other coherently excited systems. A judicious choice of intermediate points is necessary to characterize a system and, when extreme nonlinearities are present, a study under a series of limit cycles also becomes essential. For completely digital systems, the pulse generators and word generators assume the role of frequency synthesizers. However, the master clock is the most essential component to prevent any drift in the pulse generators which completely destroys the stability of the limit cycle.

VI. ACKNOWLEDGMENTS

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APPENDIX

A1. ADM CODEC DESCRIPTION

Adaptive delta modulation (ADM) decoders are D to A converters in which digital data are translated to an analog or an audio signal. Under ideal conditions, the signal from the decoder closely approximates the analog or audio signal originally used at the encoder to generate the digital stream of data. Decoders consist of three main components: (*i*) the compander, (*ii*) the polarity selector, and (*iii*) the integrator. The compander function controls the current step size which directly accumulates or depletes the charge on the integrator capacitor. The polarity selector controls the charge or depletion of the integrator capacitor; charging it if the last bit was a one, and depleting it if the last bit was a zero. The action of the compander is generally accomplished by controlling the voltage on another capacitor (step-size capacitor). The attack time constant for syllabic companding is about 3 ms, and the decay time is about 9 ms. The history of the received bits dictates the functioning of the compander, forcing a charge on the step-size capacitor (thus increasing the step size) if the last four bits were identical. In the absence of any companding, the step size of incremental current on to the integrator capaciter decays to about 1/200 of the maximum current step size. The change of step size is quite nonlinear, changing dramatically when the step size is low, and absolutely saturating as the step size approaches the 46-dB range.

The encoder has a comparator in addition to the decoder. The decoder voltage and the incoming voltage are continuously compared, and the output of the comparator (0 or 1) is forced back into the decoder and also constitutes the digital stream from the encoder. The encoder-decoder pair is called the codec, and the characteristics of this device are examined by the limit cycle techniques in this paper.

A2. ADM ENCODER CHARACTERIZATION WITH SINUSOIDAL INPUT

In this configuration, the system is hybrid with audio input (which is obtained from a frequency synthesizer tuned to the master clock at 1 mHz) and digital clock input (derived from a triggered pulse generator also synchronized to the same master clock). The ADM encoder is a nonlinear device in which the step size can vary within a range of 46 dB. Hence, the stability of the limit cycle critically depends on the value of the input voltage. Limit cycles, even though possible for any time period encompassing integral cycles of audio frequency and clock frequency, were obtained readily at 240, 480, 720, 1000, 1200, 1500, 1800, 2000, 2400, 2700, 3000-Hz audio frequency and at 18-kHz or 24-kHz clock frequency. Two examples of the limit cycle are shown in Figs. 1a and 1b. In Fig. 1a, the 240-Hz cycle is shown with an 18-kHz clock. The period of the limit cycle is 12.5 ms spanning three 240-Hz cycles and 225 18-kHz cycles. The binary bits pattern is generated $b\ \bar{b}\ b'\ \bar{b}\ b\ b''$,*

where b = 00001000010001001000101010101001000100 (= 38 bits)
b' = 000111000001110011100011001110111011 (= 36 bits)
and $b'' = \bar{b}'1$ (= 37 bits).

The entire number of these bits totals 225, corresponding to one bit generated by the encoder every clock cycle. The lower trace indicating the output from the codec exhibits a fairly satisfactory 240-Hz wave shape generated at its output.

In Fig. 1b, when the audio frequency is at 2700 Hz and the clock frequency is at 24 kHz, the performance of the codec is evident from the lowermost trace. Here the codec is incapable of regenerating a satisfactory 2700-Hz signal at the output. The limit cycle is generated every ⅓ ms to span 9 cycles at 2700 Hz and 80 cycles at 24 kHz. The bit pattern can be denoted as

$$(b\ \bar{b}\ b\ \bar{b}'\ b\ \bar{b}'\ b'\ \bar{b}\ b\ \bar{b}\ b'\ \bar{b}'\ b\ \bar{b}\ b'\ \bar{b}'\ b'\ \bar{b}),$$

where b is equal to 1111 and b' = 11111. This is a perfectly balanced example of b and $\bar{b}$; b' and $\bar{b}'$. The total number of bits amount to 80, covering 9 cycles of input frequency.

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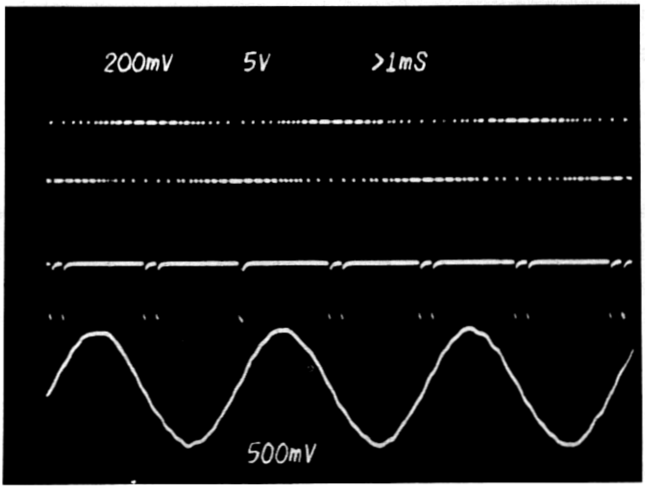
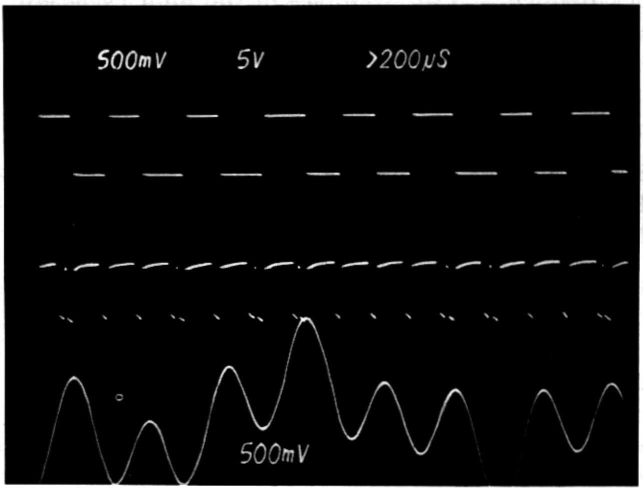
* $\bar{b}$ represents the complement of the block b.



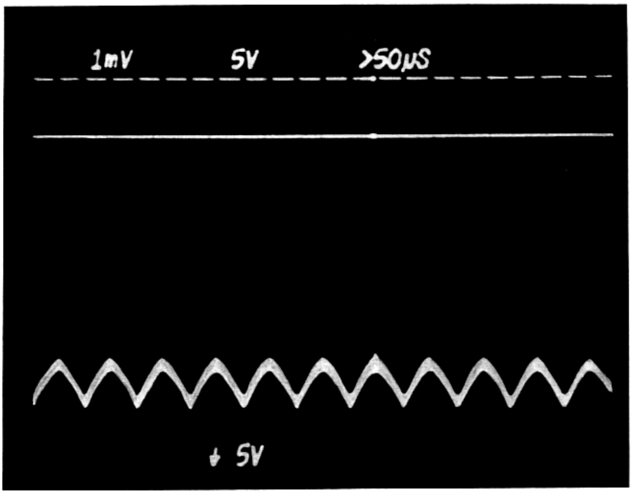
(a)



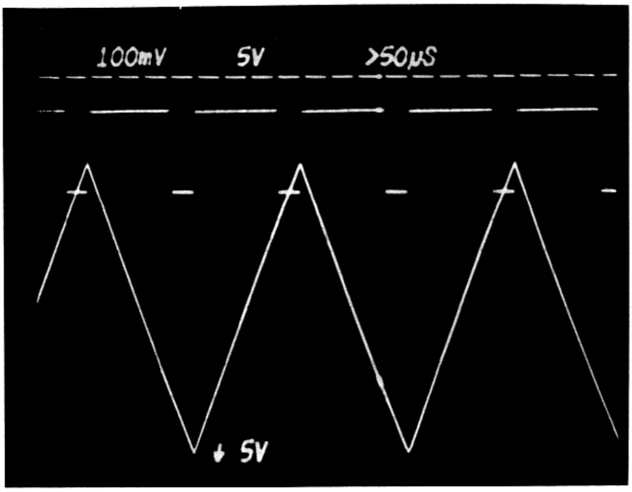
(b)

Fig. 1—Generation of encoder limit cycles. Top trace: Binary data. Middle trace: Compander action. Lower trace: Output of the ADM decoder. (a) Limit cycle obtained by 240 Hz at the AF input and 18 kHz at the clock frequency input into a *SLC*®-40 encoder. (b) Limit cycle obtained by 2700 Hz at the AF input and 24 kHz at the clock frequency input into a *SLC*-40 encoder.

In other cases where the relation between audio frequency input and the clock rate is a lower integer number such as (8 or 10), the binary repeat patterns are simpler and generally far more stable than the examples presented.



(a)

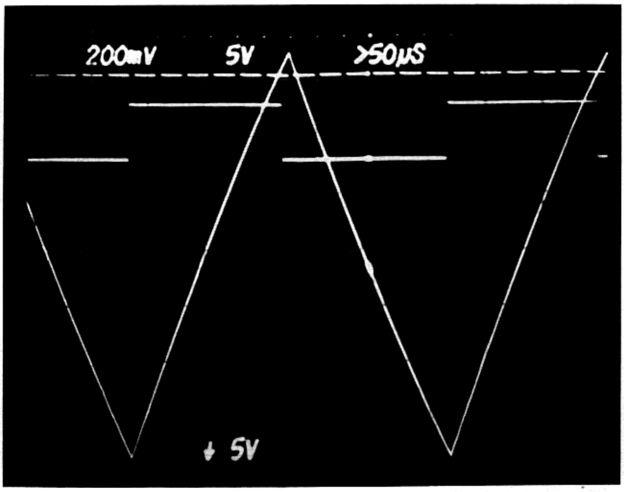


(b)

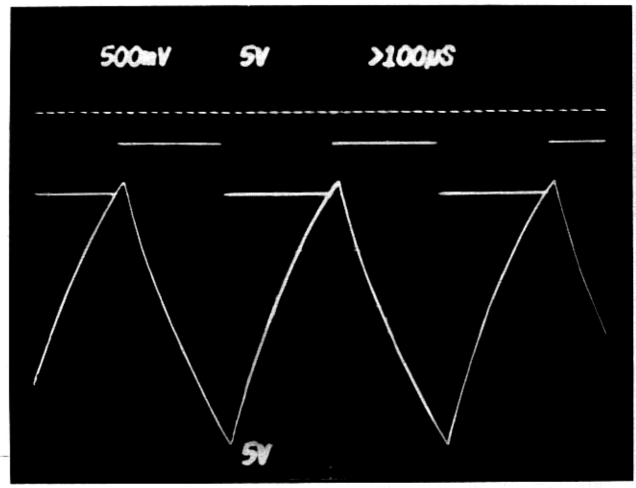
Fig. 2—Generation of decoder limit cycles. (a) Integrator voltage (lower trace) from a *SLC*®-40 decoder for a 0101 ··· sequence of coherent data input. (b) Integrator voltage from the decoder for a 00001111 ··· sequence of coherent data input. (*Continued*)

A3. ADM DECODER CHARACTERIZATION

When the clock and the binary bit pattern are synchronized, the operation of the decoder can be made perfectly repetitive. In the three sections of this appendix, three such models are presented (*i*) characterization with (0101, 00110011, etc.) inputs (to study the stable step



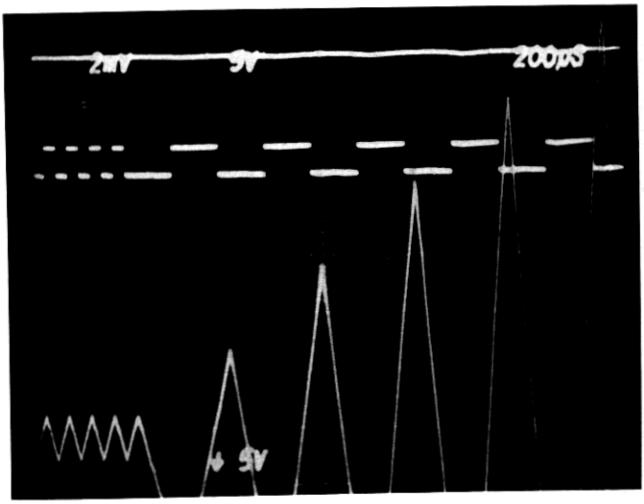
(c)



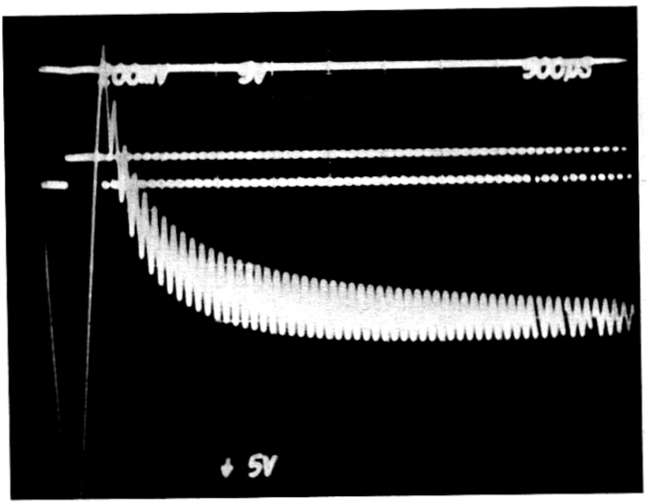
(d)

Fig. 2 (*continued*)—(c) Integrator voltage for a 111111000000 ··· sequence of coherent data input to the decoder. (d) Integrator voltage for a 1111111100000000 ··· sequence of binary input data.

sizes at different frequencies), (*ii*) characterization with (010101 ··· 00001111 00001111 ···) inputs (to study the decay and build-up of step sizes) and (*iii*) characterization with (0000 ··· or 1111 ···) ··· 010101 ···) input (to study growth and decay to the maximum step size).

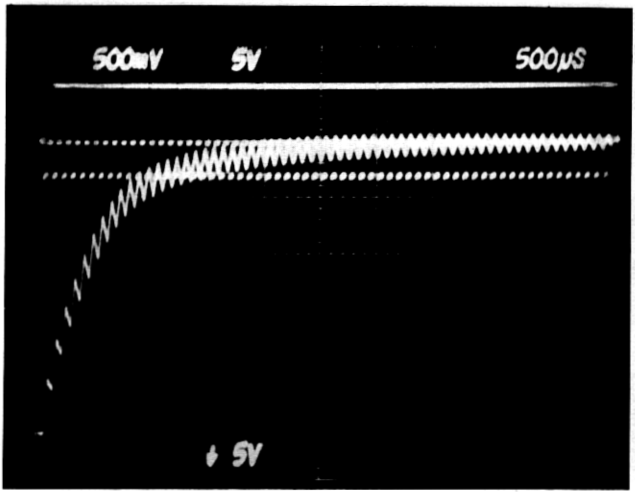


(a)

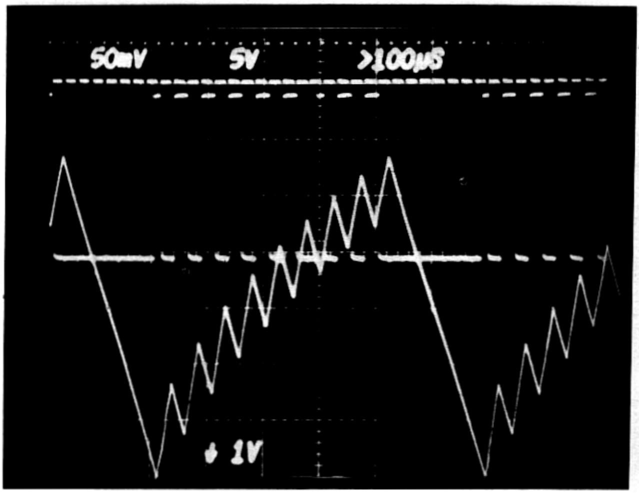


(b)

Fig. 3.—(a) Growth of step size at the decoder integrator capacitor by a sequence of 0101 ··· 00001111 ··· data. Limit cycle is generated by accommodating the 0101 sequence in 64 cycles of the master clock and 00001111 sequence within the 64 clock cycles of the master ADM clock. The periodicity of the limit cycle is 128 master clock cycles. (b) Decay of step size at the decoder integrator voltage by a sequence of 0101 ··· 0100000000111111111 ··· binary data. The 0101 sequence is lodged in 256 master clock cycles at 24 kHz and 0000000011111111 sequence within the next 256 cycles. The limit cycle repeats every 10⅔ ms.



(a)



(b)

Fig. 4—(a) Decay of integrator voltage from high values. The system is forced into a limit cycle by a string of 256 zeros and by a string of 0101 ··· for the next 256 clock cycles. The periodicity of the entire limit cycle is 10⅔ ms at 24-kHz master clock. (b) Limit cycle generated by a sequence of 000001010101010101010101 (repeat) from a 24-kHz clock showing the change in step size of the decoder at medium ranges of integrator voltage. Three synthesizers were used in synchronization to generate the more complicated coherent bit patterns.

CORE LOCATION	BINARY DATA							
002000	020057	001377	027762	177440	171002	020057	001377	027762
002010	177440	171002	020057	001377	027762	177440	171002	020057
002020	001377	027762	177440	171002	020057	001377	027762	177440
002030	171002	020057	001377	027762	177440	171002	020057	001377
002040	027762	177440	171002	020057	001377	027762	177440	171002
002050	020057	001377	027762	177440	171002	020057	001377	027762
002060	177440	171002	020057	001377	027762	177440	171002	020057
002070	001377	027762	177440	171002	020057	001377	027762	177440

ONE LIMIT CYCLE

070000	177440	171002	020057	001377	027762	177440	171002	020057
070010	001377	027762	177440	171002	020057	001377	027762	177440
070020	171002	020057	001377	027762	177440	171002	020057	001377
070030	027762	177440	171002	020057	001377	027762	177440	171002
070040	020057	001377	027762	177440	171002	020057	001377	027762
070050	177440	171002	020057	001377	027762	177440	171002	020057
070060	001377	027762	177440	171002	020057	001377	027762	177440
070070	171002	020057	001377	027762	177440	171002	020057	001377

(a)

004000	177217	177077	176127	000405	176247	001561	177512	001414
004010	001150	000241	002003	176330	001427	175311	000045	176077
004020	176461	000075	176051	000747	176703	001764	000357	000770
004030	001606	177260	001735	175452	000701	175507	177203	177072
004040	176127	000410	176260	001567	177521	001425	001157	000244
004050	002001	176316	001407	175276	000024	176300	176451	000046
004060	176045	001014	176672	001713	000342	000741	001571	177252
004070	001732	175470	000677	175527	177200	177071	176127	000374
004100	176243	001543	177504	001404	001145	000237	001775	176326
004110	001421	175317	000045	176104	176456	000075	176047	000745
004120	176676	001750	000350	000764	001603	177261	001733	175465
004130	000707	175521	177215	177072	176135	000406	176253	001560
004140	177500	001421	001146	000245	002000	176322	001425	175306
004150	000053	176074	176462	000077	176050	000751	176675	001760
004160	000351	000772	001576	177261	001730	175625	000674	175506
004170	177211	177017	176121	000610	176243	001457	177467	001345
004200	001144	000212	001774	176310	001415	175536	000047	176032

ONE LIMIT CYCLE

010120	000675	175560	177217	177071	176126	000135	176256	001663
010130	177513	001442	001151	000274	002001	176335	001410	175310
010140	000036	176100	176461	177735	176041	000762	176662	002011
010150	000325	001001	001571	177265	001733	175620	000703	175505
010160	177220	177031	176127	000342	176243	001517	177470	001354
010170	001130	000223	001776	176312	001420	175526	000055	176027
010200	176463	000037	176045	000765	176666	001654	000335	001126
010210	001600	177173	001737	175574	000712	175467	177215	176777
010220	176133	000725	176244	001445	177467	001463	001135	000172
010230	002001	176240	001427	175460	000054	176200	176465	177765
010240	176041	001117	176671	002017	000331	001015	001566	177101
010250	001733	175477	000672	175541	177222	176734	176131	000660
010260	176235	001502	177462	001463	001124	000055	001774	176153
010270	001425	175466	000053	176064	176464	177662	176036	001430
010300	176650	001700	000317	000714	001557	176771	001736	176102
010310	000722	175363	177231	176644	176133	000565	176237	001621
010320	177466	001327	001140	177756	001775	176224	001417	175555
010330	000034	175767	176454	177551	176043	001324	176671	001617
010340	000341	000737	001571	176677	001734	176123	000704	175511
010350	177210	176610	176130	000422	176245	001717	177501	001402
010360	001142	177742	002000	176704	001422	175323	000044	176117
010370	176465	177422	176051	001251	176672	001625	000344	000623

(b)

Fig. 5—(a) Limit cycle generated in the stored data from the ADM encoder for the interface testing. Note that location (70040_8 to 2000_8) is a perfect multiple of 5 confirming that the intermediate locations have also received the ADM data from the interface correctly. (b) Limit cycle generated by the stored analog-to-digital converter interface testing. Note that corresponding points on a repeating sine wave as they are scanned by the A to D converter occupy corresponding locations in the computer core, thus implying a properly functioning interface.

A.3.1. Stable step size characterization

Typical voltages at the integrator of the decoder are shown in a sequence of oscillograms, Figs. 2a through 2d. The input is generated by a series of simple logic circuits but activated by the same master clock feeding into the decoder.

A.3.2. Growth and decay of step sizes

When a sequence of 0101 ⋯ is interleaved with a series of 00001111 ⋯ (or any sequence during which the compander is repeatedly activated), then the step-size build-up may be studied in any desired detail. If the time constant for the build-up and decay are not known, then results offer an exact method to experimentally determine their exact values. Typical oscillograms are presented in Figs. 3a and 3b.

A.3.3. Growth and decay up to the maximum step size

Maximum step size of the decoder can be generated by a long sequence of zeros or ones. When such a sequence is interleaved with a sequence of 0101, the transient phenomenon of the build-up or decay can be rendered cyclic. This leads to the calculation of the maximum step size and its response to the compander circuit parameters (such as the compander capacitor voltage, the changing registers, etc.). Typical oscillograms are shown in Figs. 4a and 4b, and a series of such oscillograms have been used to characterize the decoder model used for additional work.

A4. MINICOMPUTER INTERFACE TESTING

When the input of the encoder is stored in a minicomputer, it is essential to check the validity of interface effectively. Such a test can be performed by forcing the encoder into a limit cycle operation yielding known bit patterns repeatedly. When the same clock is also used to shift and store data into the core (and then into a disk storage by subjugating the computer clock to the ADM clock), then these patterns lead to a series of binary stored words. Figs. 5a and 5b show two such examples for testing the ADM interface and the ADC (analog to digital) interface. In Fig. 5a, the bit pattern generated leads to a sequence of binary words:

100177 003772 077650 175200 124007

in the computer core (and also on the disk), when the audio frequency input and the clock frequency input are 800 Hz and 24 kHz. The same input into an ADC converter (at the input and output of the codec, odd and even word count; see Fig. 5b) leads to a sequence where every 30th word repeats (within the accuracy of A to D conversion feasible with the interface).

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