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No. 4 ESS:

Prologue

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Since the cutover of the first No. 4 Electronic Switching System (ESS) office in January 1976, a program of system evolution has been carried out. As a result significant cost reduction was achieved, major new features have been added to the No. 4 ESS, and the system's performance has been enhanced. This paper gives an overview of the continuing development of the No. 4 ESS carried out during the period 1976 to 1980 as a prologue to a series of papers in this volume which describe some of the specifics of this activity.

I. BACKGROUND

In January, 1976, the first No. 4 Electronic Switching System (ESS) was placed in service in Chicago, Illinois. This culminated the largest single system development ever undertaken in the Bell System, a development which produced a high-capacity toll and tandem digital switching system. The No. 4 ESS, with its powerful central processor and time division network, brought to the Bell System telecommunications network significant improvements in flexibility, reliability, and economy compared with its electromechanical predecessors.

However, except for the large increase in capacity, the basic toll-switching features of the early No. 4 ESS machines were essentially a very modern version of the No. 4A crossbar features. Therefore, the development of the No. 4 ESS did not end with the cutover of the Chicago 7 office. Instead, a program of evolution of the system planned

to achieve significant cost reduction, as well as feature additions and performance improvements, was vigorously pursued. Stimulated by dramatic advances in integrated circuit technology and improved software design and circuit interconnection techniques, the No. 4 ESS was virtually completely redesigned in the period from 1976 to 1980. Five major new versions of the software package, called generics, along with new hardware designs, were introduced on roughly yearly intervals during this period. These generics added some additional toll functions and major new network revenue-producing features; produced reductions in cost, power, and space; and improved reliability and maintainability.

II. INITIAL SYSTEM IMPLEMENTATION

The 1976 architecture of No. 4 ESS is shown in simplified form in Fig. 1.[1] In this original design, analog signals were converted to voiceband by transmission terminal equipment and then converted to pulse-code modulated (PCM) signals and multiplexed into DS-120 streams in the Voiceband Interface Frame (VIF). A Signal Processor Type 1 (SP1) was connected to the E and M leads from/to the transmission terminal equipment. The SP1 detected and interpreted state changes on the E lead and generated appropriate state changes on the M lead. Digital carrier (T1) signals entered the system at the digroup terminal (DT), where these signals were multiplexed into the DS-120 format. The signal processor type 2 (SP2) derived supervisory states from the incoming PCM stream and generated supervisory states in the transmit direction for inclusion in the outgoing PCM stream.

The No. 4 ESS time-division switching network contains six stages of time-shared switching: time-space-space-space-space-time. The first and last pairs of switching stages are implemented in the time-slot-interchange frame (TSI). The TSI also performs a decorrelating function by which the PCM signals in successive time slots in each incoming DS-120 digital stream are spread in both time and space as a result of the switching action. This ensures spreading of traffic over the network and eliminates the need for load balancing. The middle two stages of time-shared space switching are provided by the time-multiplexed switch (TMS). The pattern of network connections in this 1024-by-1024 switch is changed 1.024×10^6 times every second. The No. 4 ESS is internally synchronized by an extremely precise and reliable clocking system consisting of four crystal-controlled oscillators operating at 16.384 MHz. In normal operation, one oscillator is designated the master, supplying the timing pulses for the network, while the remaining three oscillators are in standby, phased-locked to the master.

The entire No. 4 ESS is under the control of the powerful 1A Processor, which has a central control and three memory types:

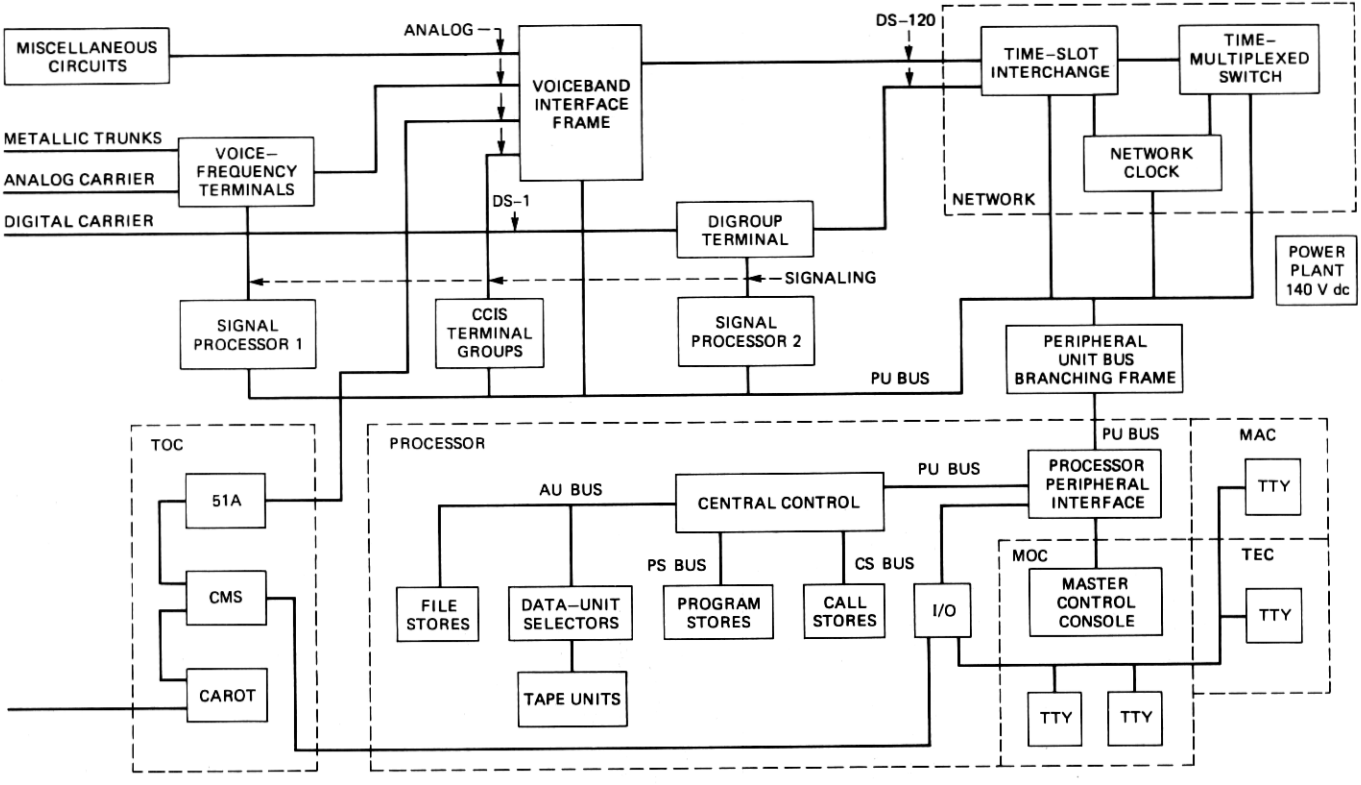

Fig. 1—No. 4 ESS: 1976.

program store, call store, and file store. The program store contains the fixed set of software instructions. The call store contains the time-variant data associated with setting up calls and handling other office activities. The call store also contains translation data describing the office configuration and prescribing the office-specific call-handling parameters. The file store on disk is used primarily as a backup for the program store and the fixed data in call store. The file store also contains less-frequently used programs, such as diagnostic routines. The original program and call stores were coincident-current ferrite-core arrays with fetch cycles of 1400 ns, twice the 700-ns cycle time of the central control.

III. SYSTEM EVOLUTION

The continuing development of the No. 4 ESS affected both the software and hardware architecture of the system. When the No. 4 ESS was first placed into service, its complement of software consisted of approximately 1.4×10^6 stored words in over 800 identifiable functional units called PIDENTS, written primarily in a language called EPL (ESS programming language). EPL is an "intermediate level" language, more powerful than assembly language, but not as powerful as a "high level" language. EPL, together with a set of macros, offers designers a degree of mechanization while maintaining tight control over the use of real time—a matter of constant concern because of the very high switching capacity requirements. However, to increase the productivity of the software development staff by taking advantage of more modern software technology, a high-level language for switching, called EPLX, (ESS programming language extra) was developed for use in the No. 4 ESS. EPLX has modern control constructs and high-level data description and data structure reference capabilities. Since the EPLX compiler produces somewhat less efficient code in terms of memory and real-time consumption, when these factors are paramount the designer can still mix EPL with the EPLX on a module-by-module basis.

An extensive amount of new software has been written for No. 4 ESS to introduce new call-processing features, expanded administrative capabilities, and improved maintenance and fault-recovery operations. As part of the development of the new international switching functions using CCITT No. 5 and No. 6 signaling, the call-processing software was restructured to improve its flexibility and maintainability. Over the last several generics the maintenance and fault-recovery software was modularized and restructured under a special operating system to facilitate the inclusion of new peripheral frames into the system. This new software was written in EPLX. Also, with each new peripheral frame type introduced into No. 4 ESS, a considerable quantity of new fault-recovery, maintenance, and diagnostic software was written. Virtually all areas of administrative function, including recent change-

and-verify, trunk-maintenance, network-management, report-generation, and operations-support-system interfaces, have been augmented and expanded. In addition to the international call-switching functions, major new functions such as Common Channel Interoffice Signaling Inward Wide Area Telephone Service, and the Mass Announcement System have been added. As a result of all this software development activity, the 1980 No. 4 ESS generic contains in excess of 2.1×10^6 words of software program.

Between 1976 and 1980, the evolution of No. 4 ESS hardware has been comparably extensive (Fig. 2). In the 1A Processor, the memory was upgraded from the original ferrite-core memory arrays to semiconductor memories. The transition was accomplished in two stages. In 1977, metal oxide semiconductor (MOS) integrated-circuit memories in 65,536-word modules were introduced into the system. The fetch-cycle time of these memories was 1400 ns, the same as that of the core memories. In 1979, newer semiconductor memories with 262,144-word modules were added. These memories have a 700-ns fetch-cycle time capability. Thus, while the 1A Processor central control was designed to function with a mixture of all three memory types, the processors equipped entirely with the newer semiconductor stores running in the fast mode (700-ns cycle) have 30 percent more processing capacity.

In addition to the memory upgrade, a new high-speed input/output processor was developed for the 1A Processor to handle all the various I/O functions for the system, including interfaces with operations support systems, such as the Engineering and Administrative Data Acquisition System and the Circuit Maintenance System.

Although the frames in the time-division network perform similar functions to the original No. 4 ESS network frames, major improvements have been made in all the frame types. The availability of medium-scale-integration bipolar memories to replace the original small-scale-integration insulated gate field-effect transistor (IGFET) memories in the random access memories of the original frames led to a redesign of the TSI and TMS frames. Also, bulk dc-to-dc power converters with 100-ampere capacity were developed. Thus, new TSI and TMS frames were produced which offered savings in cost, space, and power consumption.

The network clock was also enhanced to allow automatic synchronization to a master clock source. Even though the original network clock had excellent long-term stability, the individual clocks had to be periodically manually adjusted to ensure the synchronization necessary to prevent data from being lost when transmitted over digital facilities between digital offices. The new automatic synchronization obviates the need for manual adjustments and ensures more reliable operation of the toll network.

The original architecture of No. 4 ESS utilized echo suppressors for

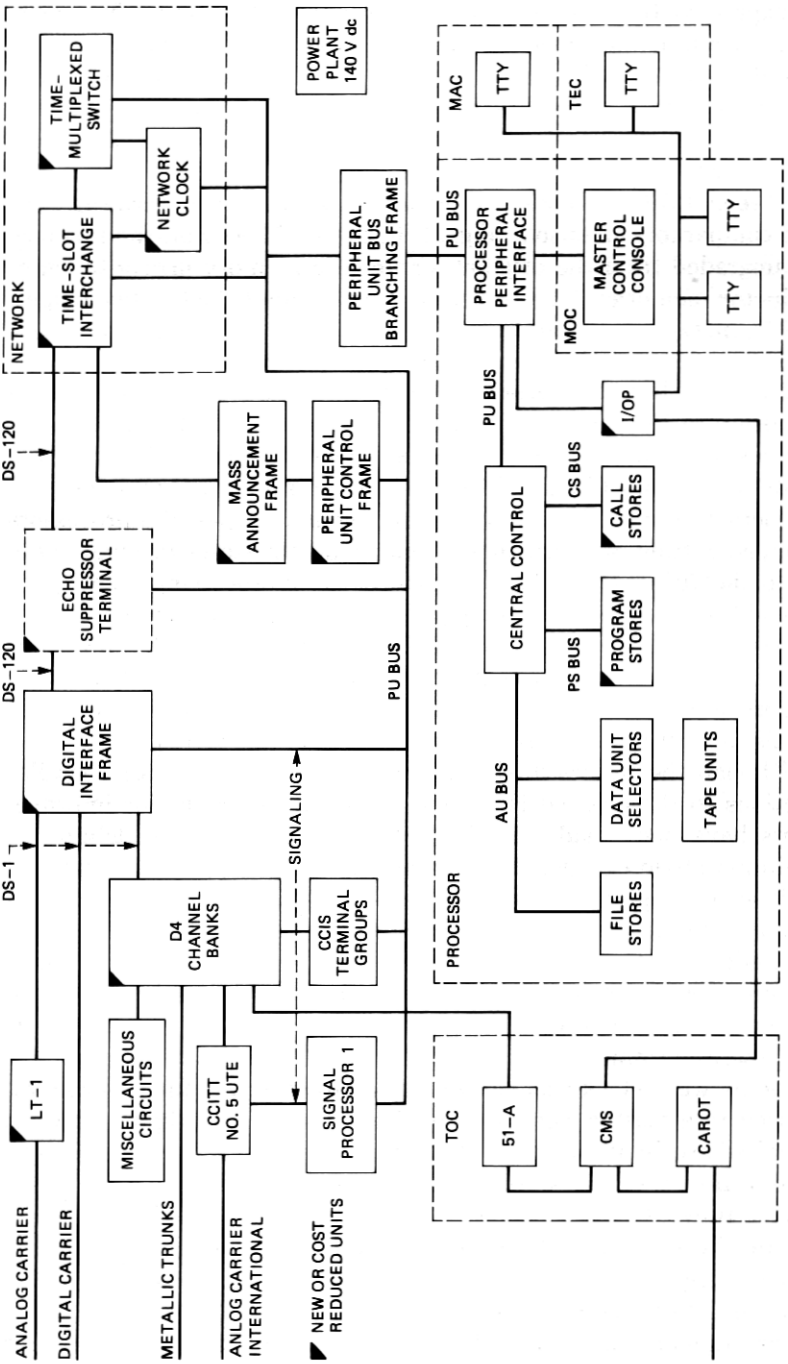

Fig. 2—No. 4 ESS: 1980.

long-transmission circuits. These echo suppressors, which employed standard analog techniques, were mounted in transmission terminal equipment, one per voice channel. Subsequently, a digital echo-suppressor terminal was designed to operate in a time-shared mode on the DS-120 stream. Functionally the digital echo suppressor is equivalent to its analog predecessor, but is significantly more economical. This evolution will continue with the provision of digital echo cancellers, implemented with very-large-scale integrated circuit chips.

There have been significant modifications to the transmission terminals in No. 4 ESS, particularly regarding the handling of the analog carrier interface. Initially, group band carrier was connected to terminal equipment that converted the signals to baseband. Signaling was extracted for processing by the SP1 while the baseband information passed into the VIF where it was converted to PCM and multiplexed into DS-120 streams. With the availability of the DT/SP2 complex, it became economically attractive to use PCM carrier terminals (such as D4) to provide the analog-to-digital conversion. Further economies were realized by combining functions. An LT-1 connector frame was developed to convert 12-channel analog carrier groups to the PCM DS-1 format. Also, a Digital Interface Frame (DIF) was developed to handle the DT/SP2 functions. The DIF is a microprocessor-controlled frame which uses the most current semiconductor device and packaging technologies.

Finally, powerful new functional capabilities have been provided in the Bell System network with the addition in No. 4 ESS of the Mass Announcement System frame and its associated Peripheral Unit Control (PUC) frame. Like the DIF, these frames are microprocessor controlled and use the latest device technology.

Table I gives a chronology of the introduction of the major new No. 4 ESS features described briefly above.

Table I—Major new features

1976	Basic toll features plus Common Channel Interoffice Signaling (CCIS).
1977	Digital echo suppressor, cost-reduced Digroup Terminal (DT), 64K-word 1400-ns semiconductor store.
1978	International-call switching exchange functions using CCITT No. 5 and 6 signaling, cost-reduced Time Slot Interchange (TSI), Input/Output Processor (IOP), and maintenance and administrative enhancements.
1979	CCIS—Inward Wide Area Telecommunications Service (INWATS), 256K-word 700-ns semiconductor stores, switching control center interface, maintenance and administrative enhancements, and reduced system reinitialization time.
1980	Digital Interface Frame (DIF), LT-1 connector, cost-reduced Time Multiplexed Switch (TMS), network clock synchronization, mass announcements, and maintenance and administrative enhancements.

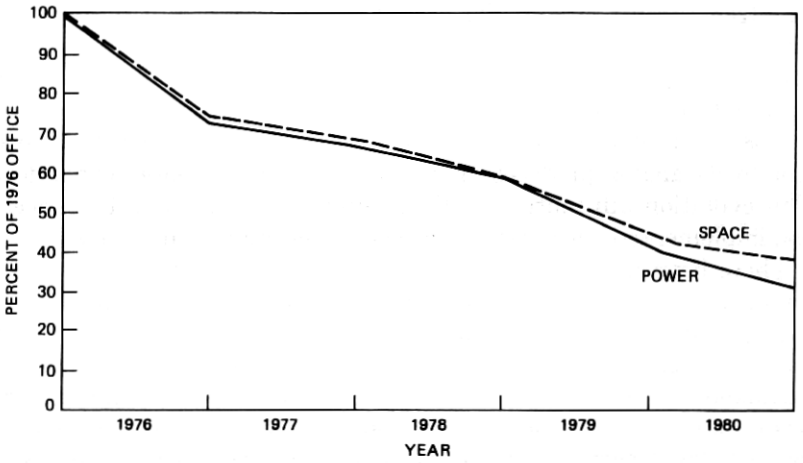

Fig. 3—No. 4 ESS evolution space and power drain (40K trunk office).

IV. SUMMARY

When the No. 4 ESS was initially designed, the best available design technology was utilized. However, as technology advanced, new opportunities were presented to simplify the No. 4 ESS architecture as well as add new features and improve overall system performance. Space and power requirements (see Fig. 3), as well as cost, were reduced. System reliability has continuously improved throughout the period and the system has been kept technologically modern.

This issue of the *Bell System Technical Journal* contains a series of papers which detail the No. 4 ESS hardware and software evolution and discuss some of the significant new capabilities which have been incorporated into the system. The issue concludes with a presentation of the performance achieved by the No. 4 ESS in the field.

V. ACKNOWLEDGMENTS

The continuing development of No. 4 ESS is the result of dedicated effort by people in many organizations throughout Bell Laboratories and Western Electric working in close concert with AT&T General Departments, Long Lines, and the operating telephone companies. The authors of this volume express their gratitude and appreciation to the entire No. 4 ESS team, without whose cooperation and support these objectives could not have been successfully met on schedule.

REFERENCE

1. B.S.T.J., *56*, No. 7 (September 1977).