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Digital Signal Processor:

An Overview of the Silicon Very-Large-Scale-Integration Implementation

By F. E. BARBER, T. J. BARTOLI, R. L. FREYMAN, J. A. GRANT, J. KANE and R. N. KERSHAW

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A programmable digital signal processor integrated circuit has been designed as a general-purpose building block for a variety of telecommunication applications. The device, known as digital signal processor, is a single-chip integrated circuit fabricated in depletion-load NMOS technology and packaged in a 40-pin DIP. This paper describes the silicon very-large-scale-integration (VLSI) implementation of the digital signal processor with emphasis on the circuit design phase. The specific areas discussed are choice of fabrication technology, layout styles, circuit design procedures, and circuit considerations.

I. INTRODUCTION

A single-chip integrated circuit has been developed as a stand-alone part for digital signal processing. This device known as a digital signal processor (DSP) functions as a special-purpose microcomputer whose instruction set, arithmetic functions, and addressing capability are optimized for real-time signal processing. The primary sections of the DSP are a read only memory (ROM), a random access memory (RAM), an address arithmetic unit (AAU), an arithmetic unit (AU), a system controller, and appropriate input/output (I/O) circuitry.

The ROM is organized as 1024 words by 16-bits per-word memory for storing the system programs and fixed data. The RAM is organized as 128 words by 20 bits per word and is used for storage of variable data and temporary results. The AAU generates the addresses for the RAM

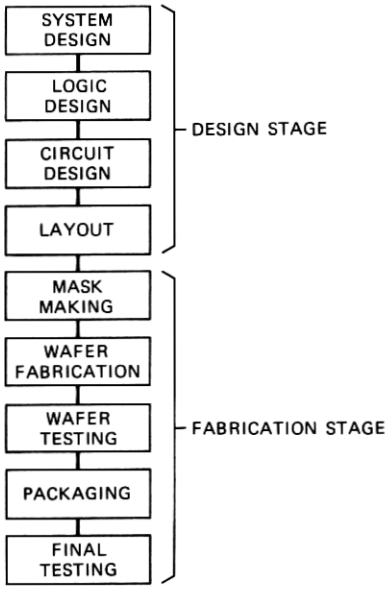

Fig. 1—Integrated circuit implementation process.

and ROM, as well as the addresses for an external ROM. The AU performs the necessary arithmetic operations for digital signal processing, e.g., 16- by 20-bit multiplication and 40-bit accumulation. The I/O unit will accept and generate a serial bit stream of either μ-255 law or linear PCM signal samples. The control unit decodes instructions and provides overall system coordination.

Figure 1 shows the process of implementing the DSP as an integrated circuit. This process is divided into a design stage and a fabrication stage. The design stage consists of four design areas: system, logic, circuit, and layout. In the case of the DSP, the system design is the process of defining the system architecture and instruction set.[1] The logic design assembles logic functions which meet the system's requirements. The circuit design implements the logic design with electrical devices so that the system's requirements are achieved. The fabrication of the integrated circuit starts with a circuit layout, which is the end result of the circuit design. The circuit layout is used to produce masks which are used in wafer fabrication to define the electrical devices. The completed wafers are tested to determine good devices that are then packaged. The completed integrated circuits are tested to verify that the system requirements are met.

This paper describes the circuit design phase of the integrated circuit implementation of the DSP.

II. TECHNOLOGY

The first consideration in circuit design is the choice of an integrated circuit technology. The choice of technology will impact the following areas: the system performance in terms of speed and power; the cost of the device which is related to silicon area or circuit density; and the type of logic functions which can be implemented by the specific technology.

The N-channel MOSFET (metal-oxide semiconductor, field effect transistor) or NMOS technology can easily implement the following logic functions: INVERT, NAND, NOR, XOR, XNOR, Flip-Flops, Shift Registers; and complex logic OR-AND-INVERT, AND-OR-INVERT. The MOS technology, by implementing these different forms of logic, can provide high functional density as compared to a technology which is restricted to fewer forms of logic gates.

The majority of DSP circuitry is a synchronous system wherein data are transferred between registers at a 5-MHz rate. The critical path is 10 logic gates deep; therefore, the technology must be capable of gate delays of 20 ns or less (worst case) at a power level compatible with the DSP level of integration.

The depletion-load NMOS technology was selected for implementing the DSP. This is an existing process presently used for manufacturing static memory devices. The existence of a manufacturable process has the advantage of decreasing the design time and decreasing the risk of developing a device. This technology provides the performance, speed and power, necessary for the DSP requirements, as well as allowing a high-density layout for implementing the 7300 TTL-equivalent gates of logic, 2.5 K bits of RAM and 16 K bits of ROM.

III. CIRCUIT LAYOUT

The final result of circuit design is a layout data base used to make masks. These masks are used in wafer fabrication to produce an integrated circuit. There are different layout approaches or styles to create and connect devices. These different styles optimize either circuit density or design time and time to produce final integrated circuits. The first style is known as custom layout, where each device is created and connected with the minimum restrictions. The custom layout style optimizes circuit density which results in the fastest speed and lowest power. The second style is known as polycell layout. This layout style uses established cells at a logic function level which have been designed, laid out, and electrically verified. A computer-aided design (CAD) system known as LTX[2] can automatically place and connect these polycell functions according to a logic description known as LSL.[3] The polycell layout style produces the shortest time interval

from the start of the circuit design stage to completion of an integrated circuit meeting the system requirements.

The DSP memories, RAM and ROM, constitute a large number of transistors in a regular pattern. For this reason, it is desirable to use a custom layout style for memories to achieve the highest possible transistor density and consume the least amount of silicon area.

The AU performs a 16- by 20-bit multiplication and a 40-bit accumulation, along with other functions. These functions require logic which is performed on many bits in parallel, resulting in bit-oriented logic. These portions have the functional logic replicated up to 40 times depending upon word length required. Exemplary of the logic performed in the AU is the 20-bit add function that must be completed within one clock cycle. This path and other similar paths are up to 10 logic gates deep, resulting in the requirement that worst-case, critical-path gate delays must be less than 20 ns to fit within the 200-ns cycle. Consideration of the speed requirements in the AU and the regular characteristics of much of the logic, lead to the choice of a custom layout style in this section to optimize circuit density, speed, and power.

The IOAC section, which consists of the I/O, AAU, and control sections, has both random and bit-oriented logic. Custom layout was selected for the bit-oriented logic to obtain the higher circuit density. The IOAC random logic is 5 gates deep and results in the requirement that a worst-case gate delay must be less than 40 ns. Polycell layout could meet this speed requirement and was chosen for the random logic sections to decrease the design time of the project. Polycells for the depletion-load NMOS technology did not exist when the circuit design stage of the DSP was started; therefore, polycells were first defined and created before the IOAC random logic sections could be started.

Both custom and polycell layout styles were used in the DSP layout. Custom layout was used in the memory and bit-organized sections to optimize circuit density, speed, and power. Polycell layout was used in the random logic section to minimize design time. The resulting layouts have shown that the custom logic section achieved about twice the functional density with a factor of 3 improvement in the speed achieved for a given power level.

IV. CIRCUIT DESIGN PROCEDURES

Knowing the type of logic functions that could be implemented with the NMOS technology, the logic designer completed the logic description for the DSP. The circuit designer, having determined the layout style, had to convert the logic gates to NMOS transistors. Figure 2 shows this circuit design procedure. The proposed circuit is analyzed using a

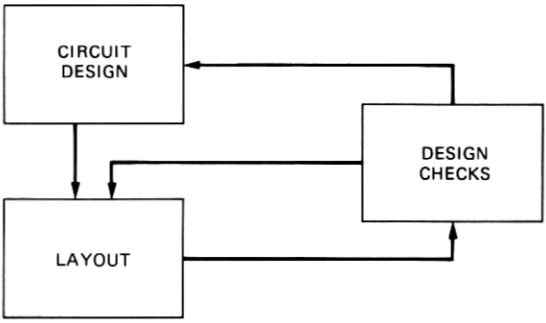

Fig. 2—Circuit design procedure.

circuit simulator such as SPICE.[4] After a successful simulation, the circuit is converted to mask levels on an in-house minicomputer graphics system. Physical layout design rules for lines and spaces are used to create geometries necessary for creating a mask for wafer fabrication. There are two computer aids for verifying the layout. The first aid checks for violation of the physical layout design rules. The second aid determines the size and type of transistors and the parasitic capacitance which is an important parameter for circuit performance. This circuit characterization represents a more accurate circuit description than was initially simulated before layout, and these results are used in the circuit simulator to determine final circuit performance. In addition, computer plots of the circuit layout are visually checked for design rule layout errors, functional errors, and interconnect errors.

V. CIRCUIT CONSIDERATION

The single most important factor which made the circuit design of the DSP practical is that the DSP is a synchronous system, wherein data flows between registers in a specified time interval. This allows for circuit simulations of relatively small sections since the exact timing is well known.

Signals, whether they are instructions or data, are passed between the major sections (AU, RAM, ROM, AAU, I/O, CONTROL) via a 20-bit data bus. The 5-MHz system clock has two phases known as a master and slave phase of 100 ns each. The data bus is charged during the slave phase and is discharged during the master phase by the sending port, if the data bit is true.

Synchronization between the various sections is achieved by distributing a master clock and a synchronization signal and locally regenerating the required clocks. De-skewing networks were included in each section to achieve precise clock synchronization even in the presence of master clock delays due to resistance-capacitance loading delay effects.

Power and ground bus distribution is important to maintain adequate noise margin. Each major section of the DSP has its own power and ground to minimize the accumulation of voltage drops and noise interactions due to transients. The size of these lines was made large enough to keep worst-case power and ground drops below 100 mv.

The input and output buffers were located at the edge of the chip and separate power and ground lines were also provided for these circuits. Both the peripheral placement of I/O buffers and provision for their separate power and ground bussing minimize externally induced noise effects on internal logic.

Internal testing probe pads were distributed along the data bus, the address bus, and selected control and timing signal paths so that the AU, RAM, ROM, and IOAC could be tested independent of each other for diagnostic testing and logic verifications. These pads did not increase

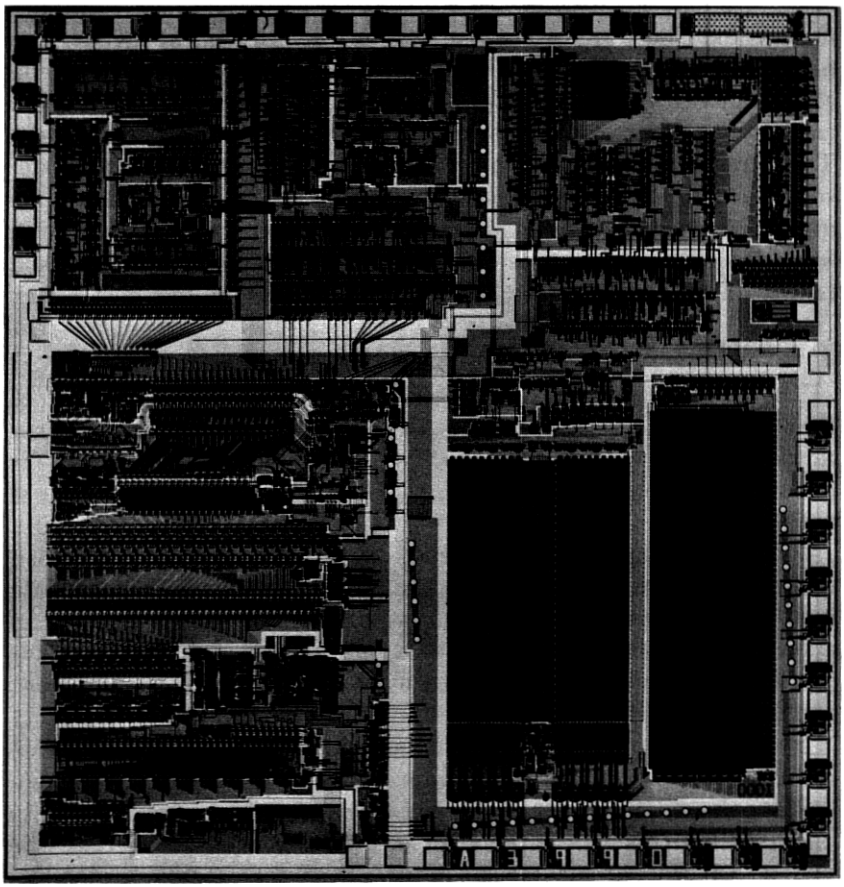

Fig. 3—Digital signal processor integrated circuit.

the final chip size and were invaluable in analyzing initial device testing results.

VI. CONCLUSIONS

The VLSI silicon implementation of the DSP has been described. The DSP integrated circuit meets the system's requirements—function, speed, and power. Figure 3 shows the chip, which contains 7300 TTL-equivalent logic gates, 16 K bits of ROM, and 2.5 K bits of RAM. The implementation requires 45,000 transistors and occupies an area of 62 mm^2 (8.1 by 8.6 mm).

VII. ACKNOWLEDGMENTS

We sincerely thank the many people at Bell Laboratories who contributed to the development of the DSP. In particular, we are very grateful to Bailey R. Jones for his efforts in wafer fabrication of the DSP.

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