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Digital Signal Processor:

Receiver for *TOUCH-TONE*® Service

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This paper describes the design of a single-package, all-digital receiver for TOUCH-TONE® service implemented by using a digital signal processor integrated circuit. The receiver is particularly suited for systems that operate on signals that have been encoded into a digital pulse-code-modulation format. The program contained in the digital signal processor was designed to emulate the signal processing functions of a central office grade receiver. Measurements of performance confirm the equivalency.

I. INTRODUCTION

This paper describes the design of a single-package, all-digital receiver for *TOUCH-TONE*® service implemented by using a digital signal processor (DSP) integrated circuit.[1] The receiver is particularly suited for systems that operate on signals that have been encoded into a digital pulse-code-modulation (PCM) format.

TOUCH-TONE service is a voice frequency signaling system in which any one of 16 digits may be transmitted by simultaneously sending two tones. The frequency of one of the tones may be either 697, 770, 852, or 941 Hz (called the low group) and the frequency of the other tone may be either 1209, 1336, 1477, or 1633 Hz (called the high group). The receiver must tolerate frequency shifts in the transmitter, operate over a wide dynamic range in the presence of noise, and be insensitive to speech (digit simulation).[2]

The program contained in the DSP was designed to emulate the signal processing functions of a central office grade receiver. Measurements of performance confirm the equivalency.

II. DESCRIPTION OF THE RECEIVER

2.1 Receiver architecture

The model for the DSP receiver architecture was the analog type-H service receiver. The type-H receiver is used in many central offices today and has a relatively high sensitivity and noise immunity, as well as good digit simulation performance.

A block diagram of the DSP receiver is shown in Fig. 1. At the input is a filter which reduces interference from power line and precise dial tone components. This filter provides loss at 60, 180, 350, and 440 Hz, and it establishes a passband between 650 and 3000 Hz. It is a fourth-order high-pass filter instead of a sixth-order bandpass filter as in the analog receiver, because the digital receiver does not have to remove cable test tones above 10 kHz. The PCM data have been converted from analog signals that are band-limited to less than 4 kHz.

The output of the input filter is then split by two sixth-order band elimination filters. The low-group band elimination filter (LGBEF) provides loss only in the frequency band from 600 to 1050 Hz. The high-group band elimination filter (HGBEF) provides loss in the high-group frequency passband and gain in the band above 1900 Hz. The use of BEFs is important for good digit simulation performance as discussed later.

Each BEF output is followed by a limiter which serves two functions. First, for signal levels above a minimum value, the limiter gives an output that is independent of the input signal amplitude. The second function of the limiter is to provide digit simulation protection, as discussed later. Each limiter output drives a set of second-order channel filters. The filters are tuned to the signaling frequencies and have a pole-Q of 16.

The channel filters drive detector circuits which sense a signal level that is greater than a fixed threshold. The threshold is set to 2 dB below the peak signal level that would be present if a sine wave of the nominal frequency and amplitude were input to the limiter. If the signal to the detector drops below the threshold, the detector continues to indicate detection for a fixed hold time.

The outputs of the detectors are packed into an 8-bit word and are applied to the routine which implements the digit validation logic. This logic checks for a valid detector output and applies a timing criterion. If the detectors show the presence of a tone pair for a continuous validation interval, the logic indicates a valid digit with the digit present (DP) flag and outputs a code word for the digit. The logic then requires the pair to be continuously absent for the validation interval before indicating no digit. An early detect (ED) flag is also provided to indicate that a tone pair is in the process of being validated.

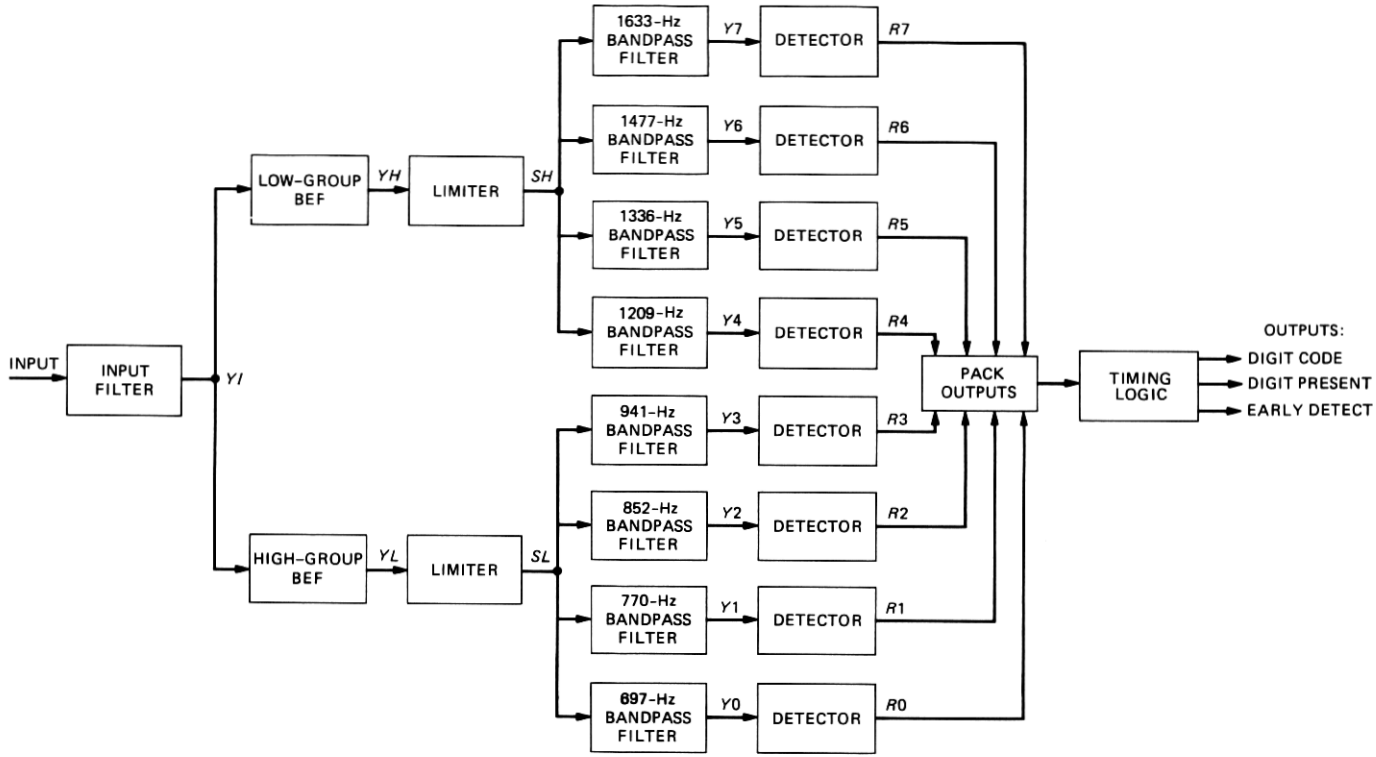

Fig. 1—Receiver architecture.

The digit simulation performance of the receiver relies on limiter guard action. If a signal with two or more frequency components is present at the input of a limiter, the magnitude of each individual signal component at the output of the limiter is reduced to less than it would be if only that component were present at the input. When valid tones are transmitted, each group limiter receives only one signaling component and the magnitude of that component at the limiter output is above a threshold, as measured by the channel filter and detector. When speech is input to the receiver, the group limiters get many frequency components—some of which might be in the range of valid signaling tones. In this case, the limiter guard action reduces the magnitude of any signaling component at the output of the limiter to a value less than the detector threshold. The use of BEFs increases the number of frequency components from speech that would reach the inputs to the limiters.

2.2 Digital signal processor program

Figure 2 shows the organization of the DSP program. After initialization, the DSP executes the main receiver routine which consists of a loop that is traversed once every 250 μs (or two 8-kHz sample periods). The main routine calls a filter subroutine twice per loop so that the digital filtering operations are performed once every 125 μs. The

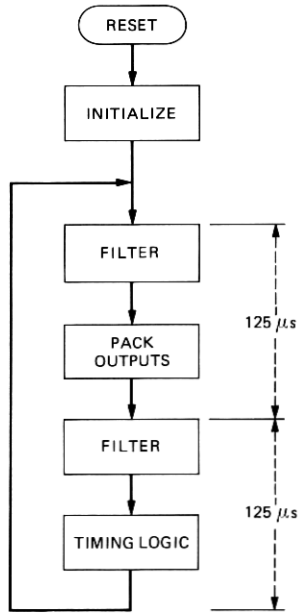

Fig. 2—Program organization.

operations done in the main routine include packing the eight detector outputs into a single word and performing the timing validation logic. The program was organized in this way because all of the filtering and digit validation cannot be done in a single 125 μs interval. However, the digit validation logic does not have to be done at an 8-kHz rate and can be split over two or more intervals.

The initialization routine sets the AU control register, AUC, for rounding and overflow protection. The I/O control register, IOC, is set for format 0, 8-bit, passive input and 2.5-Mb/s active output. The RAM is cleared and some register pointers are set.

The first operation of the main routine is to call the filter subroutine. The filter subroutine waits for an input and then converts it from μ-255 to linear. The input and BEFS are shown in a block diagram in Fig. 3. All of the second-order structures use only four multiplies. The signal levels are adjusted at the inputs to the BEFS.

The group limiters are realized by the following code:

```
                    p = lim**rya;      "rya points to YH"
        a = p;
        a = a << 14;
w = a;
```

The initial multiplication of a fraction (lim) and the output of the BEFS (YH shown here) limits the dynamic range of the receiver. The result in the accumulator is shifted up and transferred to the W register. Signals in the range of 0 to −29 dBm will cause the W register to saturate because of overflow. This limiter action using the overflow protect function is very similar to the behavior of the analog receiver.

The outputs of the limiters are applied to the eight channel filters. These filters are realized as shown in Fig. 4a, which illustrates the 770-Hz BPF.

The detector algorithm for each channel output is shown in Fig. 4b. This is the equivalent of the comparator circuit in the analog receiver. The output is compared with a threshold value (th) for every sample. If the sample is greater than the threshold, the detector output is set to a positive number (CNT) and decremented, otherwise, the detector output is just decremented. The value of CNT is such that when the signal falls below the threshold, the detector output will be a positive number for the detector hold time. The 1633-, 1477-, and 1336-Hz detectors compare the rectified channel filter output with the threshold to improve the detectability of these frequencies. It is possible to sample a sine wave at these frequencies whose amplitude is above the threshold in such a way that none of the positive samples for one cycle

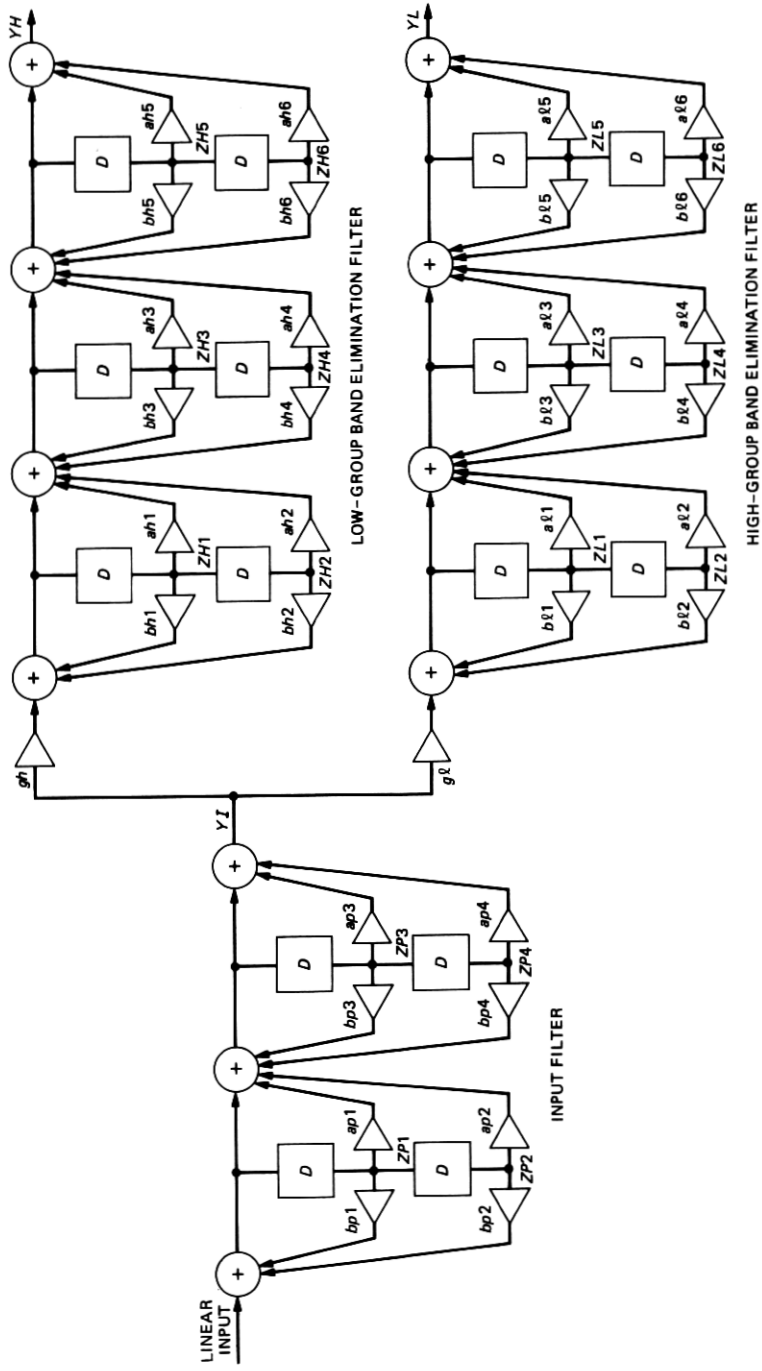

Fig. 3—Input and band splitting filters.

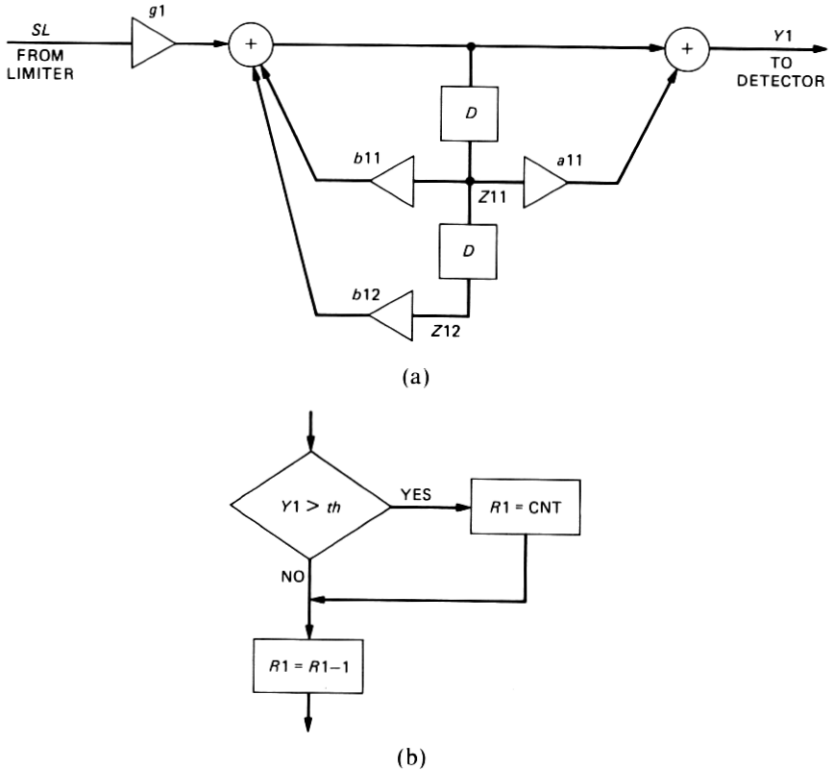

Fig. 4—Channel filter and detector for 770-Hz tone. (a) BPF (770 Hz). (b) Detector (770 Hz).

are above the threshold. The rectification operation guarantees that at least one sample per cycle will be above threshold if the amplitude of the sine wave is 1 dB above the threshold. The filter subroutine then returns to the main routine.

In the main routine, the outputs of the low-group detectors are packed into a single word using the "sgn" function which tests the sign of the detector outputs. The word is tested to see if there is a tone detected in the low group. The high-group detector outputs are packed and tested in a similar fashion. The low- and high-group outputs are then combined to form an address that can be used to access the desired output code for the detected tone pair from a table in ROM.

After calling the filter subroutine again, the main routine does the timing validation function and provides ED and DP flags on the S bits of the DSP. The latest detected tone pair (*NEW*) is compared with the tone pair that is under validation (*OLD*). The result of the validity test can be followed with the flowchart in Fig. 5. If there is no detected tone pair or the detection does not match the previous detected pair,

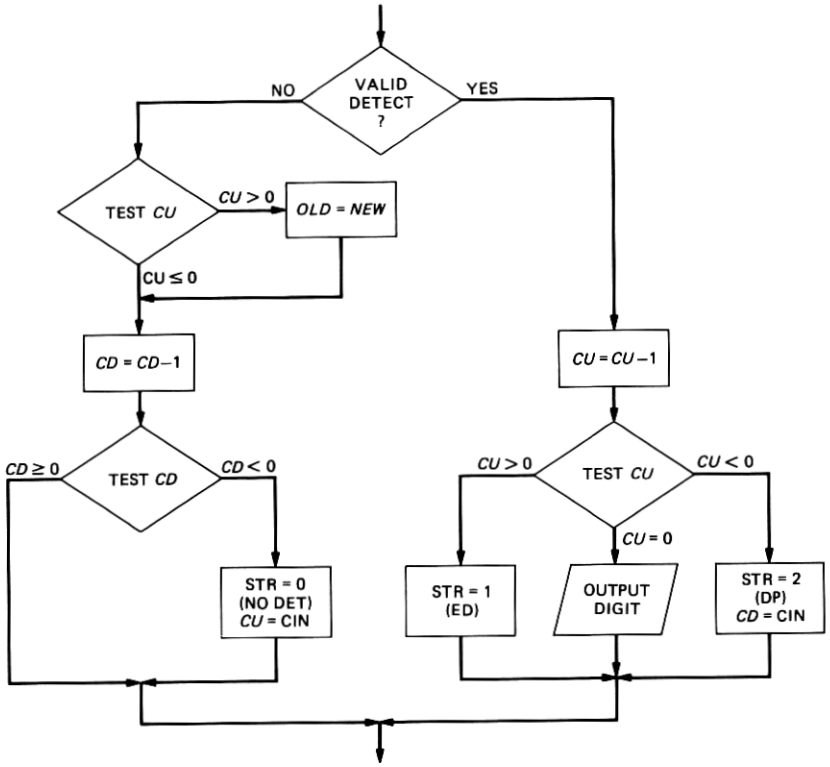

Fig. 5—Timing validation logic.

a variable, *CU*, is tested to see if no digit has been validated. If there is no digit present (positive *CU* value), the *OLD* is updated with the *NEW*. A variable, *CD*, is decremented and tested to see if a tone pair has been continuously absent for the validation interval. If so, *CD* will be negative and the S bits are cleared to indicate "no digit" and the variable *CU* is initialized (CIN). If a valid tone pair is detected, the variable *CU* is decremented and tested to see if the pair has been present for the validation interval. If not, the S bits are set to indicate ED. If *CU* is negative, indicating a continuous detection for the validation interval, the S bits are set for DP and the *CD* variable is initialized (CIN). Finally, if *CU* is exactly zero, the code for the digit pair is written in the output buffer. The program then branches to the beginning of the loop.

As written, the program uses nearly 100 percent of the time available for processing. However, it could be reorganized such that the main routine calls the filter subroutine three or four times per loop in order to do more low-speed operations if necessary. Only 42 percent of the ROM is used for the receiver program. The rest of the ROM space could

be used for other programs that are accessed by a conditional branch taken after reset and based on the state of the DSP C bits.

2.3 Hardware and interface considerations

Because the complete receiver is in a single 40-pin package, the hardware requirements are extremely simple. Also, the flexibility of the DSP I/O unit allows a variety of possible interface configurations to be realized. Figure 6 shows an arrangement that is compatible with the programmed I/O control described in the previous section. It is also the circuit that was used to test the performance of the receiver.

A number of connections are independent of the choice of I/O configuration. The DSP must be powered by a +5 volt source, the internal ROM enabled, a 5-MHz clock applied, and reset controlled. The internal ROM is enabled by connecting $\overline{\text{EXM}}$ to +5 volts. A 5-MHz clock may either be applied to the CLKIN pin (as shown) or the on-chip

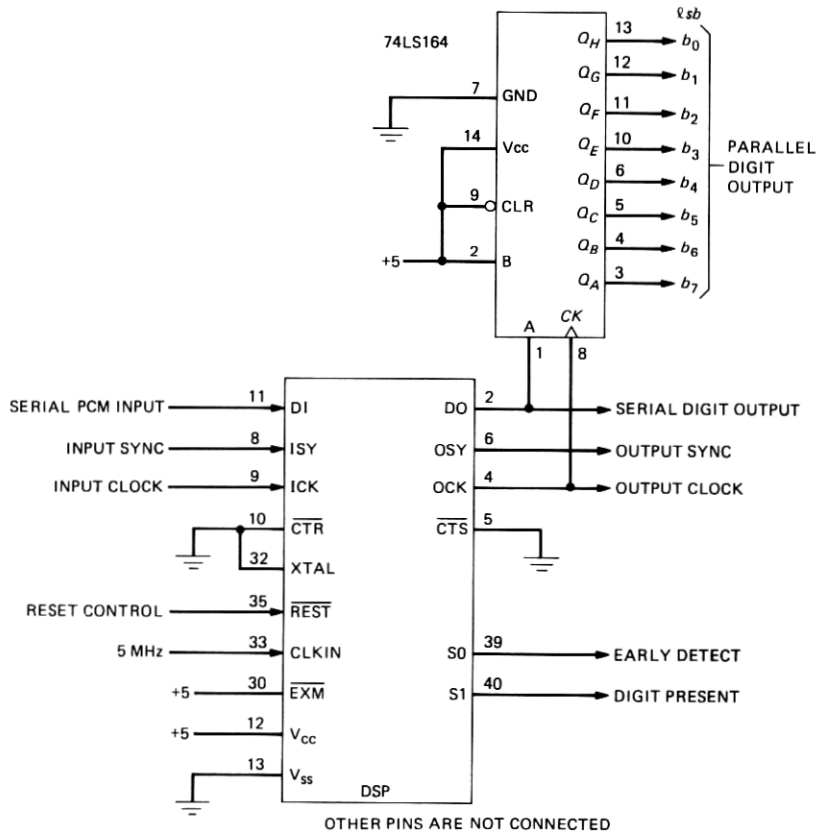

Fig. 6—Receiver hardware.

oscillator may be used with the addition of an external crystal. The reset line should be held low (TTL levels) for at least 600 ns after power up and then held high while the receiver is operating.

The input is set up in the program for passive, 8-bit operation. That is, the DSP-receives clock pulses and synchronization information from the system providing the PCM data. The input is continuously enabled by the grounding of the $\overline{\text{CTR}}$ pin.

The output is programmed for active, 8-bit transmissions at a rate of 2.5 Mb/s. All of the output signals are generated by the DSP and can be used to drive a TTL shift register to provide parallel digit output. The output is also continuously enabled by the grounding of the $\overline{\text{CTS}}$ pin.

The ED and DP flags are provided by the DSP S0 and S1 pins, respectively.

All of the other DSP pins are not used and may be left open.

III. RECEIVER PERFORMANCE

The performance measurements for the receiver were made by interfacing a μ-255 law encoder (analog-to-digital converter) with D-type channel bank filter to the DSP. The receiver could then be checked using analog receiver test facilities. A type-H receiver was tested in parallel.

The signal amplitude sensitivity of the receiver was measured with worst-case parameters. That is, the frequencies of the tones were set to their maximum allowable deviation from nominal, the levels of the two-tone groups were made different, maximum expected dial tone was added, and the duration and interdigit intervals were at their minimum values. The receiver was also tested for detection errors with tones in the presence of gaussian and impulse noise. Finally, digit simulation was tested by applying speech and music to the receiver.

In all tests the DSP receiver performed as well as the type-H receiver.

IV. CONCLUSION

This paper has described a central office quality receiver for *TOUCH-TONE*® service which accepts signals encoded in a digital PCM format. The entire receiver is implemented using the DSP, a single 40-pin dual inline package that is powered by a +5 volt supply. It can easily be customized for different input and output formats, and there is enough spare ROM capacity to implement other functions when the device is not being used as a receiver.

V. ACKNOWLEDGMENTS

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