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Transmission Cathodoluminescence

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The application of transmission cathodoluminescence (TCL) in evaluating the quality of luminescing materials is reviewed. This scanning electron microscope technique is particularly useful in imaging localized nonuniformities, such as dislocations and inclusions, in semiconductors. Understanding and analyzing such material defects are of practical importance since they greatly affect device performance and lifetime. After a detailed description of TCL, the advantages of this technique in comparison to defect etching, cathodoluminescence imaging, and electron beam-induced current (EBIC) is presented. Since TCL is simple to perform, this technique can be used to evaluate and monitor material growth and device processing procedures. Although TCL may be applied to any luminescing material, this paper demonstrates its usefulness for the GaAs/GaAlAs and InP/InGaAsP materials systems which provide most sources and detectors for optical communication.

I. INTRODUCTION

Diode lasers, light-emitting diodes (LEDs), and photodiodes are integral components of the current lightwave transmission systems. These devices are mainly based on the III–V materials systems, e.g., GaAs/GaAlAs and InP/InGaAsP. Both material and device development are recent, relative to the highly developed Si-based technology. Material defect analysis is required to evaluate and monitor material growth and device processing procedures, especially during the early stages of development.

The performance and reliability of optoelectronic devices are determined by the quality of materials and fabrication processes. Threading dislocations have been shown to increase the leakage current of both InP and GaAs photodiodes;[1,2] these dislocations are also sources of microplasmas in avalanche photodiodes.[3–5] The quantum efficiency of GaP and GaAlAs:Si LEDs is strongly dependent on the dislocation

density.[6,7] Threading dislocations and inclusions are known sources of dark line and dark spot defects in degraded LEDs and solid-state lasers fabricated from the GaAs/GaAlAs and InP/InGaAsP materials systems.[8–12] Finally, stresses from dielectric coatings are known to induce defects and accelerate device degradation.[12,13]

Characterization techniques are required to assess the effects of growth and processing procedures on material or device quality. Because of the variety of defects, materials, and devices, a number of characterization techniques have been developed. These techniques are listed and compared in Table I.

The purpose of this paper is to review the most recently developed technique of transmission cathodoluminescence (TCL) and to compare it with other defect analysis techniques currently in use.[10,14–23] Transmission cathodoluminescence is performed on a scanning electron microscope (SEM); the magnification and depth of field available in an SEM are exploited.

1.1 Defect analysis techniques

The technique with the highest magnification and resolution, transmission electron microscopy (TEM), reveals the nature and origin of

Table I—Comparison of various characterization techniques

Technique	Disadvantages
IR microscopy	Low resolution Dependent on detector sensitivity
Scanning photoluminescence	Requires removal of contact layer Dependent on detector sensitivity Difficult to identify features because of lack of an optical image
Scanning photocurrent	Requires p-n junction or Schottky barrier Requires electrical contacts Difficult to identify features because of lack of an optical image
CL	Requires removal of contact layer Dependent on detector sensitivity
EBIC	Requires p-n junction or Schottky barrier Requires electrical contacts
TCL	Dependent on detector sensitivity
Defect etching	Material, orientation, dopant, and etch dependent Destructive
X-ray topography	Low resolution Slow Restricted to relatively small samples
TEM	Difficult sample preparation Destructive Small volume of material probed

material defects. However, it cannot be used routinely for screening defective materials because it is destructive, the sample preparation is very difficult, and the volume of material probed is small relative to device dimensions. X-ray topography is relatively slow, has limited resolution, and is limited to small samples because of internal stresses generally associated with device wafers.[24,25] The evaluation of wafers by electron beam-induced current (EBIC) scan, cathodoluminescence (CL) scan, photoluminescence (PL) scan, photocurrent scan, and infrared microscopy have also been reported.[9,26–32] The electron excitation techniques—EBIC and CL scan—are more useful in comparison to the conceptually similar photoexcitation techniques, i.e. photocurrent and PL scan, because of the availability of an exactly corresponding secondary-electron (SE) image to isolate surface details. Even when this disadvantage is overcome by careful experimental design, dislocations which are responsible for poor device performance and reliability cannot be readily imaged using these techniques, although some specific examples may be found. For example, dark spots in CL images have been identified to be dislocations only for the case of GaP, GaAs, and CdTe.[6,33–35] Additionally, it is difficult to observe dislocations in GaAs:Se.[27] Moreover, dislocations have not been imaged in GaAs:Si.

Etching is the simplest and, thus, the most widely used method for revealing defects. Once the identity of etch features has been established, evaluation of material quality by etching is relatively fast. Additionally, etching has sufficient resolution to reveal a defect density as high as $\sim 10^7$ cm^{-2}. However, aside from being destructive, etching is material, material orientation, and dopant dependent. For example, the KOH etch readily reveals dislocations on the {100} and {111} surfaces of GaAs.[36,37] However, it cannot be used for the {110} surface which is the cleavage plane and, thus, forms the mirror faces of solid-state lasers. Huber etch works well for the {100} surface of InP but not for the {110} surface.[38] The A-B etch reveals dislocations on the {111} surface of InGaAsP, but no etch has been developed for the technologically important {100} surface.[39,40] To estimate dislocation densities of InGaAsP layers in a device structure, the InP confining layers had to be etched.[40] Finally, the R-C and A-B etchants are successful for the {111}B face of GaP but cannot be used for other orientations.[39,41,42]

The interpretation of etch patterns is often difficult even with known defect etchants.[21] Figure 1 shows the response of an InP crystal to four different etchants reported to reveal dislocations: (a) Huber etch, (b) 6:6:1, (c) RRE, and (d) modified A-B etch.[38,43–45] The sample is the {100} surface of a crystal doped with Sn to 2×10^{18} cm^{-3} and is a typical substrate for device wafers. A brief comparison shows large differences in these etch patterns. Dislocation and saucer pits are well

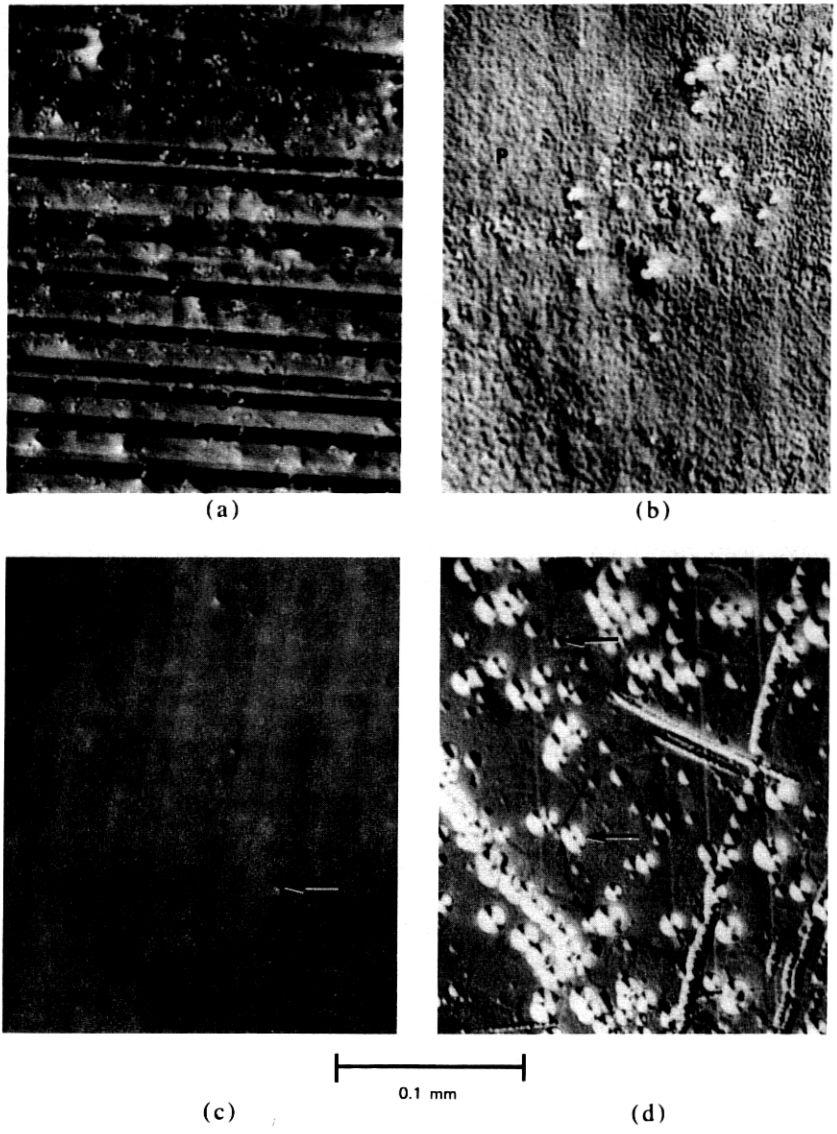


Fig. 1—Optical micrographs showing the response of InP:Sn to different etchants: (a) Huber etch, (b) 6:6:1, (c) RRE, and (d) the modified A-B etch. D, S, and P refer to dislocation pit, saucer pit, and protrusions, respectively.

delineated with the Huber etch but are not discernible with the modified A-B etch. On the other hand, growth striations, which are periodic variations in impurity concentration, are particularly well defined after A-B etching. The etch patterns of the other two etches

are in between that of the Huber and modified A-B etches. Therefore, the use of an etchant to reveal defects is often unreliable.

Transmission cathodoluminescence reveals defects as dark spots, similar to the CL and EBIC techniques.[14] The characteristic images of dislocations have been identified by a one-to-one correspondence with a known dislocation etchant.[14,15] Dislocations are roughly the same size and have a comma shape. The comma shape is due to the dislocation intersecting the surface of the sample at an oblique angle. Inclusions whose contrast is due to nongeneration of CL radiation have random shapes and sizes. The improved collection efficiency and measurement geometry of TCL in comparison to CL allows defects to be readily imaged in many more materials. The materials to which TCL has been applied is listed in Table II.

II. EXPERIMENTAL

2.1 Transmission cathodoluminescence technique

A schematic of the TCL technique is shown in Fig. 2. Transmission cathodoluminescence is accomplished by placing a light detector underneath a sample. The CL radiation generated on the top surface provides illumination which is transmitted through the sample and detected on the opposite side. Both sides of the sample must be optically smooth to reduce surface artifacts in TCL images. The TCL method has an efficient light collection geometry and no modification of the SEM is required. On the other hand, additional optics are required in the CL technique to guide the CL to an external detector. In Fig. 2, surface defects with their lower CL efficiency are detected as a decrease in CL radiation transmitted through the sample. Volume defects, i.e. defects which lie beneath the electron-hole (e-h) excitation

Table II—Different substrates and device wafers examined by TCL

	GaAs/GaAlAs	InP/InGaAsP
Impurity striations	GaAs:Te GaAs:Si	InP:S InP:Se InP:Te InP:Sn InP:Zn
Dislocations; defects	GaAs:Te GaAs:Si GaAlAs:Si LED wafer GaAs/GaAlAs LED wafer GaAs/GaAlAs laser wafer	InP:S InP:Se InP:Te InP:Sn InP:Zn InGaAsP InP/InGaAsP LED wafer InP/InGaAsP laser wafer
Degradation	GaAlAs:Si optoisolator LED GaAlAs data link LED	InP/InGaAsP transmission LED

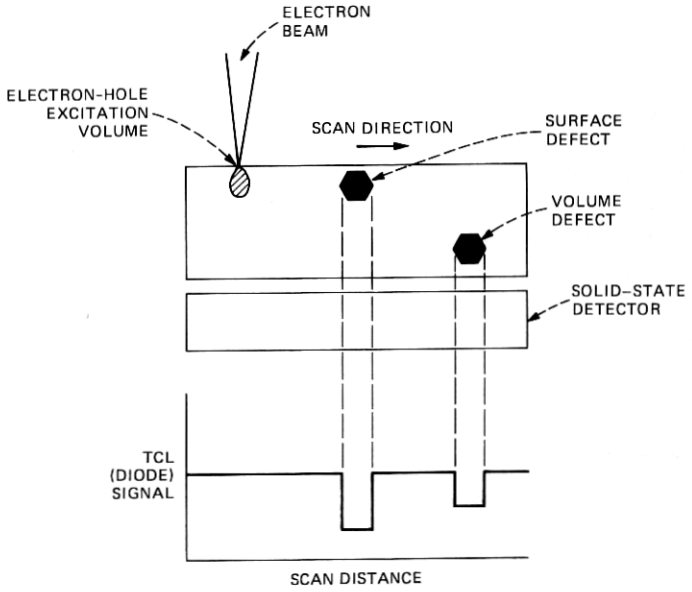


Fig. 2—Schematic of TCL measurement. Both surface and volume defects are detected by the solid-state detector as a decrease in luminescent radiation. The surface defect has a lower luminescing efficiency and the volume defect shadows the dector from the luminescing surface.

volume of the electron beam, are detected by their interaction with the surface-generated CL radiation passing through the sample to the detector below. A void in the sample volume will increase light transmission because of reduced absorption. A volume defect will decrease light transmission because of increased absorption or scattering. Using this method, defects deep within a thick sample can be observed. Although the transparency of a sample to its own CL radiation is material dependent, in the following we give TCL data on samples whose thickness is comparable to that of substrates and device wafers.

2.2 Experimental consideration

The data given was obtained with an ETEC Corporation autoscan SEM, but any SEM with similar capabilities may be used.[46] Two solid-state detectors were used for the TCL measurements, depending on the spectral region of interest. For wavelengths less than ~1.0 μm, a silicon photodiode was used; for wavelengths shorter than ~1.6 μm, a germanium photodiode was selected. These detectors have low noise equivalent power (NEP), fast response at zero bias, and output linearity with light input. The performance specifications of the photodiodes are listed in Table III.

For typical SEM parameters of 20 keV and 10^{-7}A for the electron

Table III—Characteristics of photodiodes used in TCL experiments

	Silicon Photodiode	Germanium Photodiode
Active area	0.20 cm^2	0.20 cm^2
NEP	8×10^{-13} W/$\sqrt{Hz}$ @ 850 nm	6×10^{-11} W/$\sqrt{Hz}$ @ 1300 nm
Responsivity	0.35 A/W @ 850 nm	0.22 A/W @ 1300 nm

beam, the luminescent power radiated by the sample is approximately 10^{-5}W, assuming a CL conversion efficiency of 10^{-2}. This conversion efficiency is typical of GaAs but is lower for other materials.[47] Most of this radiation is collected by the detector in the TCL configuration since it is placed 2–3 mm from the luminescing source. The solid angle subtended by the photodiode in the TCL geometry is $\sim\pi$, whereas the collection angle in the usual CL mode is $\sim 10^{-2}\pi$.

Since the silicon and germanium diodes have an NEP of 10^{-12} W/$\sqrt{Hz}$ and 10^{-10} W/$\sqrt{Hz}$, respectively, the detectors are capable of sensing 10^{-10}W and 10^{-8}W, respectively, of TCL power at a bandwidth of 10^5 Hz required for SEM imaging. Approximately two orders of magnitude greater power is required to easily image material defects without the use of difficult noise reduction techniques such as lock-in amplification coupled with beam blanking. This power is readily available from the materials listed in Table II.

2.3 Resolution

The resolution of the TCL technique is limited by the type of defect observed. The contrast from dislocations is due to nonradiative recombination; therefore, it is limited by the minority carrier diffusion length. The contrast at inclusions is due mainly to nongeneration of CL, and the resolution of these defects is limited by the electron beam conditions as in SE imaging. Finally, volume defects can be resolved to roughly the CL emission wavelength since the defect is effectively observed by optical means.

Figure 3 shows an example of two different defects appearing in the same InP:S sample. The large dark spots are due to dislocations intersecting the surface, whereas the much smaller dark spots are inclusions located within an e-h excitation volume of the surface. The identification of defects using TCL will be discussed in Section 2.4. The dislocation image is large because of the large minority carrier diffusion length. By imaging these dislocations, the minority carrier diffusion length is readily estimated in this sample to be ~ 5 μm. The images of inclusions show that defects as small as 1–2 μm can be imaged under the beam conditions of 20 keV and 10^{-7}A.

Figure 4 is an example of a volume defect imaged by TCL. Figure 4a is the SE image of an unusual feature appearing in an InP/InGaAsP

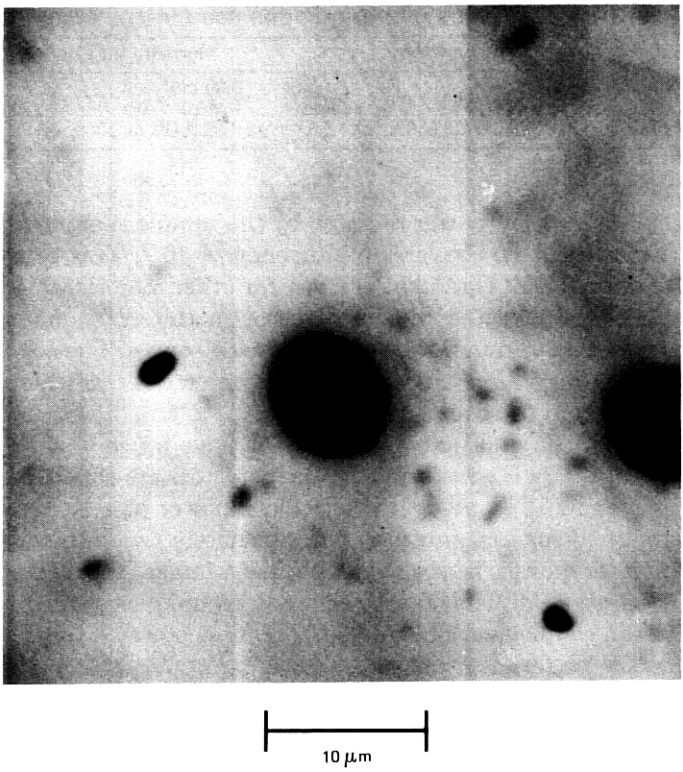


Fig. 3—Transmission cathodoluminescence image of heavily S-doped InP substrate. The large and small dark spots are dislocations and inclusions, respectively.

wafer. A CL picture of the same region, Fig. 4b, shows the area to be nonluminescent. It is only the TCL image, Fig. 4c, that explains the origin of this dark area. One can clearly see a bright spot in the center of the dark region associated with a void in the epitaxial layers. Since the void does not appear in the CL image, it lies below the e-h excitation volume.

2.4 Interpretation of TCL images

In general, defects appear as dark spots in a TCL image. To interpret images, dark spots must be identified. For the CL technique, dark spots in images of GaAs:Te, GaP, and CdTe were identified to be dislocations by demonstrating an exact one-to-one correspondence between these dark spots and dislocations revealed as etch pits produced by a known defect etchant.[6,23,34,35] We have followed this procedure for the TCL technique and applied it to GaAlAs:Si, GaAs:Te, InP:Te, and InP:S.[14,15]

Two methods were used to show that dark spots observed in a TCL

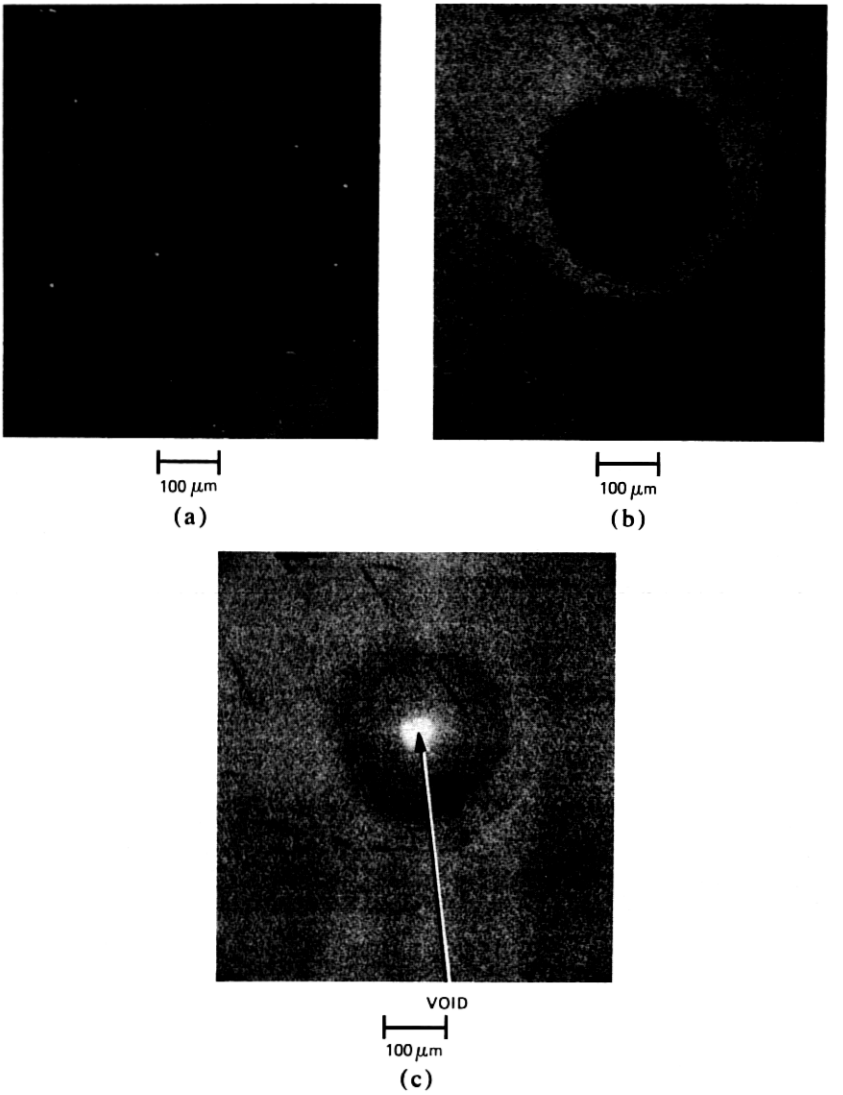


Fig. 4—(a) Secondary electron image of a surface feature on an InP/InGaAsP wafer. (b) Cathodoluminescence image of the region shown in (a). The dark circular region shows that the surface feature is nonluminescent. (c) Transmission cathodoluminescence image of the region shown in (a). The bright dot in the center of the dark area is a void.

image represent grown-in dislocations. In the first method, a TCL image of a sample was taken prior to etching to reveal dislocations. By comparison of the etch pattern with the TCL image of the same region, an exact one-to-one correspondence was established. In the second method, a {100} wafer was etched to reveal dislocations as etch pits.

Subsequently, the samples were cleaved along the {110} cleavage planes. By examining with TCL the {110} surface where it intersects an etch pit, a dark region immediately below each pit was found. Thus, each dislocation intersecting the {100} surface corresponds to a dark spot in a TCL image. The technique of first etching the surface and then showing dark spots at dislocation pits is not useful since surface features always appear in either a CL or TCL image.

In Fig. 5a, a TCL image of a Si-doped $Ga_{1-x}Al_xAs$ layer grown by liquid phase epitaxy (LPE) on a {100} oriented GaAs substrate is shown.[48] The aluminum concentration varies from $x = 0.00$ on the top surface to $x = 0.30$ at the substrate-epitaxial layer interface. This gradient occurs over a thickness of ~250 μm. The sample has been bromine-methanol polished to produce smooth, damage-free surfaces. Only dust particles are observed on the top GaAlAs surface when examined by SE imaging and no features could be seen in normal CL using an S1 photomultiplier. This observation is in agreement with previous measurements on similar material.[7] However, when examined by TCL, a number of randomly distributed dark spots appear. The size of these dark spots varies from 5 to 10 μm. At high magnification, their shape closely resembles commas; that is, the central dark region is connected with a fainter tail. The average density of these dark spots is approximately 2×10^4 cm^{-2}.

Figure 5b shows the SE image of the region shown in Fig. 5a. The

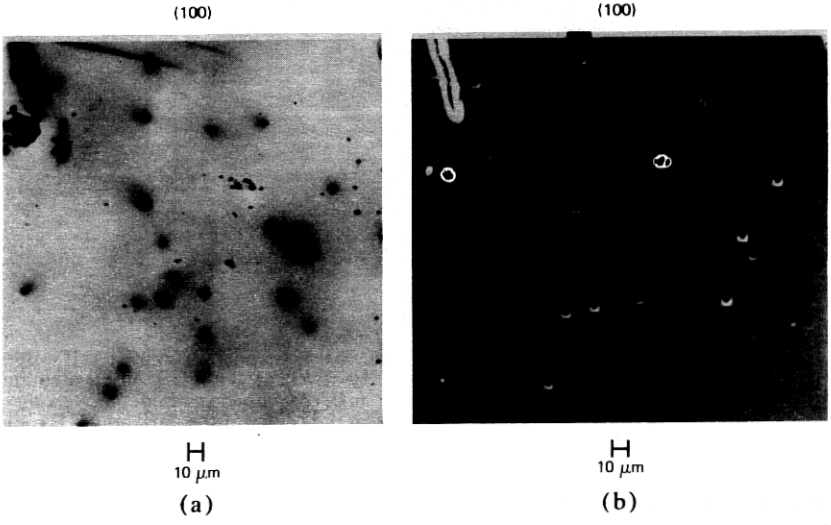


Fig. 5—Transmission cathodoluminescence image of a GaAlAs:Si epitaxial layer grown on {100} GaAs substrate. The dislocations appear as dark spots approximately 10 μm in diameter. (b) Secondary electron image of the area shown in (a) after 30 min in 300°C KOH etchant. The circles surround the small (1- to 2-μm diameter) dislocation pits. The squares surround the large (5 to 10 μm) dislocation pits.

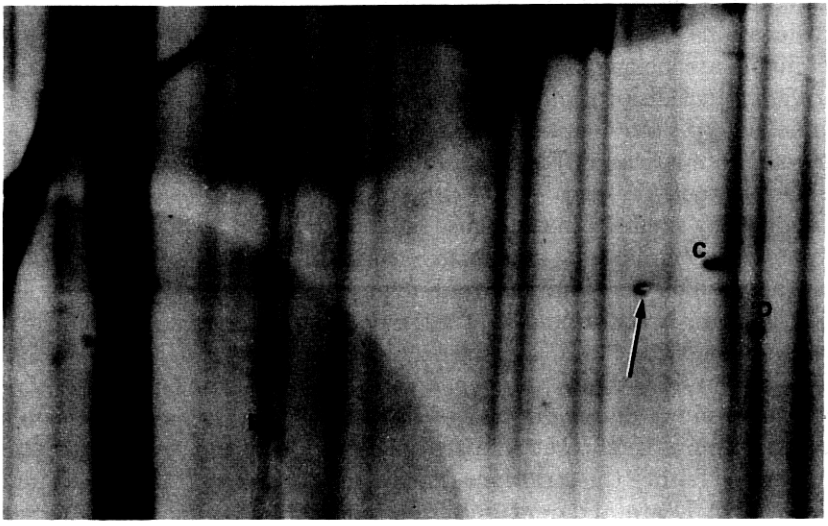
sample has been etched in molten KOH at 300°C for 30 min to reveal dislocations. The dislocation pits in {100} GaAlAs, as revealed by this etchant, are hexagonal in shape and terminate in a central point.[36] Two distinct dislocation pit sizes are observed independent of etching time. The pit size has been related to the dislocation inclination.[24] A careful comparison of Figs. 5a and 5b shows a one-to-one correspondence between the large (5- to 10-μm diameter) dislocation pits surrounded by a square in the figure and the TCL dark spots. In addition, apparently similar TCL spots also correspond to the small (1- to 2-μm diameter) dislocation pits surrounded by a circle.

Figure 6a is a TCL image of a Te-doped InP crystal. The vertical unevenly spaced lines are the impurity-induced growth striations. Their contrast is due to the dependence of the CL efficiency on doping density and not due to unresolved defects.[49] The dark band on the left of the figure is a scratch intentionally introduced to specify the location. Neither the striations nor the dark spots indicated by letters A through D are apparent on either a CL or an SE image. At higher magnifications, the dark spots have comma shapes as was found for the GaAlAs:Si sample in Fig. 5. The feature indicated by an arrow is a dust particle which appears also in the SE image.

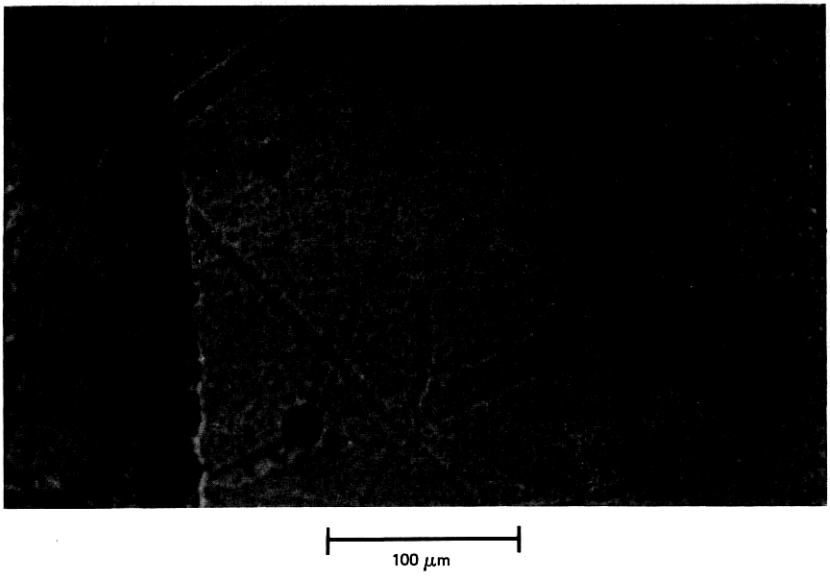
Figure 6b is a Nomarski optical photograph of the region shown in Fig. 6a after Huber etching to reveal dislocations. The magnification of Figs. 6a and 6b are slightly different. The four dislocation pits are labeled A through D for their corresponding TCL dark spot; an exact correspondence between dark spots and dislocation pits is found by comparing Figs. 6a and 6b. As compared to the freshly etched surface of Fig. 1a, Huber etching followed by TCL scanning produces a fairly poor surface. In addition, the growth striations are not clearly revealed. It is believed that carbon deposition during the TCL examination interferes with the etching process. The carbon is due to electron-beam decomposition of residual organics within the sample chamber. Etch pit D is somewhat obscure because the carbon film deposited over that area was twice as thick, a result of overlapping scan regions.

Figure 7a shows an SE image of the cleaved {110} surface of an InP:S sample after Huber etching and cleaving. Several dislocation pits produced on the {100} surface are intersected. A TCL scan of the corresponding area is shown in Fig. 7b. A dark region extending into the sample beneath each pit is observed, indicating that the pit corresponds to a dark spot on a TCL image of the {100} surface. Since the dark regions do not extend further into the crystal, the observed images could be due to portions of dislocation loops.

The above examples of correspondence between etch features and TCL images brings out several advantages of TCL over etching. First, TCL can be applied to any crystal face, whereas defect etchants are



(a)



(b)

Fig. 6—(a) Transmission cathodoluminescence image of {100} surface of InP:Te. (b) Secondary electron image of the area shown in (a) after Huber etching to reveal dislocations. Corresponding features in (a) and (b) are labeled A through D.

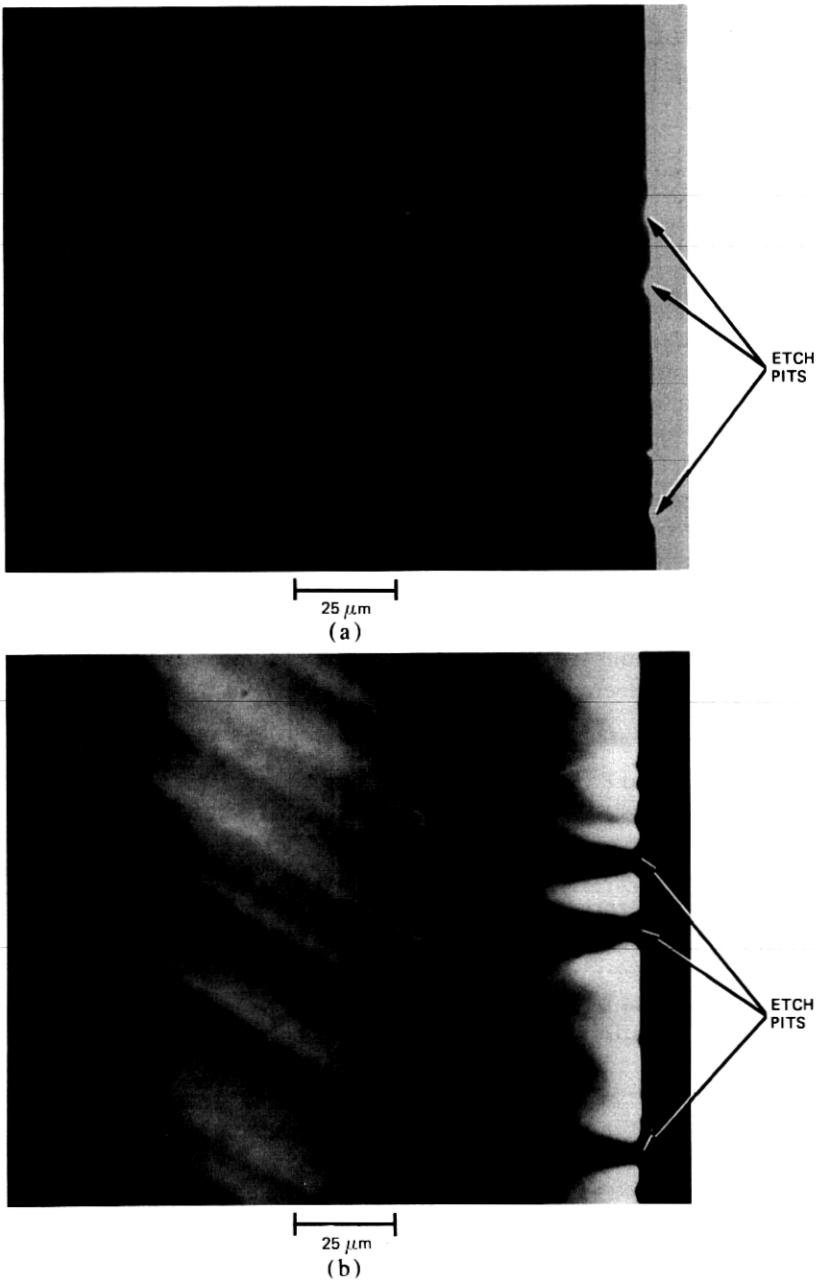


Fig. 7—(a) Secondary electron image of {110} surface of InP:S. Several etch pits on the {100} surface produced by Huber etching are intersected on the right-hand edge of the sample. (b) Transmission cathodoluminescence image of area shown in (a) displaying a dark region below each etch pit.

extremely orientation sensitive. Neither the KOH nor the Huber etch reveals defects on the {110} surfaces used as light-emission facets for lasers. Secondly, a defect etchant must be developed for each semiconductor, whereas TCL requires, at most, a change in detectors to accommodate the spectral range. Additionally, the development of a defect etchant is difficult and time consuming. Finally, etching is extremely sensitive to the surface preparation. The etchant may not work properly if the surface has been contaminated.

III. SUBSTRATES/EPILAYERS

The common substrates used for optoelectronic devices are GaP, GaAs, InP, and GaSb. Since good photodetectors at 1.6 μm are unavailable, dislocations in GaSb have not been imaged by any luminescence technique. In the case of GaP, dislocations appear readily under examination by CL or TCL. Using CL, however, dislocations in GaAs are readily imaged only for the case of Te doping; dislocations in GaAs:Se are difficult to image and have not been imaged in GaAs:Si.[27] Finally, dislocations in InP have not been observed for any dopant with CL scanning. However, using TCL, dislocations are easily observed for the commonly available GaAs and InP substrates.[10,14,15] These materials are listed in Table II. We will demonstrate the usefulness of the TCL technique on selected GaAs and InP substrates.

3.1 GaAs substrates

Figures 8a and 8b are, respectively, the SE and TCL images of a 375-μm-thick GaAs:Si substrate commonly used for the growth of LED and laser wafers. The white spot in the upper right of Fig. 8a is a dirt particle that appears dark in the TCL image; the dirt particle effectively blocks the electron beam from the semiconductor and prevents CL generation. The remaining comma-shaped dark spots with no corresponding features in the SE image are due to dislocations intersecting the surface at an oblique angle; the direction of the tail indicates the sense of inclination. This TCL image is typical of GaAs substrates grown by the gradient freeze technique; growth striations show weak contrast and are rarely observed. The dislocation image is unchanged when the dopant is changed from silicon to tellurium, another standard dopant for GaAs substrates.

3.2 InP substrates/epilayers

The recent work of Seki et al. has demonstrated that the macroscopic perfection of InP crystals grown by the liquid encapsulated Czochralski (LEC) technique can be improved by heavy doping.[50,51] The order of effectiveness in reducing the dislocation density is Zn, S, and Te. It is of considerable technological interest to assess whether or not

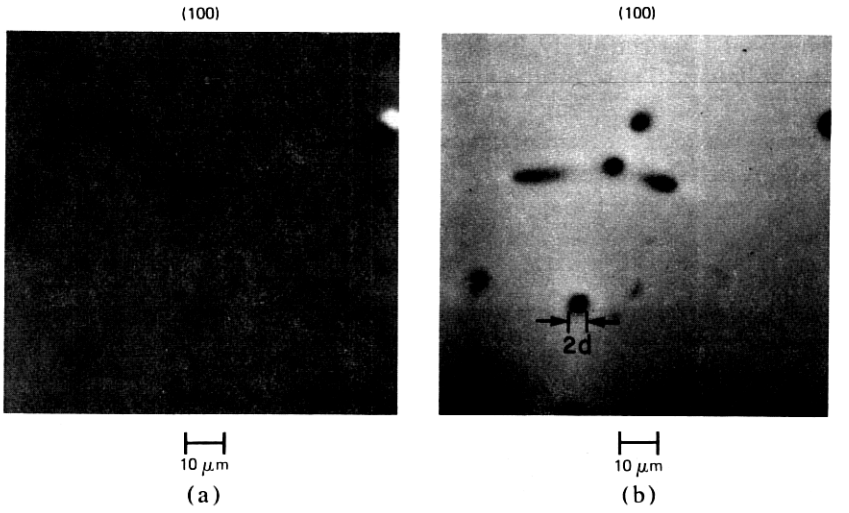


Fig. 8—(a) Secondary electron image of the {100} surface of a GaAs:Si substrate. The white spot on the upper right is a dirt particle. (b) Transmission cathodoluminescence image of the area shown in (a) displaying four dislocations. The diameter of the dislocation image is approximately twice the minority carrier diffusion length.

the macroscopic perfection of such highly doped substrates can be replicated into isoepitaxial layers grown by LPE. This is especially important since it was shown by Mahajan et al. that although heavy zinc doping reduces the dislocation density, a high density of Zn related precipitates results.[20] Similar effects have also been found for heavy Ge doping of InP.[52] Although individual precipitates, which are ~675 Å in dimension, cannot be resolved using TCL, precipitate clusters can be imaged.[20] Transmission cathodoluminescence imaging in this example is important since neither the precipitates nor their clusters show enough strain contrast to be observed either in X-ray topography or in Huber etching.[20] TEM is required for a detailed study, but TCL is useful for a simple, macroscopic investigation.

To facilitate the location of corresponding areas of substrate and epilayers in the TCL study,[23] a pattern was produced on one side of the wafers by evaporating gold through a shadow mask. This pattern may be observed irrespective of which side is excited with the electron beam. A similar CL or EBIC study would not be easy since corresponding areas of a wafer on opposite sides are difficult to locate in these techniques. In the TCL study, each side of the wafers is examined with the electron beam since maximum contrast and resolution of defects are obtained when the defects lie within the e-h excitation volume.

As ascertained by etch pitting, the quality of epilayers grown on the Zn-doped substrates was satisfactory and compared well with that of

the substrate.[23] Occasionally, etch pits in the form of clusters were observed. The TCL study, however, revealed additional features within the epilayers. These results are presented in Fig. 9. Figure 9a is the SE image of the 10-μm-thick InP:Sn epitaxial layer. This epilayer is a typical buffer layer used in device wafers. The small white features are indium-rich beads caused by localized surface decomposition. The beads appear as dark spots in the TCL image of Fig. 9b. In addition, however, a high density of light grey circular areas, whose origin at

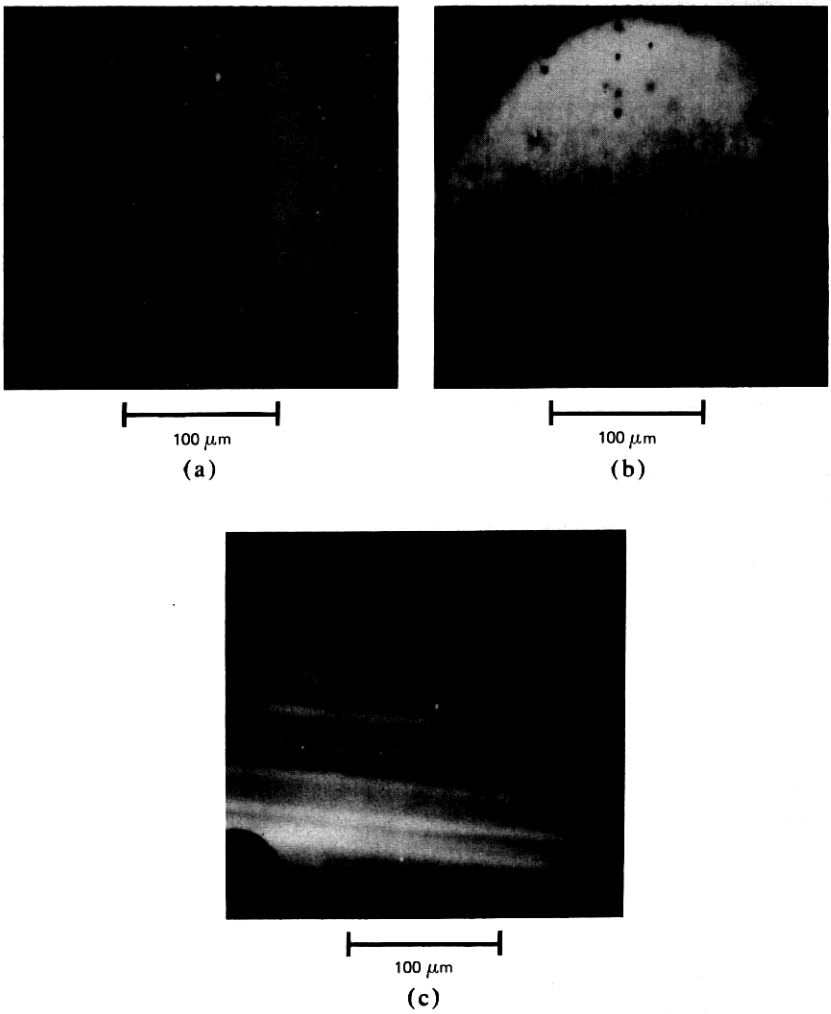


Fig. 9—(a) Secondary electron image of a 10-μm-thick InP:Sn epitaxial layer. (b) Transmission cathodoluminescence image of region shown in (a). (c) Transmission cathodoluminescence image of the underlying InP:Zn substrate.

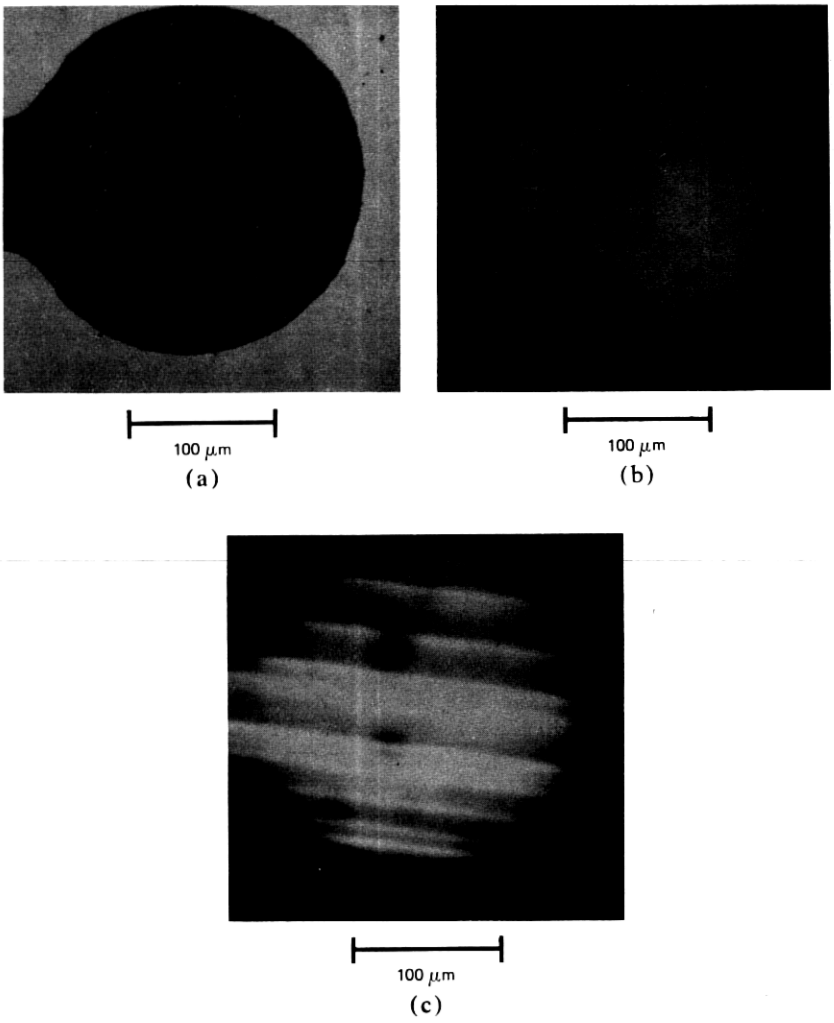


Fig. 10—(a) Secondary electron image of a 10-μm-thick InP:Sn epitaxial layer. (b) Transmission cathodoluminescence image of region shown in (a). (c) Transmission cathodoluminescence image of the underlying InP:S substrate.

present is uncertain, is apparent. These defects are likely related to the precipitates within the substrate, although corresponding features are not present in the substrate of Fig. 9c. Only growth striations and two defects are observed in the substrate. The dark border in Figs. 9b and 9c is due to the gold mask evaporated on the substrate side. A mirror inversion about a horizontal axis is required to exactly compare the image of the substrate with that of the epilayer.

Figure 10 shows images of a 10-μm-thick InP:Sn layer grown on a

heavily S-doped substrate. Figure 10a shows the SE image of the epilayer surface. The indium-rich beads on the surface are again evident. Figure 10b demonstrates that this portion of the epilayer is dislocation free and correlates very well with the quality of the substrate as illustrated in Fig. 10c. Nearly horizontal light and dark bands are growth striations, and darker regions on some of these bands may represent local dopant variations.

As a result of these studies, it was confirmed that macroscopically dislocation free InP may be obtained by heavy Zn or S doping. However, defect-free isoepitaxial layers may be grown only on the S-doped substrates. The defects in the epilayers on InP:Zn are probably a result of precipitates within the substrate. These precipitates have been observed by TEM in low-dislocation InP:Zn but not InP:S. Therefore, it is recommended that InP:S crystals having low-dislocation density be used as substrates for the growth of device wafers.

3.3 InGaAsP epitaxial layers

For InGaAsP layers whose bandgap corresponds to 1.3 μm, the Si photodetector normally used to detect transmitted CL was replaced with the Ge photodiode. Although CL radiation transmitted through the sample was detected by the Si diode in all cases, defects appeared for most of the InGaAsP samples studied only in the TCL image obtained with the Ge detector. Apparently, for these samples, the defects affected the CL emission and optical properties in the spectral region beyond the Si bandgap, i.e. wavelengths longer than 0.9 μm.

Figure 11 shows an SE and TCL image of a 2-μm-thick n-type, nominally undoped, InGaAsP epilayer grown on a 15-mil-thick, {111} oriented InP substrate. This TCL image was obtained using the Ge photodiode. The InP substrate does not contribute to the TCL image since it is transparent to the InGaAsP CL centered at 1.3 μm. Dark lines correspond to surface scratches or cracks seen in an SE image. The lower region of Fig. 11b is darker than the upper region because of a slight nonuniformity in the CL or optical properties of the quarternary layer. The dark spots, approximately 2 μm in diameter and similar in shape, have no corresponding surface features. By analogy with the TCL study of dislocations in GaAs and InP, it is suggested that these spots are caused by dislocations in the epitaxial layer. Additionally, it has been shown by etching studies that dislocations in the substrate are sources of dislocations in quarternary layers. The average density of dark spots imaged by TCL, 2–3 $\times$ 10^4 cm^{-2}, is approximately the same as that of the InP substrate. Finally, the minority carrier diffusion length of InGaAsP has been measured to be 1 to 2 μm in agreement with the diameter of the dark spots.[53]

It should be noted that the Ge detector is unsuitable for TCL imaging

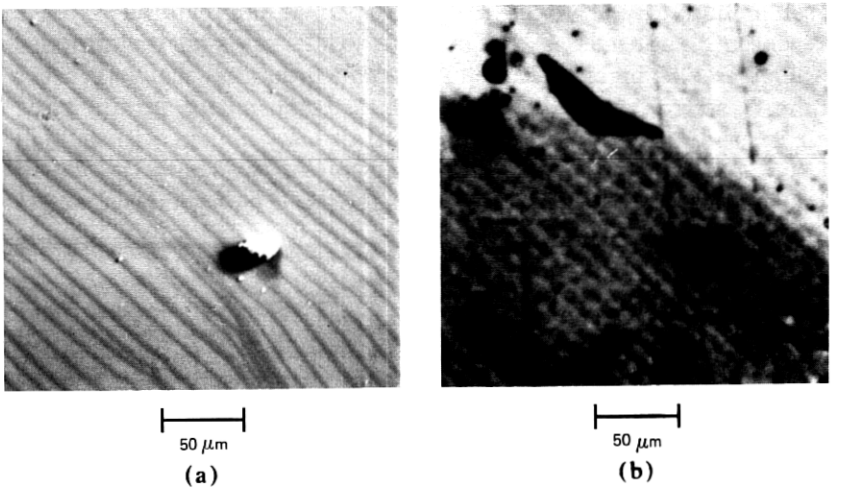


Fig. 11—(a) Secondary electron image of a 2-μm-thick *n*-type InGaAsP layer grown on a 15-mil-thick {111} oriented InP substrate. (b) Transmission cathodoluminescence image of region shown in (a). The dark spots not apparent in the SE image are dislocations.

of *p*-type InGaAsP, which has at least an order of magnitude lower efficiency than an *n*-type material. Imaging of *p*-type InGaAsP may be possible using lock-in amplification coupled with beam blanking of the electron beam.

IV. DEVICE WAFERS

The TCL imaging of device wafers differs from that of substrates because of the presence of a *p-n* junction and heterojunctions within the wafer. The built-in electric field at the *p-n* junction (depletion region) separates the generated electrons and holes and prevents recombination.[54] Thus, in the CL, EBIC, and TCL modes, the depletion region is probed indirectly. In either the CL or TCL mode, the image is complicated by this depletion width if the *p-n* junction intersects the e-h excitation volume. For the plane view configuration where the electron beam is orthogonal to the plane of the *p-n* junction, CL radiation is generated in the layers confining the *p-n* junction, i.e. the layers above and below the *p-n* junction. Thus, the image is composed of three components: the CL image of the two confining layers and variations in the depletion width. Electron beam-induced current scanning, however, is primarily composed of variations in the depletion width and comparison of EBIC images with CL and TCL images may be used to locate the position of defects within the wafer.

In this section, we will demonstrate the usefulness of TCL in evaluating the quality of device wafers used in fabricating LEDs and lasers

based on both the GaAs/GaAlAs and InP/InGaAsP material systems. Presently, TCL is used to screen out GaAs/GaAlAs wafers that produce unreliable LEDs; highly reliable LEDs are incorporated as light sources in the Western Electric (WE) 1250A optical transmitter. Additionally, TCL is used to screen out GaAs/GaAlAs laser wafers with a high density of rake lines without the removal of the contacting layer. Finally, TCL is used to screen out InP/InGaAsP LED and laser wafers with misfit dislocations.

4.1 GaAlAs LEDs

High radiance GaAs/GaAlAs LEDs and lasers operating at a current density of $J \gtrsim 10^3$ A/cm^2 can degrade rapidly by the development of dark line defects (DLDs).[8,31,55] Since these optoelectronic devices are intended for optical communication systems, a high yield of reliable devices is necessary. By detecting defects which act as sources for DLDs during processing, wafers with an unacceptable defect density may be rejected early and, thus, save processing time and cost.

A preliminary study involving single heterostructure LEDs shows that approximately 12 percent of the devices fail a stress test (burn-in) because of the growth of DLDs, whereas the remaining LEDs have a lifetime in excess of 10^6 hours.[56] Since DLDs in GaAs/GaAlAs-based devices are observed to originate at material defects, a high yield of long-lived devices may not be consistently achieved due to inevitable variations in substrate quality, epitaxial growth conditions, and processing procedures. A nondestructive technique such as TCL selects device quality material, evaluates growth and processing procedures, and reveals the degradation mechanism of fabricated devices.

The schematic of the GaAlAs LED used in the WE 1250A transmitter and the epitaxial structure is shown in Fig. 12. The growth of the GaAlAs layers by LPE and the device processing have been described elsewhere.[57] The 50-μm-thick n-type GaAlAs carrier confinement layer also serves as the window and mechanical support layer. This planar

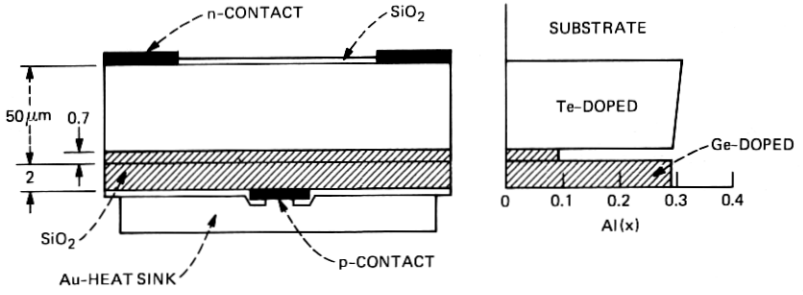


Fig. 12—Schematic of planar DH LED and device wafer. The shaded region of the device is Ge-doped.

structure facilitates device processing but the epitaxial growth is difficult. Because of the thickness of the first-to-grow window layer, the aluminum concentration gradient is large and nonequilibrium growth conditions must be controlled in forming the active and final confinement layers.

The device wafers are examined with the epilayers in the as-grown conditions. The substrate side of the wafers, normally rough polished, is bromine-methanol polished after epigrowth to reduce scattering of the TCL radiation. The electron beam of the SEM is scanned over the episide of the wafers since the quality of the epimaterial is of main interest. The typical 375-μm-thick GaAs substrate does not have sufficient absorption to reduce the TCL intensity below the limit required for good imaging using the silicon photodiode. This is in contrast to the CL or PL scan geometry where a thin (1 to 2 μm) GaAs contact layer is sufficient to reduce the signal below the detection limit.[30] No processing problems because of TCL examination of device wafers have been found; the wafers must be soaked in concentrated sulfuric acid to remove the electron beam deposited carbon prior to standard processing.

Figure 13 is a TCL image of a wafer that produced a high yield of reliable devices. Almost no dark spots corresponding to defects are observed; the faint light and dark bands are the growth lamellae normally observed in wafers grown by LPE. Figure 14a is a TCL image of an LED wafer grown under nonequilibrium conditions. Defects in the substrate are not imaged since the CL efficiency of GaAlAs is much higher than that of GaAs. The epilayers were grown on low-dislocation ($<10^3$ cm^{-2}) Si-doped substrates. However, as shown in Fig. 14b, an order of magnitude higher defect density ($\gtrsim 10^4$ cm^{-2}) is found in the TCL image of the epilayers. These defects cannot be observed using Nomarski contrast microscopy and are, thus, "hidden." An etching study using KOH was attempted to find the nature and origin of the defects. The etchant study was performed carefully so as not to remove the 2-μm-thick, last-to-grow layer. The etch pattern obtained did not distinctly reveal dislocation pits but resembled the TCL image. A similar etch study of a grooved sample showed these defects to be localized to the active and last-to-grow layers.

A TEM evaluation of the sample shown in Fig. 14a ascertained that the defects are dislocation tangles located within the epilayer. Figure 14b displays one of the dislocation tangles. The bar indicates 1 μm. A comparison of Figs. 14a and 14b shows that the TCL defect image is roughly 10 to 20 times their actual size, a result of the large minority carrier diffusion length. It is apparent from Fig. 14b that the dislocations are very closely spaced contiguous to the center, whereas interdislocation spacing increases when going toward the edges. Further-

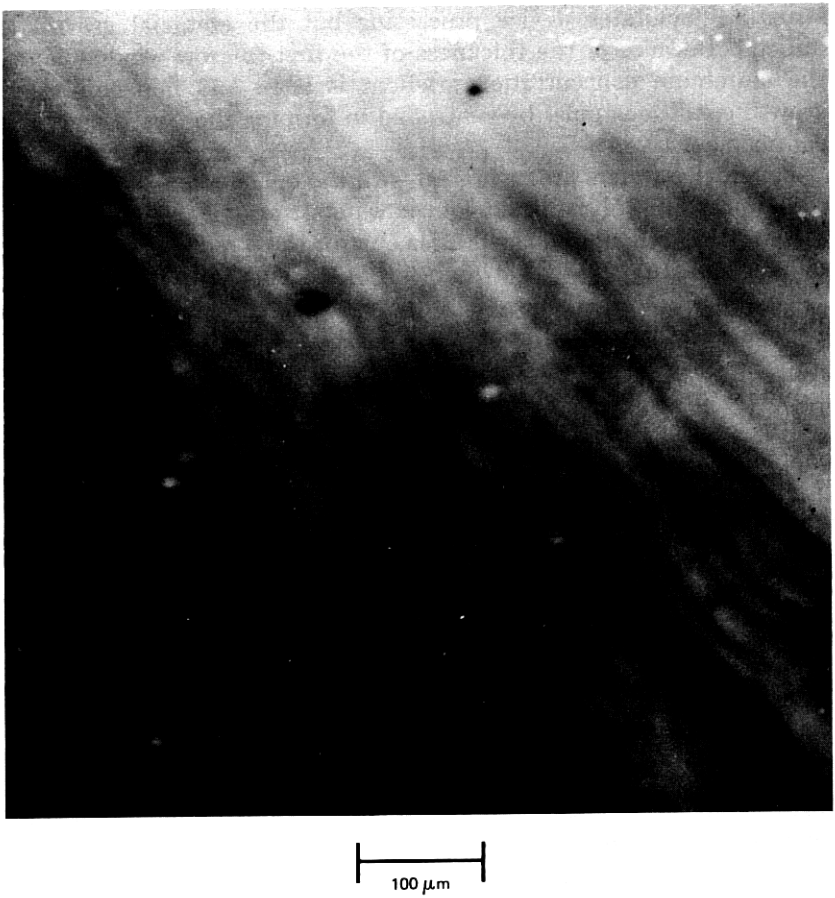
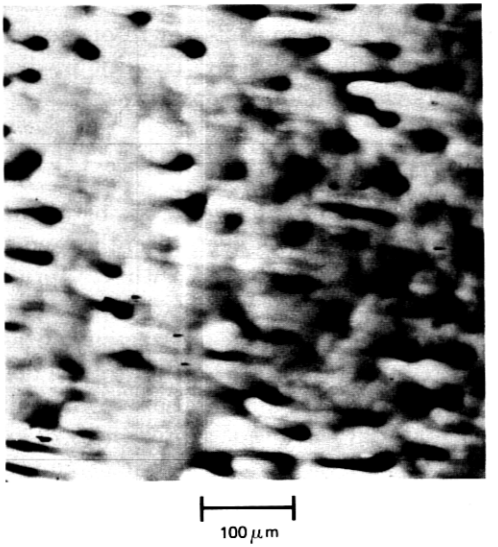


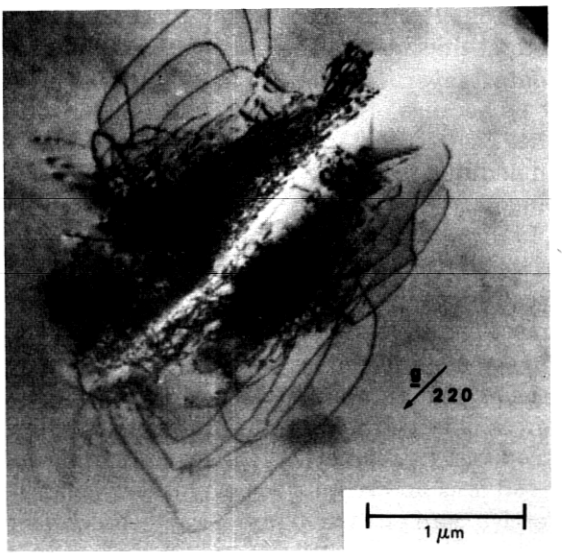
Fig. 13—Transmission cathodoluminescence image of a planar DH LED wafer-producing reliable LEDs.

more, stereomicroscopy reveals that the dense dislocation networks are essentially planar in character and are located within the active and last-to-grow layers. Since the networks appear to intersect along the [110] direction, their habit planes may be $(\bar{1}11)$ and $(1\bar{1}1)$ planes. The topology observed by stereomicroscopy is consistent with this suggestion.

A plausible explanation for the origin of dislocation networks is the following. It is suggested that at the temperature at which the growth of the thick window layer was completed, the active layer melt was supercooled in excess of 5°C. Faceted growth on {111} planes is initiated locally by this supercooling. Since the compositions of layers growing on the (001), $(\bar{1}11)$, and $(1\bar{1}1)$ planes are likely to be different, accommodation dislocation networks will be generated at the conflu-



(a)



(b)

Fig. 14—(a) Transmission cathodoluminescence image of a planar DH LED wafer grown under nonequilibrium conditions. The dark areas are dislocation tangles. (b) Transmission electron microscopy image of an individual dislocation cluster in the samples shown in (a).

ence of these different growth fronts. This growth problem encountered in the early stages of the planar double heterostructure (DH) LED development, results in a low yield of reliable devices. After adjusting the composition of the melts so that growth of the active and last-to-grow layers is under near-equilibrium conditions, dislocation tangles in the device wafers were no longer observed.

4.2 GaAs/GaAlAs lasers

The use of TCL as a nondestructive screening technique for defects in GaAlAs DH laser material has been recently reported by Gaw and Reynolds.[18] Every wafer is examined with TCL prior to processing. Wafers with a high density of rake lines are rejected since devices with this defect either do not lase or have an excessive threshold current. A nondestructive screening technique for this growth defect is especially important since ~45 percent of all material grown exhibits rake lines.[18]

The LPE laser material was prepared for the 0.83-μm lasers used in the FT-3 transmitter subsystem.[18] It has the usual four-layer DH with a Te-doped n-ternary confinement layer. Starting from the n-GaAs substrate, the layers have the compositions (*i*) N-GaAlAs ($x = 0.34$ to 0.44), (*ii*) P-GaAlAs ($x = 0.00$ to 0.10), (*iii*) P-GaAlAs ($x = 0.34$ to 0.44), and p-GaAs. The thickness of the p-active layer is 0.10 to 0.20 μm and the total thickness of the p-layers is ~1.8 μm. The p-GaAs is used for a contact layer. This contact layer prevents wafer scanning by either CL or PL because of absorption within this layer. Photocurrent scan may be used if contacts are applied, but TCL has a higher resolution in addition to the advantages provided by the SEM.

The TCL imaging of laser wafers is performed as previously for the LED wafers. In these wafers the back surface is polished prior to growth and, thus, TCL involves no additional processing.

Figure 15 compares the TCL image of a slice having severe rake lines with the almost featureless SE image of the top surface. Wafers with such a TCL image are rejected from further processing. Figure 16a and 16b shows the SE and TCL image of a wafer free of rake lines. In the absence of gross defects, the dislocations and dark spot defects which have lower contrast may be observed. By correlating the TCL evaluation with broad area and stripe geometry laser yields, TCL was shown to be an effective nondestructive screening technique for rake lines.

4.3 InP/InGaAsP LED and lasers

In InP/InGaAsP heteroepitaxy, the possibility of lattice mismatch exists. Misfit dislocations at the substrate-epilayer interface form when lattice mismatch is in excess of 0.06 percent.[58] These misfit dislocations have a deleterious effect on device performance and reliability.[40,59] In

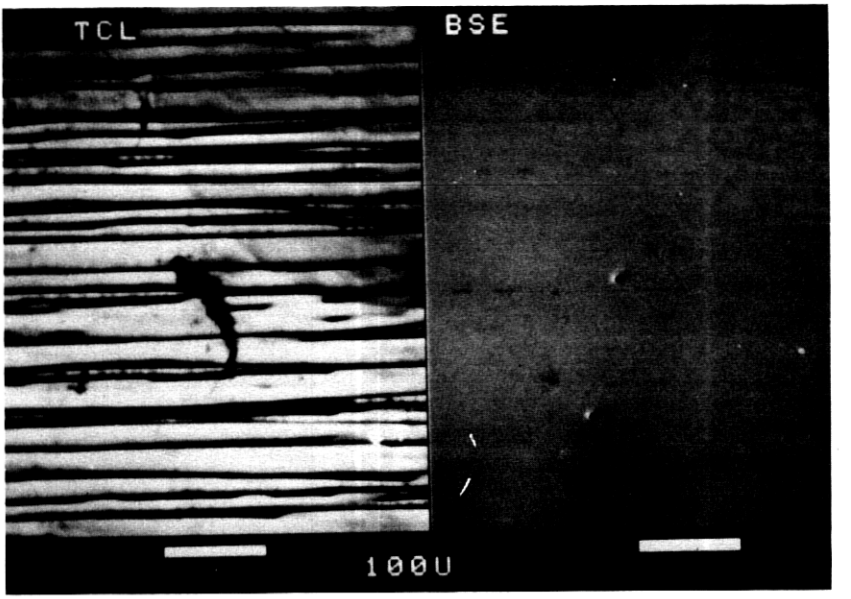


Fig. 15—Comparison of the TCL image of DH laser material having severe rake lines with the almost featureless SE image of the top surface of the slice.

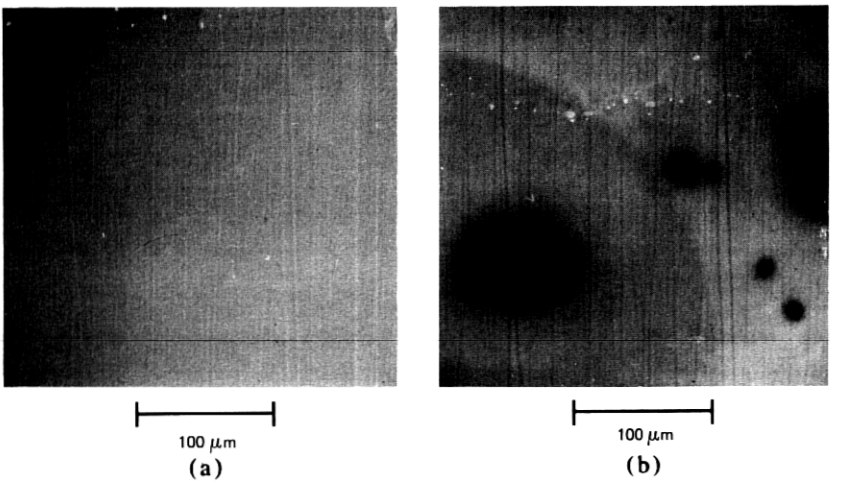


Fig. 16—(a) Secondary electron image of a DH laser wafer. (b) Transmission cathodoluminescence image of dislocations and dark spot defect in area shown in (a).

this section, we show that TCL can be used to screen out device wafers with misfit dislocations present.

Figure 17 presents the results obtained on a DH InP/InGaAsP/InP wafer intended for 1.3-μm devices. The wafer was lattice mismatched

with $\Delta a/a = 0.12$ percent. The active layer is ~0.5 μm thick and may be used for either LEDs or lasers. In Fig. 17a, the SE image of the top epitaxial layer shows growth lamellae, hillocks, and surface scratches. The epilayers were grown on a {111} oriented substrate. Most of the

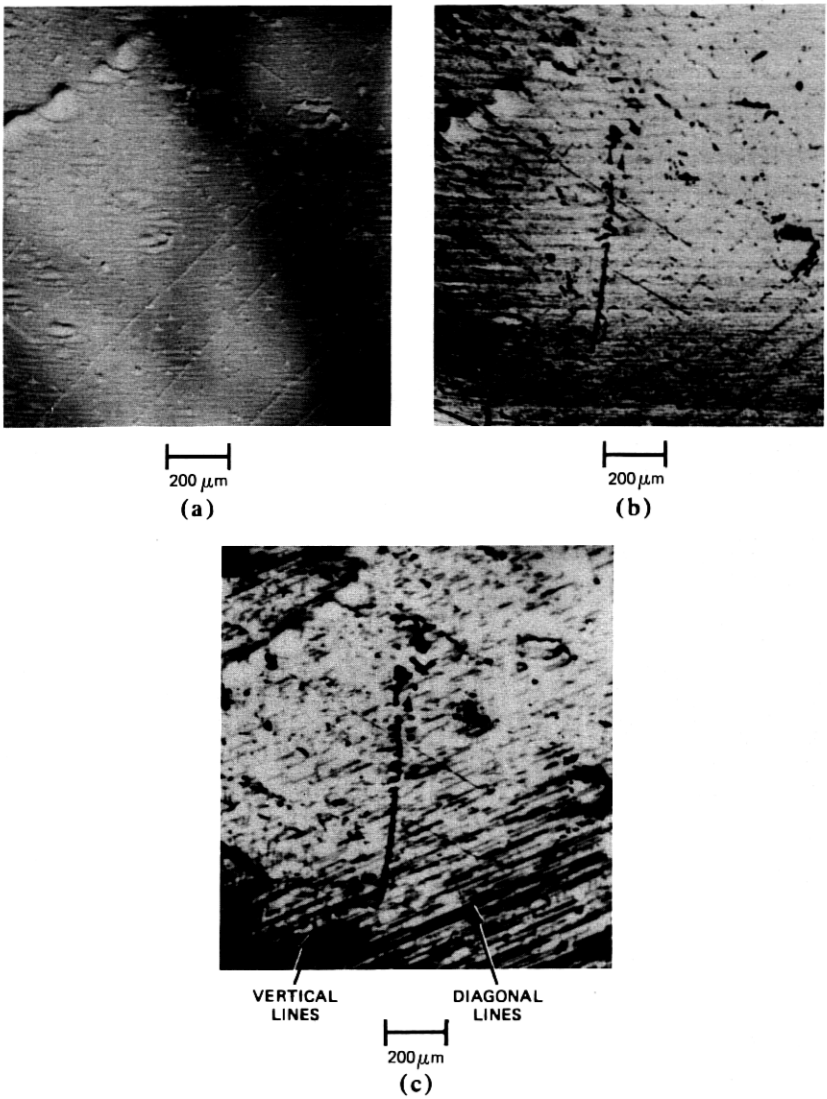


Fig. 17—(a) Secondary electron image of a DH InP/InGaAsP wafer. Growth lamellae, hillocks, and surface scratches are observed. (b) Cathodoluminescence image of the region shown in (a). The dark areas are surface defects. (c) Transmission cathodoluminescence image of the region shown in (a). The vertical and diagonal lines not seen in the CL image are misfit dislocations.

features of Fig. 17a are reproduced in Fig. 17b which shows a CL picture of the same region. The CL image was taken with an S1 photomultiplier which has a spectral response similar to that of an Si photodiode. Dark nonluminescing regions are clearly visible. Finally, in Fig. 17c, we show the TCL picture obtained with an Si detector. Additional features not observed in either SE or CL modes of the SEM are the large number of sharp diagonal and vertical dark lines which form an angle of ~60° between them. These lines are not within the electron beam range on the surface since they do not appear in the CL image. It is suggested that they are misfit dislocation at the InP buffer layer-InGaAsP active layer interface. Similar TCL imaging of lattice mismatched epilayers grown on {100} oriented substrates reveals two sets of orthogonal dark lines, providing additional support for this interpretation. Additionally, X-ray topographs of lattice mismatched {111} oriented wafers show images of misfit dislocations similar to those shown in Fig. 17c.[40,59]

V. DEGRADATION

Rapid degradation of optoelectronic devices has been due to defect growth. The overall device and especially the light-emitting region are often of extremely small dimension. Etching to reveal defects followed by visual examination is extremely difficult because of problems in sample handling and resolution. It is also difficult to perform defect analysis using the techniques of PL scan, infrared microscopy, and photocurrent scan for similar reasons. Although TEM analysis may be the only technique that can resolve defects, preparation of samples for TEM becomes an art. On the other hand, SEM techniques are both convenient and have adequate resolution and magnification in most cases. However, EBIC and CL analysis may be prohibited by the geometry of the device. The region of interest is often inaccessible to the electron beam and the sample must be demounted from the headers.

Figure 18 shows three device structures where EBIC and CL evaluation is difficult. Figure 18a shows either a planar LED or laser structure; the p-contact represents a dot for the LED and a stripe for the laser. Figure 18b shows an LED used for optoisolators. In the planar LED, the window layer is ~50–100 μm thick, thus, preventing the electron-beam excited carriers from reaching the active layer. In the laser structure, the device is usually mounted episide down for better heat-sinking. Even when the top n-metallization is partially removed to access the semiconductor, the thick substrate prevents the carriers from reaching the p-n junction. For the LED shown in Fig. 18b, the p-n junction is again located far from the excitation source. Thus, without demounting the devices, EBIC and CL provide little information about the p-n junction or active layer where the light is generated in electrolumi-

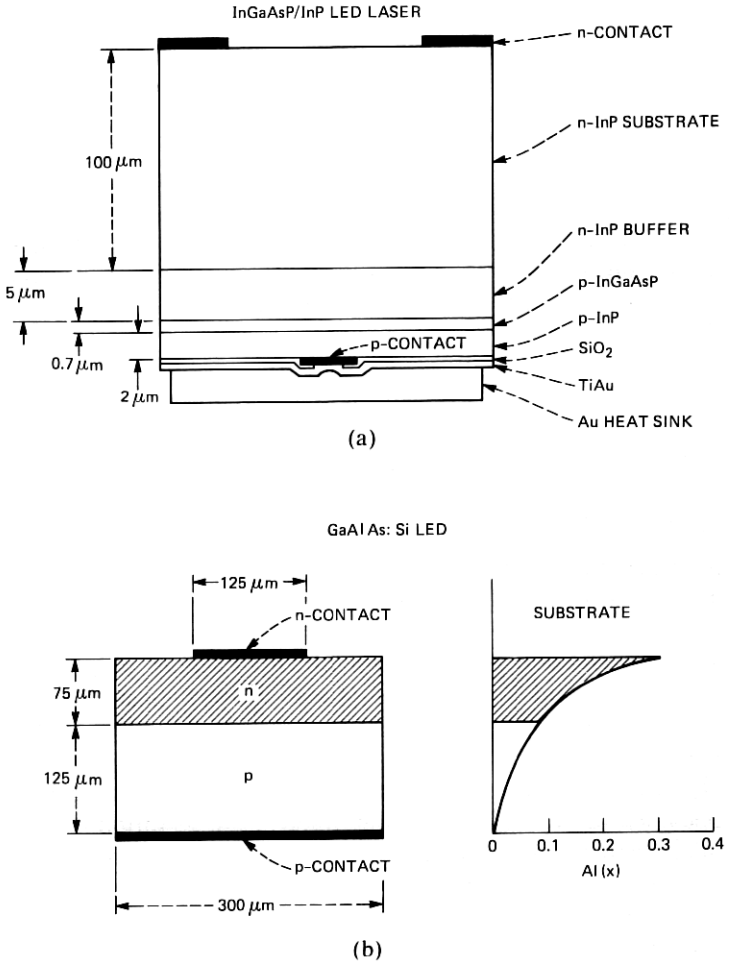


Fig. 18—(a) Schematic of InP/InGaAsP LED or laser structure. (b) Schematic of a GaAlAs:Si LED structure.

nescence. Once a device is demounted for analysis, it is impractical to rebond it for EBIC analysis. For the demounted devices, TCL is advantageous over CL because of the greater sensitivity of the technique in imaging defects. Examples will be shown where TCL is used to evaluate device degradation.

Formation of dark spots and dark lines oriented in the ⟨100⟩ and ⟨110⟩ directions is a degradation mode for LEDs and lasers fabricated from many semiconductors, e.g., GaP,[60] GaAs/GaAlAs,[8,31,54,55] GaAsP,[61,62] and InP/InGaAsP.[19,40,63,64] Dark line defects oriented along the ⟨110⟩ direction grow by glide of dislocations on the {111} slip planes,[65–68] whereas the growth of ⟨100⟩ DLDs may involve both glide

and climb of dislocations.[8,69,70] Studies have shown that formation of ⟨100⟩ DLDs require minority carrier injection, whereas ⟨110⟩ DLDs can be induced with either minority carrier injection or stress.[66]

Studies of stress-induced DLDs in GaAs/GaAlAs DH crystals provide a useful background. These studies showed that a threshold stress is required to form ⟨110⟩ DLDs.[65–68] This threshold level decreases for increasing minority carrier injection.[65,66,68] For no injection, the threshold stress is $\sim 8 \times 10^9$ dynes/cm^2.[66] This value rapidly decreases to $\sim 2 \times 10^9$ dynes/cm^2 under the lower excitation level of 3W/cm^2 from a 6471 Å Kr-ion laser beam, equivalent to a current density of $J = 1$ A/cm^2.[66] A lower stress level of $\sim 6 \times 10^8$ dynes/cm^2 is found for $J =$ 58 A/cm^2.[68] These stress values are comparable in magnitude to other typical sources of stress. Stresses from dielectric coatings can be as high as 10^{10} dynes/cm^2.[62] Stresses because of dicing damage are 2–7×10^7 dynes/cm^2,[61] and the internal stress on a mounted LED, assuming a 100°C temperature difference between header and LED, can be $\sim 10^9$ dynes/cm^2.[71] Care in processing and handling is required if stress-induced DLD formation is to be avoided.

5.1 InP/InGaAsP LED

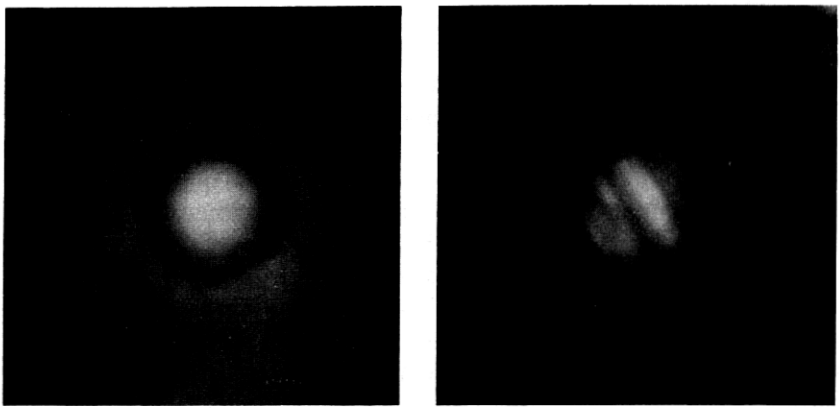
The degradation of InP/InGaAsP LEDs by the formation of ⟨110⟩ DLDs has recently been reported by Temkin et al.[19] It was demonstrated that this mode of degradation occurs for temperatures in excess of 190°C even without current bias. Although DLDs may be observed in electroluminescence and EBIC scanning, TCL was used to show that the DLDs originated at defects within the InP buffer layer. Additionally, the DLDs were confined to the InP buffer layer and did not extend into the quarternary active layer during aging.

The wafer consists of an Sn-doped InP buffer layer ($n \sim 2 \times 10^{18}$ cm^{-3}, 2 to 4 μm thick) followed by a InGaAsP active layer (not intentionally doped, 0.7 μm thick) and an Zn-doped InP confining layer ($p \sim 3 \times 10^{18}$ cm^{-3}, 2 μm thick). The p-n junction, formed by Zn outdiffusion from the confining layer, is placed at the interface between the buffer and quarternary layer. The lattice mismatch, $\Delta a/a$, between the InGaAsP active layer and InP was kept below 2×10^{-4}, and the wafer, thus, has no misfit dislocations to begin with. After thinning the wafer to ~ 100 μm, metallizations were electron-beam evaporated using shadow masks. The Be/Au p-contact, 50 μm in diameter, was made directly to the p-confining layer; the Au-Sn-Au n-contact was deposited during the same evaporation run.[72] Finally, a 20-μm-thick gold heat-sink, separated from the semiconductor by a 2000-Å-thick layer of SiO_2, was plated on the p-side of the wafer to assure low thermal impedance of the diode. The finished devices were mounted with

epoxy on heat-sink headers and wire bonded. A schematic of the device structure is shown in Fig. 18a.

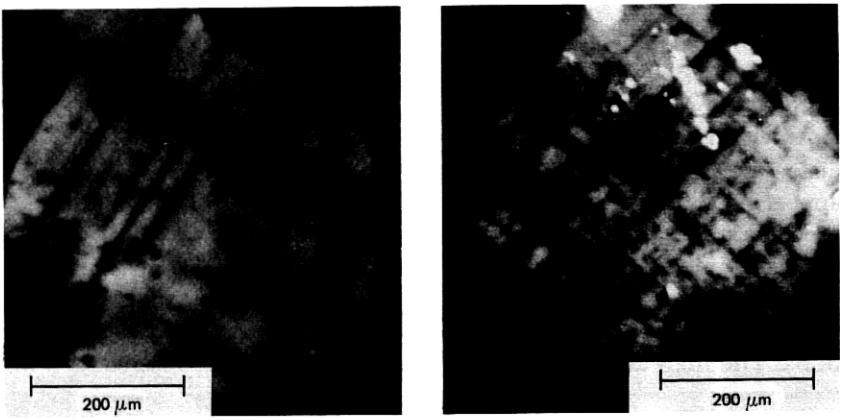
The electroluminescence (EL) images of an LED before and after the 200°C aging (300 h and no bias) are shown in Fig. 19. Figure 19a shows a uniform and well-defined light spot imaged by an infrared-sensitive vidicon tube. No inclusions or processing-induced defects could be seen. Figure 19b shows the EL pattern of the LED degraded to 40 percent of its initial light output. A large number of ⟨110⟩ DLDs could be seen throughout the entire contact area. Similar EL patterns have been seen in all of the 30 devices aged by 200°C storage (no bias) degradation.

To find the position of DLD sources within the device structure, diodes which were carefully removed from their heat-sink headers were examined by TCL. After demounting the devices, the *p*-contact and the confining *p*-InP layer were removed using appropriate etchants, and devices were evaluated by TCL. Two series of TCL scans were performed. In the first, the exposed opening in the *n*-metallization was scanned by the electron beam of the SEM and the signal detected by a Ge-PIN placed under the device. The resulting image, in which CL was generated in the InP substrate is shown in Fig. 20a. Inclusion-like defects with associated DLDs can be seen. This image is similar to an EBIC image of the device. In the second TCL scan, the chip was turned upside down with the quaternary (*Q*) active layer facing the electron beam and the detector placed directly below the *n*-InP. In this configuration, in which the CL signal originated in the *Q*-layer, inclusions and DLDs were not observed. After removal of the active layer with a selective stop-etch, the exposed surface of the *n*-InP buffer layer was



(a) (b)

Fig. 19—(a) The EL pattern of an LED before aging. (b) The EL pattern after storage aging at 200°C for 300 h with no bias.



(a) (b)

Fig. 20—(a) Transmission cathodoluminescence image obtained on a degraded device. The *n*-InP surface is imaged in the opening in the metallization. (b) Transmission cathodoluminescence image of the *n*-InP buffer layer with the quarternary active layer removed by a selective etchant.

imaged and the result is shown in Fig. 20b. Again, only the area above the opening in the *n*-metallization was imaged. The prominent DLDs observed previously are still visible (a mirror inversion is needed for comparison between Fig. 20a and 20b). However, a number of additional features can be seen. These consist of a much greater density of inclusion-like defects and a large density of shorter DLDs originating at those defects. This DLD pattern is similar to the images obtained by EL. Thus, the DLDs and their sources appear to be confined to the InP buffer layer and its interfaces with the InP substrate and the *Q*-active layer. Since these DLDs grow without current injection, they are believed to be stress induced.

5.2 Planar GaAlAs LED

For planar GaAlAs LEDs, the TCL technique is especially important since dislocations and DLDs cannot be observed in either the EBIC or CL mode of the SEM. Although good quality CL images of the LEDs were obtained on our apparatus, dislocations are still not observed probably because of a lack of instrument sensitivity. Balk et al. showed that a highly efficient CL apparatus is required to detect dislocations in GaAs:Se;[73] a similar apparatus may be required to detect dislocations in our device wafers. Also, because of the thickness of the window layer, the EBIC signal is not from primary e-h pairs generated by the electron beam, but from secondary e-h pairs generated within a minority carrier diffusion length of the p-n junction by recombination radiation from the primary electron-holes. Thus, the effect of dislocations on the EBIC signal is likely to be below the noise level.

Figure 21 is a TCL image of the back surface of an LED that degraded during the 100 h burn-in. The 50-μm-diameter area defines the contact or light-emitting region. A ⟨100⟩ DLD is observed in the contact region along with two ⟨110⟩ DLDs. These DLDs were observed in the EL image. However, the source of the two ⟨110⟩ DLDs, not seen in EL, is a dislocation lying at the intersection of the DLDs. This dislocation, appearing as the dark spot indicated by the arrow in Fig. 21, intersects the back surface outside the contact area but probably threads through the light-emission region below the surface. The source of the ⟨100⟩ DLD could not be distinguished in this image; this DLD was already well developed as shown by the larger width in comparison to the ⟨110⟩ DLDs. The high density of dark spots representing the intersection of

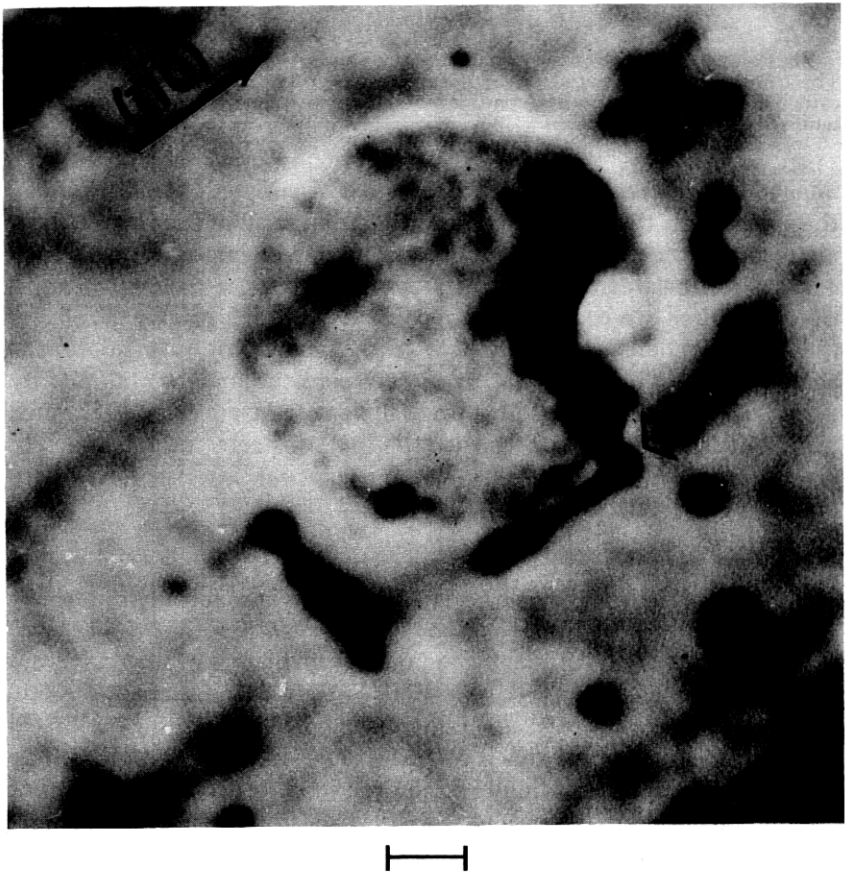


Fig. 21—Dark line defects oriented along ⟨100⟩ and ⟨110⟩ directions in a planar DH LED induced by current injection during burn-in. The circular region defines the 50-μm-diameter back surface contact.

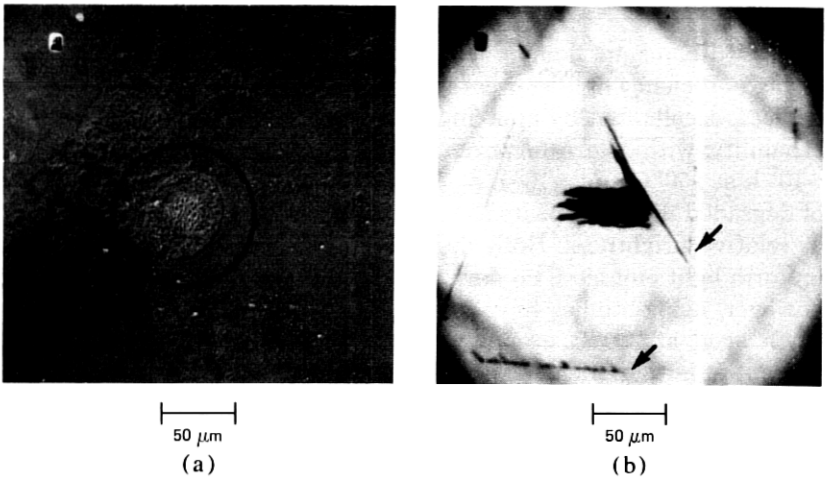


Fig. 22—(a) Secondary electron image of the *p*-surface of a planar DH LED. The circle encloses the contact. (b) Transmission cathodoluminesence image showing ⟨110⟩ DLDs induced by current injection during long-term aging. The source of DLDs are the two scratches indicated by the arrows.

dislocations with the surface in the vicinity of the contact and the identification of a dislocation as the source of the ⟨110⟩ DLDs in this sample suggest that a dislocation may also be the source of the ⟨100⟩ DLD.

The majority of the DLDs observed in samples degraded during burn-in are similar to those shown in Fig. 21. Also typical of degraded LEDs is the high density of dislocations. It is emphasized that no dislocations were observed in the contact area of undegraded LEDs subjected to the burn-in.

Figure 22 shows the *p*-surface of a device that catastrophically degraded after ~5000 h of operation at room temperature under 6 kA/cm^2 bias. From the TCL image, Fig. 22b, the method of degradation can be reconstructed. Two scratches were initially present, i.e. the two lines away from the *p*-contact indicated by the arrows. During operation, a ⟨110⟩ DLD started from one of the scratches and propagated towards the contact. Upon reaching the contact area, enclosed by a circle in the SE image of Fig. 22a, the DLDs multiplied rapidly because of the high-current density. The catastrophic degradation at ~5 × 10^3 h agrees with the slow growth of ⟨110⟩ DLDs under the low injection conditions away from the *p*-contact. Thus, TCL examination identifies a previously unreported method by which LEDs degrade; defects away from the contact area may initiate DLDs that grow into the contact area and rapidly degrade the device.

GaAlAs:Si LED

Graded-bandgap, homojunction GaAlAs:Si LEDs are presently used as high-efficiency light sources for optoisolators.[17,48] Bias tests of these devices, accelerated by applying a thermal stress, demonstrated high reliability; with 30 mA forward current bias, a mean-time-to-failure of $\sim 10^5$ h at 250°C and $\sim 10^8$ h at 25°C was determined. The EL pattern of degraded diodes appears to differ from that of unaged devices only in relative brightness. Both degraded and undegraded LEDs exhibit uniform light emission; no dark lines or spots are observed. Recently, however, aging studies have shown that some LEDs degrade rapidly when aged at 200°C even without current bias; degradation to 10 percent of initial efficiency occurred within 400 h. Examination of the EL image of many of the most heavily degraded devices showed the presence of ⟨110⟩ oriented DLDs. Thus, the drop in LED efficiency is attributed to nonradiative recombination at the DLDs. Since dark line formation has not been previously observed in graded bandgap GaAlAs:Si LEDs, TCL was used to investigate the origin and growth behavior of the DLDs.

To determine the source of the DLDs, the degraded LEDs were first visually inspected on the headers using the SEM and Nomarski interference microscopy. Some damage was found, but it was considered neither unusual nor excessive. After demounting the LEDs from the headers, small pyramids of various sizes were found on the *p*-surface of some of the LEDs.

Figure 23a is an SE image of an unaged LED with several pyramids.

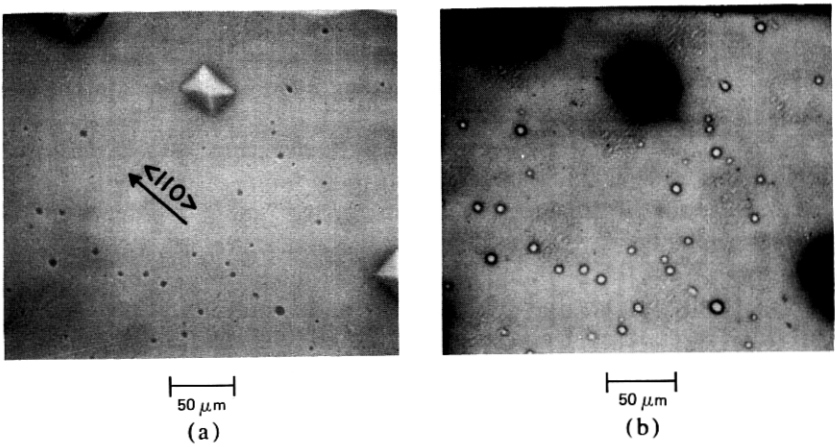


Fig. 23—(a) Secondary electron image of the *p*-surface of an unaged LED with pyramids. The sides of the pyramids are parallel to the ⟨110⟩ directions. (b) Transmission cathodoluminesence image of the region shown in (a). The dark area surrounding each pyramid is a dislocation network. The short dark lines are dislocations extending along the ⟨110⟩ directions.

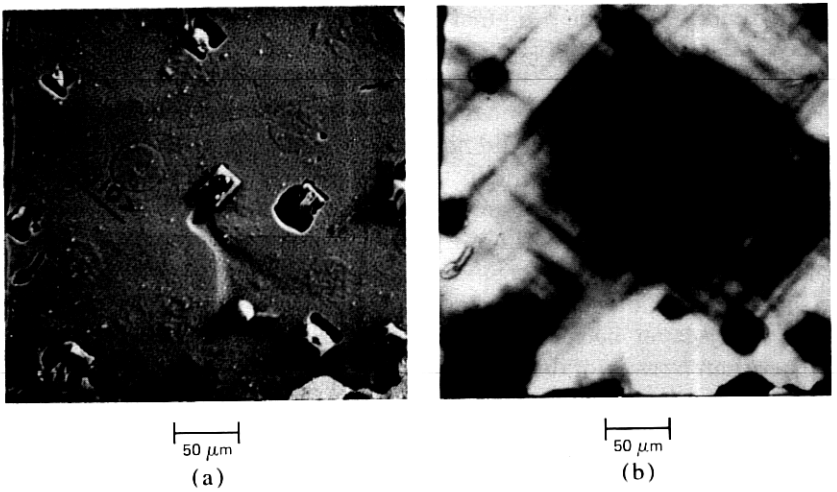


Fig. 24—(a) Secondary electron image of the *p*-surface of a degraded LED with pyramids. (b) image of region shown in (a). Dark line defects oriented along ⟨110⟩ direction initiate at the pyramids.

X-ray microanalysis on the SEM showed that these pyramids are composed mainly of silicon. Figure 23b is the TCL image of the region shown in Fig. 23a. The pyramids appear dark because of the low luminescence efficiency of these regions. In addition to the dark regions, dark lines extending from the pyramids along the ⟨110⟩ directions are observed. These dark regions and lines are part of a dislocation network and have no corresponding features in the SE image, Fig. 23a. These dislocation networks are probably a result of lattice mismatch between the GaAlAs epilayer and the Si pyramids.

Figures 24a and 24b are, respectively, the SE and TCL images of the *p*-surface of typical degraded, bonded LEDs. Although Figs. 23 and 24 correspond to two different LEDs, comparison of these figures show clearly that with aging, the dislocation networks originating at the pyramids enlarge along the ⟨110⟩ directions and form ⟨110⟩ DLDs.

The above study was carried out exclusively on the *p*-surface because of the presence of pyramids. To determine whether the DLDs originate only on the *p*-surface, the top *n*-surface and {100} sides of the LEDs need to be examined. In unaged devices, the usual dislocations, stacking faults, and processing damage were found on these surfaces. In degraded devices, irrespective of the degree of degradation, TCL images of the *n*-surface were similar to those of unaged LEDs, but ⟨110⟩ DLDs were found on the {100} side faces. By examining the {100} planes of partially and highly degraded LEDs, the DLDs were found to initiate at the *p*-surface and propagate towards the p-n junction; the DLDs did

not extend beyond the p-n junction into the n-region even in the most heavily degraded LEDs ($\eta/\eta_o < 0.01$).

Figures 25a and 25b show the TCL image of the {100} side of a partially ($\eta/\eta_o \sim 0.6$) and heavily degraded ($\eta/\eta_o \sim 0.1$) LED, respectively. The LED in Fig. 25a did not show DLDs in the EL image, whereas several DLDs were apparent in the EL image of the LED in Fig. 25b. The explanation of the EL images is evident by comparing Figs. 25a and 25b. In both figures, the p-n junction appears as a dark line since the built-in electric field separates the e-h pairs generated by the electron beam and prevents recombination. The n-layer is brighter than the p-layer because of higher intrinsic luminescence efficiency rather than a result of degradation. In Fig. 25a, the DLDs initiate at the p-surface and extend up the sides. The DLDs intersect the {100} p-surface at an angle of 45 degrees, suggesting that the DLDs lie on the {111} slip planes. Dark line defects do not appear in the EL image since they have not propagated to the p-n junction where the EL image is generated. In Fig. 25b, the DLDs propagate up to the p-n junction but do not penetrate into the n-layer. Thus, DLDs appear in the EL image, but not in a TCL or EBIC scan of the n-layer. Figure 25 also demonstrates the ineffectiveness of EBIC in obtaining similar images. Electron beam-

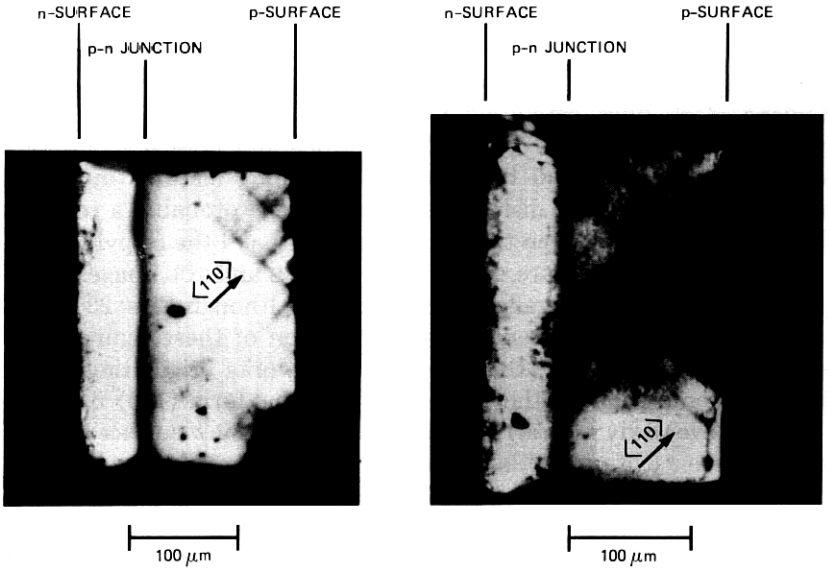


Fig. 25—(a) Transmission cathodoluminesence image of ⟨100⟩ side of a degraded LED. Dark line defects oriented along ⟨110⟩ direction initiate at the p-surface and propagate along the ⟨111⟩ planes toward the p-n junction. (b) Transmission cathodoluminesence image of ⟨100⟩ side of a degraded LED. ⟨110⟩ DLDs terminate at the p-n junction.

induced current images the region approximately twice the minority carrier diffusion length on either the p or n region. However, as shown in Fig. 25, the DLDs form far from the p-n junction. Additionally, the EBIC signal varies dramatically at the p-n junction. The small perturbations on the EBIC signal produced by the DLDs are hard to image on such a strongly varying background signal.

The DLDs stop their growth upon reaching the p-n junction probably because of lower stress in the n-layer. Since the etch used to remove the saw damage during die separation removes more of the n-layer than the p-layer, the n-layer may have a lower surface damage-induced stress as found for GaP LEDs. A high internal electric field at the p-n junction is unlikely to hinder the propagation of the DLDs. Similar stress induced ⟨110⟩ DLDs in GaAs/GaAlAs wafers have been shown to propagate through the p-n junction.[74] Further study, e.g., an examination of degraded LEDs using TEM or a reliability study of LEDs that have been etched more uniformly, is required to determine the exact cause of this effect.

As a result of this TCL study, wafers with Si pyramids evident in a visual inspection are rejected prior to processing since the wafers produce unreliable LEDs.

VI. SUMMARY

We have demonstrated a new SEM imaging technique which we have called transmission cathodoluminescence (TCL). Defects within the e-h excitation volume are imaged as in the familiar CL mode but with a much higher collection efficiency and, thus, with a much higher detection sensitivity. In addition, this technique can be used to image defects within the sample volume that changes the optical properties of the materials; these defects cannot be imaged with the CL mode. We have demonstrated the TCL technique on a variety of defects in a variety of semiconducting materials used in optical communications. Transmission cathodoluminesence can be used to screen out low-quality substrates and device wafers to save processing time and cost, provide rapid evaluation of growth and processing procedures, and evaluate degraded devices where other defect revealing techniques are either unsuitable or very difficult.

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