THE BELL SYSTEM TECHNICAL JOURNAL
Vol. 60, No. 9, November 1981
Printed in U.S.A.

A Fault-Collapsing Analysis in Sequential Logic Networks

By S.-J. CHANG and M. A. BREUER*

(Manuscript received September 11, 1980)

Although a sequential circuit M reduces to a combinational network C_M after all feedback paths have been cut, an application of Bossen and Hong's checkpoint labeling procedure to C_M does not necessarily yield a minimal solution. The set of checkpoints so obtained will include all feedback lines. In this paper, it is shown that these feedback lines are not necessary checkpoints under a "delay equivalence" relation. In addition to this, we also show that not every fanout branch is a necessary checkpoint. Any "singular fanout branches" can be removed from consideration. The results of our analysis lead to a minimal checkpoint labeling procedure for sequential logic networks.

I. INTRODUCTION

Because there are $3^w - 1$ possible multiple stuck faults in a logic network containing w distinct locations where signals may fail (each location may assume one of the three possible states: normal, stuck-at-0, or stuck-at-1), test generation and simulation procedures often resort to fault collapsing techniques to reduce the number of faults which need to be considered. To date reported results in the literature deal only with combinational logic. This prompted our interests in the research to be discussed in this paper.

Bossen and Hong introduced a fault collapsing technique for combinational logic networks called checkpoint labeling procedure.[1] Checkpoints, as defined by them, are a number of specified points in the network such that any multiple fault in the network is equivalent to some multiple fault among these specified checkpoints.[1] The checkpoints defined in Ref. 1 are a minimal set of points having the property

* M. A. Breuer is with the Departments of Electrical Engineering and Computer Science, University of Southern California, Los Angeles, California.

just stated. A natural question is, What are the checkpoints in a sequential circuit? It is well known that by cutting all the feedback lines, a sequential network can be mapped into a combinational network. A reasonable approach would be to apply Bossen and Hong's labeling procedure to the resulting combinational network. The checkpoints obtained would then include all the feedback lines. In this paper, we show that in general all these feedback lines need not be checkpoints under a relation called "delay-equivalence" to be defined later. We will see that the number of checkpoints can be greatly reduced for a highly sequential logic network if our results are utilized. This, in turn, greatly reduces computational complexities for multiple fault analysis in sequential networks. A possible application of our results can be found in a paper by Chang, Su, and Breuer.[2]

II. FAULT COLLAPSING IN SEQUENTIAL NETWORKS

The checkpoints in a circuit are specially designated signal lines. Checkpoints are defined so that for an arbitrary stuck-at-fault α there exists at least one equivalent fault defined on the checkpoints. Hence, if there are $u \ll w$ checkpoints, we need only consider $3^u - 1$ multiple faults. Bossen and Hong have developed a labeling procedure for specifying the minimal set of checkpoints in a combinational circuit. Their results seem to be an extension of the work of Shertz and Poage.[3,4]

For convenience, Bossen and Hong's procedure is as follows:

(*i*) All the primary inputs that do not fan out are checkpoints.

(*ii*) All the fanout branches are checkpoints.

(*iii*) NOT gates are considered as lines.

Although a sequential circuit M reduces to a combinational network C_M after all feedback paths have been cut, Bossen and Hong's labeling procedure does not necessarily yield a minimum number of checkpoints for such circuits.

Consider a synchronous sequential circuit M represented by Huffman's model as shown on Fig. 1, where C_M is the combinational portion of M, and D is the set of delay elements. We assume that faults in C_M are restricted to stuck-at type and faults in delay elements (D f/f's) result in stuck outputs. Gates and flip-flops of M are connected by edges. An edge of M is either a line or a branch. Namely, it is either a primary input, a primary output, a fanout stem, or a fanout branch. Also we shall assume the following:

Assumption 1: The output value of a gate is a function of each of its inputs.

Assumption 2: The number of edges in M is finite.

Assumption 3: There are no "inaccessible" edges in M. An edge of

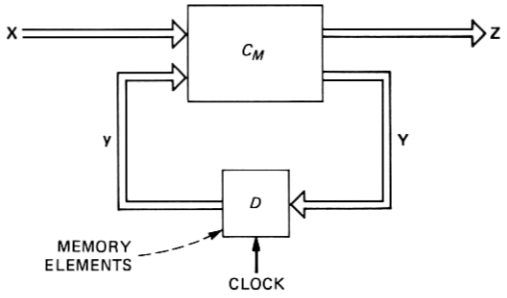

Fig. 1—Huffman's model of a sequential circuit M.

M is said to be inaccessible if it is not a primary input and, moreover, if it is not driven by any gates or memory elements of M.

Almost all practical sequential circuits satisfy the above assumptions. Figure 2 shows a fictitious integrated circuit chip. Edge 5 is inaccessible.

Restricting our attention to stuck-at-faults, we define a single fault as exactly one edge stuck-at-1 (s-a-1), or stuck-at-0 (s-a-0), and a multiple fault as a collection (one or more) of single faults, each associated with a different edge. Also, we shall not consider intermittent faults.

By applying Bossen and Hong's procedure to the combinational network C_M, the set of checkpoints so obtained will include all feedback lines denoted by the vector $\mathbf{Y}$. However, we shall show that this subset of checkpoints is not necessary under a delay-equivalence relation. Later we shall consider asynchronous sequential circuits.

III. SEQUENTIAL NETWORK WITH D FLIP-FLOPS

Definition 1

Two faults u and v in M are said to be *delay-equivalent* (*d-equivalent*) *of order* k, if M with u is equivalent to M with v after an application of an input sequence of length at least k.

If the specific value of k is not of interest to us, we shall simply say

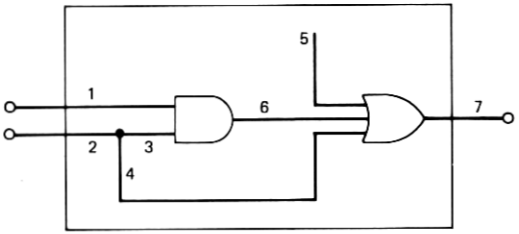

Fig. 2—A fictitious integrated circuit chip.

that u and v are d-equivalent. To demonstrate this concept, let us refer to the sequential circuit shown in Fig. 3. The fault a s-a-0 is d-equivalent of order 1 to the multiple fault b s-a-0 and c s-a-0.

Lemma 1: *Any multiple fault in a delay flip-flop is d-equivalent of order* 1 *to a stuck input.*

Proof: Let y and $\mathbf{Y}$ denote, respectively, the output and input of a delay f/f. Then, $y(q + 1) = Y(q)$ for all q. Thus, a stuck output is d-equivalent of order 1 to a stuck input. Also, a stuck input and output is d-equivalent of order 1 to a stuck input only, and is d-equivalent of order 0 to a stuck output only.

Because of this lemma, we shall consider a delay f/f as a 1-input gate under the d-equivalence relation.

Definition 2

(*i*) A sequence of edges of M, denoted by $[s_1, s_2, \cdots, s_i, \cdots, s_n]$, where $s_i \neq s_j$ for all $i \neq j$, is said to be a *forward path*, if for each $i < n$ either (a) s_i is a fanout stem and s_{i+1} is a fanout branch of s_i, or (b) there exists a gate of M, say g, such that s_i and s_{i+1} are, respectively, an input and the output of g.

If $s_1 = \alpha$ and $s_n = \beta$, the path $[s_1, s_2, \cdots, s_n]$ is said to be a *forward path from* α *to* β. If β is a primary output, the path is said to be a *terminal forward path of* α.

(*ii*) A sequence of edges of M, denoted by $[s_1, s_2, \cdots, s_i, \cdots, s_n]$, where $s_i \neq s_j$ for all $i \neq j$, is said to be a *backward path*, if for each $i < n$ either (a) s_i is a fanout branch and its stem is s_{i+1}, or (b) there exists a gate of M, say h, such that s_i and s_{i+1} are, respectively, the output and an input of h.

If $s_1 = \alpha$ and $s_n = \beta$, the path is said to be a *backward path from* α *to* β. If β is a primary input, then the sequence $[s_1, s_2, \cdots, s_i, \cdots, s_n]$ is said to be a *terminal backward path of* α.

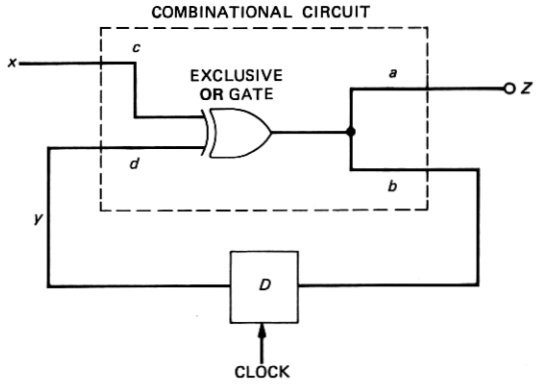

Fig. 3—A simple sequential circuit.

A backward path from α to β, denoted by p, is said to be a backward path of α, if there exists no edge Γ in M such that a backward path from α to Γ contains every element of p. The path p is said to *terminate* at β.

Clearly, if β is a primary input of M, then a backward path from α to β is also a terminal backward path of α.

The path $[s_1, s_2, \cdots, s_n]$ is said to *pass through* each s_i. Conversely, each s_i is said to be *contained* in the path. Branch s_i is also said to be an *element* of the path $[s_1, s_2, \cdots, s_n]$.

As an example, consider M_1 on Fig. 4. The sequences [12, 18, 6, 8, 9, 11, 20] and [12, 17, 19, 5, 8, 9, 11, 20] are forward paths of edge 12. However, the sequence [12, 18, 6, 8, 10, 12, 15, 16, 19, 5, 8, 9, 11, 20] is not a forward path of 12 because edges 12 and 8 appear twice in the sequence. All backward paths of edge 20 are shown in the graph of Fig. 5. Note that this graph is a tree with edge 20 as the root, and the leaves are either primary inputs or fanout branches.

Definition 3

If every edge of M possesses at least one terminal forward path, then M is said to be a *regular* sequential circuit. Otherwise, M is said to be *irregular*.

We will focus our attention on regular sequential circuits.

Definition 4

A *sensitized path* from an edge $\alpha = x_i$ to an output β in M is a terminal forward path from α to β, along with constant signal values assigned to some of the other edges such that changing the logic value of x_i will change the logic value of β.

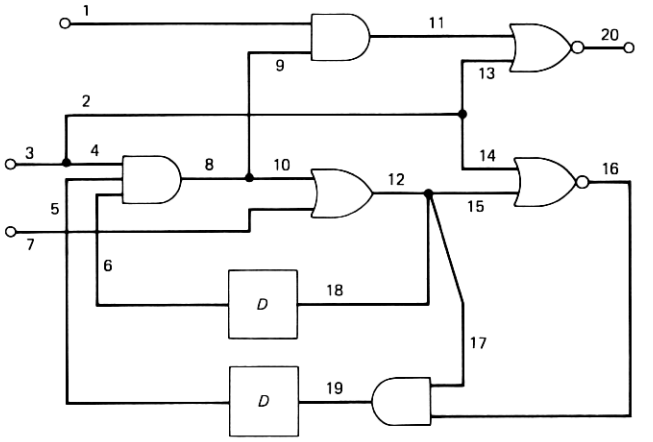

Fig. 4—Sequential circuit M_1.

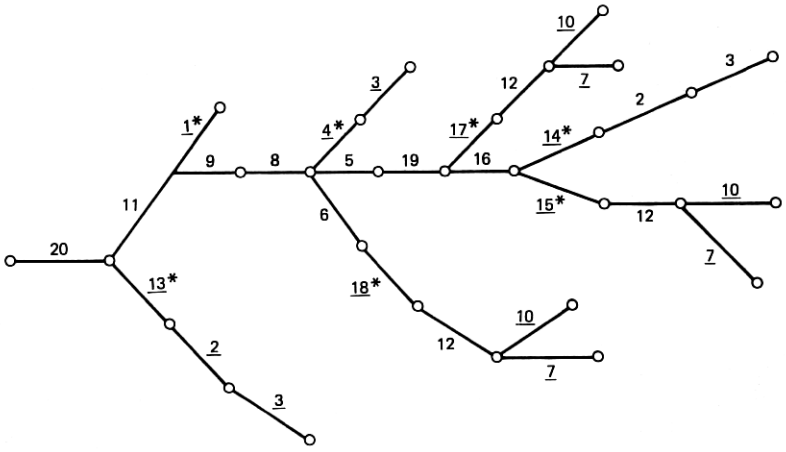

Fig. 5—Backward paths of edge 20 of M_1. Underline indicates either a primary input or nonsingular fanout branch. Starred edges are members of $K(20)$.

In the circuit shown in Fig. 4, we can sensitize the edge 1 to the output 20 by setting edge 9 to s-a-1 and edge 13 to s-a-0.

Lemma 2: Let g be a gate in M, a regular sequential circuit, and x_1, x_2, $\cdots$, x_n be the inputs to g. For each i, there always exists a multiple fault in M which will sensitize x_i to an output.

Proof: Since M is regular there exists at least one terminal forward path from x_i to an output β. Using the concept of Boolean difference,[5] the condition for sensitizing the output of g to the input x_i is given by the equation

$$\frac{dg}{dx_i} = g_0 \oplus g_1 = g_0\bar{g}_1 + \bar{g}_0 g_1 = 1,$$

where

$$g_0 = g(x_1, \cdots, x_{i-1}, 0, x_{i+1}, \cdots, x_n),$$

and

$$g_1 = g(x_1, \cdots, x_{i-1}, 1, x_{i+1}, \cdots, x_n).$$

Now select any minterm of $g_0\bar{g}_1$ or $\bar{g}_0 g_1$. If this minterm specifies $x_j = \sigma_j$, where σ_j is either 0 or 1, then let the x_j input to g be stuck at σ_j. Now assume that for the terminal forward path from x_i to β, the output of g is an input to gate h. Repeating the process just described, h can be sensitized to g. This chaining process is continued until β is reached.

Definition 5

Let α and β be two edges of M. Edge α is said to *dominate* edge β, if both α s-a-0 and α s-a-1 will cause M to become independent of the signal on β regardless of whether or not other edges are normal.

To illustrate this, let us consider Fig. 2. Edge 6 dominates edges 1 and 3. Edge 7 dominates all other edges. However, edge 2 does not dominate edge 1, because when edge 3 s-a-1 and edge 4 s-a-0, edge 7 is a function of edge 1 independent of the state of edge 2.

Theorem 1: *Edge α dominates edge β, if and only if all terminal forward paths of β contain α.*

Proof: Suppose all forward paths of β pass through α. A stuck α will block any signal on β. Thus, M becomes independent of β if α is stuck. Therefore, α dominates β. Suppose there exists one terminal forward path of β that does not contain α. Then, by Lemma 2, one can always find a multiple fault on M, which will sensitize the signal on β to at least one of the primary outputs of M. Thus, M is dependent on β and α does not dominate β. This proves the only if part.

Theorem 2: *Dominance relation induces a partial ordering.*

Proof: Every forward path of α passes through α. Thus, α dominates α. Let α_1 dominate α_2 and α_2 dominate α_3. By Theorem 1, all forward paths of α_3 and α_2 pass through α_2 and α_1, respectively. Thus, all forward paths of α_3 also pass through α_1. This implies that α_1 also dominates α_3. Suppose α dominates β and β dominates α. By Theorem 1, all forward paths of β pass through α and all forward paths of α pass through β. This means that if $\alpha \neq \beta$, none of α and β has a forward path. Therefore, α dominates β and β dominates α implies $\alpha = \beta$. Namely, dominance relation is reflexive, transitive, and antisymmetric. We conclude that it induces a partial ordering.

In a combinational network, a fanout branch never dominates other fanout branches of its stem. However, in a sequential circuit a fanout branch may dominate other fanout branches of its stem. Consider, for example, the sequential circuit M_1, which is shown on Fig. 4. Branches 9 and 10 are fanout branches of stem 8. Since every forward path of 10 passes through 9, branch 9 dominates branch 10.

Definition 6

A fanout branch that dominates other fanout branches of its stem is said to be *singular*; otherwise, it is said to be *nonsingular*.

Theorem 3: *(i) A stem possesses at most one singular branch. (ii) Every singular branch dominates all other fanout branches of its stem.*

Proof: Let a stem which possesses singular branches be denoted by β and its fanout branches be denoted by $\alpha_1, \alpha_2, \cdots, \alpha_n$, where α_1 is singular. By definition, α_1 must dominate at least one α_i ($\neq\alpha_1$). If α_j, where $j \neq 1$ or i, is also singular, then α_i will have at least one forward path that does not pass through α_1 because every forward path of α_i contains the fanout stem β. Thus, α_i will no longer be dominated by α_1. This contradiction proves *(i)*. Suppose some α_k is not dominated by

α_1. Then, α_k possesses at least one forward path that does not pass through α_1. It follows that α_i, for all $i \neq 1$, also possesses at least one forward path that does not pass through α_1. Part (*ii*) of the theorem follows as a result of Theorem 1.

Definition 7

The *kernel set* of edge α of M, denoted by $K(\alpha)$, is a set of edges of M such that

(*i*) every backward path of α contains exactly one member of $K(\alpha)$,

(*ii*) members of $K(\alpha)$ are either primary inputs that do not fanout or nonsingular fanout branches, and

(*iii*) every forward path from each member of $K(\alpha)$ to α does not contain any other nonsingular fanout branches.

Let us consider M_1 again (see Fig. 4). All backward paths of edge 20 are shown on Fig. 5. Each underlined edge is either a primary input or nonsingular fanout branch. Every starred edge is an element of the kernel set of edge 20 [i.e., $K(20)$]. From Fig. 5 we have $K(20) = \{1, 4, 13, 14, 15, 17, 18\}$. The following kernel sets can be easily verified: $K(1) = \{1\}$; $K(12) = \{7, 10\}$; and $K(8) = \{4, 14, 15, 17, 18\}$.

Lemma 3: *Let α and β be any pair of edges of M.*

(*i*) *A stuck α is d-equivalent to some multiple fault among its kernel set $K(\alpha)$.*

(*ii*) *If $K(\alpha)$ and $K(\beta)$ are disjoint, then any multiple fault among α and β is d-equivalent to some multiple fault among $K(\alpha) \cup K(\beta)$.*

Proof: Part (*i*) follows jointly from the fact that any multiple faults of a logic gate are equivalent to multiple faults among the input lines only,[1] and the definition of $K(\alpha)$ which requires that every backward path of α contains exactly one member of $K(\alpha)$. Part (*ii*) follows part (*i*) of the lemma.

Lemma 4: *If α does not dominate β, then either* (*i*) *there exists no forward path from β to α, or* (*ii*) *every forward path from β to α contains at least one nonsingular branch.*

Proof: If statement (*i*) is true, then α does not dominate β.

Suppose there exists a forward path from β to α, denoted by $p = [s_1, \cdots, s_n]$, that does not contain any nonsingular branch. Then s_i is either a fanout free stem or a singular branch. Let s_i be singular. Then, s_{i-1} is a fanout stem. By Theorem 3, all other fanout branches of s_{i-1} are dominated by s_i. Therefore, all forward paths of s_{i-1} pass through s_i. Thus, all forward paths of β also pass through α. This implies that α dominates β. Suppose every s_i is a stem without fanout, then p is a fanout free path. But by Theorem 1, this also implies that α dominate β. The contradiction proves the lemma.

Theorem 4: *If α does not dominate β and β does not dominate α, then their kernel sets are disjoint.*

Proof: Let $\sigma \in K(\beta)$. Then, σ falls into exactly one of the following categories.

(*i*) σ lies in a backward path of β which does not contain any edge in common with any backward path of α.

(*ii*) σ is contained in a forward path from α to β.

(*iii*) σ is contained in a backward path of β, say p, that does not contain α but p, and a backward path of α, say q, contains common branches.

Clearly, if σ belongs to category (*i*), $\sigma \notin K(\alpha)$. If σ belongs to category (*ii*), by Lemma 4 and category (*iii*) of the definition of $K(\alpha)$, $\sigma \notin K(\alpha)$. So, consider only category (*iii*). Let $p = [s_1, s_2, \cdots, s_n]$, and $q = [t_1, t_2, \cdots, t_m]$. Category (*iii*) implies that there exists u and v such that $s_u = t_v$ and $s_i \neq t_j$ for all $i < u, j < v$. Namely, s_u (or t_v) is a fanout stem. If s_{u-1} and t_{v-1} are nonsingular, by definition σ lies in a forward path from s_{u-1} to β; that is, $\sigma \notin K(\alpha)$. If s_{u-1} is singular, by Theorem 3 t_{v-1} is not. Thus, branch t_{v-1} is dominated by s_{u-1} and so is α. If s_{u-1} is dominated by β then so is α. This contradicts the assumption. Therefore, s_{u-1} is not dominated by β. By Lemma 4, there exists $k \leq u - 1$ such that s_k is a nonsingular branch. This implies that $\sigma \notin K(\alpha)$. Therefore, $K(\beta)$ and $K(\alpha)$ are disjoint.

Theorem 5: *In a regular sequential circuit, every singular branch is not a necessary checkpoint, but all nonsingular fanout branches are necessary checkpoints.*

Proof: Let β be a fanout stem with fanout branches $\alpha_1, \cdots, \alpha_n$, where α_1 is singular. By Theorem 3, every $\alpha_i \neq \alpha_1$, is dominated by α_1. Thus, a stuck α_1 edge is d-equivalent to a stuck β edge. As to a stuck α_i edge, for any $i \neq 1$, it is not d-equivalent to either a stuck β edge, or stuck α_1 edge, or stuck α_j edge for $j \neq i$. Therefore, all nonsingular fanout branches of β are necessary checkpoints.

Theorem 6: *For any irregular sequential circuit M there exists a regular sequential circuit M^* such that M and M^* are equivalent, and furthermore, M^* preserves fault behavior of M under stuck-type fault assumption.*

Proof: Being irregular, M possesses two sets of edges, denoted by Ω and Ω^*, where each member Ω does not have any terminal forward paths, and each member of Ω^* possesses at least one terminal forward path. It follows that no primary output of M is a function of the signals on any member of Ω under fault-free or any stuck-type fault conditions. Therefore, removing all members of Ω will not alter the normal or abnormal functional behavior of M. The resulting circuit consists of only edges in Ω^* and is regular.

To illustrate this theorem, consider sequential circuit M_2 on Fig. 6a. One can easily verify that $\Omega = \{4, 5, 8, 11, 13, 14, 16\}$ and $\Omega^* = \{1, 2, 3, 6, 7, 8, 9, 10, 12, 15, 17\}$. After removing Ω from M_2 and

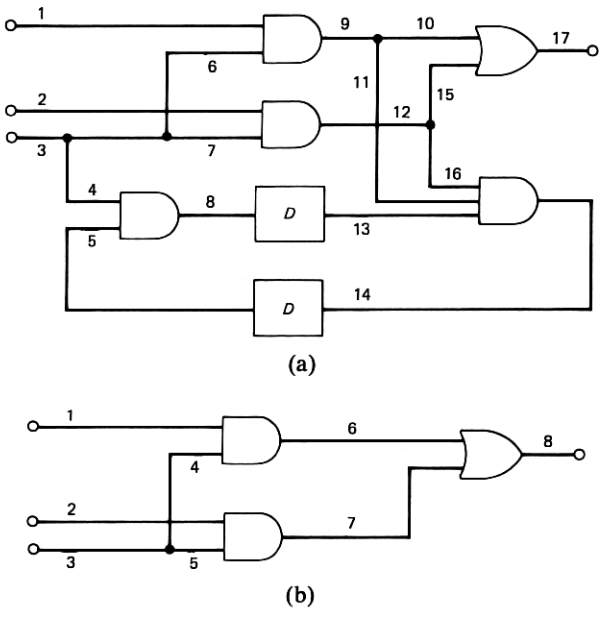

Fig. 6—Use of Theorem 6. (a) Sequential circuit. (b) Circuit M_3.

relabeling, one obtains the sequential circuit M_3, shown on Fig. 6b, which is actually a combinational circuit.

Theorem 7: *In a sequential circuit M, either* (*i*) *the kernel set for any edge in M exists, or* (*ii*) *M is irregular.*

Proof: Suppose α is an edge of M. Let a backward path of α be denoted by $p = [s_1, s_2, \cdots, s_n]$, where $s_1 = \alpha$. Then, p belongs to one of the following categories.

(*i*) p is a terminal backward path; namely, s_n is a primary input of M.

(*ii*) There exists $\tau < n$ such that s_n and $s_{\tau-1}$ are fanout branches of τ. (See Fig. 7a.)

(*iii*) There exists a gate g such that α is an input of g and s_n is the output of g. (See Fig. 7b.)

(*iv*) s_n is inaccessible.

Category (*iv*) never occurs because of Assumption 3.

Suppose p falls into either category (*i*) or (*ii*). Then every backward path of α contains at least one nonsingular fanout branch or a primary input. This implies that $K(\alpha)$ does exist if case (*iii*) does not apply.

Now consider case (*iii*). Suppose there exists no s_i, $1 \leq i \leq n$, that is, a fanout branch. This means that every element of p does not have a terminal forward path. Thus, M is irregular.

Suppose there exists some s_i, $1 \leq i \leq n$, that is a fanout branch. If s_i

is singular, then s_{i+1} is the stem of s_i. Moreover, s_{i+1} is dominated by s_i. If all other fanout branches of p are also singular, then by the transitivity of dominance, s_i would be dominated by s_{i+1}. This would imply that neither s_i nor s_{i+1} has a forward path. Thus, we conclude that some s_j must be a nonsingular fanout branch and, hence, the theorem follows.

From the foregoing analysis, we now derive a checkpoint labeling procedure for a sequential circuit M.

Step 1. If M is irregular, convert M into M^* as in the proof of Theorem 6.

Step 2. All primary inputs that do not fanout are checkpoints.

Step 3. All nonsingular fanout branches are checkpoints.

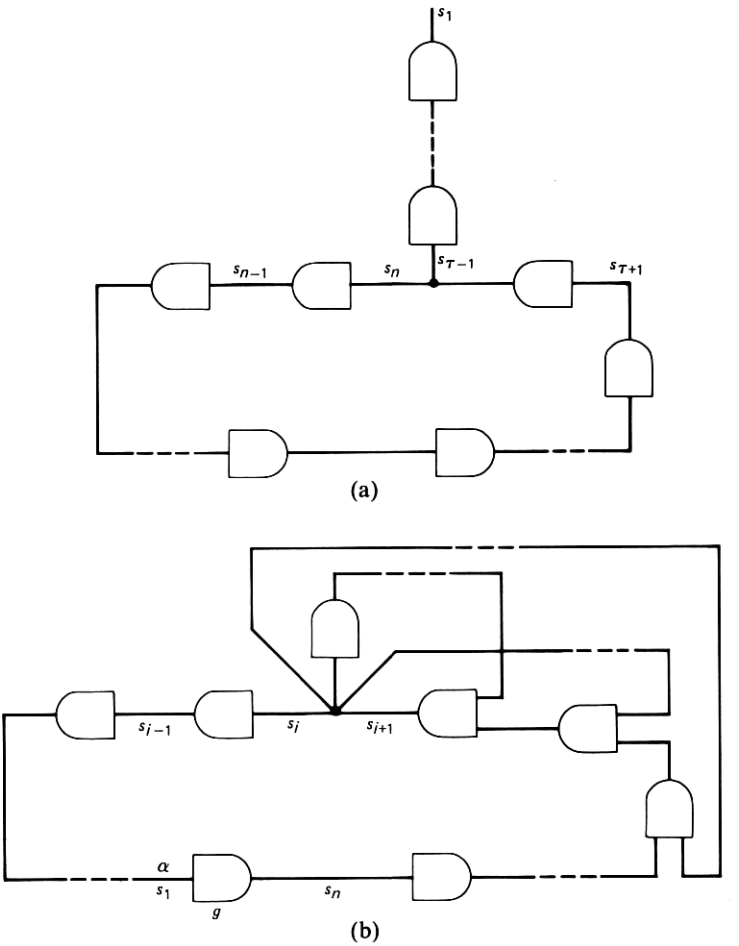

Fig. 7—Proof of Theorem 7. (a) Category (*ii*); (b) Category (*iii*).

Step 4. NOT gates are considered as lines and delay f/f's are considered as 1-input gates.

Theorem 8: *The above procedure yields the necessary and sufficient checkpoints to represent all the multiple faults in M which are detectable.*

Proof: Clearly, faults among the edges of Ω of Theorem 6 are undetectable and can be ignored. Let ϵ be a multiple fault defined over a set of edges of M^*, denoted by $A = \{\alpha_i\}$. Let $B = \{\beta_j\}$ be constructed from A by removing all elements of A which are dominated by some other elements of A. Then B is the largest subset of A such that no member of B is dominated by any member of B. Because any signal on a dominated edge will be blocked by the edges which dominate it, ϵ is equivalent to a multiple fault among B. Furthermore, since $\beta_i \in B$ does not dominate $\beta_j \in B$ for all $i \neq j$, $K(\beta_i)$ and $K(\beta_j)$ are disjoint. By Lemma 3, a multiple fault among B is equivalent to a multiple fault among the following collection of edges of M^*:$\Gamma = \cup_{\beta_i \in B} K(\beta_i)$. Since Γ is a subset of the collection of checkpoints W given by the above procedure, ϵ is equivalent to a multiple fault among W. This proves the sufficiency. The necessity follows from Theorems 5 and 6.

In comparison with the set of checkpoints obtained by applying Bossen and Hong's procedure to the combinational network C_M of Fig. 1, we see that we have removed from consideration the following edges: (i) all feedback lines represented by the vector **Y**; and (ii) all singular fanout branches.

Therefore, our work greatly simplifies fault analysis of cyclic logic networks.

It is important to point out that Definition 6 and Theorem 1 can be used to identify the singular edges.

IV. ASYNCHRONOUS SEQUENTIAL CIRCUITS

Having found a minimal checkpoint labeling procedure for synchronous sequential circuits with delay flip-flops as memory elements, we now consider asynchronous sequential circuit. The structure of an asynchronous sequential circuit can be represented as shown in Fig. 8.

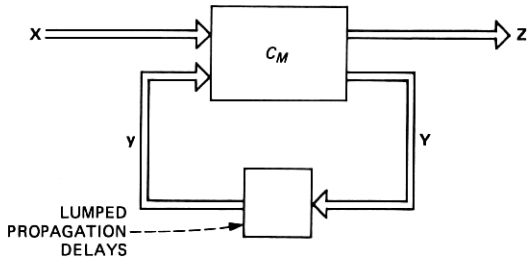

Fig. 8—Asynchronous sequential circuit.

It can be seen that the model is almost identical to the one shown in Fig. 1. The only difference is that the clocked delay flip-flops of Fig. 1 are now lumped propagation delays of the feedback lines. Because of this, one might conjecture that the checkpoint labeling procedure is applicable without modification to asynchronous sequential circuits. This conjecture is indeed true.

Consider Step 3 of the labeling procedure. It states that a delay flip-flop is considered as a 1-input gate. Under stuck-type fault assumption, this is equivalent to saying that a delay flip-flop is considered as an edge in the procedure. Therefore, we ascertain that the foregoing analysis carries over to an asynchronous case under the permanent stuck-at fault assumption.

V. SUMMARY AND DISCUSSION

In our analysis, we have developed a minimal checkpoint labeling procedure for squential circuits. This procedure is applicable to both synchronous sequential circuits with delay flip-flops as memory elements and asynchronous sequential circuits. Since most of the clocked flip-flops in use today, such as *JK f/f*, latch *f/f*, etc., are actually made of asynchronous sequential circuits, the procedure is applicable to any synchronous sequential circuits whose memory elements are either delay flip-flops or the aforementioned clocked flip-flops.

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