THE BELL SYSTEM TECHNICAL JOURNAL
Vol. 61, No. 3, March 1982
Printed in U.S.A.

A General Class of Zero- or Minimum-Delay Fractional Rate Change Circuits

By S. V. AHAMED

(Manuscript received July 14, 1981)

Rate changing occurs whenever sequences of data undergo transformations in rate without undergoing a change in the order of sequence. When the ratio of transformation is not an integer, fractional rate changes are necessary. These are generally, a prerequisite for the time-compression multiplexing mode of data transmission. Zero or minimal delay is a desirable characteristic, for example, in reducing the annoyance from the far-end echo whenever voice is encoded and transmitted. Conventional fractional rate changing entails an inherent delay in the rate change circuits. Segmenting shift registers reduces the delay of the last bit without completely eliminating it, unless the shift-register length is reduced to one bit. In this paper, a method of partitioning the shift registers by logarithmic counts is developed to reduce the complexity of the gating and the counting circuits. Zero last-bit delays are attainable in all cases where the rate increase is greater than two or, conversely, the rate reduction is less than half. For the remaining cases, the compromise between circuit complexity and the last-bit delay is outlined.

I. INTRODUCTION

Under the time-compression mode of data transmission, the round trip delay time is critically important in controlling the echo from the far end, as well as the direct transmission delay. The excess delay of the last bit, in changing the rate from the primary (or terminal) rate to the secondary [or time-compression multiplexing (*TCM*)] rate and vice versa, which can be a significant fraction of the overall delay, in any particular block is reduced to zero by the circuits presented in this paper. In general, it is shown that the last-bit delay can be reduced to zero whenever the required rate change is more than two, while increasing the number of shift registers (SRs) and the gating functions

logarithmically. Further, the gating signals are shown to be derived as combinations of logarithmic counts of the primary (terminal) clock or those of the secondary clock. The general principle of fractional rate changing is extended to fractional rate collating circuits. The compromise between zero last-bit delay and the complexity of the circuit for fractional rate changing between half and one is delineated.

In 1971, a general class of rate change circuits was presented[1] for use in the magnetic domain technology. The constraint on the design of such circuits was that all the individual bits of information (domains) be propagated by one period (the physical spacing between one pattern to the next in domain technology) in one clock cycle of the rotating magnetic field. To conform to this design requirement in domain technology, the number of patterns in different paths of the rate change circuit were arranged to follow a geometric progression. The topological arrangement of SRs and gates, if operated in conventional semiconductor technology, will perform satisfactorily. However, it imposes two unnecessary restrictions: (*i*) this version in semiconductor technology ignores the capability of SRs to shift-in (SI) at one rate and shift-out (SO) at another rate, and (*ii*) fractional rate change is a two-step procedure, thus, demanding a large number of SR locations. The essential feature retained in these circuits is that the delay between the reception of the last bit of block of data and its transmission would be zero. Zero last-bit delay fractional rate change is not possible with a conventional arrangement* of SRs, unless the number of independent registers is increased to the number of bits in the block, thus, demanding extremely complex arrangements of gating and shifting functions.

In this paper, we present circuits that retain the zero last-bit delay characteristics and the simplicity of the gating function *without* linearly increasing the number of SRs, or the complexity of gating and shifting functions. Even though most of the emphasis is placed on fractional rate changing, integral rate changing is equally easily accomplished by the circuit arrangements presented here.

II. ZERO-DELAY FRACTIONAL RATE INCREASING

For the cases presented in this section, let the proportional rate increase be greater than two. Cases where the rate change is between one and two are discussed in Section IV.

2.1 Fractional rate between two and three

Consider a block 42 bits long where the rate change ratio is 3:7. Forty-two, being a multiple of 3 and 7, generates a situation where one

* Conventional arrangement consists of having one or more SRs in which data are sequentially shifted in at the incoming rate and shifted out at the output rate.

block of data 42 bits long experiences the same set of gating functions* that was performed for the last 42-bit data block or the next 42-bit data block. Next, consider an arrangement of 7 SRs shown in Fig. 1. Data are received uniformly one bit ever t seconds. Data are generated in a burst of 42 bits. Burst repeats every $42t$ seconds and lasts for $18t$ seconds. Effective rate change is 3:7 during the burst. Here, the SRs follow a sequence 2^0, 2^1, 2^2, 2^3, 2^4, $(42 - 2^5)$. The signals C and C' are clock signals at t and t', where t denotes the primary (terminal) clock and t' denotes the secondary clock durations in seconds. The signals a_6, a_5, —, a_1, a_0 are generated every $42t$ seconds and last for $(42 - 2^5)$, 2^4, —, —, 2^0, 1 t seconds, etc. Similarly, b_6 through b_0 are generated by identical circuits operated at the secondary clock t' but delayed for the $24t$ of the $42t$ seconds cycle time. The operation of the SRs is summarized in Table I.

It can be seen that all SRs have a positive duration between the finish of the SI and start of SO (see column 6, Table I). As proved in Appendix A, the kth SR experiences a delay of:

$$d_k = 2^{k-1}t - 2^k t' \text{ seconds.} \tag{1}$$

If t is defined as $>2t'$, d_k is always positive. In the example presented here, the delays for SRs 1 to 5 can be equated to d_k in (1) by substituting $t' = \frac{3}{7}t$ both in (1) and in the sixth column of Table I. The delay of the 42nd bit is zero since the ending instants of received and the transmitted bits coincide at the end of the block.

The four distinct characteristics of the circuit configuration presented in this section can, thus, be summarized as follows:

(*i*) The SI-SO duration is always positive for all SRs.

(*ii*) The gating signals a_6 through a_0 and b_6 through b_0 are generated simply by identical binary (in cases where the fractional rate change ratio $r > 2$ and < 3) counters each being driven by a primary (terminal) clock and by a secondary clock, respectively.

(*iii*) The delay in the circuit as measured by the difference between the end of arrival of the last data bit and the end of transmission of that same data bit at the higher clock is zero.†

(*iv*) The number of SR locations required is always the bit length of the block reduced by one.

2.2 *Fractional rate increasing between three and four*

In Section 2.1, the number of locations in the SR progresses as 2^0, 2^1, $\cdots$, 2^i, $(N - 2^{i+1})$, depending on the size of the block (N).

---

* Systems considerations usually require such a repetitive set of functions for continuous operations.

† It is possible to advance the operation by an extra $(t - t')$ second by advancing t' by this period and loading the last bit into an SR. But, we have ignored this situation as it needs only a trivial modification of the circuits shown here.

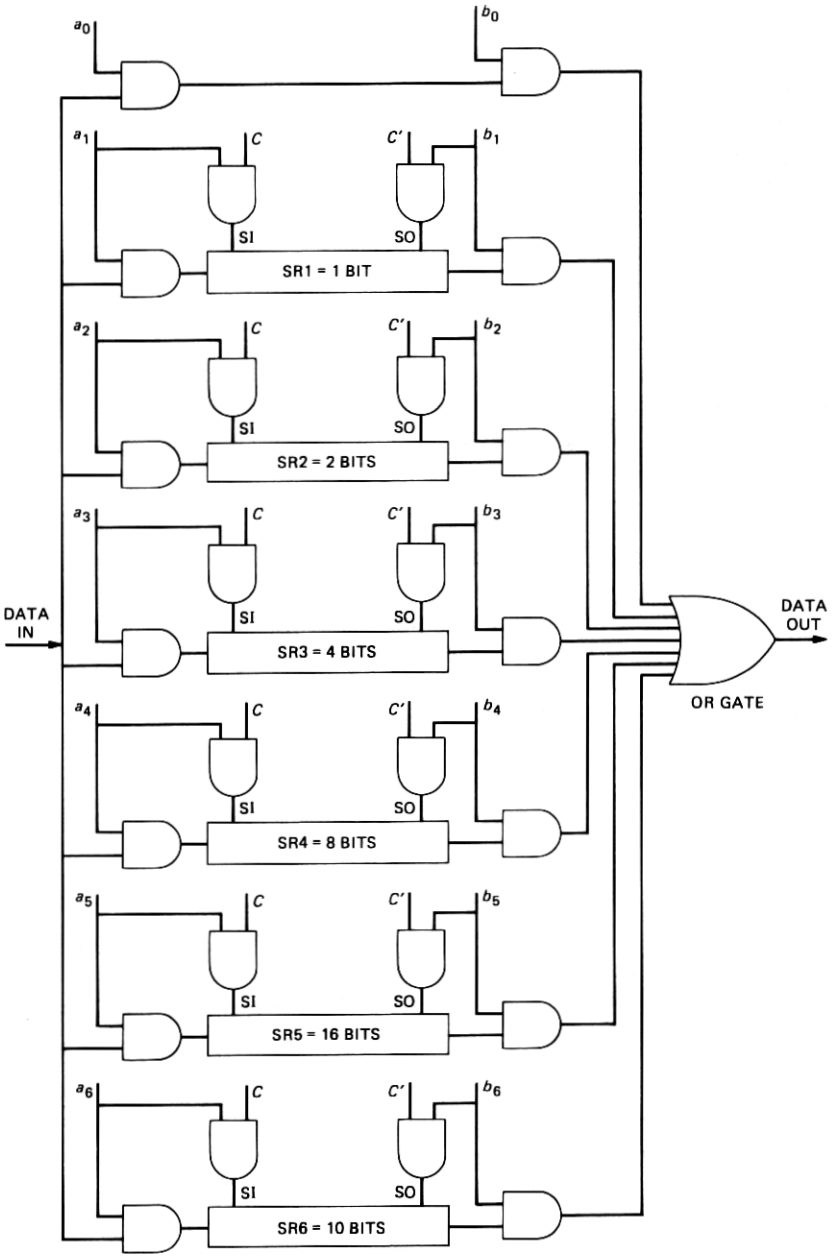


Fig. 1—Shift register arrangement for a 42-bit data block.

Table I—Details of 42-bit block—3:7 rate increasing circuit

SR	Start of SI (a)	Finish of SI (b)	Start of SO (c)	End of SO (d)	SI-SO Interval ($c - b$)*	On Time	
						SI	SO
SR6	0	$10t$	$\Delta = 24t$	$\Delta + 10t'$	$14t$	$10t$	$10t'$
SR5	$10t$	$26t$	$\Delta + 10t'$	$\Delta + 26t'$	$10t' - 2t$	$16t$	$16t'$
SR4	$26t$	$34t$	$\Delta + 26t'$	$\Delta + 34t'$	$26t' - 10t$	$8t$	$8t'$
SR3	$34t$	$38t$	$\Delta + 34t'$	$\Delta + 38t'$	$34t' - 14t$	$4t$	$4t'$
SR2	$38t$	$40t$	$\Delta + 38t'$	$\Delta + 40t'$	$38t' - 16t$	$2t$	$2t'$
SR1	$40t$	$41t$	$\Delta + 40t'$	$\Delta + 41t'$	$40t' - 17t$	t	t'
Signal	Start	Finish	Signal	Start	Finish	Finish b_0 −Finish a_0	
a_0	$41t$	$42t$	b_0	$\Delta + 41t'$	$\Delta + 42t'$	Zero	

* This interval can be always verified as being positive at $t = 7/3 \times t'$.

Notes:

1. Shift-in takes place during one clock cycle at t.
2. Shift-out takes place during one clock cycle at t'. For maintaining zero delay, it is assumed that the end of the 42nd clock cycle at t coincides with the end of the 98th cycle at t'. This condition ascertains that a_0 and b_0 end simultaneously at the end of $42t$ or $98t'$.

When the fractional rate change ratio r is between 3 and 4, all the essential characteristics of this class of rate change circuit may be maintained by changing the numbered locations in the SRs to follow the progression

$$3^0, 3^1, 3^2, \cdots, 3^i, \left(N - 1 - \sum_{i=0}^{i} 3^i\right).$$

Consider a rate change ratio of 7:23 with a 161-bit block. The SR progression becomes a 1-, 3-, 9-, 27-, 81-, 39-bit position constituting 160 locations. The six SR circuit is shown in Fig. 2, and the shifting times are tabulated in Table II.

The generalization of this arrangement for an N-bit block with any fractional rate change r is presented in Appendix B.

III. FRACTIONAL RATE DECREASING CIRCUITS

When the decrease in rate equals or becomes less than 0.5, we have a situation where the circuit arrangement presented in Section II can be used to decrease the rate. Two changes however, are necessary: (*i*) the direct transmission of data between a_0 and b_0 (Figs. 1 or 2 have to be replaced by a flip-flop to load and hold the first data bit and, (*ii*) the signals $a_0, \cdots, a_n$ and $b_0, \cdots, b_n$ must start at the beginning of the block instead of ending at the end of the block.

Consider a data block 680 bits long where the desired rate change ratio is 0.425. The minimum size of the data block is 680, being the least common multiple of 17 and 40, even though equally satisfactory arrangements can be conceived for all blocks that are multiples of 680 bits long. Once again the SR sizes (Fig. 3) can be written down as 1, 2^0,

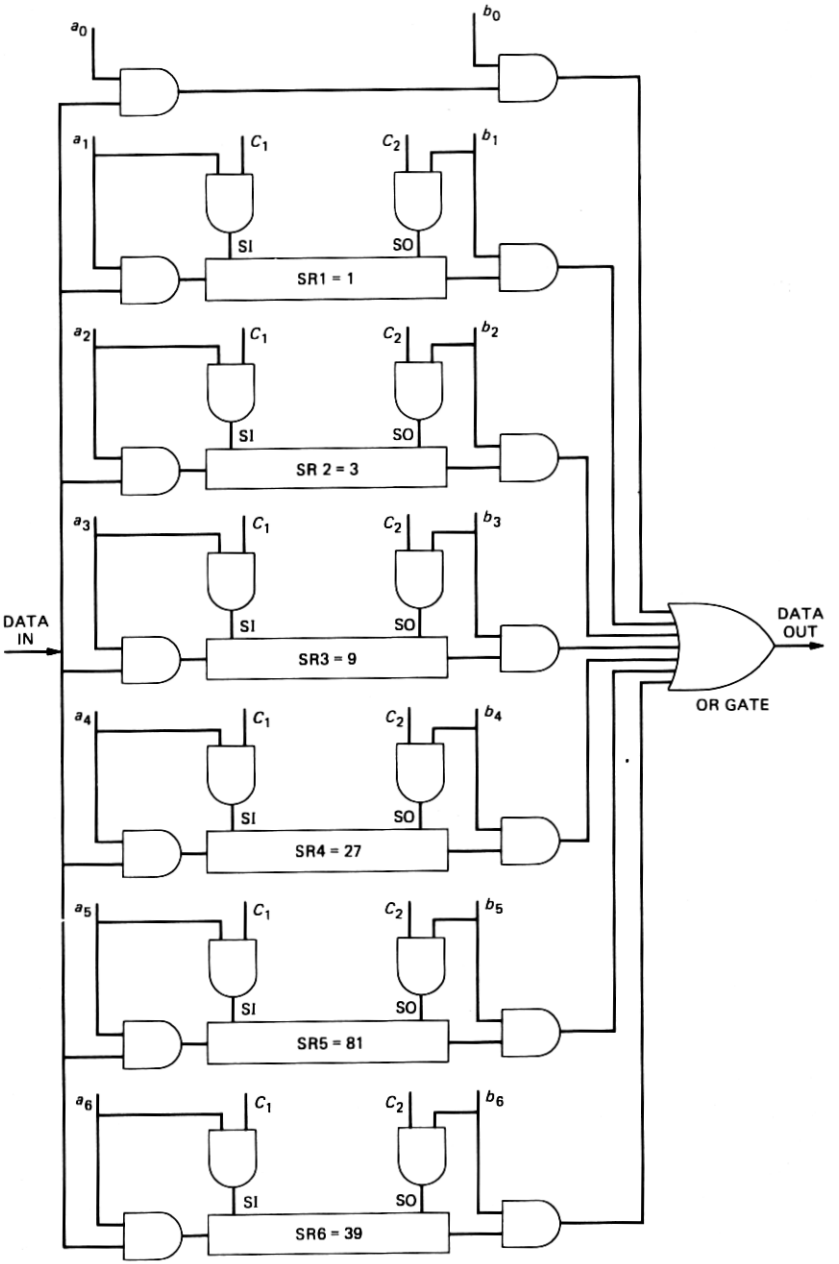


Fig. 2—Shift register arrangement for a 161-bit block. Rate change ratio is 7:23.

Table II—Details of 161-bit block—7:23 rate increasing circuit

SR	Start of SI (a)	Finish of SI (b)	Start of SO (c)	Finish of SO (d)	SI-SO Interval ($c - b$)*	On Time	
						SI	SO
SR6	0	$39t$	$\Delta = 112t$	$\Delta + 39t'$	$73t$	$39t$	$39t'$
SR5	$39t$	$120t$	$\Delta + 39t'$	$\Delta + 120t'$	$39t' - 8t$	$81t$	$81t'$
SR4	$120t$	$147t$	$\Delta + 120t'$	$\Delta + 147t'$	$120t' - 35t$	$27t$	$27t'$
SR3	$147t$	$156t$	$\Delta + 147t'$	$\Delta + 156t'$	$147t' - 44t$	$9t$	$9t'$
SR2	$156t$	$159t$	$\Delta + 156t'$	$\Delta + 159t'$	$156t' - 47t$	$3t$	$3t'$
SR1	$159t$	$160t$	$\Delta + 159'$	$\Delta + 160t'$	$159t' - 48t$	t	t'
Signal	Start	Finish	Signal	Start	Finish	Finish b_0 Finish a_0	
a_0	$160t$	$161t$	b_0	$\Delta \pm 160t$	$\Delta + 161t'$	Zero	

* This number can be verified as always being positive when $t = 23/7 \times t'$.

2^2, 2^3, 2^4, 2^5, 2^6, 2^7, 2^8, $(680 - 2^9)$. The clocks C and C' are in the proportion of 17:40. The signals a_0, $a_1 \cdots a_8$, a_9 and b_0, $b_1 \cdots b_8$, b_9 are generated for $(1, 2^0, 2^1, \cdots, 2^8, 168)t$ and $(1, 2^0, 2^1, \cdots, 2^8, 168)t'$ seconds,* starting at the beginning of the block. The starting instants of these signals are $(0, 1, 2^0, 2^1, \cdots, 2^8)t$ seconds and $(0, 1, 2^0, 2^1, \cdots, 2^8)t'$ seconds from the starting position of the block for a_0, a_1, $\cdots$, a_9 and b_0, b_1, $\cdots$, b_9, respectively. The circuit arrangement is presented in Fig. 3, and the gating times are tabulated in Table III. The principle may be extended to an N-bit block whose effective rate reduction is r, and a circuit configuration similar to that shown in Fig. 6 may be derived.

IV. FRACTIONAL RATE CHANGES BETWEEN ONE AND TWO

A zero-delay circuit configuration for these rate changes may also be derived by extending the general principles of Sections II and III. However, the number of SRs increases ($1^i = 1$) to the number of bits in the block, and the circuit configuration becomes trivial. On the other hand, it is possible to compromise the zero delay requirement slightly and obtain the advantages of reducing the number of SRs and simplifying the gating functions. These considerations are discussed next.

4.1 Rate increasing ratios between one and two

Consider a data block 84 bits long. If the desired rate increase is 4:7, one can arrange a circuit shown in Fig. 4a that is consistent with the arrangement shown in Fig. 1. However, if SR7 is emptied after a delay of $36t$† seconds, then SR6 would not have completely shifted in before it becomes necessary to shift it out, and it is here that the compromise becomes necessary. If the shifting out sequence is now delayed by a

* Durations t and t' are cycle times at faster (TCM) and slower (terminal) clocks, respectively.

† The duration t is a clock cycle time at the terminal (primary) rate and $36 = 84(1\text{-}4/7)$.

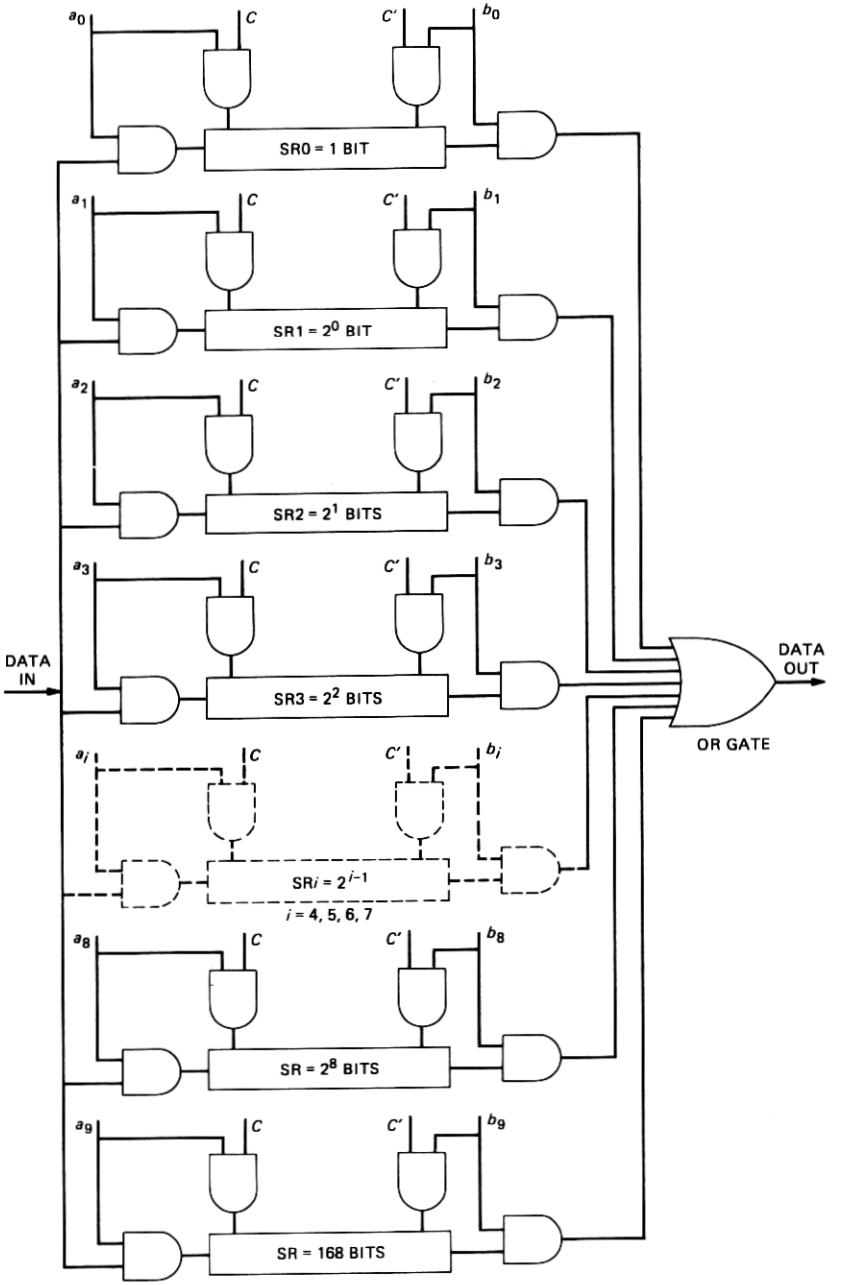


Fig. 3—Rate-reducing circuit for a 680-bit data block. Rate change ratio is 17:40.

Table III—Details of 680-bit block—40:17 rate decreasing circuit

SR	Start of SI (a)	Finish of SI (b)	Start of SO (c)	Finish of SO (d)	SI-SO Interval	On Time	
						SI	SO
SR_0	0	0*	0*	t'	0	0*	t'
SR_1	t	$2t$	t'	$2t'$	$t' - t$	t	t'
SR_2	$2 \times t$	$4 \times t$	$2t'$	$4t'$	$2(t' - t)$	$2t$	$2t'$
—	—	—	—	—	—	—	—
SR_i	$2^{i-1} \times t$	$2^i \times t$	$2^{i-1}t'$	$2^it'$	$2^{i-1}(t' - t)$	$2^{i-1}t$	$2^{i-1}t'$
—	—	—	—	—	—	—	—
SR_8	$2^7 \times t$	$2^8 \times t$	$2^7 \times t'$	$2^8t'$	$2^7(t' - t)$	2^7t	$2^7t'$
SR_9	$2^8 \times t$	680	$2^8t'$	$680t'$	$2^8(t' - t)$	$168t$	$168t'$

* Indicates shift-in time of SR0. This is $\ll t$ or t' and can be used effectively to mark the beginning and end of a 680-bit data block.

minimal amount to just accommodate the binding requirement on this SR, then it can be seen that the delay should be $4.571t$* seconds. Further, this minimal delay depends on the length of the block, the fractional rate change ratio r, and the SR position in the hierarchy of registers. The generalized calculations for the delays are presented in Appendix C.

For the particular case presented in Fig. 4 for the 84-bit block, it is now possible to compute the gating times and the delays for the overall functioning of the circuit. These results are tabulated in Table IV, and Fig. 4b depicts the timings. The minimum delay of $4.571t$ seconds plays a central role in the operation of the circuit. This delay being essential for the functioning of SR6 appropriately, gets fragmented into $2.286t$, $1.143t$, $0.571t$, $0.286t$, $0.143t$, $0.071t$ and, finally, $0.071t$ for SR6 through SR0 to add up to the net delay of $4.571t$ seconds for the circuit. Once this delay is generated by an additional circuitry, the functioning of the gates at the higher clock rate can be normal binary counters, delayed by this appropriate amount. This feature eliminates the need for complicated gating circuits, even when the fractional rate increasing is less than two.

4.2 *Compromise between circuit complexity and minimum delay*

It can be seen that the entire delay of $4.571t$ seconds can be cut into half by partitioning SR6 into two sixteen-bit registers. In this case, SR7 is delayed by $2.286t$ and the SI finish coincides with the SO start for SR5, and the delay reappears as the summation $1.143t$, $0.571t$, $0.286t$, $0.143t$, $0.071t$, and $0.071t$ for the remaining SRs at the end of the block. If one extends this reasoning indefinitely, then all the SRs become partitioned to single-bit registers for zero delay. It is at this stage that the compromise between SR complexity and minimum delay becomes obvious. All the same, these circuits outperform conventional circuit

* $4.571 = (20 + 32) - (36 + 20 \times 1/7)$.

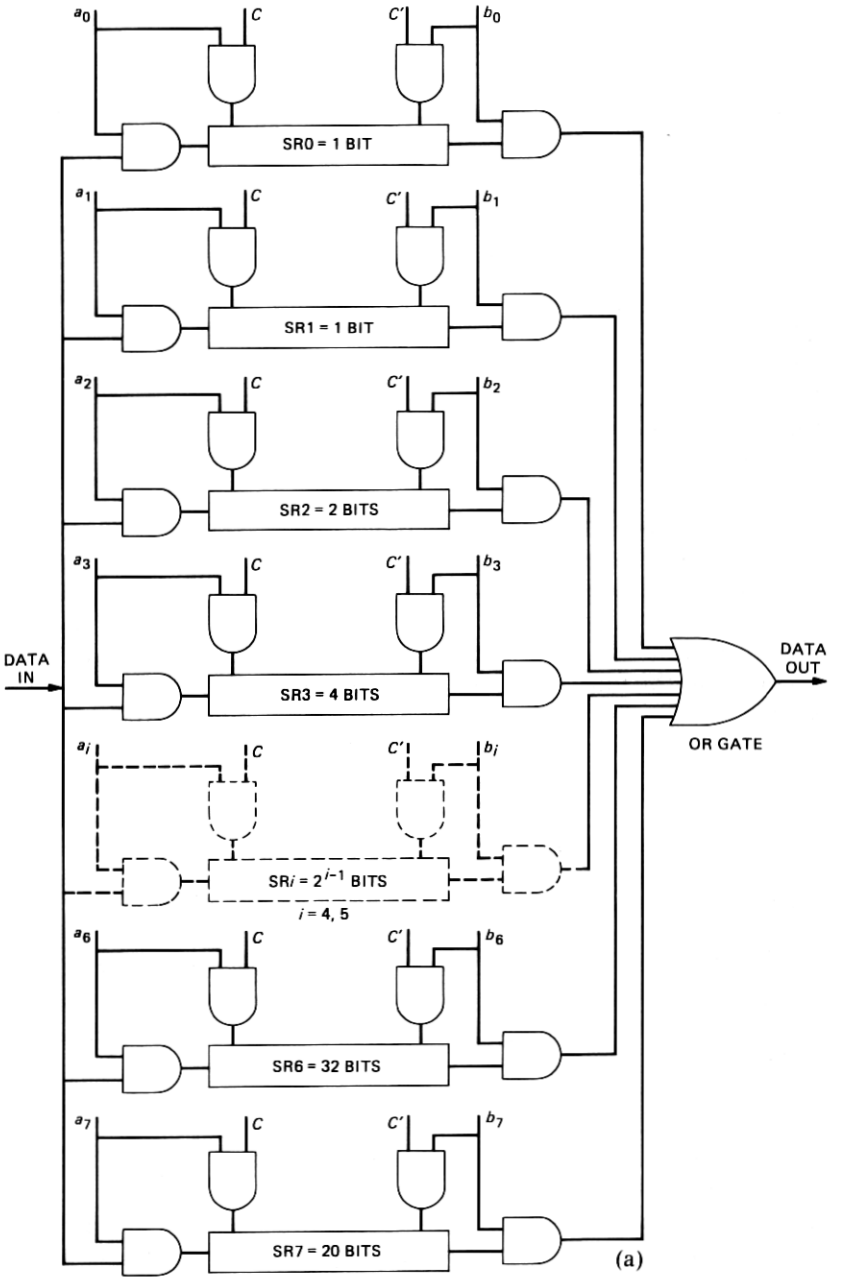
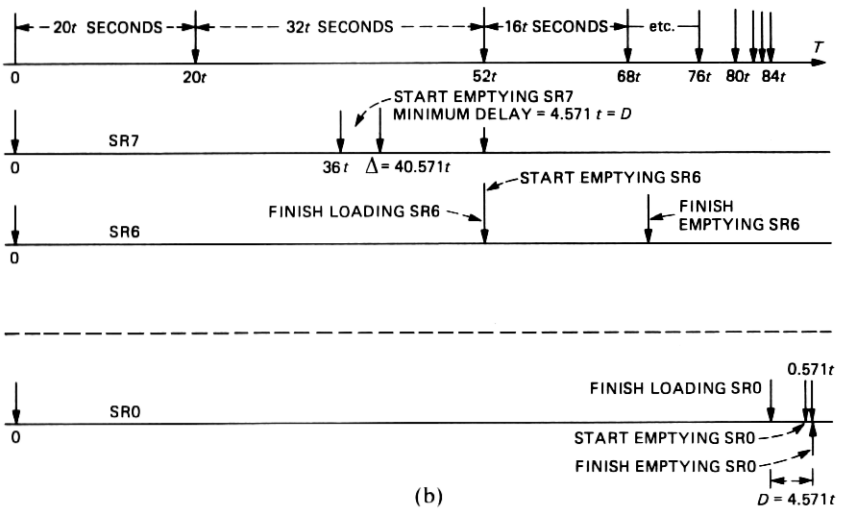


Fig. 4a—Rate-increasing circuit for an 84-bit block. Rate change ratio is 4:7.

Table IV—Details of 84-bit block—4:7 rate increasing circuit

SR	Start of SI (a)	Finish of SI (b)	Start of SO (c)	Finish of SO (d)	SI-SO Interval $e = (c - b)$	On Time	
						SI	SO
SR7	0	$20t$	$\Delta = 40.571t$	$\Delta + 20t'$	$20.571t$	$20t$	$20t'$
SR6	$20t$	$52t$	$\Delta + 20t'$	$\Delta + 52t'$	0	$32t$	$32t'$
SR5	$52t$	$68t$	$\Delta + 52t'$	$\Delta + 68t'$	$2.285t$	$16t$	$16t'$
SR4	$68t$	$76t$	$\Delta + 68t'$	$\Delta + 76t'$	$3.429t$	$8t$	$8t'$
SR3	$76t$	$80t$	$\Delta + 76t'$	$\Delta + 80t'$	$4.000t$	$4t$	$4t'$
SR2	$80t$	$82t$	$\Delta + 80t'$	$\Delta + 82t'$	$4.286t$	$2t$	$2t'$
SR1	$82t$	$83t$	$\Delta + 82t'$	$\Delta + 83t'$	$4.429t$	t	t'
SR0	$83t$	$84t$	$\Delta + 83t'$	$\Delta + 84t'$	$4.571t$*	t	t'

* Minimum delay = $4.571t$ and $\Delta = (36 + 4.571)t$. In the case of SR0, $(c = d - b)$ to prove that the end of the block at the faster rate ends as late as the minimum delay imposed upon shifting the first data bit out of SR7. (See Fig. 4a.)



(b)

Fig. 4b—Timing diagram for an 84-bit data block in a 4:7 rate-increasing circuit configuration.

arrangements because the delay time of 7 SRs, each 12 bits long, would be a $12t$ second compared to $4.571t$ for the arrangement suggested here with 8 SRs, or of $2.286t$ with 9 SRs. The extent of gain depends on the length of the block and the rate change ratio. The circuit complexity has to be chosen by a designer depending on the particular requirements.

V. FRACTIONAL RATE COLLATING CIRCUITS

To illustrate the example of fractional rate collating, consider 17 independent data lines each carrying independent data uniformly at a primary rate of one bit every t seconds. The 18th line also carries

binary data but a tertiary rate of one bit every t_1 seconds. Let the block time be T seconds, corresponding to 7 bits at the primary rate t, and 4 bits at the tertiary rate t_1 (i.e., $7t = 4t_1$). The collating circuit will be able to present the first bit of the first channel followed by the first bit of the second channel etc., until the 17th channel, then the second bit of the first channel, followed by the second bit of the second channel, etc., and so on, until the 7th bit of the 17th channel. The final section of the output data block would be the four bits of the 18th channel. The output data rate will be at a uniform secondary bit rate of t' (i.e., $T/123$).

A collating circuit to perform this function is presented in Fig. 5a. Data arrive uniformly every t seconds on 17 channels, $C_1, \cdots, C_{17}$, and t_1 seconds on channel C_{18} with $7t = 4t_1$ data are transformed to 123-bit blocks. The first bit of C_1 is collated with first bit of C_2, etc., until C_{17} the second bit of C_1 is collated with the second bit of $C_2, \cdots$, etc., and the last four bits of the block are bits received on C_{18}. The output rate is t' with $123t' = 7t = 4t_1 = T$. The first bits of all the 17 channels are collated into SR1, the second bits of all the 17 channels are collated into SR2, etc. The 17 blocks of SI signals $m_1, \cdots, m_{17}; m_{18}, \cdots, m_{34}, \cdots$, etc., $\cdots, m_{119}$ are generated by ANDing signals $t, 2t, 3t, \cdots, 7t$, with t'—the signal t being long enough to accommodate 17 full cycles of t'. The SO signals $n_1, \cdots, n_{17}; n_{18}, \cdots, n_{34}; \cdots$, etc., $\cdots, n_{123}$, are generated by delaying the secondary block t' by 21 (i.e., 17 + 4) full cycles of the secondary clock t'. The SI signals are in two classes: $m_1, \cdots, m_{119}$ are generated as indicated earlier, and $m_{120}, \cdots, m_{123}$ are generated at the tertiary rate of one signal every t_1 seconds. The signal timings are shown in Fig. 5a. Shift-in signals $m_1, \cdots, m_{119}$ are generated by ANDing t with 17 of t'. Signals $m_{120}, \cdots, m_{123}$ are generated by ANDing t with one of t'. Shift-out signals $n_1, \cdots, n_{123}$ are generated at t' after delaying clock by $21t'$ from the start of the block. It is interesting to note that SR1 has a delay time of $4t'$ seconds between SI and SO. However, this time gradually diminishes by $\frac{4}{7}t'$ as one progresses through SR2 to SR7, with SR7 itself shifting out as soon as it is shifted in. (See Fig. 5b.) It is this limit that specifies the minimum delay of the collating circuits.

Other collating circuits can be generated by the principles indicated, and the generalization of such circuits is also possible but omitted here.

VI. DISCUSSION OF RATE CHANGING AND COLLATING CIRCUITS

Conventional SR arrangements lead to a delay in the transmission of data, unless the size of the register diminishes to one. For circuits described here, there is a geometric progression in the sizes of the registers and in the logarithmic number of registers. The base of the

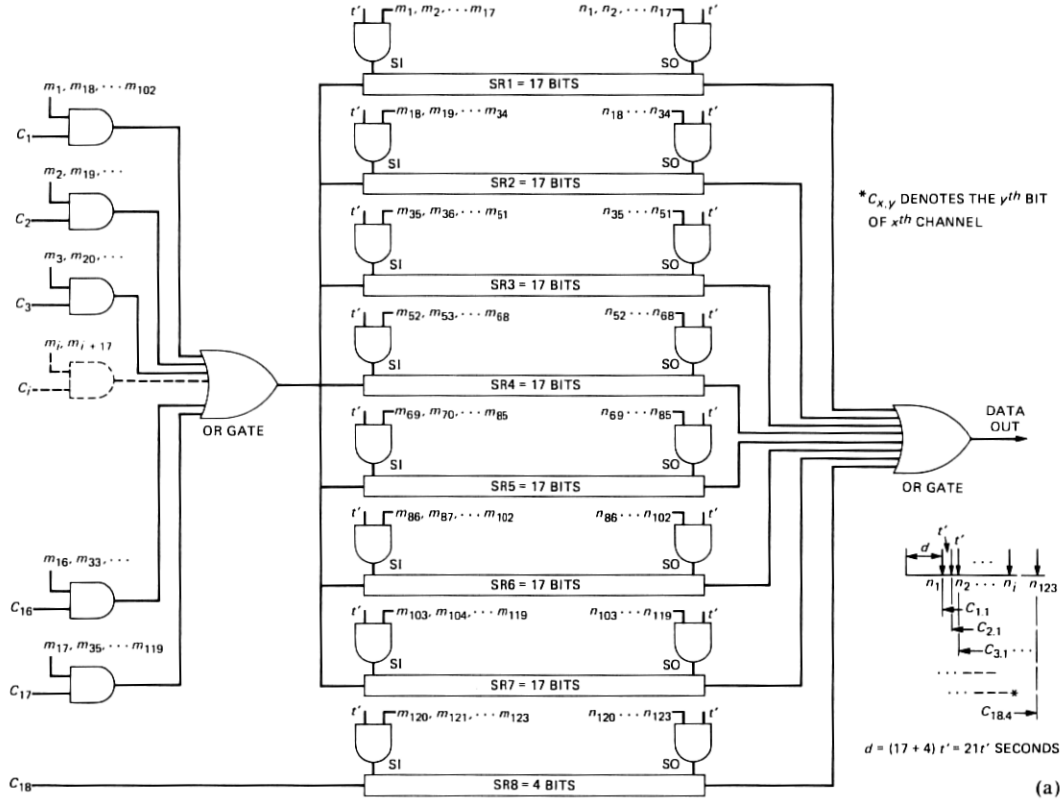


Fig. 5a—Fractional rate collating circuit for a 123-bit data block.

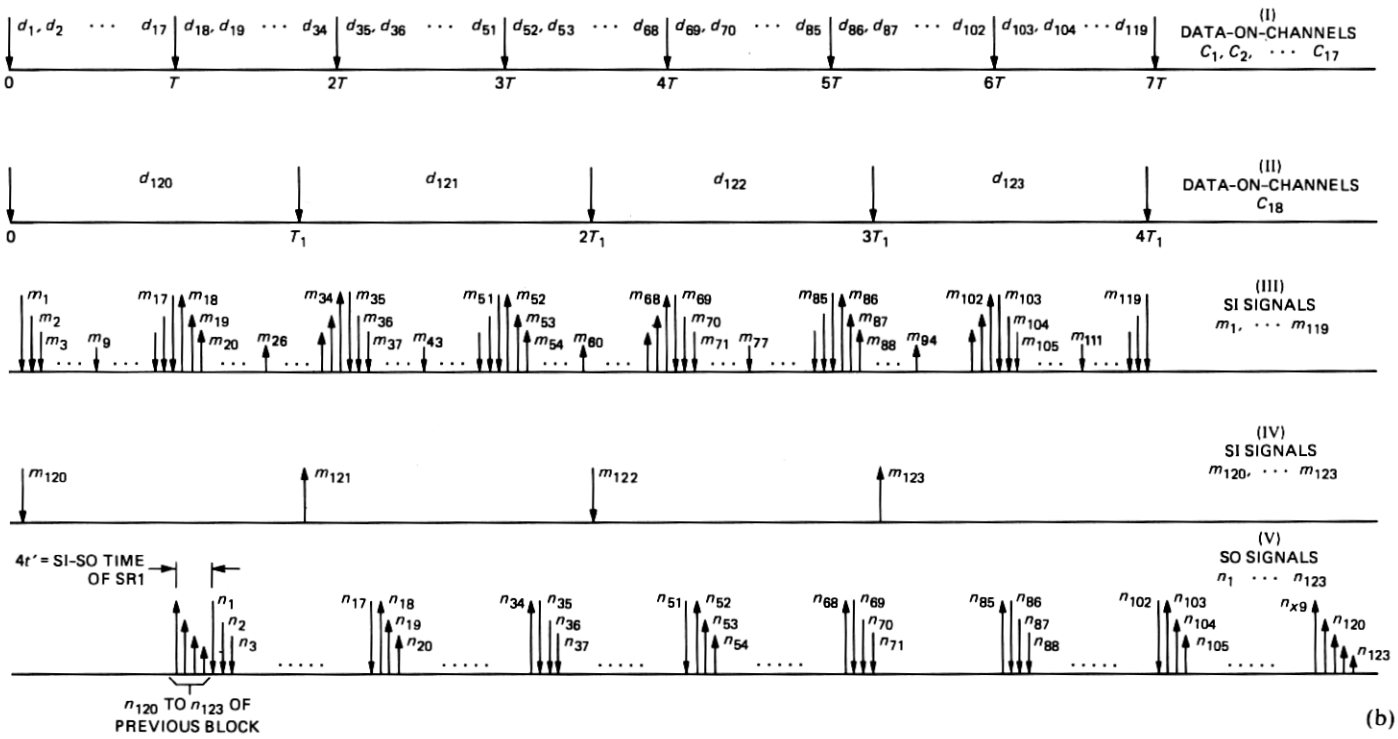


Fig. 5b—Timing diagram for circuit shown in Fig. 5a.

geometric series is chosen to be an integer just under the fractional rate change ratio. The time for shifting out any particular register in the series is made to overlap with the time for shifting in of the next lower-sized register of the series. Two definite advantages arise by this arrangement of SRs: (*i*) the number of registers can be reduced exponentially (see Appendices A through C) for a given delay, and (*ii*) the gating can be performed very simply by counters that block out exponentially varying sizes of time at the primary or secondary clocks. These features are absent in the conventional arrangement of registers.

When the fractional rate change falls between one and two, the arrangement suggested still outperforms conventional arrangement as far as delay is concerned for a given number of SRs. In a limit, the two systems converge to a minimum delay with one-bit registers. The compromise between circuit complexity and minimum delay is offered to the designer.

Collating circuits also retain some features of minimizing the delay. Consider the circuit presented in Section V. Here, conventional arrangements would have two extremes of implementation. First, consider 17-seven and 1-four bit SRs, all shifting in and then shifting out. The delay is obviously $123t'$ since all the registers have to be shifted in before shifting out. Second, consider 123 one-bit registers. With an immense amount of complexity in gating and clocking, one-bit delay may be achieved. The first arrangement does not compare favorably, from the delay consideration, with the configuration of the 18 registers—the delay being $123t'$ versus $21t'$. The second arrangement offers an advantage in delay time (t' versus $21t'$) but at an enormous complexity (123 timing circuits and SRs versus 18 such circuits). As indicated in Section 4.2, a compromise between circuit complexity and minimum delay also exists for collating circuits.

VII. CONCLUSIONS

Fractional rate changing may be achieved with zero last-bit delay *without* increasing the number of SRs to the number in the bits in the block. In the circuit arrangement presented, the number of SRs increases logarithmically. The base for the logarithmic increase is the highest integer just below the rate change ratio. When the rate change ratio is between one and two, the simplicity of the SR arrangement and gating may be retained by accepting a slight last-bit delay in the circuit. Such an arrangement, even though not reducing the last-bit delay to zero, still outperforms a conventional arrangement by a large margin. The exact compromise between complexity and delay is left to the circuit designer.

Fractional rate collating of data blocks have some of the advantages so far as the simplicity of SR arrangement and gating is concerned.

VIII. ACKNOWLEDGMENT

The author thanks J. T. Peoples for an exacting review of the derivations in the appendices.

APPENDIX A

Shift Register Delays

Consider an N ($>2^{j-1}$ and $<2^j$) bit block in which a rate change of r (≥ 2 and <3) is being accomplished. The arrangement of a circuit with j SRs consists of $2^0, 2^1, \cdots, 2^{j-2}, (N - 2^{j-1})$ bits each. The size of the kth ($k < j - 1$) SR being 2^{k-1} finishes at an instant of:

$$d_i = \left(N - 1 - \sum_{i=0}^{i=k-2} 2^i\right)t \text{ seconds.}^* \tag{2}$$

Similarly, the start of the SO of the kth SR does not take place until an instant

$$d_o = N(t - t') + \left(N - 1 - \sum_{i=0}^{i=k-1} 2^i\right)t' \text{ seconds.} \tag{3}$$

The duration between the instant at which SO starts and the instant at which SI ends can be obtained by subtracting (2) from (3) leading to

$$d_k = 2^{k-1}t - 2^k t' \text{ seconds,} \tag{4}$$

since

$$2^k = 1 + \sum_{i=0}^{i=k-1} 2^i. \tag{5}$$

For this Appendix, by definition[†] we have $t \geq 2t'$ and d_k always remains positive.

APPENDIX B

Generalized Fractional Rate Increasing Circuit

Let the rate of an N-bit block be increased by a fractional rate of r. The general configuration of the circuit is shown in Fig. 6. The number j of SRs is chosen to satisfy the condition that:

$$\sum_0^{j-1} r_1^i < N - 1 \leq \sum_0^j r_1^i, \tag{6}$$

where r_1 is an integer just less than r. The first

$$N - 1 - \sum r_1^{j+1}$$

---

* In eq. (2), t corresponds to the duration of a clock cycle at the terminal rate and t' corresponds to the duration at the burst rate. The origin of time is chosen to coincide with the start of the block.

† The fractional change in rate is ≥ 2.

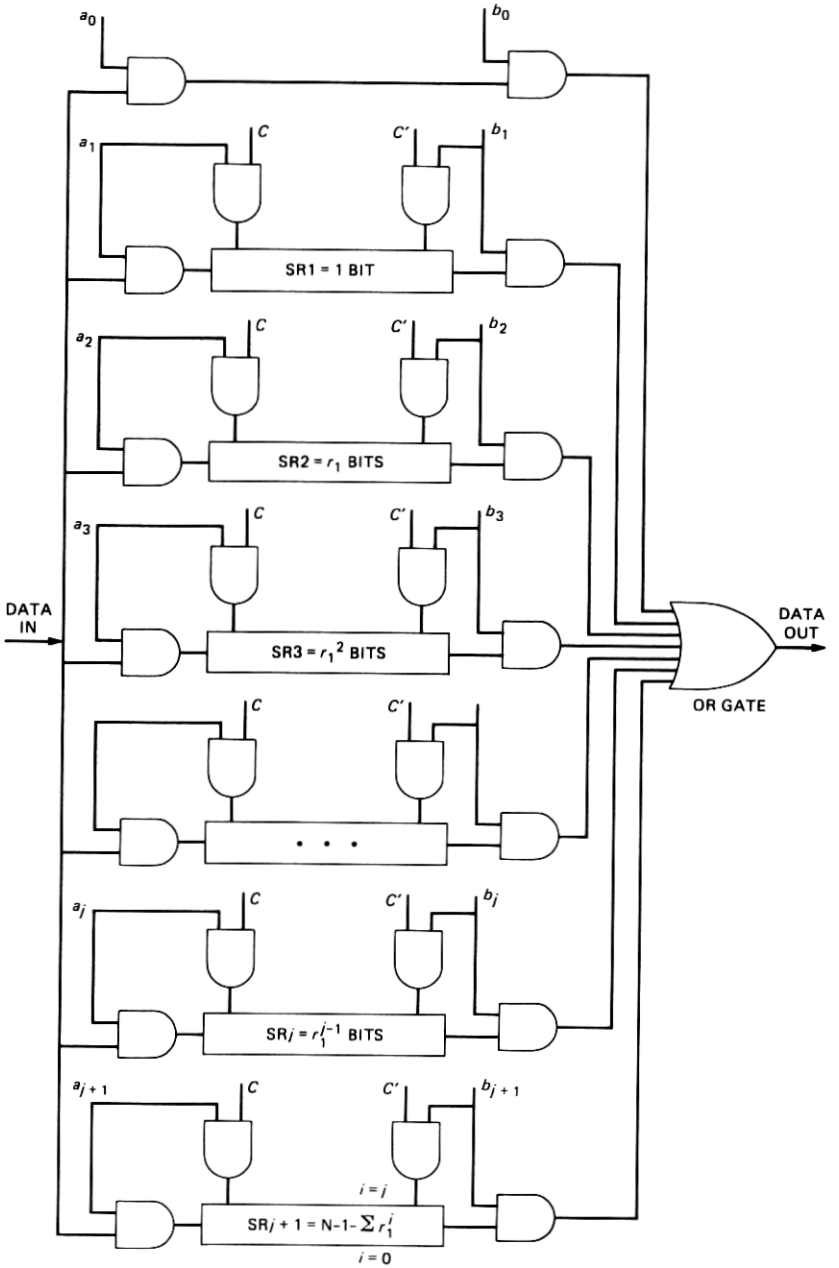


Fig. 6—Generalized fractional rate change circuit.

bits of the block are channeled into SR_{j+1} and the rest r_1^j bits into SR_j, etc. Now consider the kth SR, r_1^{k-1} bits long. The ending instant of SI for this register takes place at:

$$d_i = \left(N - 1 - \sum_{i=0}^{i=k-2} r_1^i\right)t \text{ seconds}, \tag{7}$$

where t denotes the duration at the primary clock and the start of the so time takes place at an instant:

$$d_o = N(t - t') + \left(N - 1 \sum_{i=0}^{i=k-1} r_1^i\right)t' \text{ seconds}. \tag{8}$$

The duration between the instant at which the SO starts and the instant at which the SI ends is given by

$$\begin{aligned} d_{ol} &= t - t' + \sum_{i=0}^{i=k-2} r_1^i t - \sum_{i=0}^{i=k-1} r_1^i t' \\ &= \left(1 + \sum_{i=0}^{k-2} r_1^i\right)t - \left(1 + \sum_{i=0}^{i=k-1} r_1^i\right)t'. \end{aligned} \tag{9}$$

In the limiting case where $t = r_1 t'$, we have:

$$d_{ol} = r_1 t' - 2t'. \tag{10}$$

The value of d_{ol} becomes zero when $r_1 = 2$ and eq. (10) becomes the same as eq. (4) in its limiting case. However, d_{ol} always remains equal to or greater than zero, thus, validating the basic law of all SRs—that they may not start to SO, unless they are completely shifted in.

APPENDIX C

Delay Requirement on Fractional Rate Increasing Between One and Two

Consider an N-bit block with a rate change ratio of r (<2 and >1). Let r' be the reciprocal of r. Then it can be seen that an arrangement of SRs shown in Fig. 7, and zero delay leads to a situation where the jth register would not have been shifted in before it is ready to be shifted out. To avoid this and to assure that SO takes place immediately after shifting in, the delay necessary can be calculated as

$$\begin{aligned} d_{in} &= [(N - 2^{k+1}) + 2^k - N(1 - r') - (N - 2^{k+1})r']t \text{ seconds} \\ &= 2^k(2r' - 1)t \text{ seconds}. \end{aligned} \tag{11}$$

The first two terms in (11) denotes the time required to fill the last two SRs with $(N - 2^{k+1})$ and 2^k register positions at the primary rate of t seconds per clock cycle. The third term denotes the length of the block at a difference of clock rates between the primary clock rate of t second and a secondary clock of t' ($= r't$) seconds. The fourth term

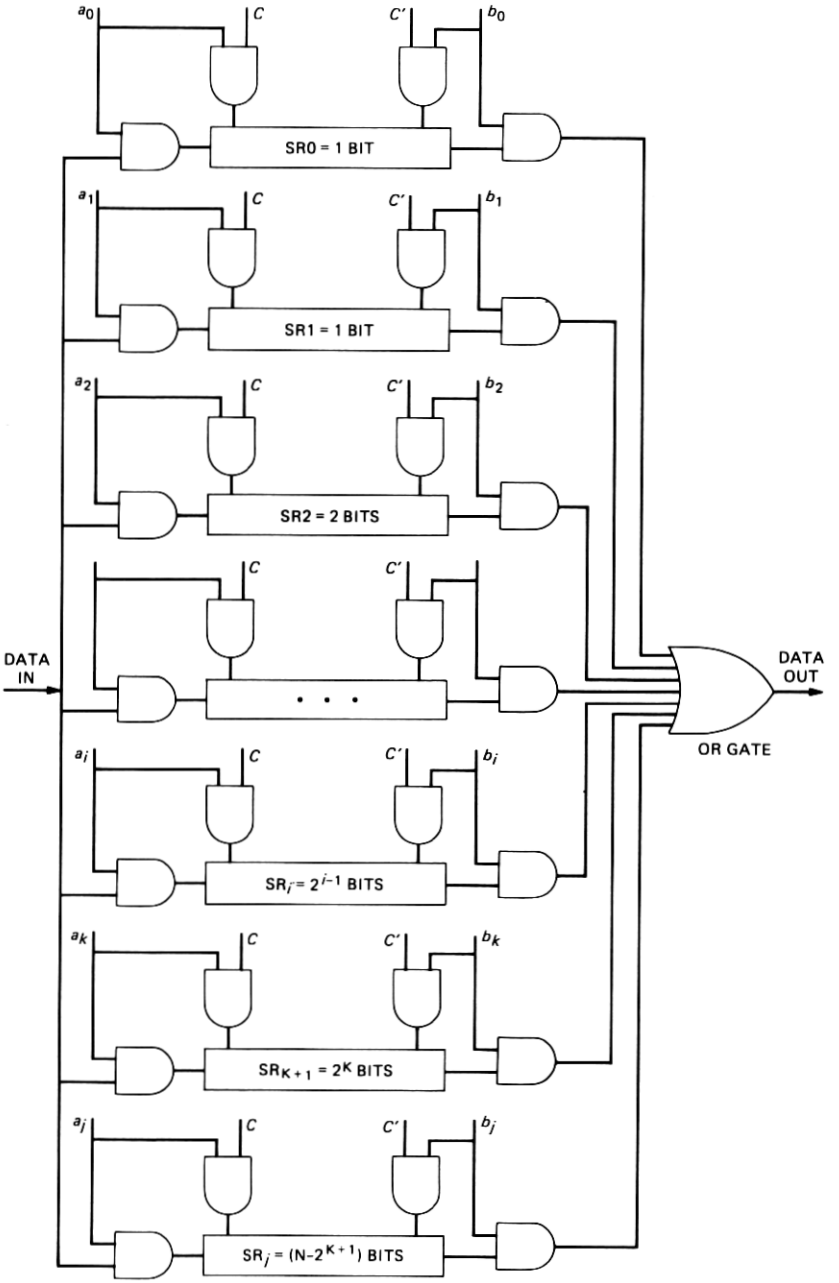


Fig. 7—Generalized fractional rate change circuit for ratios between 1 and 2.

represents the time to empty the last register at the secondary rate. It can be seen that in the limiting case when r' tends to 0.5 the delay necessarily tends to become zero.

The physical significance of this delay is to adjust the coincidence of the finish of the SI instant with the start of the SO of the last but one SR, thus, finishing the binary sequences of register locations. It is also interesting to note that the time delayed in emptying the first SR reappears at the end of the block as a summation of delays in the various other registers before the last register. For instance, the delay between shifting in and shifting out of the $(i + 1)$st; $(0 < i < k)$ SR can be written as:

$$d_{(i)} = \left[r' \sum_{j=i}^{j=k} 2^j - \sum_{j=i-1}^{j=k-1} 2^j \right] t \text{ seconds.} \tag{12}$$

The delay for SR1 becomes

$$d_1 = [r' \times 2(2^k - 1) - (2^k - 1)]t \text{ seconds.} \tag{13}$$

The delay for SR0 causes an incremental increase in delay of $(2r' - 1)t$ seconds. Hence, the total delay of the last bit coming out of SR0 is:

$$d_o = (r' \times 2^{k+1} - 2^k)t \text{ seconds,} \tag{14}$$

which is consistent with eq. (11).

REFERENCE

1. S. V. Ahamed, "A General Class of Rate Change Circuits," B.S.T.J., *50*, No. 10 (December 1971), pp. 2177–93.