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No. 10A Remote Switching System:

Control-Complex Architecture and Circuit Design

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The Remote Switching System (RSS) control complex contains the common circuitry needed to communicate with the host ESS and operate the other equipment in the RSS frame (switching network, line interface circuits, transmission channels, service circuits, etc.) as required to perform the functions of detecting originations, establishing and tearing down network connections, ringing telephones, and all of the other basic functions of a telephone switching system. In this capacity, the RSS control complex is analogous to the central control of a conventional ESS, rather than being a simple frame controller. This control complex contains two equivalent processors. One is active and the other is standing by to ensure reliability.

I. INTRODUCTION

The purpose of this paper is to give a detailed description of the architecture and circuit design of the No. 10A Remote Switching System (RSS) control complex. The RSS control complex contains the common circuitry needed to communicate with the host ESS and operate the other equipment in the RSS frame (switching network, line interface circuits, transmission channels, service circuits, etc.) as required to perform the functions of detecting originations, establishing and tearing down network connections, ringing telephones, and all of the other basic functions of a telephone switching system. In this capacity, the RSS control complex is analogous to the central control of a conventional ESS, rather than being a simple frame controller. This analogy becomes even more exact when one recognizes that the RSS must, when its connection to the host is severed, operate in a stand-

alone mode, and in this mode the RSS control complex provides the entire intelligence for operating the system.

1.1 Elements of the control complex

The RSS control complex can be functionally subdivided into five elements: the processor, which provides the data manipulation and decision-making functions; the memory, which includes both the non-volatile program store and the writable store used for translations and transient data; the data link, which provides communication with the host ESS; the peripheral access circuitry, which links the control complex with the other circuits in the frame; and the maintenance panel, which provides a rudimentary human interface. An additional piece of equipment, used for writing the circuit packs which contain the operating program, is also described here, although it has no direct connection to the RSS frame.

1.2 Design objectives

The principal constraint on the design of the control complex derives from the size of the RSS—typically a single frame. This severely limits the space available for the control complex which must nonetheless, as pointed out above, provide many of the processing functions of a conventional ESS office.

The RSS control complex utilizes the current state of integrated circuit technology which makes possible a processor on a single circuit pack and five circuit packs containing a total of 240K* of memory. These six circuit packs, together with a data link circuit pack, one miscellaneous/interface circuit pack, and 16 fanout circuit packs (located throughout the frame near the peripheral circuits which they control) make up one side of the duplicated control complex. When the RSS is expanded to its maximum size by the addition of a mate frame, an additional 16 fanout circuit packs in that frame (32 including duplication) complete the control complex.

II. GENERAL ORGANIZATION

Figure 1 is a block diagram of the RSS control complex. With the exception of the maintenance panel, the entire control complex is duplicated. Certain of the duplicated elements of the control complex are associated in groups that are always used together. Thus, one processor, one set of memory circuit packs, and one set of fanout circuit packs form a "processor complex" which can be considered as a single unit. A processor complex contains a memory bus, which connects the processor to its memory, and a peripheral bus, which

* As is customary when speaking of memory sizes and addressing, $1K = 1024 = 2^{10}$

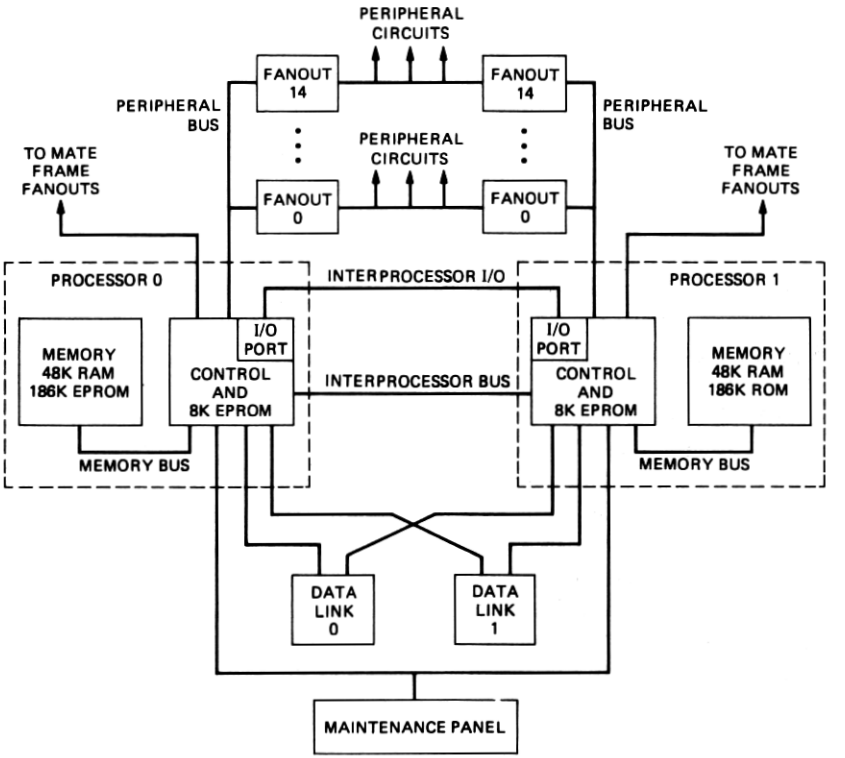

Fig. 1—Remote switching system control complex.

connects the processor to the fanout circuit packs. When a mate frame is provided, a separate peripheral bus provides access to the fanout circuit packs in that frame. Each processor has completely separate access to each of the data links. Thus, there are four possible operating modes for the control complex, as determined by the two processor complexes and the two data links.

2.1 Processor interactions

In normal operation, one processor is active (on-line) and the off-line processor is halted, allowing the on-line processor to gain access to the internal busses of the off-line processor via the interprocessor bus. Through this bus, the on-line processor can keep the off-line memory up-to-date and perform diagnostics to verify the health of the off-line processor complex. This manner of operation is referred to as "dual simplex," i.e., the processor is duplicated (dual) but the on-line processor runs alone (simplex) and does not depend for its error checking upon matching with a synchronously operated mate processor, as would a "duplex" system.

It is possible for both processors to be running simultaneously. This is the case during certain diagnostics, and it can also occur when the system is trying to find a working configuration. The interprocessor bus cannot be used in this condition, and so an eight-bit-wide I/O port is provided to allow messages to be passed between the processors.

III. PROCESSOR

The RSS processor is built around the *BELLMAC**-8 processor, an 8-bit microprocessor with an extensive, general-purpose instruction set. Some of the significant architectural features of the *BELLMAC*-8 processor are as follows:

(*i*) A 16-bit address bus, permitting direct addressing of 65536 (64K) 8-bit bytes.

(*ii*) A single address-space, with no special instructions or control for input/output (I/O) operations as opposed to memory reads and writes (memory-mapped I/O), and no differentiation between the instruction address-space and the data address-space.

(*iii*) Sixteen general-purpose 16-bit registers which, rather than being located within the microprocessor chip itself, occupy a block of memory locations which can lie anywhere in the 64K address space.

(*iv*) One maskable interrupt which can be automatically vectored anywhere in the first 256 bytes of the address-space.

(*v*) One nonmaskable interrupt (reset) which always vectors to location zero.

(*vi*) The ability to synchronize itself with slow memory or peripheral devices by means of an external "ready" indication.

Processor circuitry surrounding the *BELLMAC*-8 processor provides other functions required in the RSS application. These include:

(*i*) Buffering and timing generation for interface to other circuits.

(*ii*) An expansion of the address-space beyond the 64K provided by the *BELLMAC*-8 processor.

(*iii*) Provision for multiple interrupts and generation of the required vector.

(*iv*) Error checks needed to assure proper operation of the system.

(*v*) Circuitry for interfacing and coordination with the mate processor.

3.1 Expanded address structure

The addressing requirements for the RSS processor greatly exceed the 64K that the *BELLMAC*-8 processor can address directly. The addressing must encompass the nearly 200K of program store, the

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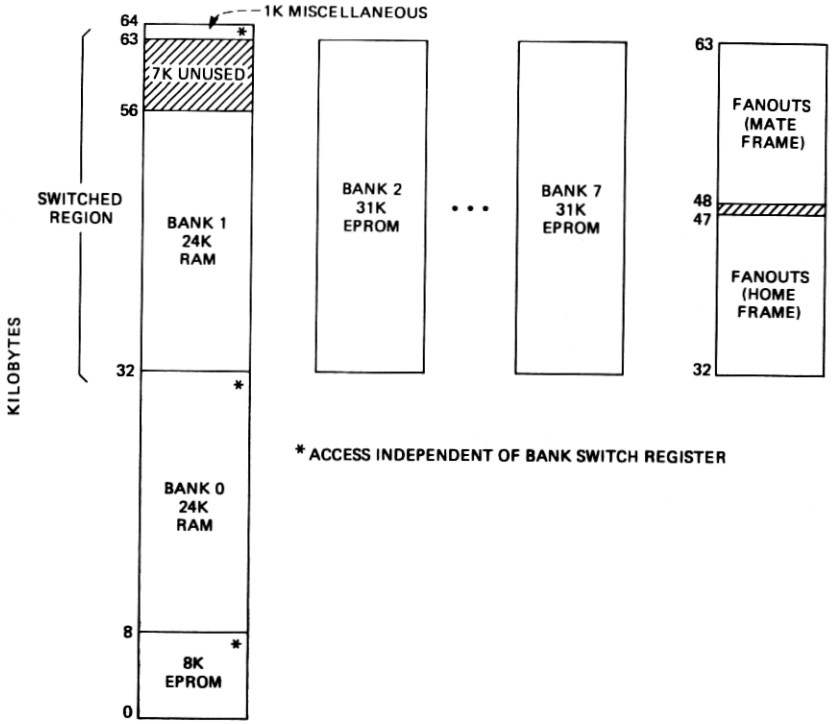

Fig. 2—Remote terminal address space.

48K of writable memory, and the 30K addresses required by the bit-addressable periphery. To accomplish this, a bank-switching scheme is employed.

Figure 2 depicts the bank-switch architecture. The low 32K locations of the address space are not switched, and the memory which occupies this space is, therefore, always accessible. Included in this space, are 8K of program store beginning at address zero and 24K of writable memory. The program store is used for programs which must always be available or which access locations in the switched portion of the address space. Examples of programs which must always be available are the handlers for the maskable and nonmaskable interrupts and the bank-switch monitor. Programs which access the switched portion of the address space include the subroutines which read and write the periphery. The writable memory in this unswitched space includes not only the transient database for the system, but also memory required by the *BELLMAC*-8 processor for use as its general-purpose registers and subroutine-calling stacks.

The uppermost 1024 addresses are also unswitched. This space is

used for I/O port addresses (recall that the *BELLMAC*-8 processor uses memory-mapped I/O). These locations must always be accessible because they include the bank-switch register itself, as well as the interrupt-acknowledge address, from which the *BELLMAC*-8 processor reads the value of the interrupt vector whenever an interrupt occurs.

The remaining 31K portion of the address space (i.e., all but the top 1024 of the upper 32K locations) can be switched either to the fanout circuit packs which control the periphery or to one of seven additional memory banks, which can be either writable memory (as is bank 1, 24K) or program store (banks 2 through 7, 31K each). It should be noted that this architecture prohibits direct references between the switched banks, i.e., a program residing in one of the switched banks cannot directly access anything which lies in a different switched bank. All such references must be performed via subroutines residing in the unswitched portion of the address space.

3.2 Interrupts (maskable)

The processor provides for five sources of interrupts in a software-assisted priority arrangement. The interrupt sources are

(*i*) Data link 0.

(*ii*) Data link 1.

(*iii*) A programmable timer, used to generate the 10-ms interrupt.

(*iv*) A programmable timer, used for miscellaneous timing functions.

(*v*) The interprocessor I/O port.

The *BELLMAC*-8 processor has a single input for requesting a maskable interrupt. This interrupt is termed "maskable" because it is masked internal to the *BELLMAC*-8 processor by an "interrupt-enable" status bit which is under program control. When the *BELLMAC*-8 processor recognizes an interrupt request, it reads a predetermined address (the interrupt-acknowledge address) and interprets the 8-bit value received as an address (in the first 256 bytes of memory) to which control should be transferred. Whenever an interrupt occurs, the *BELLMAC*-8 processor automatically inhibits further maskable interrupts by clearing the interrupt-enable bit. Additional circuitry in the processor provides:

(*i*) An interrupt source register, which records the occurrence (possibly momentary) of an interrupt request from each source. The program can also read and write this register to control processing and aid diagnostics.

(*ii*) An interrupt mask register, which permits the program to enable or disable individual interrupt sources.

(*iii*) Vector generation logic, which generates the data presented to

the *BELLMAC*-8 processor when it reads the interrupt-acknowledge address. These data are determined by the highest-priority interrupt source which is active and enabled.

The hardware-determined priority is only effective for resolving the vector to be generated when multiple interrupt requests are present simultaneously. There is no automatic masking of interrupts having priorities equal to or lower than the one currently being processed. If an interrupt handler is to permit other interrupts to occur, it must, prior to reenabling interrupts in the *BELLMAC*-8 processor, adjust the interrupt mask register such that only higher-priority interrupts are enabled. It must, then, restore the original mask before terminating.

3.3 Error checks

The RSS processor utilizes a combination of software and hardware checks to ensure proper operation of the system. As a consequence of the improved reliability brought about by the use of large-scale integration, the amount of error checking hardware has been considerably reduced from what has been traditional in ESS processors. The most significant change relates, naturally, to the microprocessor itself. The *BELLMAC*-8 processor, like other microprocessors, is almost completely lacking in internal checks. A reasonable way to check such a circuit is to utilize a matcher between two synchronously-operated devices. However, in view of the anticipated failure rate of the *BELLMAC*-8 processor, it is expected that most RSS installations will never experience a single *BELLMAC*-8 processor failure in their 40-year life. Similar, although less dramatic, reliability improvements in other areas have suggested that error-checking circuits should be confined to those areas in which simple circuits can produce a significant benefit rather than having a goal of 100 percent fault coverage. The areas not covered by the hardware check circuits, such as the microprocessor itself, can be tested periodically by software exercise routines.

3.3.1 Nonmaskable interrupt architecture

There are seven circuits in the processor which generate nonmaskable interrupts (resets). The *BELLMAC*-8 processor has a single "reset" input which acts like the interrupt-request input, except that it is unaffected by the internal interrupt-enable bit and it always vectors to address zero, regardless of the data which are read from the interrupt-acknowledge address. The processor contains circuitry to support the various reset sources in a manner somewhat like the maskable interrupt sources, specifically:

- A reset source register which records the occurrence of each condition. The program can read and clear this register.
- A reset mask register (actually, selected bits of the interrupt mask

register) which can individually mask the conditions. This differs from the interrupt mask in that a masked interrupt remains pending, whereas a masked reset is cleared and ignored.

3.3.2 Hardware check circuits

Each of the following circuits can cause a reset and has an associated bit in the reset source register:

(*i*) Miscellaneous decoder check—This detects faults in the circuits which decode the individual enable signals from the top 1024 locations in the address space. Each time an address in this space is accessed, an odd or even parity indication is reconstructed from the decoder output and compared to the parity over the original address. A mismatch raises this error condition. This check has no mask bit.

(*ii*) Write-protect—Memory is write-protected in 4K blocks. An attempt to write into a protected block or an attempt to write into program store is suppressed and this error condition is raised. This check has no mask bit, but the protection status of the writable memory is under program control.

(*iii*) Manual reset—A key on the maintenance panel generates this reset in both processors. It cannot be masked.

(*iv*) Sanity timer—The processor contains a sanity timer which the program must clear at least every 200 ms but not twice within a 40-ms period. A violation of either the minimum or maximum interval raises this error condition, which cannot be masked.

(*v*) Data parity check—On every write operation, the processor generates odd parity over the eight data bits. Whenever data are read from memory or from a data link, parity is checked, and this error condition results if the parity is not odd. This check has an associated mask bit. It should be noted that no parity bit is supplied on reads from the periphery or from any of the special addresses in the processor itself, and this check is, therefore, suppressed in these cases.

(*vi*) Peripheral addressing check—This check is similar to the miscellaneous decoder check, above. On every peripheral access the fanout board reconstructs a parity indication and sends this signal back to the processor. The processor compares this with the parity computed over the original address, and a mismatch raises this error condition. This check has an associated mask bit.

(*vii*) Mate processor reset—This signal is generated under program control in the mate processor. It is used when the on-line processor wishes to initialize the off-line. This reset can be masked.

To simplify the task of the processor diagnostic program, an additional level of control over the resets has been provided. This is a "block hardware checks" bit in a status control register. When this bit is set, only the sanity timer and the manual reset can actually send a

reset signal to the *BELLMAC*-8 processor. The other reset sources can still set their bit in the reset source register, but any further action is suppressed.

3.3.3 Firmware checks

To complement the above check circuits, tests and defensive checks are built into the firmware. Although a full discussion of these safeguards is beyond the scope of this article, certain areas are worthy of note.

(*i*) The processor sanity test (a subset of the processor diagnostic tests) is run on a continuous basis, completing its cycle about every five minutes. This verifies the operation of the *BELLMAC*-8 processor itself, as well as the other parts of the processor not covered by check circuits.

(*ii*) The peripheral data bus is checked during normal use by such techniques as readback checks to verify that an expected state change actually occurred in a peripheral circuit and operational checks which verify the ability to read and write both zeros and ones over each data bit path.

(*iii*) The interprocessor bus is tested as part of the continuous process of verifying that the contents of the on-line and off-line memories match.

3.4 Interface with the mate processor

In addition to the "mate processor reset" described above, there are three areas of explicit interaction between the processors: the interprocessor bus, the interprocessor I/O port, and the peripheral lockout circuit.

3.4.1 Interprocessor bus

The interprocessor bus consists of a 16-bit bidirectional address bus, an 8-bit bidirectional data bus, and a group of control and timing leads. It couples the internal buses of the two processors in a manner which gives the on-line processor almost unrestricted control over the off-line. Whenever a processor is running, its internal bus is protected against interference from the mate. When a processor decides that it should be off-line, it puts itself into a special "hold" state which stops the microprocessor and opens the bus coupling gates to control signals from the mate. The off-line processor is released from hold by the occurrence of a reset or under program control from the on-line. This hold state is controlled by a bit in the processor's bus control register.

Bits in the on-line processor's bus control register control the operating mode of the bus. The bus can be operating in "split" mode, i.e., not accessing the mate at all. Another mode, "double write," causes all

write operations to be performed in both the on-line and off-line processors. A third mode, "mate read," causes read operations having addresses in a specified range to be performed in the mate and the resulting data returned to the on-line processor. It is also permissible for the "double write" and "mate read" modes to be active simultaneously. The 8-bit bus control register, then, contains one bit to control the double-write mode, one bit to activate the mate-read mode, and a bit which causes the hold state to be entered. The other five bits of the register define a 2K block of addresses for which the mate-read mode will be effective.

A processor is prevented from writing into the bus control register of its mate. This is done so that the on-line processor can freely alter its own bus control register without inadvertently releasing the mate from hold. When the on-line processor wishes to release the mate, it can perform a write (with any data) to a special "bus control clear" address while in the double-write mode, thus clearing both bus control registers. The mate processor will resume execution with the instruction following the one that put it in hold, unless it finds an active interrupt request. Of course, it is the responsibility of the software to ensure that the state of the off-line processor has not been so altered while in hold that the resumption of execution would cause an error.

3.4.2 Interprocessor I/O port

The interprocessor I/O port provides communication between the two processors when both are running. This is necessary under certain conditions when the processors are trying to decide which of them should be on-line. The interconnection consists of an 8-bit bidirectional data bus with additional control and interlock leads and both an input buffer and an output buffer at each end. When a processor wishes to send a message to its mate, it writes a byte into its output buffer. These data will be transferred to the input buffer of the mate processor provided that this buffer is not already full and that the interconnecting bus is not busy. The processor can then write another byte into its output buffer, and this will be transferred as soon as the mate reads the first byte from its input buffer. A processor can arrange to be interrupted whenever its input buffer is full or when its output buffer is empty or both.

3.4.3 Peripheral lockout

The processor contains circuitry designed to ensure that the on-line processor can prevent its (possibly insane) mate from accessing the periphery or the data links while, at the same time, keeping its own access unimpeded. This problem is a difficult one in the RSS environment since the office is unattended and there is no independent

communication link over which an outside agency could exercise control of the system—the existing data links function only with the aid of the processor.

Each processor has two flip-flops which control peripheral lockout. One, designated *A*, affects the processor's own access to its fanout boards and to the data links. The other, designated *B*, affects the mate processor's peripheral and data link access. A processor's access is determined by exclusive OR-ing its own *A* flip-flop with a signal from the mate's *B* flip-flop. If these two flip-flops are in the same state, the processor is locked out from its fanout boards and from the data links. Thus, as long as the mate processor's *A* and *B* flip-flops do not change state, a processor can control its own peripheral access with its *A* flip-flop, while its *B* flip-flop controls the mate processor's access.

To reduce the probability that an insane off-line processor would continually alter the state of its *A* and *B* flip-flops, thus making it impossible for the on-line processor to control the system, two separate actions are required to load data into the flip-flops. First, two bits of a register in the processor must be loaded with the data bits destined for the *A* and *B* flip-flops. Then a write must be performed (with any data) to a special "lockout strobe" address. This write clocks the two data bits into the actual *A* and *B* flip-flops. As an additional precaution, this lockout strobe is ineffective if any bit of the reset source register is nonzero.

IV. MEMORY

The RSS control complex contains two types of memory: writable random-access memory (RAM) and nonwritable erasable programmable read-only memory (EPROM). Each of the duplicated processors has its own dedicated memory.

4.1 Memory organization

To permit access from the *BELLMAC*-8 processor's limited 64K address space, memory is divided into banks (see Fig. 2). The low 32K addresses are used to access one 24K bank of RAM and a special 8K block of EPROM. The remaining banks, one 24K RAM bank and six 31K EPROM banks, are accessed selectively from the upper half of the address space, under control of the processor's bank switch register.

4.1.1 Physical arrangement

Each RAM circuit pack contains 24K by 9 bits of storage (24K with parity) built up from 4K by 1 bit devices in a straightforward array. Each RAM circuit pack corresponds to a logical bank.

The 8K block of EPROM is located on the Processor B circuit pack (one of the two packs that make up each processor). The 8K by 9 bits

of storage are provided on five 2K by 8-bit devices in a manner similar to that used for the 64K EPROM circuit packs described below, although the details of the parity-bit mapping are different.

The 31K EPROM banks are contained on circuit packs, each of which contains 64K by 9 bits of storage built up from 2K by 8-bit devices. Each circuit pack contains two banks. The devices which contain the eight data bits are arranged in a conventional fashion with all of the devices paralleled onto a common data bus and selectively enabled by decoding the higher-order address bits and the bank-select. The required 64K parity bits are contained in four additional devices.

The data outputs from these devices are paralleled into an 8-to-1 multiplexor which selects one of the eight data bits, with the selection being determined by the low-order three address bits. The address bits supplied to these four EPROM devices, and to the decoder which selects them, are shifted three bits compared to the address supplied to the array containing the data bits. Thus, the first address in the first parity EPROM contains the eight-parity bits which correspond to the first eight bytes in the data EPROMs, with the multiplexor selecting the proper parity bit for the particular location being read. Of the 64K bytes on each EPROM circuit pack, only 62K can actually be accessed by the processor. The missing addresses (1024 in each bank) are occupied by the "miscellaneous decoder" locations at the high end of the processor's address-space.

The EPROM circuit packs and the processor B circuit pack contain additional control and access which permit the devices to be programmed after the board has been assembled. Thus, the devices can be soldered directly into the circuit pack, avoiding the reliability problems inherent in having large numbers of sockets, while still allowing the devices to be erased (by UV light) and reprogrammed as needed. The RSS frame provides neither the 25V power supply nor the necessary control signals for the programming operation, thus protecting the data against alteration while the packs are installed in the system. A separate piece of equipment, called *PROMUS** reprogrammer is required to erase and program data into these circuit packs.

4.2 Memory access

The memory does not contain any identifiable controller. All of the required address, data, and timing signals are generated in the processor itself.

4.2.1 Random-access memory

The access time of the RAM circuit pack (250 ns) is such that a single

* Trademark of Western Electric Company.

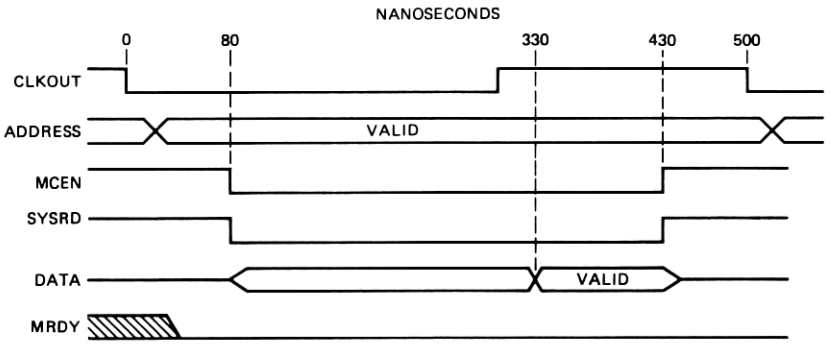

Fig. 3—Random-access memory read cycle.

BELLMAC-8 processor clock cycle is sufficient for the operation. Figure 3 shows the timing of a RAM read cycle. The *BELLMAC*-8 processor's CLKOUT signal is used as a timing reference. The primary timing signal to the memory is the chip-enable, MCEN, which is applied to the selected memory devices to define the access cycle. It is a 350-ns pulse delayed 80 ns from the negative transition of CLKOUT to allow the address and bank selection to propagate. The SYSRD signal going to a low level identifies this cycle as a read access and controls the buffers which gate the data from the memory onto the backplane bus. The selected memory circuit pack pulls MRDY low to indicate to the processor that the access can be completed in a single clock cycle.

4.2.2 Random-access memory write cycle

The write cycle (Fig. 4) is initially the same as a read. The SYSRD remains high, however, turning on the buffers which gate the data off of the backplane bus into the memory. Late in the cycle a write pulse, MWRT, causes these data to be loaded into the addressed memory cells.

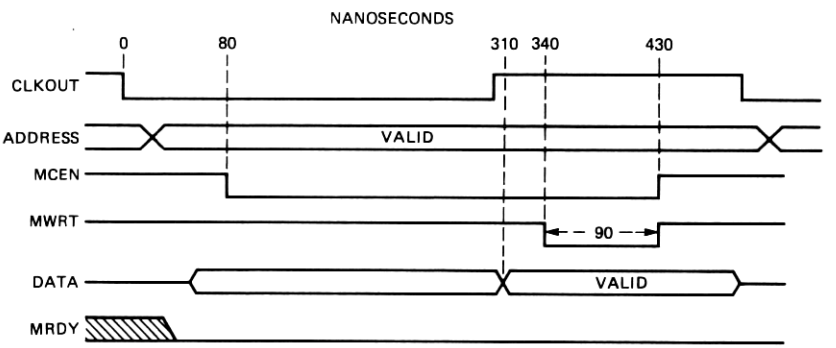

Fig. 4—Random-access memory write cycle.

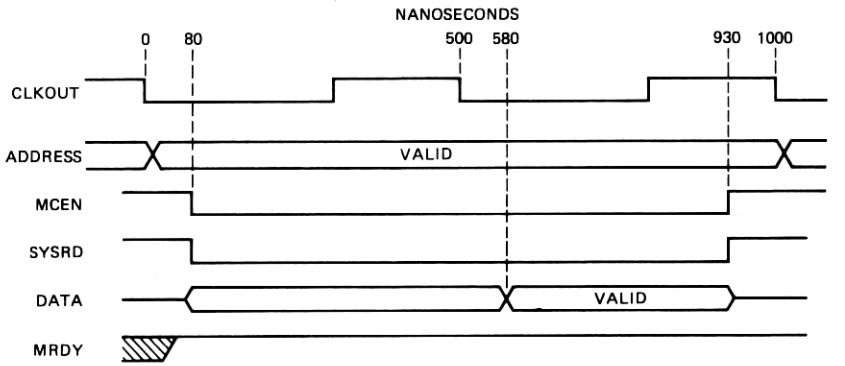

Fig. 5—Erasable programmable read-only memory read cycle.

This write pulse is short (90 ns) because the data from the *BELLMAC*-8 processor are not available until late in the cycle. This, of course, represents a significant requirement imposed on the devices used in the memory.

4.2.3 EPROM access

The EPROM devices are too slow to be accessed in a single clock cycle. The access (Fig. 5) is otherwise similar to a RAM read. The MCEN timing signal enables the addressed devices, and SYSRD turns on the data buffers. The MRDY signal remains high throughout the cycle, informing the processor that it must wait an extra clock cycle for the data to become valid.

4.2.4 Write protection

The write-protect circuitry is intended to prevent accidental alteration of semipermanent data in RAM (e.g., translations). The RAM is write-protected in 4K blocks. Each RAM circuit pack contains an 8-bit register which holds the protection status for the six 4K blocks on the pack (two of the bits are unused). Whenever a protected block is addressed, the memory pack grounds a backplane lead, WPBLK, which informs the processor that any write should be suppressed and treated as an error. The RAM circuit pack does not itself suppress the write. The EPROM circuit packs also ground WPBLK whenever an EPROM bank is addressed. Although the "write" in this case would be harmless, the resulting error indication does help to catch program bugs that cause writes to EPROM.

V. REMOTE SWITCHING SYSTEM DATA LINK

The RSS data link provides a fully duplicated path for the flow of control messages between the RSS remote terminal and its associated host ESS. Two voice channels, among the many provided by the

transmission system between the remote terminal and the host, are dedicated for use by the two data links. Serial, full-duplex information flows at a rate of 2.4 kb/s. The two voice channels used by the data link may be provided by either analog or T1 carrier facilities. Channel 12 of the first two carrier groups is used. The X.25 version of the Synchronous Data Link Control (SDLC) protocol is used to provide message synchronization and error control.

5.1 Overview of the data link

Figures 6 and 7 show the various units in the data link path for a T1 carrier and an analog carrier application. The T1 carrier specifies a frame format that time division multiplexes 24 voice channels together onto a high-speed line. The data rate on the high-speed transmit pair and on the receive pair of wires is 1.544 Mb/s. The analog carrier may be a metallic connection, radio, or N carrier. The N3 and N4 carrier frequency division multiplexes 24 voice channels onto two pairs of wires; the N2 carrier multiplexes 12 channels.

Data links from various systems attach to the Peripheral Unit Controller (PUC), and each line attaches to a separate Line Interface Unit (LIU). The PUC acts as a front-end processor for the ESS by performing the processing associated with the X.25 protocol, including acknowledging received messages and autonomously retransmitting messages as needed.

5.1.1 The T1 data path

Figure 6 shows only one data link; the other link follows a similar path. Both data links connect to the same PUC, but separate *D*4 banks are used at the host end and separate T1 circuits are used at the remote terminal.

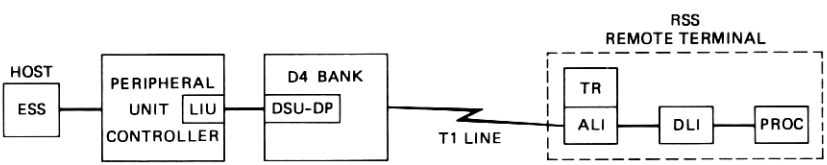

Fig. 6—Block diagram of digital carrier data link.

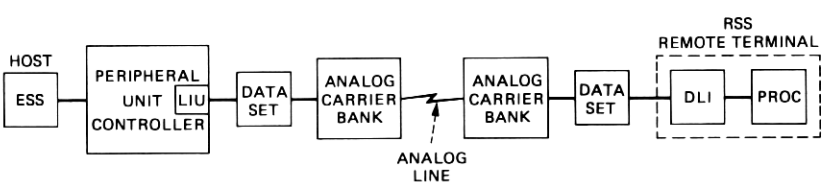

Fig. 7—Block diagram of analog carrier data link.

The time multiplexed frames of information on the T1 line are encoded and decoded by the *D4* channel bank at the host end of the link. This bank has a separate plug-in for each of the 24 channels; slot 12 contains a Data Service Unit, Data Port (DSU-DP) plug-in. Channel 12 is used by the data link and the other slots contain voice channel units. The DSU-DP converts the serial 2.4 kb/s data to a speed and format suitable to the T1 carrier. The interface between the PUC-LIU and the DSU-DP is specified by the Electronics Industries Association (EIA) Recommended Standard (RS) 449 interface described in section 5.2.3.

The length of the T1 span from host to remote terminal is constrained by the need to provide an acceptable grade of voice service, not by the data link. The Alarm-Line Interface (ALI), and Transmit-Receive (TR) circuit packs located in the remote terminal integrate the function of the *D4* bank common equipment into the RSS frame.

A portion of the Data Link Interface (DLI) circuit pack is a subset of the DSU-DP. The remainder of the DLI provides the hardware needed to process the X.25 protocol and an interface to the two processors in the remote terminal. The connection between the DLI and the RSS processors is cross-coupled to allow either processor to access both data links.

5.1.2 Analog data path

Figure 7 shows the data link path for the analog carrier. Again, two of the channels provided for voice are dedicated for data link use. The functions and connections to the PUC are the same as for the T1 carrier. The 201*C* data set uses phase-shift modulation to convert the 2.4 kb/s serial data to and from the PUC to a form suitable for the voice channel. A four-wire connection is made from the data set at each end of the link to the analog carrier facility. This data set allows the use of a standard voice channel unit in the analog carrier bank for the data link. The restriction on the length of the analog carrier data link is similar to the limit for the T1 carrier, i.e., the link length is restricted by the voice transmission requirements.

A connection is made, at the remote terminal, between the data set and the DLI circuit by means of the EIA RS-449 interface described in section 5.2.3. The connection between the DLI and the processors is the same as described for the T1 carrier.

5.1.3 Maintenance features

There are three data link loop-back modes under control of the ESS processor and three loop-backs under control of the RSS processor. When a processor activates a loopback any data sent from that

processor travel down the link until it reaches the loopback point. It is then "reflected" back to the originating processor.

Data from the host may be looped back at the PUC, at the DSU-DP (the data set for analog carrier), or at the DLI (data set) at the remote terminal. Data from the RSS processor may be looped back at the DLI protocol section, at the T1 circuit on the DLI (data set for analog carrier), or at the host DSU-DP (data set). One of the bits generated in the T1 data port encoding is reserved for controlling the remote T1 loopback mode. Note that for both T1 and analog carriers these loopbacks affect only the data link channel.

5.1.4 Link duplication

With the exception of certain data link diagnostic routines, only one data link needs to be used, but two links are provided to achieve a high degree of reliability. To ensure that a single fault cannot affect both links, they do not share any common equipment. The PUC is internally duplicated, and separate LIUs are used for each link. Separate cables from the two LIUs connect to separate DSU-DPs that are in different T1 digroups. In the case of an analog carrier, the PUC-LIUs attach to separate data sets which use different analog carrier facilities. Regardless of the type of carrier used, the two links utilize independent transmission facilities. In the ideal case, the facilities would be geographically diverse. This philosophy of link duplication is continued in the design of the remote terminal with two processor interfaces to the two DLI circuit packs.

5.1.5 Data link protocol

The host ESS always decides which data link to use. On an average there is more link traffic from the host, than to it. Typical messages from the host include call processing commands such as set up a path, ring a phone, or collect a coin. Other messages from the host request diagnostics, or request a reconfiguration. Typical messages from the remote terminal include: order acknowledgment, line origination, diagnostic results, audit results, traffic measurement results, and error reports.

The widely used X.25 protocol provides message synchronization and error control. The protocol operations are supported by hardware located in the PUC-LIU and the RSS-DLI. This protocol is a refinement of the SDLC protocol proposed by IBM.[1] For the RSS application, the messages are formed into blocks of 0 to 16 bytes of data, with 6 bytes of protocol overhead. The first and last eight bits of each block are a flag character (01111110). An extra zero is inserted after every fifth contiguous one before transmission to prevent the body of the block

from mimicking the flag character. The extra zeros are automatically stripped upon reception of the data.

Every block has a 16-bit Cyclic Redundancy Code (CRC) word to provide error control. This word results from the successive division using the CRC-CCITT polynomial. The CRC check was selected because it requires only a shift register with a few feedback gates and a comparator. Also, the probability of the CRC check detecting even a large burst of errors is better than 99.99 percent.

If a message is garbled or entirely lost it will be ignored and a retransmission will be requested. Several retrials will be made before a protocol impasse is reported to the host.

5.2 Data link interface circuit pack

The DLI connects to the two remote terminal processors via parallel data buses. The data pass through the X.25 protocol logic where protocol control fields are added. The data then undergo a speed and/or level conversion, and are presented to either the T1 circuits integrated into the remote terminal, or to an outboard data set for analog carrier. The DLI uses mostly TTL SSI, and MSI technology, with some PMOS and NMOS LSI circuits. The few analog functions of the DLI are performed by a handful of discrete devices. The two DLIs are powered from separate converters, and reside at opposite sides of the frame. Figure 8 shows the DLI block diagram.

5.2.1 Processor interface

There are four busses that connect the two processors to the two DLIs. Each is a private connection between one processor and one DLI. Two identical circuits on the DLI provide interfaces to the two processors.

Each bus has 8 bidirectional data bits and a bidirectional odd parity bit. The three low-order address bits are sent from the processor to select which register on the DLI is used. The upper bits of the address are decoded on the processor boards to generate two enables. The Data Link Enable A (DLENA) selects the group of registers that reside in the protocol circuit. The Data Link Enable B (DLENB) selects the group of registers that support the processor interface. A signal called INHIB from each processor sanity circuit indicates if signals from a processor should be ignored. The WE and RE signals are timing strobes used for the read and write operations.

Any data link interrupt condition is passed to each processor by the Interrupt (INT) signal. Most of the actions by the data link control program are prompted by an interrupt. During normal operations an interrupt results from a data byte being received, or the transmitter being ready for the next byte of out-going data. The following error

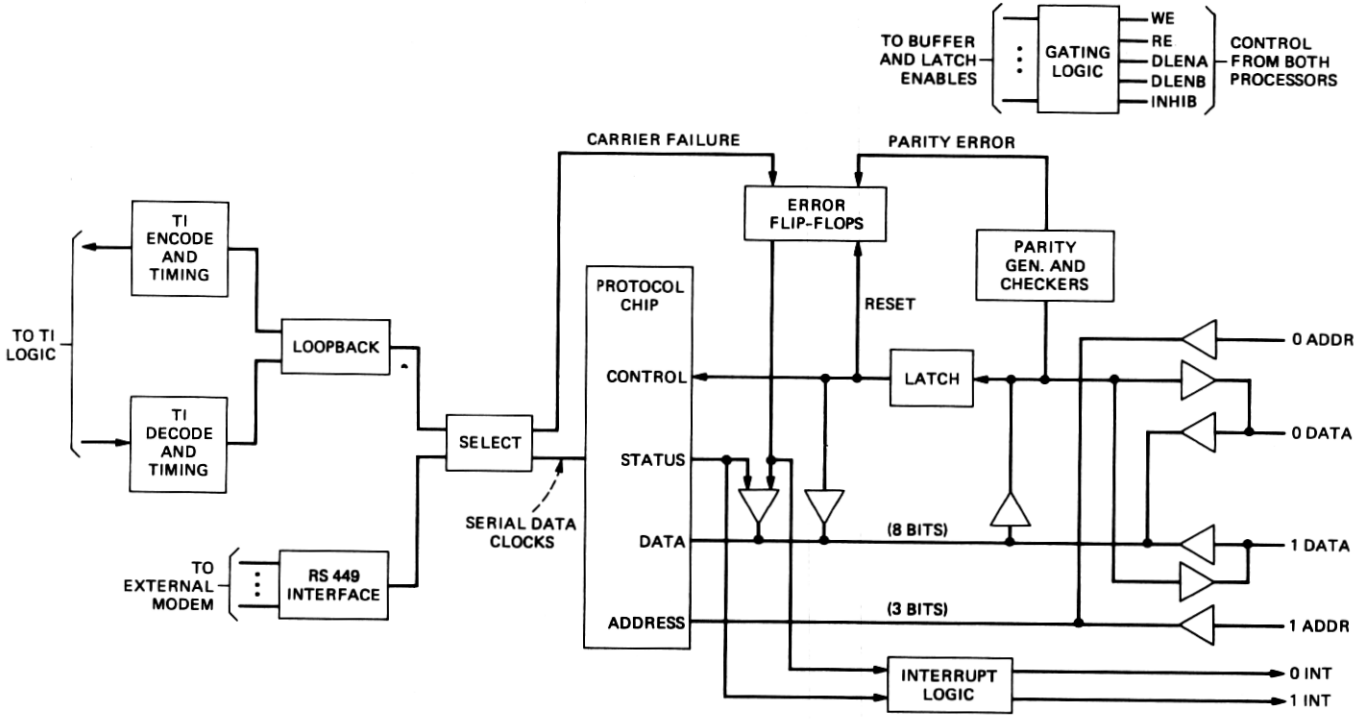

Fig. 8—Remote switching system data link interface functional block diagram.

conditions will also cause an interrupt: overflow of the receiver, underflow of the transmitter, received message with bad CRC, write parity error, and carrier loss on the transmission facility. An interrupt will remain pending until all causes are serviced by program action.

The first action taken by the DLI control program to service an interrupt is to read the interrupt cause register in the DLI. A separate bit in this register is assigned to each cause for an interrupt. Depending on the state of the DLI, the control program will then either read the received data register, write the transmit data register, or operate the DLI control latch to clear an error condition.

A timing wait-state is generated by the processor to allow the DLI a 1-μs operation cycle. If both processors access the same DLI at the same instant, a bus conflict may result internal to the DLI.

During read operations, the DLI generates an odd parity bit. To allow diagnosis of the processor parity checker, the DLI has a parity error register which, when read, places bad parity on the data bus.

5.2.2 Protocol logic

Almost all of the X.25 protocol circuity is held in a single 40-pin, dual-in-line package integrated circuit. This NMOS LSI circuit is made by Signetics Corporation,[2] and is called the 2652 Multiprotocol Universal Synchronous Receiver/Transmitter. The 2652 interfaces parallel data to a serial synchronous data communications channel, with the high-level protocol functions left to the processor. The 2652 is a full duplex interface; thus, the transmit and receive sections operate independently of each other.

The 2652 performs a serial/parallel conversion, and buffers up to two bytes of data in both the transmit and receive directions. If the buffering capability is exceeded, an error flag is set.

To start the transmission of a block, the processor toggles the "transmit start of message" bit in the transmitter status register. The 2652 then generates a beginning flag character and indicates that the transmitter is ready for out-going data. During the body of the block, the 2652 inserts a zero after every fifth contiguous one to ensure that a flag-like character will not appear in the middle of a block. When the end of a block is reached, the processor toggles the "transmit end of message" bit in the transmitter status register. This causes the CRC check-word that the 2652 has been accumulating to be transmitted followed by an ending flag, also generated by the 2652.

When the start of a message is received by the DLI, the 2652 recognizes the in-coming flag and sets the "receive start of message" bit in the receiver status register. Every time another data byte is received the "received data available" condition causes an interrupt to the processor. During the body of the received block, the zeros inserted

after five contiguous ones are automatically removed making the zero insertion transparent to the processor. When the ending flag is received, the "receive end of message" bit is set in the receive status register, and the preceding CRC check-word is automatically examined by the 2652 to determine if the message was garbled.

Setting the "maintenance loop" bit in the DLI control latch causes data to be looped back to the remote terminal processor after passing through the processor interface and the 2652 IC.

5.2.3 Analog carrier interface

When the carrier select input, CARSEL, to the DLI is not grounded at the remote terminal backplane, the analog carrier serial interface is selected. The functions of the analog interface signals are specified by EIA RS 449.[3] The electrical characteristics for the unbalanced signals are described by EIA-RS 423.[4] Wave-shaping is used to limit the high-frequency content of the signals. This allows the signals to travel up to 1000 ft. The only departure from the standards is that a separate ground is used for each data and clock signal to improve noise immunity. This interface is compatible with the digital interface provided by the 2024A data set and the DSU-DP.

A positive 5-volt potential on the TR data lines represents a logic zero, and negative 5-volt potential represents a logic one. A voltage transition from +5 volts to −5 volts on the receive clock signal causes the DLI to sample the receive data signal. A voltage transition from negative to positive on the transmit clock input to the DLI causes it to shift out the next bit on the transmit data line.

The local and remote loopback signals from the DLI cause the data set to loop data when at a potential of +5 volts. Minus five volts on the signal quality line from the data set informs the DLI that the data set has lost its receiver carrier.

5.2.4 The T1 carrier interface

When the carrier select input, CARSEL, to the DLI is grounded at the remote terminal backplane, the T1 carrier interface is selected. The 2.4 kb/s data from the protocol logic is encoded and transformed in speed by the T1 carrier interface, and presented to the ALI and TR circuits in the remote terminal. The T1 carrier interface circuitry is a close copy of the primary logic in the DSU-DP. The next section discusses this logic.

5.3 Data service unit—data port (DSU-DP)

The DSU-DP is a channel unit that allows synchronous, binary data to pass over a T1 channel. A switch in the DSU-DP selects a data rate of 2.4, 4.8, or 9.6 kb/s. For the DSU-DP to operate in a *D*4 bank, an OIU-

2 (Office Interface Unit) must be installed in the common equipment section and backplane wiring must be present to convey an integrated 8- and 64-kHz clock from the OIU-2 to the data port(s). The "customer" interface is the same as the RS-449 interface described in section 5.2.3. After data channel control information and data redundancy are added, the steady 2.4 kb/s data rate is converted to 1.544-Mb/s bursts of 8 bits every 125 μs. This yields an average T1 line per data channel bit rate of 64 kb/s.

5.3.1 D4 bank signals

Transmit data from the DSU-DP are gated on the time multiplexed TNDATA line to the *D*4 common equipment. Receive data to the DSU-DP are sampled from the time multiplexed RNPCM line from the *D*4 common equipment. The multiplexing of the 24 channels is controlled by two sets of signals. One set is a 1-out-of-6 select and the other is a 1-out-of-4 select. The TDCLK, and RCLK signals provide the TR 1.544-MHz data bit timing. The TWD and RWD indicate the timing windows for transmit and receive channels at an 8-kHz rate.

When the DSU-DP sees its channel selected, and the timing window present, data are transferred to/from the common equipment. The RNDIS signal from the common equipment goes low as soon as a loss of T1 synchronization is detected, and the DSU-DP passes this along to the signal quality indicator at the RS-449 interface.

5.3.2 Encode/decode

The data between the DSU-DP and the *D*4 common equipment are in a Digital Data System (DDS) line format. The first bit of each 8-bit T1 data byte is a zero. The last bit is a one for data and a zero for the remote loop command. The center 6 bits are the data from the "customer interface." This byte is transmitted 20 times, and then the next six bits, plus control bits, are sent 20 times, and so on. Error correction is performed by majority logic on reception. A random line bit error rate of one bit error per 10^6 improves to one bit error per 10^{17} after error correction.

5.3.3 Loopback operation

When the local loop command is active at the RS-449 interface, the transmit data from the RS-449 interface are looped back after passing through only the first stage of many levels of encoding. When the remote loop command is active at the RS-449 interface, a remote loop code is sent over the T1 line. It is interpreted at the remote end after passing through all but one level of decoding. The remote DSU-DP logic then returns the code and the originating end loops the data from its transmit line to its receive line.

A "fly-wheel" mechanism is used to turn the remote loop made on and off. To turn it on, the remote loopback code must be received three times in a row. It is turned off when no remote loopback code is received in five successive bytes.

5.4 Analog carrier data set

The 201C data set is a 2.4-kb/s synchronous private-line modem. This full duplex data set has a 4-wire, 600-ohm analog interface. The digital interface is the RS-232C interface described above. To prevent the data set and carrier system from over-driving each other, a resistive attenuator must be placed between the two.

The 201C uses phase-shift keyed modulation to send digital data over a 3002-type private line channel.

VI. PERIPHERAL ACCESS

The basic architecture for the peripheral access can be seen in Fig. 1. The peripheral busses and fanout circuit packs are duplicated and dedicated to a particular processor. The peripheral bus, which interconnects the processor and the fanouts, contains a unidirectional address bus and a bidirectional 8-bit data bus. For reasons of electrical loading and fault resolution, the peripheral busses for the home frame are separate from those for the mate frame. Each fanout board connects to its associated peripheral circuits via a set of wires which is common with its mate fanout board. The peripheral circuit packs are divided into groups of eight which share a common set of leads from the duplicated fanout boards. The peripheral bus is dc-coupled, as is the interface between the fanout boards and the peripheral circuits.

6.1 Fanout circuit pack

The fanout circuit pack provides the following functions:

(*i*) Recognition of its address on the peripheral bus.

(*ii*) Enabling of the addressed peripheral circuit(s).

(*iii*) Writing a single bit of data to an addressed peripheral circuit.

(*iv*) Reading digital data or an analog voltage level from a group of eight peripheral circuits.

(*v*) Generation of error-checking signals to verify proper addressing.

6.1.1 Data flow

The data paths shown in Fig. 9 provide for both reading and writing of peripheral circuit packs, as well as control of the fanout circuitry which permits measurement of analog signal levels from the peripheral packs.

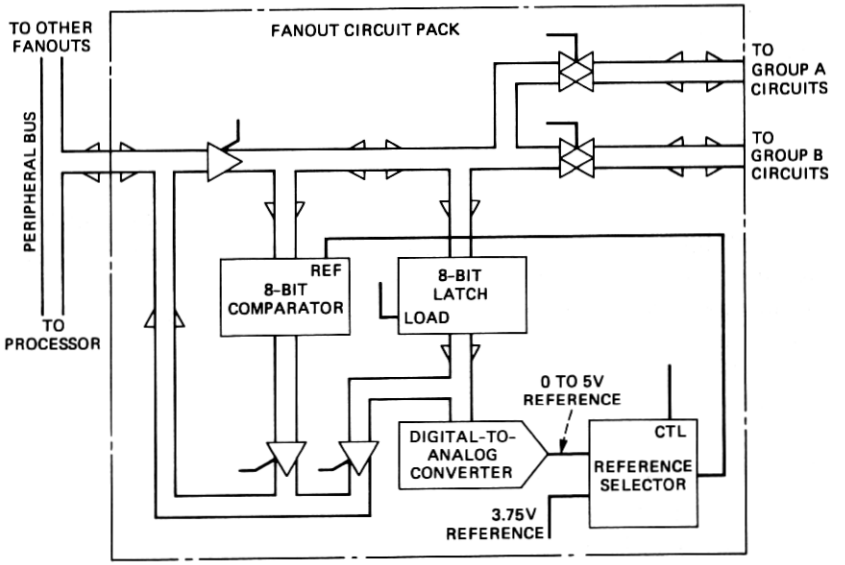

Fig. 9—Fanout data paths.

The data paths for the write operation are straightforward. The buffers which receive data from the processor (via the peripheral bus) are turned on by the lack of the READ signal. One of the two groups of analog switches is turned on, steering the data to the addressed circuit group. Within this group, each of the eight circuit packs receives one of the eight data leads. One of the peripheral packs is then enabled by the addressing logic (see below) to receive its data bit. Thus, writing is performed on a single-bit basis.

The read operation is more complex. One of the two groups of analog switches is turned on as before, gating a signal from each of the eight circuit packs into its corresponding comparator. The reference inputs of all eight comparators are supplied with the output from a digital-to-analog converter (DAC) located on the fanout board. The DAC can be program-controlled to provide an output from 0.0 volts through 5.0 volts in 25-mV steps. Alternatively, a control lead on the peripheral bus can select a fixed 3.75-volt reference. The READ signal turns on the buffers which gate the comparator outputs onto the peripheral bus. Thus, 8 data bits are returned—the results of the 8 comparisons of the voltages from the circuit packs against the selected reference.

The 3.75-volt fixed reference is provided to assist certain interrupt-level programs which perform directed (i.e., nonsequential) read operations. This reference is selected on all fanout boards by a single bit in a processor register in contrast with the DAC reference, which is controlled by a register on each fanout board. By selecting the fixed

reference, the interrupt-level program is relieved of the task of saving and restoring the DAC setting during each operation. The 3.75-volt reference value was chosen to be optimal for scanning lines.

6.1.2 Addressing

Figure 10 shows the peripheral address format and the associated fanout circuitry. The address bits on the peripheral bus can be considered in three groups: those bits which select a particular fanout board and circuit group, those bits which select a peripheral circuit pack within the group of eight, and those bits which select particular circuits and functions within a peripheral circuit pack.

The address bits which select a particular fanout board are present in the peripheral bus in both their true and complemented form. The address for a particular fanout board is determined by the wiring of its connector position such that a unique combination of true and complemented bits is presented to the NOR gates which enable the pack. Each fanout board accesses two electrically separate groups of eight circuit packs. The access to these groups is kept as separate as possible for reliability reasons, but the required circuitry is placed on a single fanout board for economic considerations. Thus, the fanout board has two enabling NOR gates whose addresses differ only in the group-select bit (bit 9).

Address bits 6 through 8 are used in write operations only and serve to select the single circuit pack to be written. These bits are decoded on the fanout board to generate a single write pulse in the proper group when a write timing pulse is received from the processor. If the operation is a read rather than a write, a common READ signal is sent to all eight packs in the group.

The remaining address bits (0 through 5) are simply passed on to the selected circuit group. They are bussed to all eight circuit packs, where they are used to address particular circuits and functions within the packs. Bits 0 through 2 are called the circuit select bits, and bits 3 through 5 the function select bits, corresponding to their usage on line interface circuit packs. This usage, however, is not universal.

6.1.3 Miscellaneous operations

The fanout board reserves the address combinations of function code 7 with circuit select codes 4 through 7 for internal operation involving the DAC. One code is used to read or write the 8-bit register which provides the input to the DAC. Another code gates the output from the DAC to the data input of one of the comparators. By performing a read of this address and using the fixed reference, the DAC output can be compared to the 3.75-volt reference as a maintenance check.

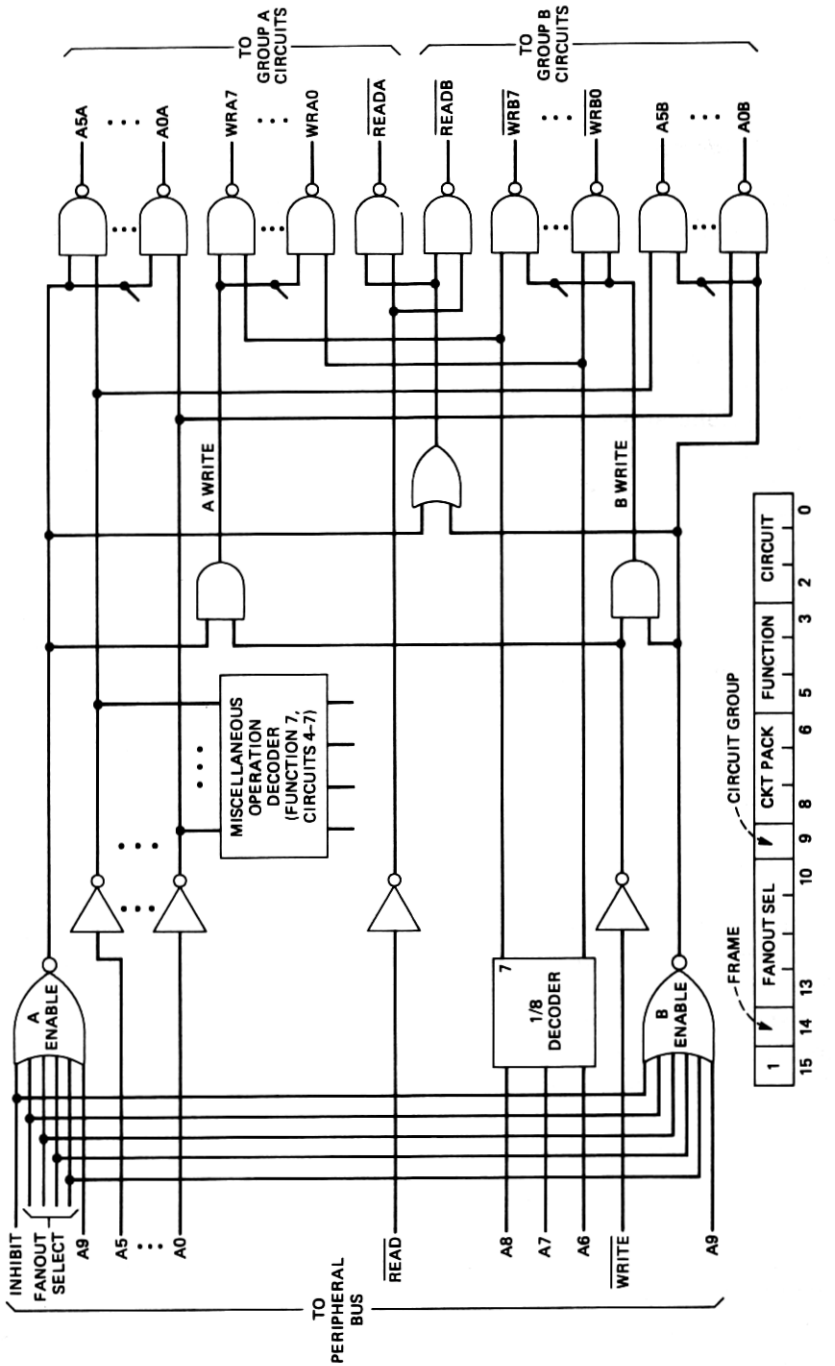

Fig. 10—Fanout addressing.

6.1.4 Error detection

The fanout board returns address checking signals to the processor during every operation. A parity signal is reconstructed from the fanout board selection and from the address, read, and write signals which the fanout sends to the peripheral circuits. The result is returned to the processor on a one-out-of-two basis. The processor can then check the parity signal received against the expected parity computed over the address bits. This check gives assurance that the correct circuit was addressed. Verification of the data paths is left to program checks which observe the operation of the controlled circuits.

6.2 Peripheral timing

Peripheral read and write operations take 6.5 μs. The timing on the peripheral bus is shown in Fig. 11. Initially, all address and control signals are high. The cycle begins when the processor places the address on the bus. In the case of a read cycle, the READ signal goes low, 1.0 μs later. The selected fanout board passes the READ signal and the low-order address bits to the circuit packs in the selected group. The voltages returned from these packs pass through the comparators on the fanout board, and the resulting digital signals returned to the processor on the data bus. The processor latches up the returned data about 0.5 μs before the end of the cycle. The address and READ signals then go high, ending the operation. While the READ signal is active, the fanout board also returns the parity check signal used for address verification.

In the case of a write cycle, the processor places the data on the bus about 0.5 μs after the address. After a 2.0-μs delay to ensure that the address and data have reached the peripheral circuit, the processor

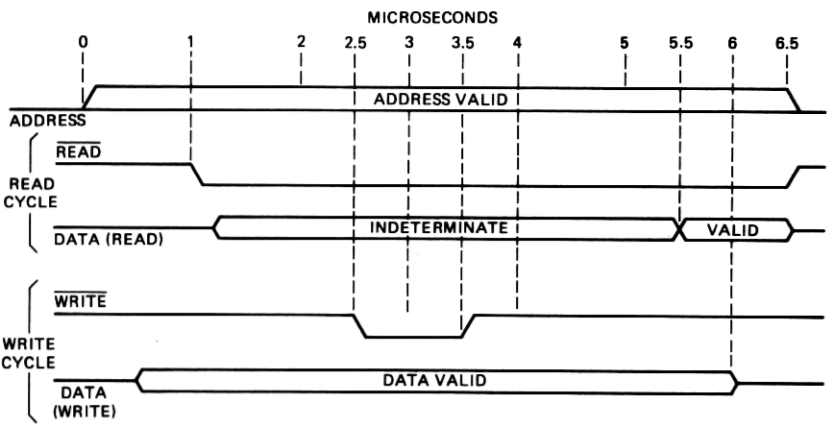

Fig. 11—Peripheral timing.

generates a 1.0-μs write pulse. The fanout board passes this write pulse to the addressed circuit pack and returns a parity check signal. The processor then provides a 2.5-μs hold time on the address and data before ending the cycle.

VII. MAINTENANCE PANEL

The maintenance panel provides the local human interface to the RSS frame. Inasmuch as the primary control of the RSS is from the host ESS via the data link, the maintenance panel assumes a position of minor importance. It is provided mainly as a convenience for certain maintenance operations. Accordingly, the design objective of simplicity took precedence over providing additional functions and even over making the processor-to-panel interface tolerant of faults in the off-line processor.

The panel keys and indicators, shown in Fig. 12, can be separated into two groups: those which have a direct interaction with the hardware, and those which only connect to I/O ports on the processors.

7.1 Direct hardware interactions

There are five keys and two indicators which fall in this category. The two RMV PWR (remove power) keys and the RST PROC POWER (restore process power) key are used to remove and restore power from a processor complex. They directly control the relays which sequence the processors' power. The two associated PWR OFF indicators are controlled by these relays to show that power has been removed. To reduce the likelihood of an unfortunate human error, the RMV PWR keys are individually enabled under processor control. The circuitry which performs this function, however, is not part of the maintenance panel but is located on the Power Alarm and Monitor circuit pack which is accessed via a fanout board.

The PANEL PWR key simply removes and restores power to the panel indicators. As a safety precaution, the other panel keys are disabled whenever the indicator power is off.

An additional SYSTEM BOOTSTRAP key, not shown in the figure, provides a direct reset to both processors. This key provides a means, independent of the data links, to force the system to its highest level of initialization.

7.2 System status indicators

Nine indicators are controlled by the processor to indicate the system status. These are

(*i*) MAJOR, MINOR, and CRITICAL, which are the standard system alarm indicators.

(*ii*) MASTER PWR ALARM, which indicates a blown fuse or trouble with a power converter.

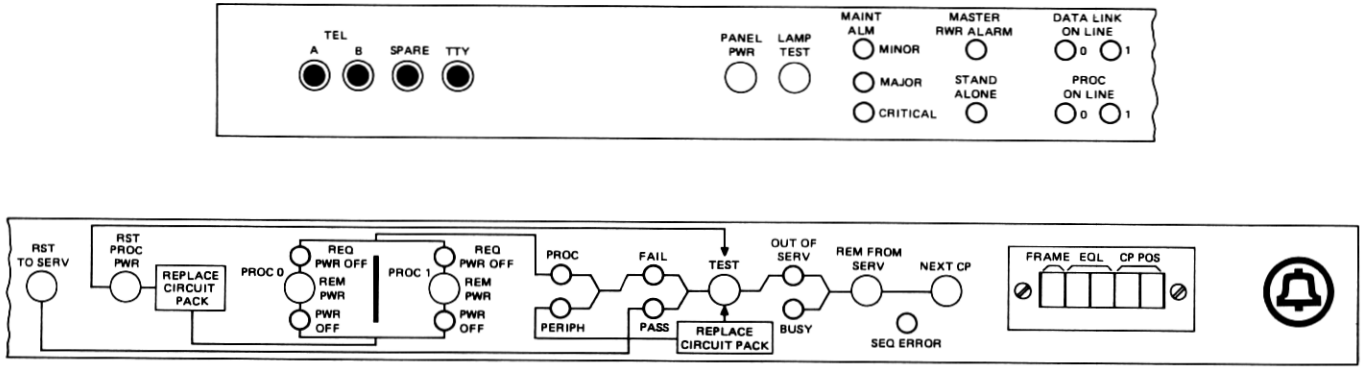

Fig. 12—No. 10A RSS maintenance panel.

(*iii*) STAND ALONE, which indicates that the system is operating without a data link to the host.

(*iv*) The two DATA LINK ON LINE indicators.

(*v*) The two PROCESSOR ON LINE indicators.

7.3 Diagnostic control keys and indicators

The remaining keys and indicators and the digital display are used by a craft person who is attempting to repair a fault by replacing circuit packs. To do this, the RSS is first "primed" with a list of suspect circuit packs. When this has been done, pressing the NEXT CKT PACK (next circuit pack) key will step through this list, displaying each pack's equipment location in the digital display. The pack indicated in the display can be removed from service, tested, and restored to service by means of the other panel keys. The other indicators inform the craft person of the results of tests and indicate other actions which should be taken. For example, the REQ PWR OFF (request power off) lamps indicate when power should be removed before replacing a defective circuit pack in a processor complex.

7.4 Processor interface

The processor interface was designed to require a minimum of circuitry in the panel itself. Each indicator is controlled directly by a lead to a processor I/O port. The digital display contains its own latches to hold the digit values, and the processor interface consists of four leads to carry the binary-coded value and five-digit enable leads to load this value into one of the digit positions. These leads as well are driven by I/O ports in the processor. Each key simply grounds a corresponding lead to each processor. These leads connect to bits of an I/O port which is periodically scanned to detected operated keys.

The processor I/O ports which drive the indicators and the digital display are simply wire OR-ed together by the connecting cable. Thus, either processor can keep an indicator on or ground one of the control leads to the display. The only indicators not wired in this fashion are the PROCESSOR ON LINE indicators, where each processor controls only its own, and the REQ PWR OFF indicators, where each processor controls the indicator for its mate. The keys, on the other hand, each have a separate contact for each processor. This prevents a fault in one processor from making it appear to the other processor that a key has been pressed.

VIII. *PROMUS*

The *PROMUS* reprogrammer is a piece of bench-top equipment (J1C144A) that programs or reprograms memory circuit packs used to

Table I—Programming time for *PROMUS* compatible memory packs

System	Circuit-Pack Type	Size	Approximate Programming Time
RSS	Program store	64K by 9	1.5 h
RSS	Processor B	8K by 9	12 min
RSS	Remote line test	6K by 8	8 min
PUC DL/DCT	Program store	16K by 9	25 min
PUC DL/DCT	Processor	8K by 8	10 min
PUC DL	Line interference CCIS	8K by 8	10 min
PROMUS	Program store	28K by 9	40 min

store firmware. Circuit packs containing EPROM devices to be updated must be removed from the RSS and first placed in the *PROMUS* reprogrammer's erase chamber. Ultraviolet (UV) light erases the old data in all the EPROMS. The new data to be programmed may be obtained from a remote computer via a dial-up data link, or may be copied from an already-programmed memory circuit pack. The sequencing needed to program each EPROM is performed by a control complex in the *PROMUS* using a *BELLMAC*-8 microprocessor. After the data are programmed, they are extensively verified.

The initial version of the *PROMUS* reprogrammer can program two circuit packs at once; the later version will provide eight programming slots. Because of the ease of reconfiguration, any of the circuit packs listed in Table I may be programmed. Other circuit pack types or systems may be added in the future. The set of signals at the edge connector of these circuit packs provides all the control necessary to individually program the many EPROM devices on a given circuit pack. This allows the *PROMUS* equipment to update firmware on a circuit-pack basis; there is no need to remove the devices from the board. A potential reliability problem is eliminated by not placing a large number of devices in sockets.

The erase operation requires 45 minutes, and may be done at the same time a pack in the programming chamber is being programmed or verified. Operations are invoked by typing commands on a hard-copy terminal connected to the *PROMUS* reprogrammer.

IX. CONCLUSION

The RSS processor complex has proven to have sufficient processing capacity and long-term reliability.

X. ACKNOWLEDGMENTS

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