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Parasitic Insensitive, Biphase Switched Capacitor Filters Realized With One Operational Amplifier Per Pole Pair

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Practical techniques are given for reducing the number of operational amplifiers (op-amps) in switched capacitor filters. Op-amp count is typically reduced to one op-amp per pole pair, while maintaining the insensitivity to top and bottom plate parasitics heretofore associated with one-op-amp-per-pole structures. These techniques are used to develop a parasitic insensitive single amplifier resonator and a general single amplifier biquad. Next, complete design procedures are given for these circuits. Finally, the same methods are applied to leapfrog structures, where similar op-amp savings are demonstrated.

I. INTRODUCTION

The use of active switched capacitor (SC) filters[1-3] as constituents in large-scale integrated (LSI) subsystems[3-10] has been rapidly expanding. Crucial to the realization of manufacturable metal-oxide-semiconductor (MOS) SC filters has been the development of parasitic insensitive SC networks.[6,11,12] As a consequence, it has become a commonly accepted notion that insensitivity to both top and bottom plate parasitic capacitances requires realization with one op-amp per pole (i.e., two op-amps per pole pair). However, since op-amps consume power, represent about 20 percent of a filter's die area, and are sources of noise and power supply feed, it is useful to consider techniques that reduce the number of op-amps required to implement a given transfer function. The purpose of this paper is to introduce practical techniques for achieving this, while retaining the crucial parasitic insensitivities mentioned previously. A straightforward technique for reducing op-amp count is to time share or multiplex[13,14] each op-amp among two or more storage capacitors. A problem with this approach is that each op-amp operates without feedback during the dead zones of the non-

overlapping clocks and can drift to one of the supply rails. To remedy this problem, a simple SC feedback circuit is introduced which ensures that closed loop stability is maintained at all times. In addition to the stability problem, multiplexing within a single filter tends to result in a parasitic-sensitive implementation.[14] This is because many operations within such a filter involve sensing voltages during a clock phase and transferring a proportional charge during a latter phase. In the past, when inverting transfers of this nature were needed, the only recourse has been to use the parasitic-sensitive "toggle" switched capacitor. However, using the parasitic-compensated integrators[15,16] introduced by the authors, SC filters involving multiplexed op-amps can be realized which are insensitive to parasitics. In this paper, we show how additional features provided by these new integrator realizations enhance the design flexibility available with multiplexed op-amp SC structures. In addition, we develop practical, parasitic-insensitive realizations for single-amplifier biquads and $N/2$ op-amp Nth order* leapfrog structures. The op-amp-reduced circuits are derived step-by-step from conventional one-op-amp-per-pole prototypes.

II. NEW PARASITIC-COMPENSATED SC INTEGRATOR REALIZATIONS

Prior to developing the single-amplifier biquad, let us review the parasitic-compensated integrators[15,16] mentioned in the previous section. Consider first the integrator in Fig. 1a with the relevant parasitic capacitances at nodes 1 and 2 denoted as C_{p1} and C_{p2}, respectively. To establish the conditions for parasitic insensitivity, let us first determine the voltage across the holding capacitor at node 2 during the even (e) time slot. From Fig. 1b it follows that

$$V_2^e = \frac{2C}{4C + C_{p1} + C_{p2}} V_{\text{in}}^e. \tag{1}$$

Hence, the net charge transferred to the integrating capacitor D, during the odd(o) time slot (obtained from the circuit in Fig. 1c) is

$$Q^o = (2C + C_{p2}) z^{-1/2} V_2^e \tag{2}$$

$$= \frac{2C(2C + C_{p2}) z^{-1/2}}{4C + C_{p1} + C_{p2}} V_{\text{in}}^e. \tag{3}$$

Note that if we set $C_{p1} = C_{p2} = C_p$, terms involving the parasitics cancel, i.e.,

$$Q^o = C z^{-1/2} V_{\text{in}}^e$$

* For N odd, $(N + 1)/2$ op-amps are required.

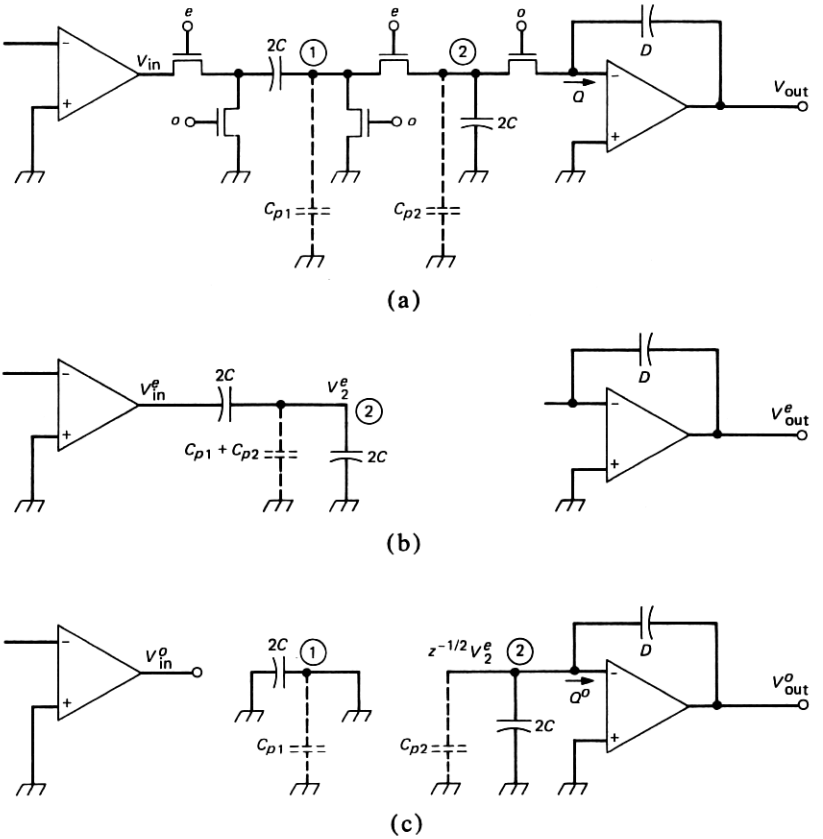


Fig. 1—Parasitic-compensated inverting integrator. (a) Complete circuit with parasitic capacitances. (b) *e*-phase connectivity. (c) *o*-phase connectivity.

when

$$C_{p1} = C_{p2} = C_p. \tag{4}$$

In practice, equality of $C_{p1} = C_{p2}$ is obtained by matching the geometries of the switches connected to nodes 1 and 2, and by matching the routing associated with nodes 1 and 2 using careful layout. In contrast, predistorting[14] the capacitors to compensate for parasitics is an imprecise operation because of the lack of tracking between unlike capacitors. It should be noted that in the proof given by eqs. (1) to (4), the parasitic capacitors were assumed to be linear. A more general proof establishing the validity of the matching conditions when the parasitics are nonlinear is given in Ref. 16. Throughout the remainder of this text, we shall assume parasitic matching when such an integrator is used. Under these circumstances, the input/output relations become

$$V_{\text{out}}^{o} = \frac{-[C/D]z^{-1/2}}{1 - z^{-1}} V_{\text{in}}^{e} \tag{5a}$$

and

$$V_{\text{out}}^{e} = \frac{-[C/D]z^{-1}}{1 - z^{-1}} V_{\text{in}}^{e}. \tag{5b}$$

Note that the classical inverting toggle-switched integrator shown in Fig. 2 has the same transfer functions. However, by virtue of the matched parasitics, the implementation in Fig. 1 is parasitic insensitive. We, therefore, refer to the input circuit of this integrator as a parasitic-compensated toggle (PCT).

The noninverting integrator realization in Fig. 3 obtains its parasitic insensitivity via the same matching condition derived for the inverting integrator in Fig. 1. Derivation of the conditions for parasitic insensitivity follows identically that given in eqs. (1) through (4); hence, it will not be shown. Perhaps more interesting are the input/output relations, which are given below:

$$V_{\text{out}}^{e} = \frac{[C/D]z^{-1}}{1 - z^{-1}} V_{\text{in}}^{e} \tag{6a}$$

and

$$V_{\text{out}}^{o} = \frac{[C/D]z^{-3/2}}{1 - z^{-1}} V_{\text{in}}^{e}. \tag{6b}$$

Particular attention is directed to the extra one-half-clock-period delay produced by this circuit when compared to the standard noninverting structure.[1-3] We shall see in later sections that this extra delay, heretofore available only by using additional clock phases, provides considerable flexibility for multiplexing op-amps in switched capacitor filters. In further references to the structure in Fig. 3, proper parasitic matching will be assumed. Since the input circuit to the integrator in Fig. 3 provides inversion at the summing junction, it will be referred to as an inverting parasitic-compensated toggle (IPCT).

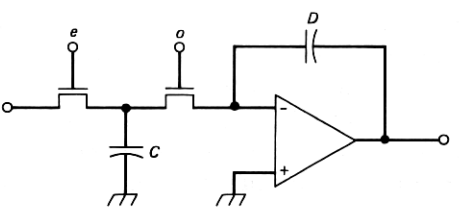


Fig. 2—Classical inverting toggle-switched integrator.

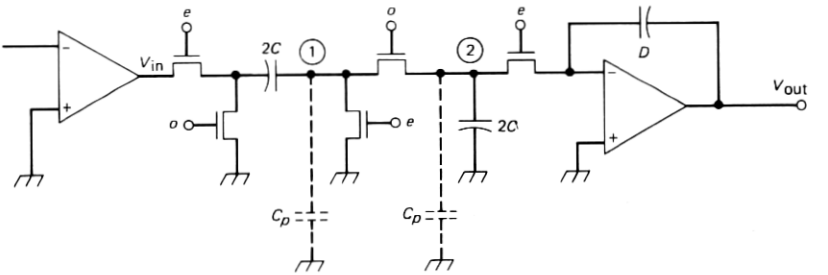


Fig. 3—Parasitic-compensated noninverting integrator.

III. ALL POLE, PARASITIC-INSENSITIVE, SINGLE-AMPLIFIER SC BIQUAD

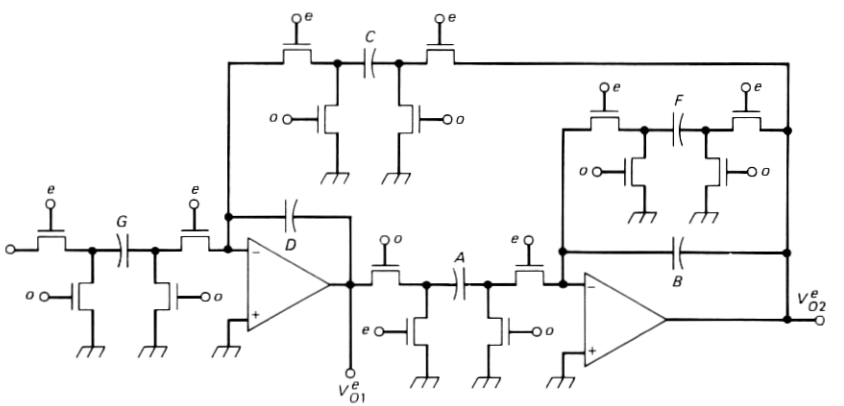
To begin the derivation of the single-amplifier biquad, consider the conventional, parasitic-insensitive two-op-amp biquad[11,12] in Fig. 4a. The transfer functions[12] to each of the op-amp outputs (V_{o1}, V_{o2}) are readily obtained from the z-domain equivalent circuit[3,12,17] in Fig. 5a. That is,

$$T = \frac{V_{o2}^e}{V_{in}^e} = \frac{-AGz^{-1}}{D(B+F) - (2DB + DF - AC)z^{-1} + DBz^{-2}} \tag{7a}$$

and

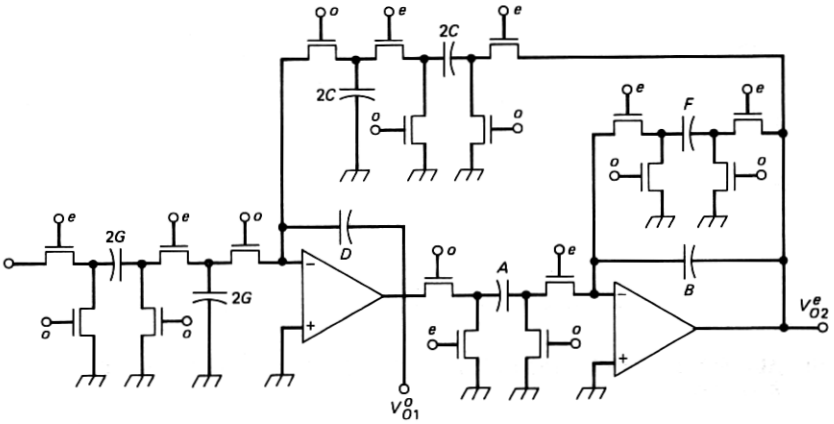
$$T' = \frac{V_{o1}^e}{V_{in}^e} = \frac{-G(B + F - Bz^{-1})}{D(B+F) - (2DB + DF - AC)z^{-1} + DBz^{-2}}. \tag{7b}$$

Let us now replace the SC elements G and C with corresponding PCTS according to the schematic in Fig. 1a. The resulting circuit is shown in



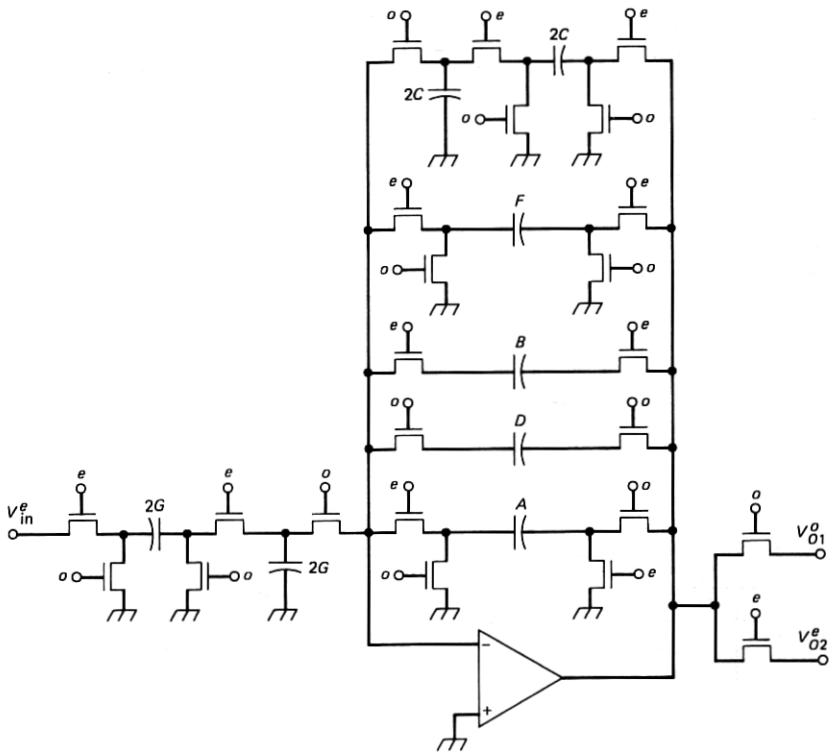
(a)

Fig. 4a—Switched-capacitor all-pole biquad—parasitic-insensitive realization.



(b)

Fig. 4b—Switched-capacitor all-pole biquad—parasitic-compensated equivalent to Fig. 4a.



(c)

Fig. 4c—Switched-capacitor all-pole biquad—single-amplifier equivalent to Fig. 4b.

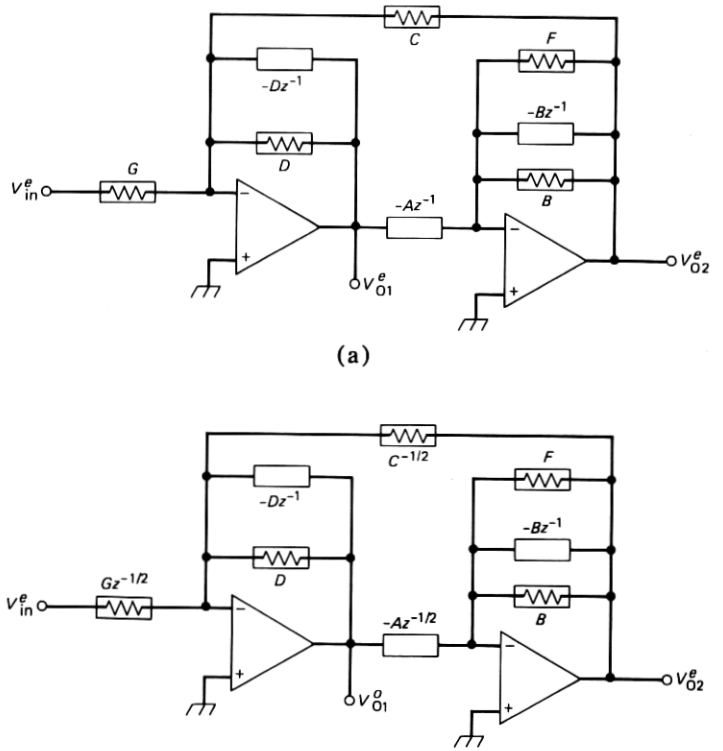


Fig. 5—Switched-capacitor all-pole biquad equivalent circuits. (a) Equivalent circuit for the sc biquad in Fig. 4a. (b) Equivalent circuit for the sc biquads in Figs. 4b and 4c.

Fig. 4b and its z-domain equivalent in Fig. 5b. The following observations regarding the biquads in Figs. 4a and 4b can be made:

(*i*) In both circuits, the integrating (storage) capacitors are updated during only one clock phase. During their respective hold phases, the op-amps are idle.

(*ii*) In the circuit of Fig. 4a, storage capacitors D and B are updated during the same phase (in this case the e-phase). In contrast, for the circuit of Fig. 4b, storage capacitors D and B are updated on alternate phases.

(*iii*) Referring to the equivalent circuits in Fig. 5a and 5b, we see that the loop gains for both circuits are identical. The only difference is the additional half-clock-period delay in the transfer function introduced for the first op-amp output. The delay between the filter input and the output of the second op-amp is the same in both cases. The transfer functions for the biquad in Fig. 4b are

$$\frac{V_{o2}^{e}}{V_{in}^{e}} = \frac{-AGz^{-1}}{D(B+F) - (2DB + DF - AC)z^{-1} + DBz^{-2}} \tag{8a}$$

and

$$\frac{V_{o1}^{o}}{V_{in}^{e}} = \frac{-z^{-1/2}G(B + F - Bz^{-1})}{D(B+F) - (2DB + DF - AC)z^{-1} + DBz^{-2}}. \tag{8b}$$

Reflecting on observation (1), it is seen that since each op-amp is idle during half the time, all the processing might be performed by one op-amp. Since, in addition, capacitors B and D are updated during alternate clock phases, according to observation (2), the two op-amps in Fig. 4b can be replaced with a single op-amp, multiplexed between the two storage capacitors D and B. The resulting single amplifier circuit is shown in Fig. 4c.

Let us now make some observations regarding the single-amplifier biquad in Fig. 4c.

(*i*) Biquads 4b and 4c share the same equivalent circuit (Fig. 5b). It will often be found that the equivalent circuit is a convenient mechanism for "untangling" single-amplifier biquads so that they may be analyzed in a straightforward fashion. Thus, the equivalent circuit provides a useful link between the single-amplifier biquad and its two-op-amp counterpart.

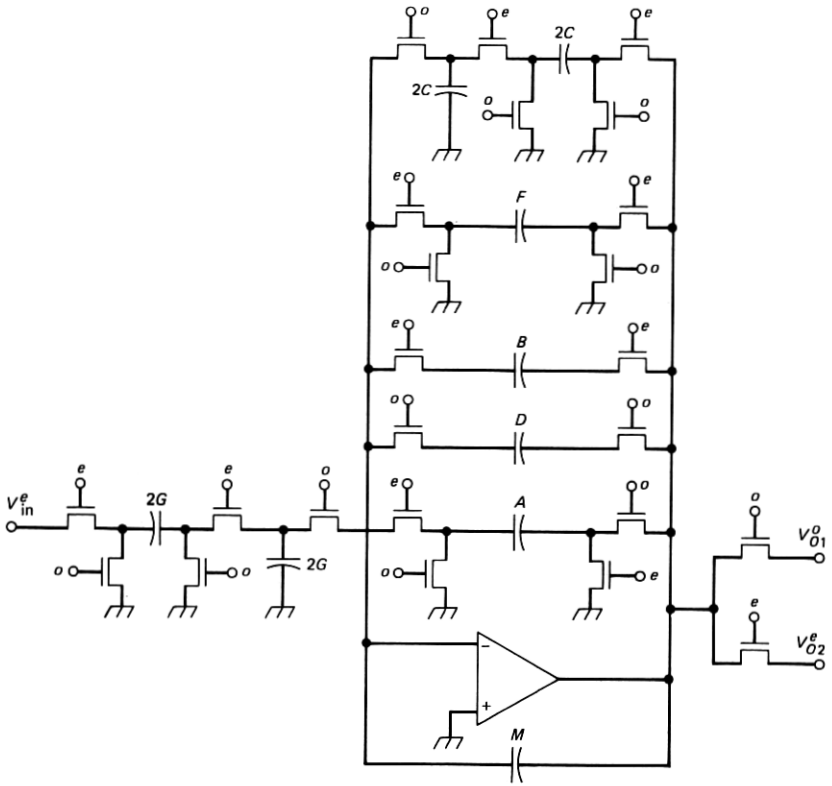
(*ii*) It has been shown that to multiplex the op-amps within a two-amplifier biquad, the storage capacitors must be updated during different clock phases. Hence, the use of either PCTs or parasitic-sensitive toggles[14] seems unavoidable.

(*iii*) The two transfer functions in eqs. (8a) and (8b) are available at the op-amp output on alternate phases. Sampling the output on the *e*-phase yields eq. (8a), while sampling on the *o*-phase yields eq. (8b).

(*iv*) Damping is provided by a switched capacitor which has been called "*F*-type" damping.[12] Referring to the two op-amp biquad in Fig. 4a, an alternative form of damping is obtained by placing an unswitched capacitor across switched capacitor C. This has been called[12] "*E*-type" damping. Unfortunately, *E*-type damping constrains the D and B charge updates to occur on the same phase. Consequently, *E*-type damping is not available in single-amplifier biquads.

Now that the basic implementation has been derived, let us examine the integrity of the feedback loop as the switches open and close. Since the clocks are nonoverlapping, it is readily seen that there are periods of time during which the op-amp in Fig. 4c operates without feedback. Clearly, this is a potentially dangerous circuit condition.

An interesting but impractical way to maintain loop closure is to place an unswitched capacitor of value M across the op-amp as shown in Fig. 6a. Although the M capacitor solves the stability problem, an



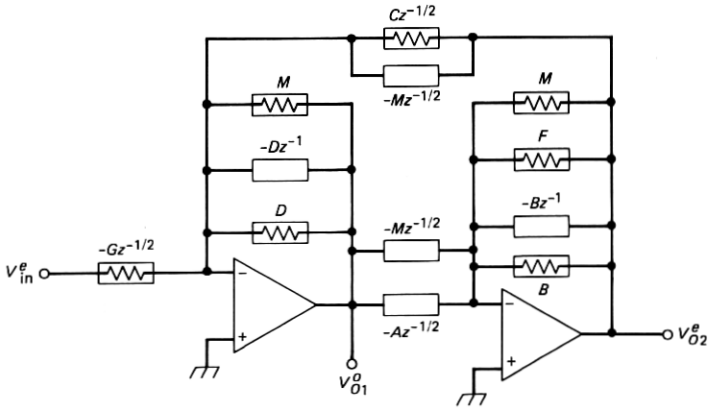
(a)

Fig. 6a—Single-amplifier biquad stabilization via continuous feedback—circuit schematic.

analysis of this circuit reveals the impracticality of the solution. Since the results of the analysis are rather interesting we present them, in spite of our reluctance to recommend the M capacitive feedback. First, let us examine the equivalent circuit in Fig. 6b. Note that while in the actual SC circuit the M capacitor appears once, in the equivalent circuit it appears virtually everywhere. This is a consequence of the fact that M introduces coupling between B and D. Using the equivalent circuit in Fig. 6b, the transfer functions for the two-op-amp outputs can be easily derived. For this presentation we need only concern ourselves with output V^e_{o2}, i.e.,

$$\frac{V^e_{o2}}{V^e_{in}} = \frac{-(A+M)Gz^{-1}}{\{D(B+F)+M(B+D+F)+M^2\}-\{2DB+DF-AC+M(B+D+A-C)\}z^{-1}+DBz^{-2}}. \quad (9)$$

Because of the coupling provided by M, the coefficient for the constant



(b)

Fig. 6b—Single-amplifier biquad stabilization via continuous feedback—equivalent circuit.

term of the denominator depends quadratically on M. In addition, M provides a leakage path for both B and D which can severely enhance the damping heretofore provided by F alone. In order for M to have an insignificant effect on the circuit performance, $DF \gg M(B + D)$, where B and D are typically large, while F is near minimum value. Hence, if B and D are roughly equal, then $M \ll F/2$. Capacitor M is then too small to be practical.

A practical solution which does not affect the biquad's transfer characteristic is illustrated in Fig. 7. The SC network involving X and Y is seen to provide feedback around the op-amp when both clocks e and o are low, i.e., the dead zones of the nonoverlapping clocks. When either e or o is high, X, Y simply introduce capacitance to ground from the op-amp summing junction and output, respectively. The values of X and Y are relatively unimportant and can be set conveniently to one unit each. The crosstalk introduced by this arrangement is insignificant. If the clock rise and fall times are reasonably fast, the opportunities for crosstalk, i.e., interaction between X, Y and B, D, are minimal. Even if this is not the case, the interaction is self-compensating. For example, if X, Y happen to pull out of the loop more slowly than D enters the loop, some fraction of the charge stored on D will leak onto X, Y. However, when the X, Y common junction is grounded, the charge which previously leaked off D is returned to it. This self-compensating property will be imperfect as a consequence of finite op-amp gain. However, for op-amp dc gains of 1000 or more, the interaction between X, Y and B, D will be negligible. Thus, the X, Y SC network provides an elegant and practical solution to the op-amp stability problem.

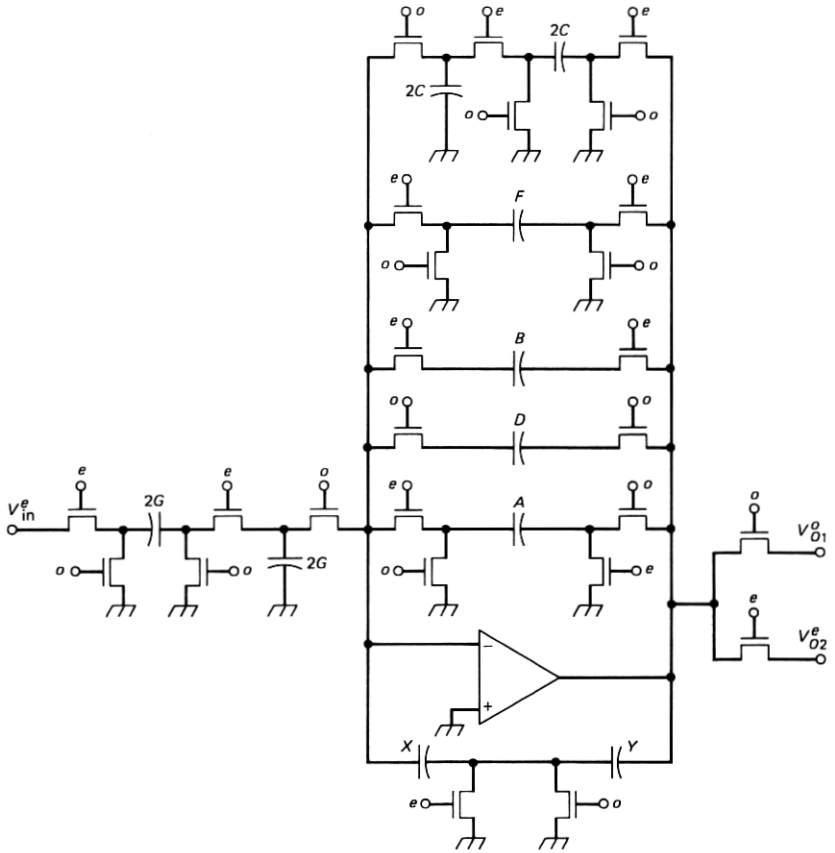


Fig. 7—Single-amplifier biquad stabilization via XY SC feedback.

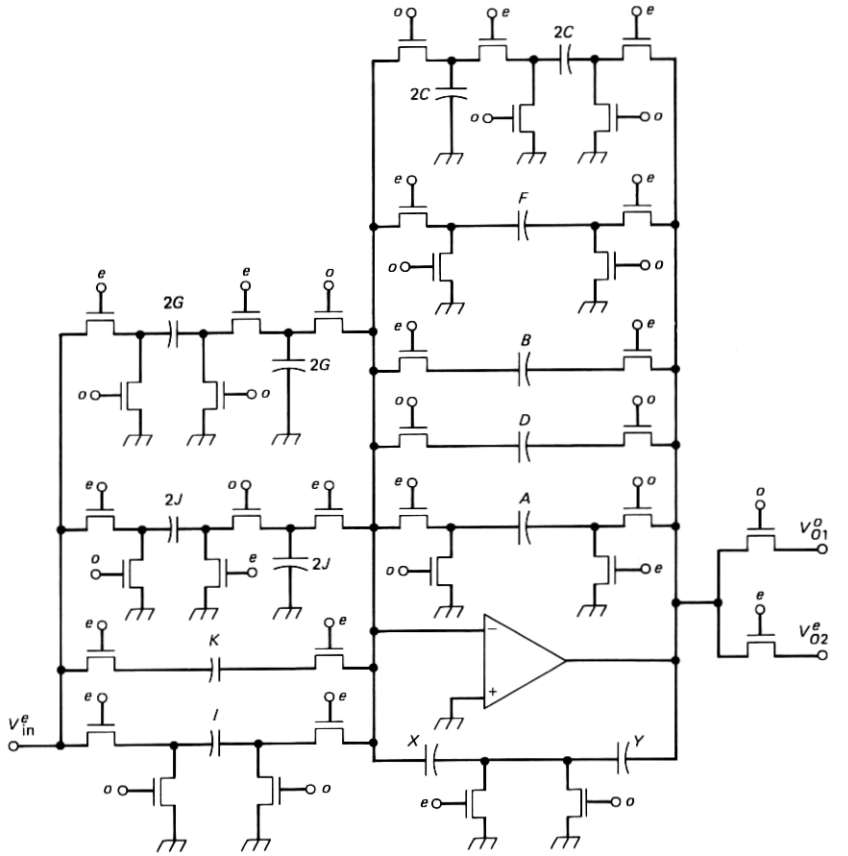
IV. REALIZING SINGLE-AMPLIFIER BIQUADS WITH TRANSMISSION ZEROS

The all-pole resonator in Fig. 7 can be easily generalized to realize transfer functions with transmission zeros by adding the feed forward circuitry shown in Fig. 8a. The z-domain equivalent circuit is given in Fig. 8b. The transfer function for each time slot can be readily derived from the equivalent circuit:

$$T = \frac{V_{o2}^e}{V_{\text{in}}^e} = \frac{\begin{array}{r}-\{D(K+I) - (2DK + D(I+J) - AG)z^{-1} \\ + D(K+J)z^{-2}\}\end{array}}{D(B+F) - (2DB + DF - AC)z^{-1} + DBz^{-2}} \quad \text{(10a)}$$

and

$$T' = \frac{V_{o1}^o}{V_{\text{in}}^e} = \frac{\begin{array}{r}z^{-1/2}\{C(K+I) - G(B+F) \\ - (C(K+J) - GB)z^{-1}\}\end{array}}{D(B+F) - (2DB + DF - AC)z^{-1} + DBz^{-2}}. \quad \text{(10b)}$$

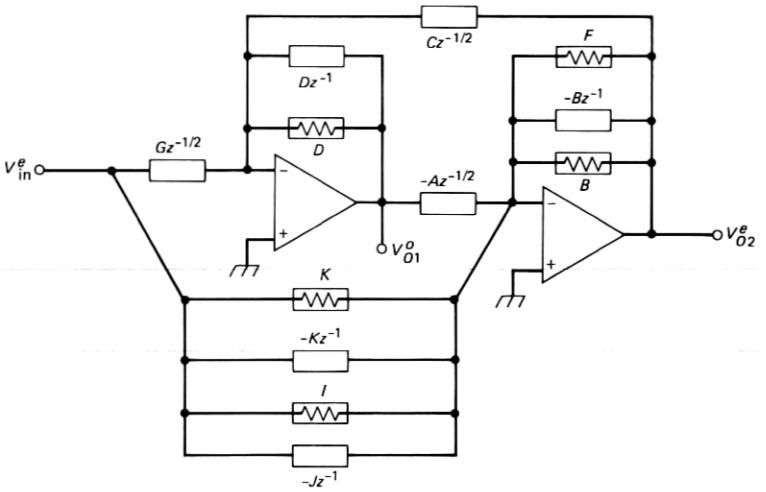


(a)

Fig. 8a—Single-amplifier biquad which realizes the transfer functions in eq. (10)—circuit schematic.

The design of this single-amplifier biquad follows along previously published design procedures[12] for two-op-amp biquads. Note the manner in which the delay property of the IPCT has been exploited. Comparing the transfer functions T and T', we observe that only T has a quadratic numerator. Hence, by focusing our attention on T, little generality and flexibility is lost. As in Ref. 12, we can simplify T by arbitrarily setting $A = B = D = 1$. At the end of the design process, one can adjust the values of A, B, and D to set the gain level of T' and to independently scale the capacitances, which share common time slots. Setting $A = B = D = 1$ in eq. (10a) yields

$$T = \frac{V^e_{o2}}{V^e_{in}} = \frac{-\{(K + I) - (2K + I + J - G)z^{-1} + (K + J)z^{-2}\}}{(1 + F) - (2 + F - C)z^{-1} + z^{-2}} \qquad (11)$$



(b)

Fig. 8b—Single-amplifier biquad which realizes the transfer functions in eq. (10)—equivalent circuit.

If the desired transfer function is given by

$$T = \frac{m\{\gamma - \epsilon z^{-1} + \delta z^{-2}\}}{1 - \alpha z^{-1} + \beta z^{-2}}, \tag{12}$$

the unscaled values for capacitors C, F, G, I, J, and K are obtained by matching the like coefficients of eqs. (11) and (12). For the poles, the design equations are

$$F = \frac{1 - \beta}{\beta} \tag{13a}$$

and

$$C = \frac{1 + \beta - \alpha}{\beta}. \tag{13b}$$

To place the transmission zeros, the general design equations and a simple solution, are given in Table I for each generic filter type.[12] The generic filter types are listed in Table II for convenient reference. Note that the actual capacitor values G, I, J, and K are related to the scaled values $\hat{G}$, $\hat{I}$, $\hat{J}$, and $\hat{K}$ by the relation

$$\hat{x} = (1 + F)x, \tag{14}$$

where

$$x = G, I, J, K.$$

Examining the numerator of T in eq. (11), one observes that real zeros

Table I—Zero placement formulas for T

Filter Type	Design Equations	Simple Solution
LP20	$\hat{K}+\hat{I}=\lvert m\rvert$ $2\hat{K}+\hat{I}+\hat{J}-\hat{G}=-2\lvert m\rvert$ $\hat{K}+\hat{J}=\lvert m\rvert$	$\hat{I}=\hat{J}=0, \hat{K}=\lvert m\rvert, \hat{G}=4\lvert m\rvert$
LP11	$\hat{K}+\hat{I}=0$ $2\hat{K}+\hat{I}+\hat{J}-\hat{G}=-\lvert m\rvert$ $\hat{K}+\hat{J}=\lvert m\rvert$	$\hat{I}=\hat{K}=0, \hat{J}=\lvert m\rvert, \hat{G}=2\lvert m\rvert$
LP10	$\hat{K}+\hat{I}=\lvert m\rvert$ $2\hat{K}+\hat{I}+\hat{J}-\hat{G}=-\lvert m\rvert$ $\hat{K}+\hat{J}=0$	$\hat{J}=\hat{K}=0, \hat{I}=\lvert m\rvert\ \hat{G}=2\lvert m\rvert$
LP02	$\hat{K}+\hat{I}=0$ $2\hat{K}+\hat{I}+\hat{J}-\hat{G}=0$ $\hat{K}+\hat{J}=\lvert m\rvert$	$\hat{I}=\hat{K}=0, \hat{J}=\lvert m\rvert, \hat{G}=\lvert m\rvert$
LP01	$\hat{K}+\hat{I}=0$ $2\hat{K}+\hat{I}+\hat{J}-\hat{G}=-\lvert m\rvert$ $\hat{K}+\hat{J}=0$	$\hat{I}=\hat{J}=\hat{K}=0, \hat{G}=\lvert m\rvert$
LP00	$\hat{K}+\hat{I}=\lvert m\rvert$ $2\hat{K}+\hat{I}+\hat{J}-\hat{G}=0$ $\hat{K}+\hat{J}=0$	$\hat{J}=\hat{K}=0, \hat{I}=\lvert m\rvert, \hat{G}=\lvert m\rvert$
BP10	$\hat{K}+\hat{I}=\lvert m\rvert$ $2\hat{K}+\hat{I}+\hat{J}-\hat{G}=0$ $\hat{K}+\hat{J}=-\lvert m\rvert$	Not realizable
BP01	$\hat{K}+\hat{I}=0$ $2\hat{K}+\hat{I}+\hat{J}-\hat{G}=\lvert m\rvert$ $\hat{K}+\hat{J}=\lvert m\rvert$	$\hat{G}=\hat{I}=\hat{K}=0, \hat{J}=\lvert m\rvert$
BP00	$\hat{K}+\hat{I}=\lvert m\rvert$ $2\hat{K}+\hat{I}+\hat{J}-\hat{G}=\lvert m\rvert$ $\hat{K}+\hat{J}=0$	$\hat{G}=\hat{J}=\hat{K}=0, \hat{I}=\lvert m\rvert$
HP	$\hat{K}+\hat{I}=\lvert m\rvert$ $2\hat{K}+\hat{I}+\hat{J}-\hat{G}=2\lvert m\rvert$ $\hat{K}+\hat{J}=\lvert m\rvert$	$\hat{G}=\hat{I}=\hat{J}=0, \hat{K}=\lvert m\rvert$
HPN and LPN	$\hat{K}+\hat{I}=\lvert m\rvert$ $2\hat{K}+\hat{I}+\hat{J}-\hat{G}=\lvert m\rvert\epsilon$ $\hat{K}+\hat{J}=\lvert m\rvert$	$\hat{I}=\hat{J}=0, \hat{K}=\lvert m\rvert, \hat{G}=\lvert m\rvert(2-\epsilon)$
AP	$\hat{K}+\hat{I}=\lvert m\rvert\beta$ $2\hat{K}+\hat{I}+\hat{J}-\hat{G}=\lvert m\rvert\alpha$ $\hat{K}+\hat{J}=\lvert m\rvert$	$\hat{I}=0, \hat{K}=\lvert m\rvert\beta, \hat{J}=\lvert m\rvert(1-\beta), \hat{G}=\lvert m\rvert(1+\beta-\alpha)$

on alternate sides of $z = 0$ are nonrealizable. As a result, the bilinear bandpass BP10 function is not realizable with this circuit. This is not a severe restriction since the other bandpass types are realizable.

As noted previously, the synthesis equations result in unscaled capacitor values. To obtain properly scaled capacitors, one must first scale the level of V_{o1}^{o} to a suitable level. By adjusting A and D, the level of V_{o1}^{o} (i.e., T') can be scaled without affecting V_{o2}^{e} (i.e., T). More precisely, if the gain constant of T' is to be scaled to

Table II—Generic biquad transfer functions

Generic Form	Numerator $N(z)$
LP20 (bilinear transform)	$m\,(1 + z^{-1})^2$
LP11	$mz^{-1}\,(1 + z^{-1})$
LP10	$m\,(1 + z^{-1})$
LP02	mz^{-2}
LP01	mz^{-1}
LP00	m
BP10 (bilinear transform)	$m\,(1 - z^{-1})(1 + z^{-1})$
BP01	$mz^{-1}\,(1 - z^{-1})$
BP00	$m\,(1 - z^{-1})$
HP	$m\,(1 - z^{-1})^2$
LPN	$m\,(1 - \epsilon z^{-1} + z^{-2}),\ \epsilon > \alpha/\sqrt{\beta},\ \beta > 0$
HPN	$m\,(1 - \epsilon z^{-1} + z^{-2}),\ \epsilon < \alpha/\sqrt{\beta},\ \beta > 0$
AP	$m\,(\beta - \alpha z^{-1} + z^{-2})$
General	$m\,(\gamma - \epsilon z^{-1} + \sigma z^{-2})$

$$T' \rightarrow \mu T', \tag{15}$$

then it is only necessary to scale

$$(A, D) \rightarrow \left|\frac{1}{\mu} A, \frac{1}{\mu} D\right|. \tag{16}$$

The gain constant associated with T will remain constant under this scaling.

Once satisfactory gain levels have been achieved, one can scale all capacitors associated with each time slot so that the minimum capacitance corresponds to a single unit. The two groups of capacitors which are to be scaled together are

Group 1: (C, D, G)
Group 2: (A, B, F, I, J, K).

Note that the capacitors in each group are distinguished by the fact that they are connected to the input node of the op-amp during the same clock phase. The groupings are easily identified in the equivalent circuit where the groupings are determined by the amplifier input they are incident on.

To cascade single-amplifier biquads, it is important that the input be accepted by all feed-ins on the same clock phase. The biquad in Fig. 8 possesses this property.

Note that the inputs to the single-amplifier resonator can be chosen differently from those selected in Fig. 8. An alternate realization is shown in Fig. 9. The transfer functions for this circuit are

$$T = \frac{V_{o1}^e}{V_{in}^e} = \frac{\begin{array}{r}-\{(B + F)(G + L) - [2BL + B(G + H) \\ + F(H + L) + CI]z^{-1} + B(H + L)z^{-2}\}\end{array}}{D(B + F) - (2DB + DF - AC)z^{-1} + DBz^{-2}} \tag{17a}$$

and

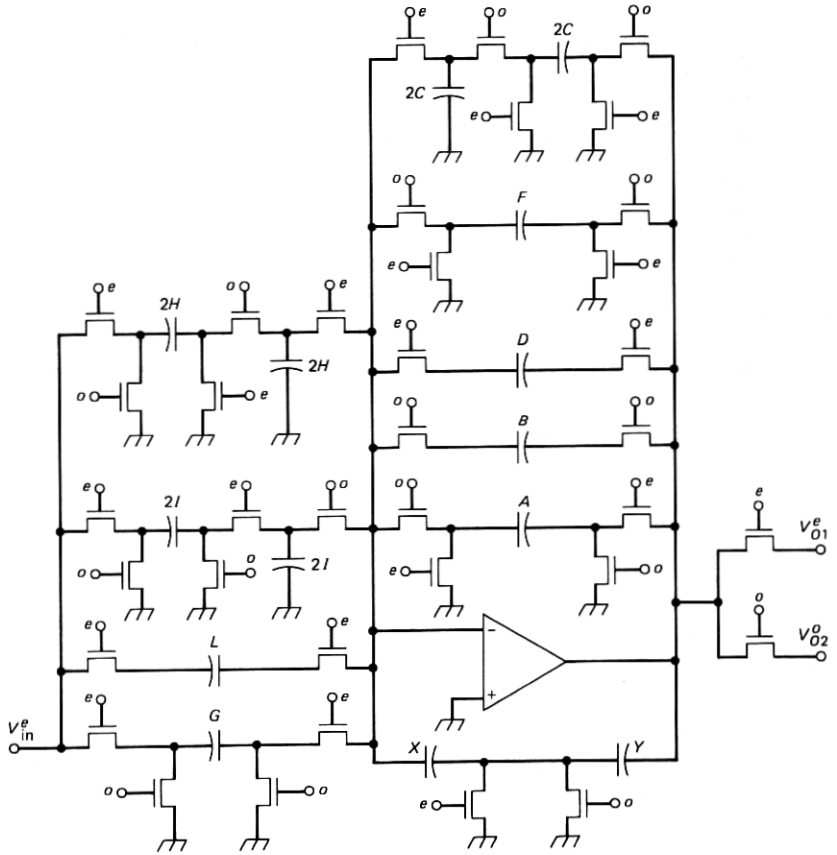
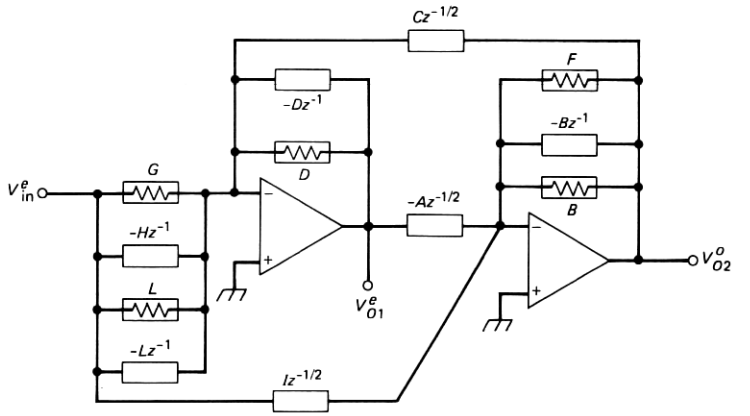


Fig. 9a—Single-amplifier biquad which realizes the transfer functions in eq. (17)—circuit schematic.

$$T' = \frac{V^o_{o2}}{V^e_{in}} = \frac{-z^{-1/2}\{A(G+L) + DI - (A(H+L) + DI)z^{-1}\}}{D(B+F) - (2DB + DF - AC)z^{-1} + DBz^{-2}}. \quad (17b)$$

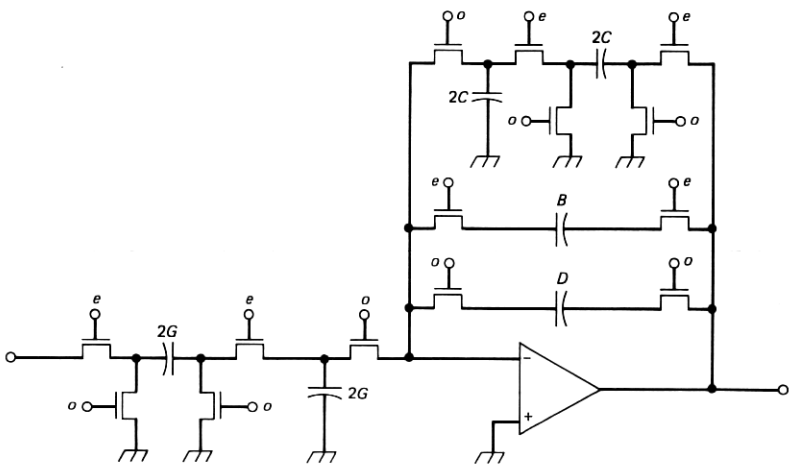
This circuit is not as general as the circuit in Fig. 8, hence, it will not be pursued further.

It is well known[12] that, by sharing switches operating in synchronism between common nodes, the switch count for a given SC filter can be significantly reduced. Circuits involving PCTs can also share switches. Switch sharing for PCT branches is demonstrated in Fig. 10. Note that sharing switches and combining the toggling capacitors $2G$ and $2C$, as shown in Fig. 10b, retains the parasitic cancellation property. In this operation, three switches are saved. Sharing of switches within the



(b)

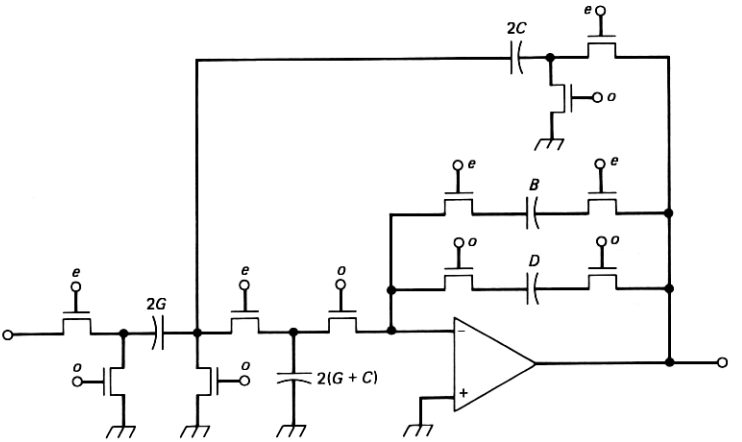
Fig. 9b—Single-amplifier biquad which realizes the transfer functions in eq. (17)—equivalent circuit.



(a)

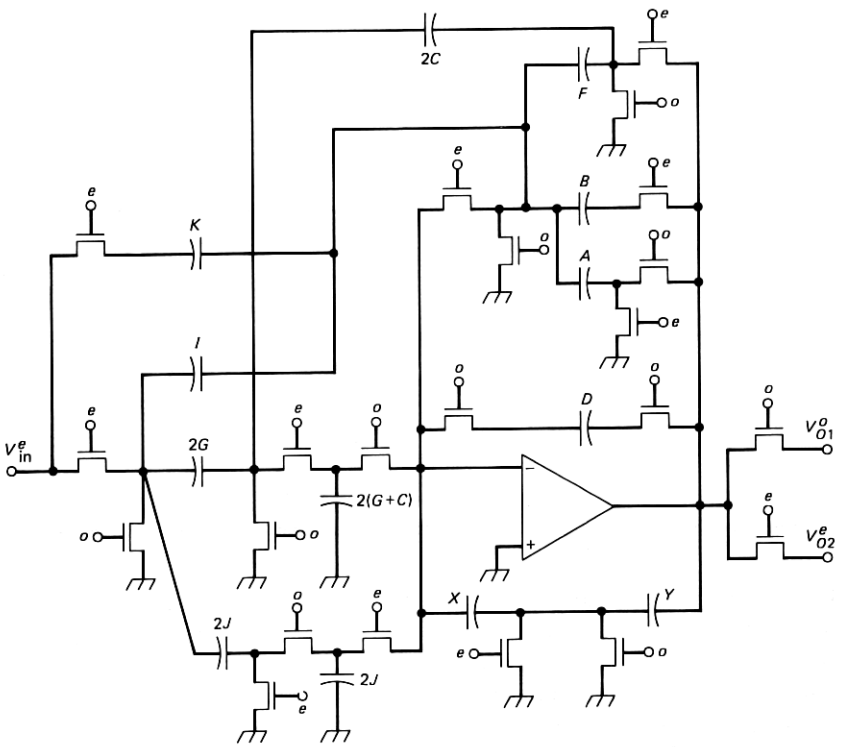
Fig. 10a—Switch sharing among parasitic-compensated toggles—original circuit.

biquads in Figs. 8 and 9 yield the switch-reduced circuits in Figs. 11a and 11b, respectively. Also note that one of the switches associated with a storage capacitor can often be eliminated by judicious sharing with one of the single-pole-double-throw (SPDT) switches associated with a switched capacitor. For example in Fig. 11a, the *e* switch on the top plate of *B* is shared with the *e* half of the SPDT switch on the top plates of *F* and *A*. The fact that the top plate of *B* is switched to ground during *o* does not adversely affect circuit operation. However,



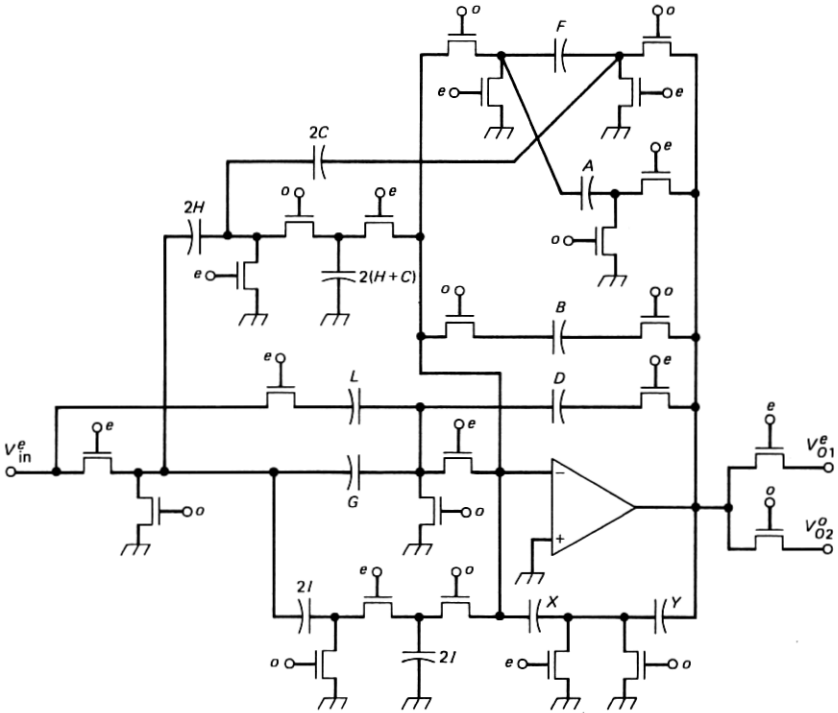
(b)

Fig. 10b—Switch sharing among parasitic-compensated toggles—switch-reduced equivalent of Fig. 10a.



(a)

Fig. 11a—Switch sharing in single-amplifier biquads—switched shared equivalent to the circuit in Fig. 8a.



(b)

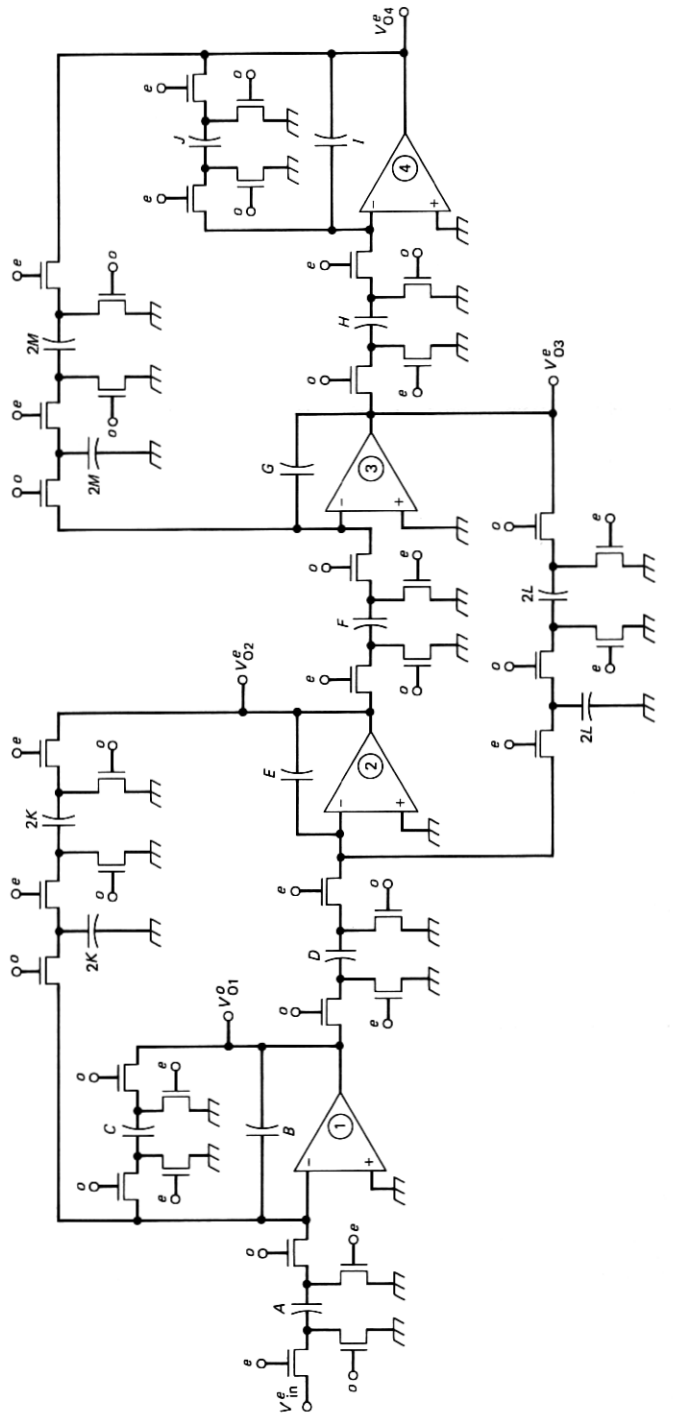
Fig. 11b—Switch sharing in single-amplifier biquads—switched shared equivalent to the circuit in Fig. 9a.

when sharing storage-capacitor switches, one must be careful to avoid inadvertently including storage capacitors in a closed loop of capacitors during their holding phases.

V. LEAPFROG STRUCTURES

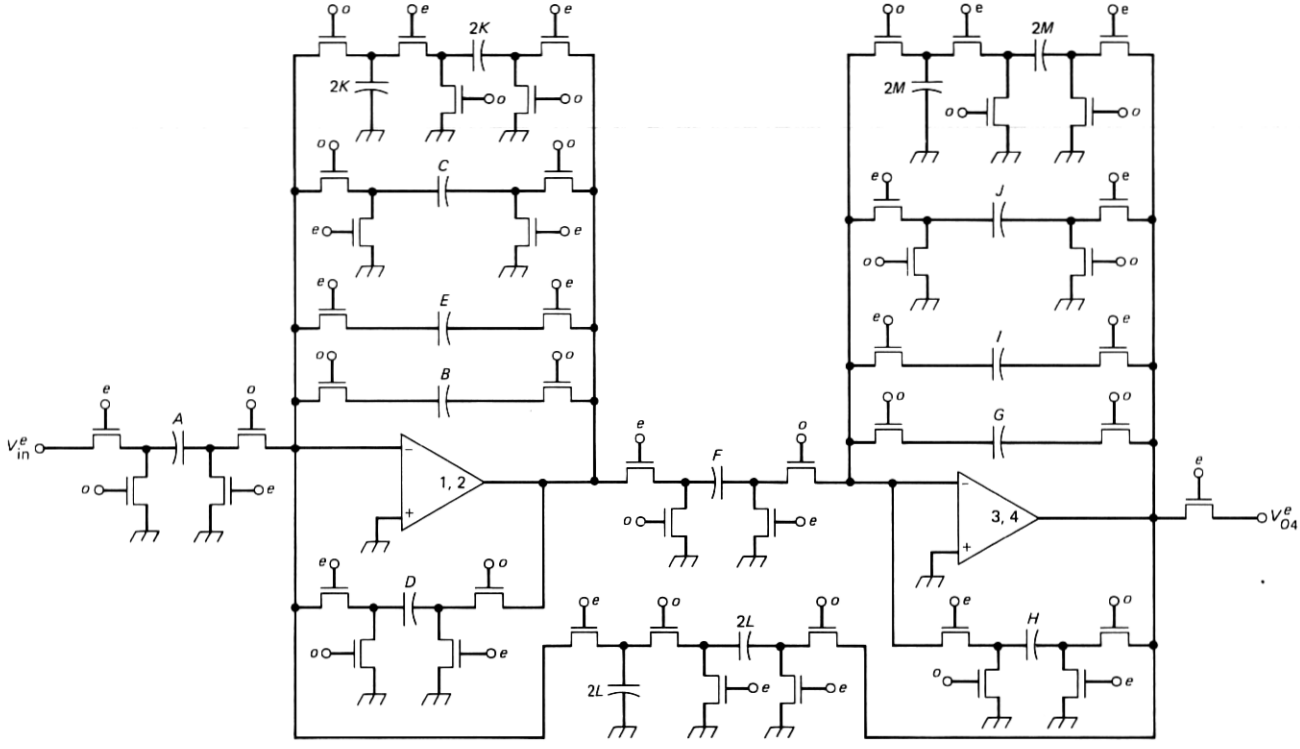
The circuit techniques illustrated in the previous sections are readily applied to reduce op-amp count in leapfrog structures. The resulting structures are parasitic insensitive. As before, closed loop stability during clock dead zones can be ensured by using the feedback network of Fig. 7 for every op-amp. It is readily shown that Nth order leapfrog structures can be implemented with $N/2$ op-amps for N even and $(N + 1)/2$ op-amps for N odd.

It is interesting to note that lossless discrete integrator (LDI) derived[1-3] leapfrog structures are inherently multiplexable. An implementation of a four op-amp, fourth-order low-pass leapfrog structure is shown in Fig. 12a. Note that all parasitic-sensitive toggle-switched



(a)

Fig. 12a—Fourth-order low-pass SC leapfrog filter—four-amplifier realization.



(b)

Fig. 12b—Fourth-order low-pass SC leapfrog filter—two-amplifier realization.

capacitors have been replaced by PCTs. Hence, the implementation in Fig. 12a is parasitic insensitive. In the implementation shown, op-amps 1 and 3 update charge during the odd phase, while op-amps 2 and 4 update charge on the even phase. To derive the two-op-amp implementation, one simply multiplexes alternate time-slotted op-amps in a pairwise fashion. For the implementation in Fig. 12b, op-amps 1, 2 and op-amps 3, 4 are pairwise multiplexed. One could alternatively pairwise multiplex op-amps 1, 4 and 2, 3. However, it appears that the interconnecting network is simpler if adjacent op-amps are multiplexed as is the case in Fig. 12b. To complete the structure, X, Y SC feedback circuits should be added to each op-amp. Switch sharing can also be used to reduce the switch count, but this will not be shown here.

VI. CONCLUSION

Circuit techniques which reduce by a factor of two the number of op-amps required to implement a given SC filter, while maintaining all parasitic insensitivity, have been given. Both biquad and leapfrog structures have been considered. Although only all-pole leapfrog structures were discussed in this paper, the techniques presented are readily applicable to elliptic-type leapfrog structures as well.

Breadboards have been constructed to establish feasibility and to examine the severity of the stability problem. Our experience has been that some sort of feedback is required around the op-amps at all times and that the X, Y SC feedback circuit works as expected. However, to determine whether such op-amp multiplexed circuits are really practical, sample designs will have to be realized in integrated form and characterized. In particular, the effects of op-amp slew rate and settling characteristics, as well as the noise and power supply rejection properties of these circuits, need to be investigated further.

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