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A Josephson Parallel Multiplier

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This report describes the operation of an 8- x 12-bit parallel multiplier which employs Josephson tunnel junctions (Fig. 1).[1]* The device contains 548 junctions used in two-junction "Jaws"-type logic elements.[2] Ninety-six of these logic elements function as AND gates to form the partial products. Their outputs are fed into a Wallace-tree[3] arrangement of 89 full adders, each having one Jaws for the CARRY computation and one for the SUM. The thirteen most significant bits of the product are returned to the outputs.

A latching-logic mode of operation is used.[1] This employs a five-phase ac current supply for power and timing, provided by unipolar pulses from a room-temperature word generator. The minimum cycle time achieved is 75 ns, with a latency time delay between input and output of 30 ns measured at the room-temperature connectors. Both times are within design specifications. The latency time is determined primarily by the time required for settling of the power-supply pulse amplitudes (20 ns total) and by the round-trip cable delay (8 ns) from the room-temperature connectors to the chip immersed in liquid He. The worst-case logic delay for the Jaws elements (ripple carry through 18 stages) is estimated as <2 ns, based on the <100 ps computer-simulated Jaws delay. In initial tests after preliminary adjustment of bias levels (chiefly the five-pulse amplitudes from the word generator), the multiplier operates correctly on all of several hundred selected combinations of inputs, as judged by oscilloscope monitors. Both exhaustive testing and optimization of bias levels remain to be carried out.

* (See Ref. 1 for two recent publications devoted to reviews of the state of the art in Josephson digital circuits.)

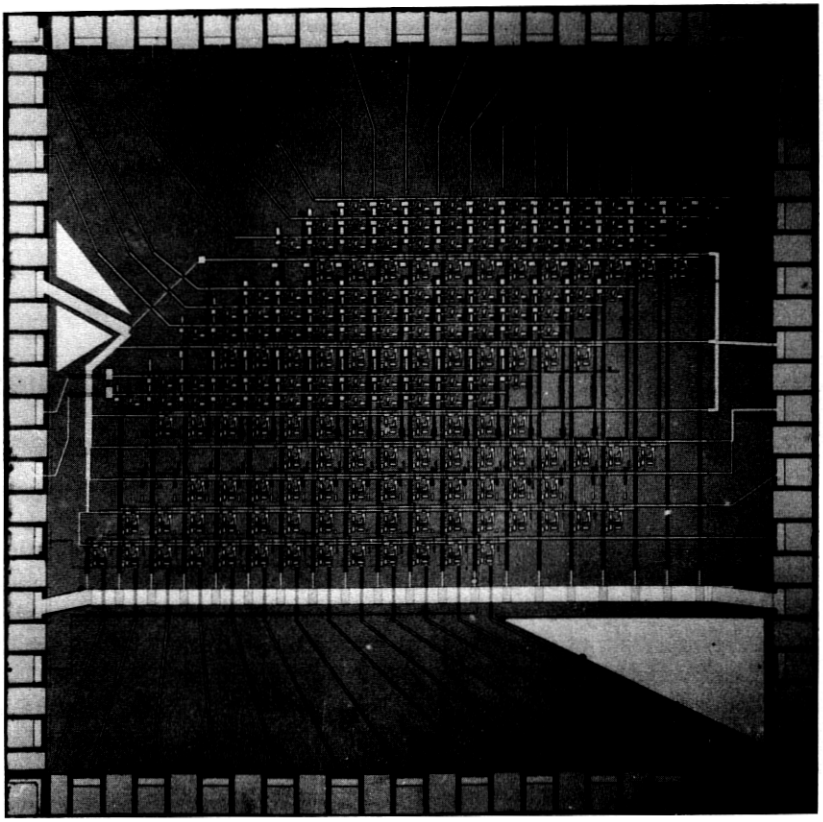

Fig. 1—A photomicrograph of the multiplier chip.

Circuits were fabricated on 2-inch-diameter oxidized Si wafer substrates having 12 chips per wafer. The circuit has seven levels. These are the Nb ground plane, two levels of ground-plane insulation (anodized Nb and an evaporated Ge-SiO sandwich), the Cu-Ge resistors, the Pb-alloy y-direction wiring and junction-base electrodes, the Ge-SiO crossover insulation, and the Pb-alloy x-direction wiring and junction-upper electrodes. Linewidths of 10 μm are used predominantly in the wiring and junctions, while some resistors are of 2.5-μm linewidth.

Fabrication was performed in a small class-1000 clean-room facility. Failures were caused primarily by lithographic or other fabrication-related defects and, secondarily, by nonuniformities in junction-critical currents. Estimates for the yield for defect-free fabrication are roughly 25 percent.

The very-high-speed capabilities of Josephson junctions are not well utilized in the particular design chosen for the multiplier. It was

decided to emphasize simplicity at the expense of performance (within the speed specifications mentioned previously) to minimize fabrication difficulties. Nevertheless, to our knowledge the circuit is the most complex, fully working Josephson circuit described to date.

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