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Using Magnetic Bubble Memories to Provide Recorded Announcements

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Recorded announcement systems have traditionally been electromechanical in nature, and have required routine maintenance and adjustments. An electronic system, the 13A Announcement System, was designed to replace many of these older systems and eliminate the need for routine maintenance. It is the Bell System's first application of magnetic bubble memories, and can provide from one to eight announcements of up to 24 seconds in length each. Entering the fifth year of production, the 13A is being installed in almost every type of central office of the telecommunications network.

I. INTRODUCTION

In the Bell System, audio recorders and announcement systems are used for a variety of applications to provide customers and operators with information. One group of applications are those associated with calls that cannot be completed. Announcements in this group tell the customer why the call was not completed. Examples of problems explained by these announcements are: non-working numbers, incorrectly dialed calls, damaged equipment and heavy traffic conditions. In general the announcements associated with these conditions are non-revenue producing. These announcements are fairly brief, many lasting only twelve seconds. Another major group of announcements are those which are customer requested. These announcements are longer, often about a minute in length. Examples of these are: the weather, stock market quotations, the news, department store sales, jokes, sports phone, etc. In general this group of announcements are revenue producing.

Traditionally, the machines used to provide these announcements have been categorized as being either light-duty or heavy-duty ma-

chines. The light-duty machines were generally designed for customer premises or for central offices where their use was not continuous. The heavy-duty service machines were characterized by a much higher calling rate, requiring that the machines run continuously 24 hours a day.

The majority of the recording machines presently being used by the Bell System are approximately 25 years old in design. These recorders are all basically electromechanical in technology, employing magnetic drums for analog storage. In addition these designs require magnetic heads, mechanical drives, and a variety of moving parts. The problem associated with these designs has been the need for frequent routine maintenance in the form of lubrication, mechanical adjustments, and the replacement of worn parts. There is also a high cost associated with the special mechanical skills required for this type of maintenance. Other drawbacks of these electromechanical systems include their large physical size and their large power requirements.

In contrast a solid-state design employing digital storage has the advantage of no moving parts and, hence, no routine maintenance. It also has the advantage of high reliability, extremely long life and small size. This technology also leads itself to modular construction with standard components and circuit boards.

A study conducted in 1975 showed that for the shorter announcements a memory system employing magnetic bubble technology would be economically attractive. The Bell System had extensive development under way in this technology. It was clear that the magnetic bubble memory architecture was ideal for use in a solid-state announcement system and that the nonvolatility which the bubble memory offered was very desirable for this application. The large storage capacity of the bubble memory was another important consideration. All of these factors combined to make magnetic bubble memories the ideal choice for a storage medium.

In the attempt to define what type of announcement system would be appropriate for the present and near future market, a survey of operating companies was conducted in 1975. This survey showed that 90 percent of the shorter announcement market could be served by an eight-channel system. It also indicated that 85 percent of the market would be served by a system capable of providing recordings up to 24 seconds in length. To minimize digital storage requirements various digital coding techniques were considered. Based on human factors tests, adaptive delta modulation (ADM) at 24 kb/s was selected as the best compromise of bit rate and intelligibility.

With message length, bit rate, and multiple channel capability defined, the basic design requirements of a solid-state announcement system, coded the 13A, were established.

II. GENERAL DESCRIPTION OF THE 13A ANNOUNCEMENT SYSTEM

The design of the 13A system evolved as a multichannel system that can record and play back up to eight messages. Each message can be, and usually is, different. With appropriate distribution circuits, each message can serve up to 500 customers simultaneously. For many applications, the 13A is used as a direct replacement for up to eight 7A electromechanical machines. Figure 1 shows the 13A as compared to eight commonly used 7A machines in standard central office frames. Figure 2 shows the 13A fully equipped with eight message modules.

To minimize the cost of the system, circuitry that is common to all messages resides on three circuit packs at the left side of the system. A minimum 13A system requires one additional message-module circuit pack, which contains the memory and other circuitry necessary for that particular message. The remaining seven positions at the right side of the 13A can be equipped or not, as desired.

There are two different message module circuit packs. Both types offer a variable-length message feature. One records announcements from 3 to 12 seconds in length, and the other can record messages up to 24 seconds long. The message length can be adjusted in 3-second increments by means of a thumb-wheel switch on the message module pack. Each pack can be set to a different message length, if desired, contingent upon its associated switching system.

The 13A requires a maximum of 77 watts from the -48 volt central office battery for eight channels. This is an improvement over previous announcement machines, such as the 7A, which requires 30 watts from 110 volts ac for one channel.

Each message channel of the 13A has a START input which controls the start of a message. After a closure to ground on this input, the message starts at the beginning with an average waiting time of 2.5 seconds. As long as the start input is grounded, the message will continue to repeat with a 3-second silence interval between message repetitions.

In addition to the message audio, several other outputs are available on a per-channel basis. To provide interchangeability between the 7A and the 13A, 7A output signals and their nomenclature were adopted. These outputs are contact closures that provide timing information that can be used by trunk circuits to ensure that the customer hears the message from the beginning, rather than from any point within the message.

Each message-module channel also provides a voice-alarm output. A contact closure on this pair of leads signals an absence of audio output from the message channel. A loss of power to the 13A system will also result in a voice alarm. A system input called VATEST can be used to test the operation of the voice-alarm circuit.

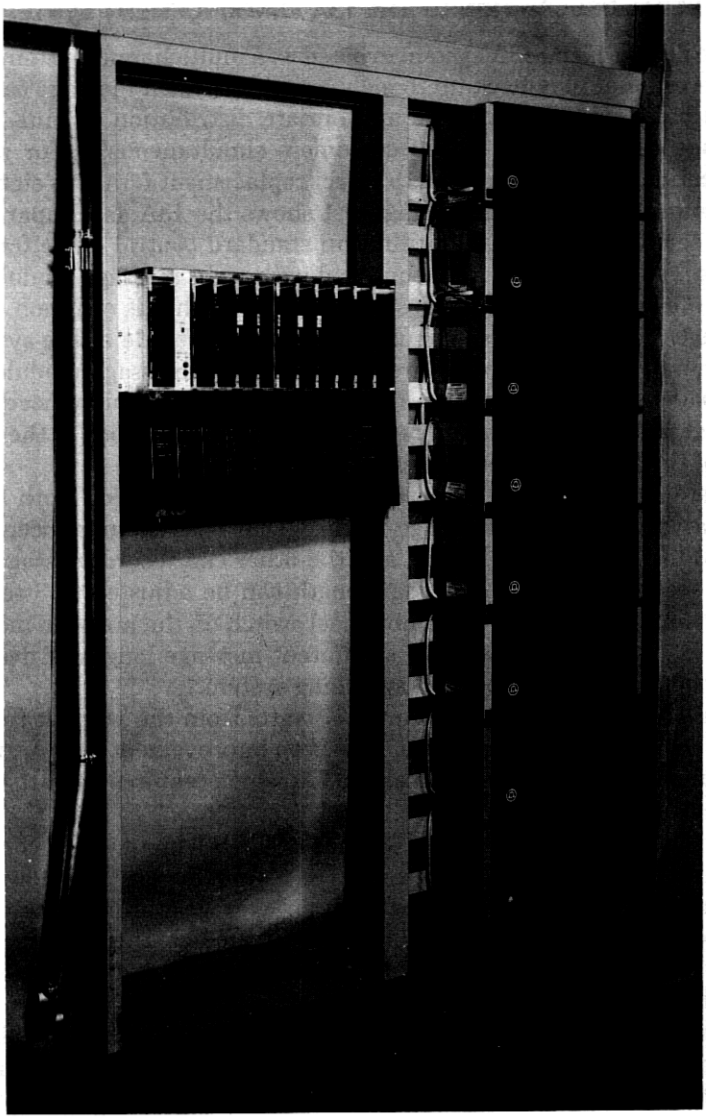


Fig. 1—Frame-mounted 13A Announcement System (left) compared to eight 7A units.

There are two methods for recording a message on the 13A. One method is to use a G3CR-type handset. The preferred method is to use a prerecorded tape and dub the message from a cassette recorder (typically) onto the 13A. The latter method produces the highest-quality announcement, since the tape can be prepared in a quiet environment by a professional speaker. The 13A provides a tape input

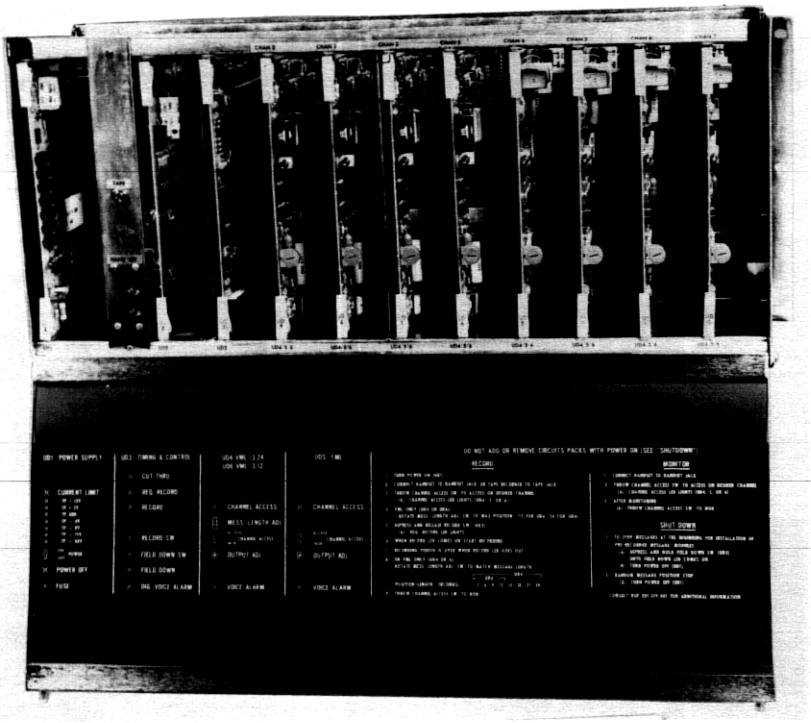


Fig. 2—The 13A Announcement System with eight message modules.

jack for this purpose. With the introduction of special information tones on standard intercept, vacant code, no circuit, and reorder announcements in 1981, dubbing from prerecorded tapes will become the standard method for recording these messages.

A simplified block diagram of the 13A system is shown in Fig. 3.[1] In recording, the input speech is filtered, converted into a digital representation using adaptive delta modulation (ADM), and written into the 29A magnetic bubble memory. Reproducing the message involves recovering the data from the memory, conversion back to an analog signal, and amplification for driving the output, which interfaces with trunk circuits. A large portion of the 13A circuitry is used to generate signals that are peculiar to the 29A memory. Therefore, some knowledge of the bubble memory is helpful in understanding the 13A system.

III. THE 29A MAGNETIC BUBBLE MEMORY

The 29A package, shown in Fig. 4, is a 32-pin dual in-line package 2.49 inches long and 1.2 inches wide. A permalloy outer case protects

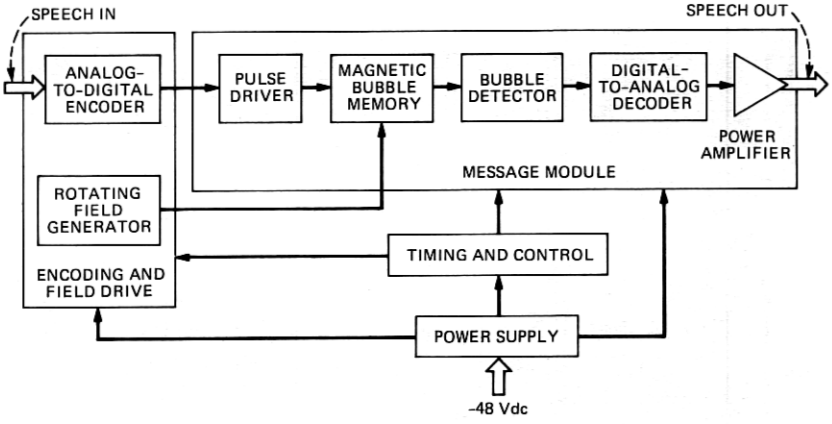
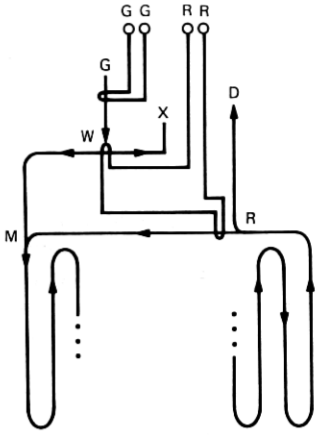


Fig. 3—Block diagram of the 13A Announcement System.

Fig. 4—The 29A bubble memory.

the bubble chips, rotating field coils, erase coil, and bias magnet from stray external fields.[2]

The package contains four 68,121-bit chips for a total of 272,484 bits. At the 24-kb/s encoding rate, storage capacity is approximately 3 and 12 seconds for chip and package, respectively. Each chip, approximately 5 mm by 6 mm, is organized as a single serial shift register. Ones and zeros are represented by the presence or absence of bubbles, respectively. Generation of new information and detection of the



D ACTIVE DETECTOR
G DATA INPUT GENERATOR
W WRITE TRANSFER
R READ REPLICATE OR TRANSFER
M PASSIVE MERGE POINT
X GUARD RAIL ANNIHILATOR

OPERATION	IN-PLANE FIELD ROTATIONS
DATA LOOP	68,121
R TO D	60
G TO W	8
R TO M EQUALS W TO M	81

Fig. 5—The 29A chip organization.

existing memory contents are both done outside the 68,121-bit shift register loop.

A line diagram of the chip organization is shown in Fig. 5. A bubble is generated at point G by an appropriate current pulse in the G conductor. Eight steps later, the bubble is at the write transfer point, W. If no current pulse is present in the R conductor, the bubble will travel along the path which ends in an X and be annihilated. If the proper current pulse is present in the R conductor, the bubble will take the other path, which will put the bubble into the data loop at point M. This is a passive merge point, and no signals are required to merge the generated bubble into the 68,121-bit loop.

Once in the main loop, the bubbles require no conductor signals to keep them circulating in the loop. However, no bubbles will go to the detector unless a proper current pulse is applied to the R conductor. Two different types of pulses can accomplish this. A transfer pulse, applied to the R conductor, will cause all bubbles at point R to travel to the detector. A series of 68,121 of these could be used to clear the memory. Or, in combination with the generator lead, a smaller number of transfer pulses could be used to rewrite a portion of the 68,121 locations. Another pulse, a replicate pulse, will cause a bubble at point R to split into two. One bubble stays in the main loop, the other travels to the detector. This pulse type is used for nondestructive readout of the memory's contents. The transfer pulse is not used in the 13A, since the 13A does not write a portion of a chip. In the 13A, clearing of the 29A memory is done by using the z coil.

In the *z* axis, which is perpendicular to the plane of the chip, there is a bubble-stabilizing bias field, nominally 160 Oe, which is supplied by a pair of permanent magnets inside the package. This field can be

aided or opposed by a current in the z coil. The z coil is used in manufacture to test the bias margins of the four chips. A much larger z coil current, aiding the bias field, will cause collapse of the bubble domains and can be used to bulk erase the entire memory.

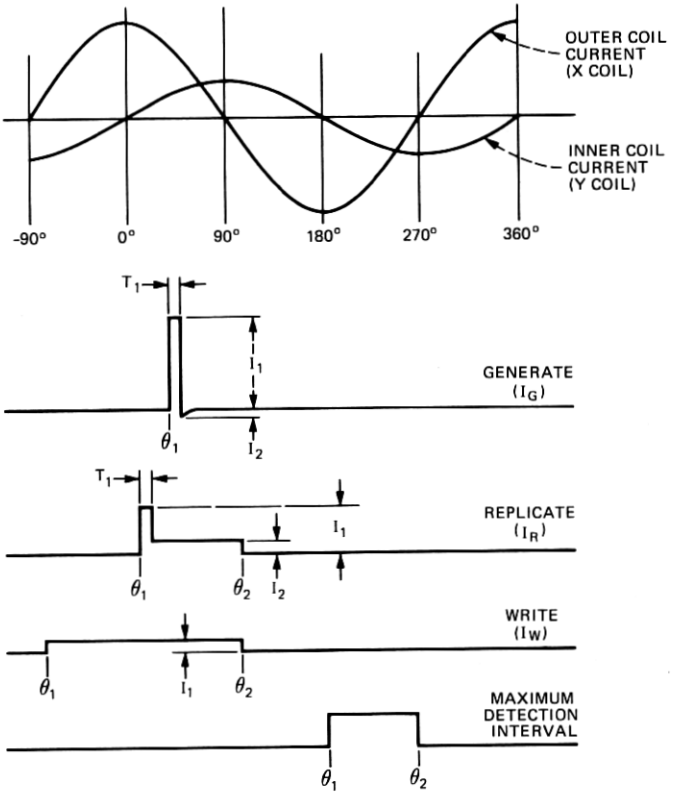
In a semiconductor shift register, a clock signal advances the memory. In the 29A, an in-plane, constant-magnitude, rotating magnetic field does this. One 360-degree revolution of the rotating field advances the bubbles by one position. The rotating field is formed by applying two sinusoidal currents, 90 degrees out of phase, to the inner and outer field coils. In the 13A, these coils are driven by voltage sources, so the inductance of the coils must be tightly controlled in order to obtain control of the current amplitudes. At the 48-kHz rotating field frequency, the required inner coil drive voltage is 25.15 volts peak to peak, and the current is 0.50 ampere peak to peak. The outer coil requires 25.15 volts peak to peak at 1.34 amperes peak to peak. The tolerance on both voltages is ±5 percent. Because the Q of the two coils is different, the desired 90-degree phase shift in currents is achieved by having the outer coil voltage lead the inner coil voltage by 95 ± 3 degrees.

The timing of the other functions of generate, replicate, and strobe (for data detection) is related to the phase angle of the rotating field. The timing requirements, as well as the current amplitudes, are shown in Fig. 6. It should be noted that the function drives must be current sources, since the function resistances have a tolerance of ±20 percent and the current tolerance, for example, of high replicate current is 110 mA ± 13.6 percent.

In the 29A package, the generators of all four chips are connected in series, and one pair of generator leads is brought out. Similarly, the detectors and dummy detectors are connected in series. The replicate leads are brought out individually, and they function as chip-select leads, determining which chip is being written into or read from.

The bubble arrives at the detector 60 rotating field cycles after being replicated at point R. The bubble field is detected by a magnetoresistive detector. Since other fields (especially the rotating field) are picked up, a similar dummy detector, under which no bubbles pass, is included to cancel out unwanted signals. Both active and dummy detectors are driven by constant current sources of 4.5 mA ± 0.2 mA. The match between the two current sources must be better than 1 percent. One side of the active and dummy detectors is connected together inside the 29A, and external circuitry must place this node at ac ground. The remaining two leads, one active and one dummy, must be amplified differentially. Since the detectors are insensitive to field polarity, the unwanted common mode signal is mostly at twice the rotating field rate and is about 80 mV peak to peak.

The desired bubble signature occurs during the strobe interval and is seen differentially across the active and dummy leads. To obtain a digital result, the signal is processed as shown in Fig. 7. A "1" (bubble) signature is typically 5 mV in magnitude, and a "0" response is somewhat smaller, as shown in Fig. 8. A technique known as dc restoration is used after this waveform is obtained. This references the signal level to the level at the start of the strobe interval. That is, within the strobe interval:



SIGNAL	I_1 mA	I_2 mA	T_1 μs	θ_1 DEGREES	θ_2 DEGREES
GENERATE	280 ± 35	<10	0.4 ± 0.1	40 ± 15	--
REPLICATE	110 ± 15	30 ± 6	0.7 ± 0.1	10 ± 10	110 ± 15
WRITE	30 ± 6	--	--	-75 ± 10	110 ± 15
MAXIMUM DETECTION INTERVAL	--	--	--	185°	276°

Fig. 6—The 29A timing requirements.

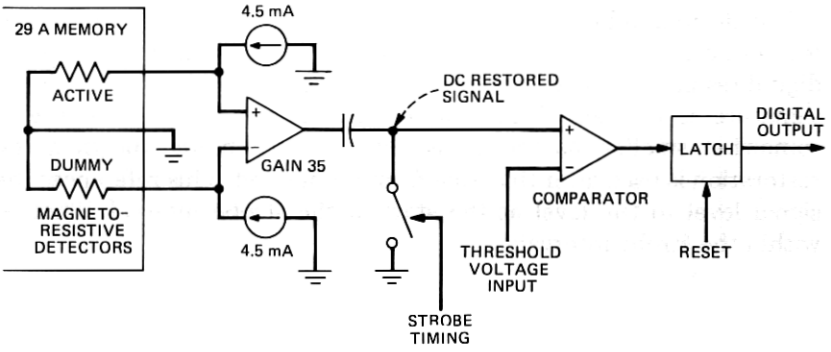


Fig. 7—Memory output signal processing.

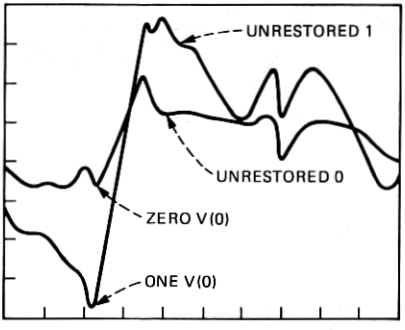


Fig. 8—Amplified bubble signal before dc restoration.

$$V(t)_{\substack{\text{AFTER}\\\text{RESTORE}}} = V(t)_{\substack{\text{BEFORE}\\\text{RESTORE}}} - V(0)$$

where V(0) is the signal amplitude at the start of the strobe interval. Since V(0) is higher for 0's than for 1's, this process increases the separation between 0's and 1's, as shown in Fig. 9.

The specifications of 29A outputs are based on dc restored waveforms. Output amplitudes vary widely from module to module. In the 13A, these variations are dealt with by varying the amplitude of a decision threshold until it is one-third of the distance between the 0 and 1 amplitudes.

One advantage of bubble memories is that data can be retained during loss of power, provided the rotating field signals are turned off properly. The rotating field must turn on and off within the ±45-degree segment as shown in Fig. 10. Failure to do this will result in loss of memory contents.

The 29A memories undergo extensive testing during manufacture.[3] This includes test of worst case amplitude and timing margins at room temperature, as well as a ±3 Oe bias margin test. In addition, each

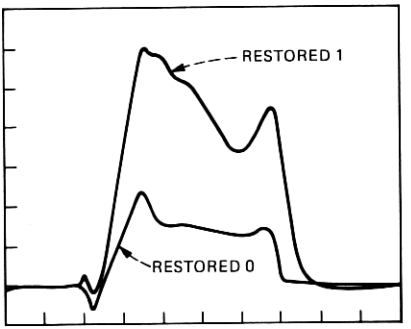


Fig. 9—Amplified bubble signal after dc restoration.

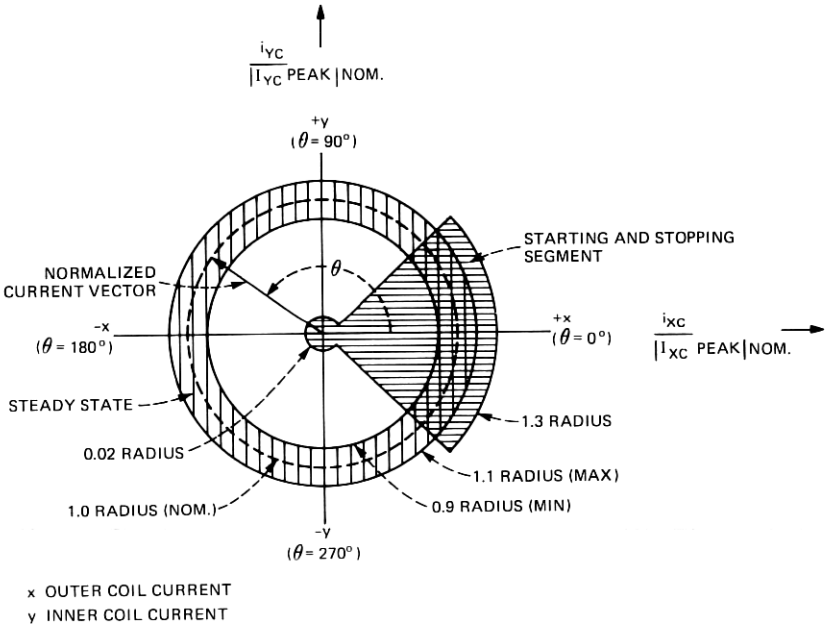


Fig. 10—Normalized coil-current polar plot showing the 29A start/stop requirements.

device must pass a less severe test at both 13°C and 60°C case temperature.

IV. THE AUDIO ENCODING-DECODING CHAIN

The 13A, viewed as a digitized audio system, is shown in Fig. 11. The signal flow can be traced through the audio-processing stage, the audio-encoding section, and the bubble memory. After the memory, the signal goes to a decoding circuit and then to an output amplifier.

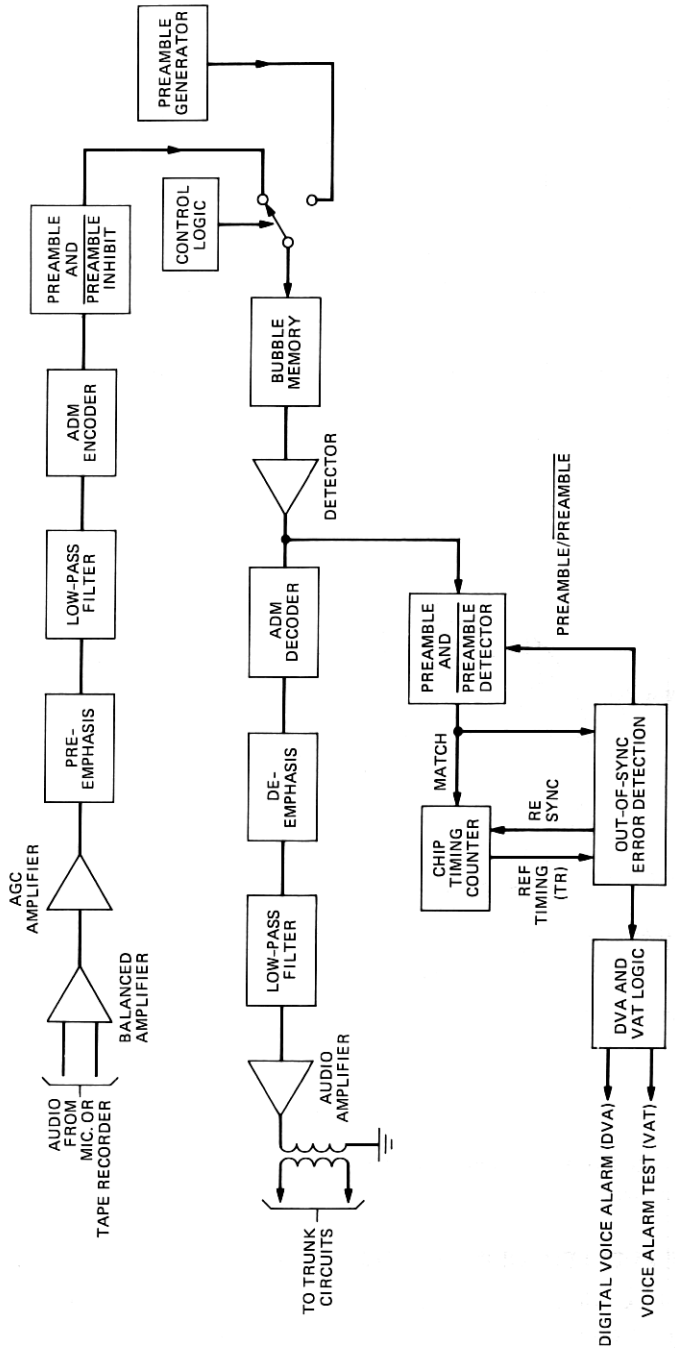


Fig. 11—Audio-chain and error-detection circuitry.

The first stage is a balanced amplifier which provides an input for a T1-type transmitter or a tape recorder source. The input of this stage is designed to bias a T1-type transmitter for up to 850 ohms of loop resistance and provide ac coupling for a tape recorder input.

The AGC amplifier provides 40 dB of input dynamic range to allow for various speaker levels, record levels, and loop resistance losses. With the input dynamic range compressed to 4 dB, an equalizer provides a signal increase at a slope of 6 dB/octave above 1 kHz and a signal decrease at 6 dB/octave below 1 kHz. This preemphasis is coupled with a corresponding deemphasis at the decoder output so that a flat frequency response is maintained. The overall preemphasis/deemphasis was subjectively determined to improve the response of the encoder/decoder chain by eliminating quantization noise at the decoder output. The last analog stage before encoding is a third-order, 2.8-kHz, low-pass filter defining the 13A bandwidth.

The filtered audio signal is digitized using an adaptive delta modulator (ADM) encoder operated at 24 kb/s. This is an ADM chip-set originally developed for the *SLC**-40 system and operated at approximately 38 kb/s.[4] For the 13A, the reduced clock rate is made possible because of the input AGC and the reduced importance of speaker identification. The output of the ADM encoder is processed by a preamble pattern inhibiter. The purpose of this circuitry is to inhibit bit patterns of 15 or more 1's and patterns of 15 or more 0's. A pattern of 15 or more 1's is modified by changing the eighth 1 to a 0. A pattern of 15 or more 0's is modified by changing the eighth 0 to a 1. This procedure ensures a unique bit pattern for use as a data preamble. With the ADM encoder used in the 13A, patterns of greater than 14 1's or 14 0's have a low frequency of occurrence. This procedure, therefore, introduces a negligible distortion into the ADM encoding. The preamble is generated by inserting a bit sequence of 15 1's surrounded by 0's as the first data loaded into the bubble memory during a message recording. The bubble memory output is converted to logic levels by the detector amplifier. The detector drives both an ADM decoder and circuitry associated with preamble detection, synchronization and error detection (see Section VIII). The ADM decoder decodes the digitized speech into audio. The inverse equalizer normalizes the speech to a flat spectrum and the low-pass filter eliminates quantizing noise residing outside of the audio band.

The final stage in this chain is a low-output-impedance amplifier capable of driving up to 500 trunk circuits at a maximum level of -9 volume units. Referring to Fig. 11 it should be noted that all circuitry

* *SLC* is a trademark of Western Electric.

after the preamble generator is duplicated for each message channel. All circuitry before this point is shared by all message channels for both record and playback operations.

V. TIMING AND FIELD DRIVE

A major consideration in the use of bubble memories is the overhead represented by the necessary circuitry for control and timing-signal generation. In the 13A, this circuitry takes the better part of two printed-circuit boards. However, this circuitry is shared by all message modules in the system.

Figure 12 shows a functional diagram of the circuitry for the field drive, field-cycle timing, and chip-cycle timing signals. The field drive used in the 13A is sinusoidal. The basic system timing is derived from the crystal oscillator which drives the control and timing counter. The control counter in turn supplies a clock to the quadrature sinewave generator, chip-timing counter and the timing Read Only Memory (ROM). The start and stop timing for the quadrature sinewave generator and for the application of the generator outputs to the power amplifiers is provided by the timing ROM. The timing ROM also provides basic timing for the field-cycle timing signals previously described. The chip-timing counter provides signals necessary for timing during the chip cycle.

On the message-module boards, where the bubble memories reside, are capacitors in parallel with both the inner and outer coils. These form parallel resonant circuits at the 48-kHz rotating field frequency. They reduce the power required for steady-state operation by a factor of 10, but they also change the start-up and shutdown loads that the power amplifiers drive.

To maintain nonvolatility with bubble memories it is important that the power up and power down cycles occur within the ±45-degree quadrant of the field drive cycles. When a system is powered up, the timing ROM starts the quadrature sinewave generator, allowing enough time for the generator to stabilize; then the timing ROM provides the start signal for the closure of the analog switches. The analog switch associated with the outer-coil drive is closed first. After a delay corresponding to 95-degrees of the field drive cycle, the inner coil drive analog switch is closed. At this point the inner and outer coil field drive signals must meet the previously outlined amplitude and phase requirements.

For nonvolatility upon power down, the inner and outer coil drive analog switches are shut off simultaneously at the point in the field drive cycle where the outer coil current is a maximum and the inner coil current is a minimum. This results in a gradual decay of the outer coil current and a slight oscillatory decay for the inner coil current.

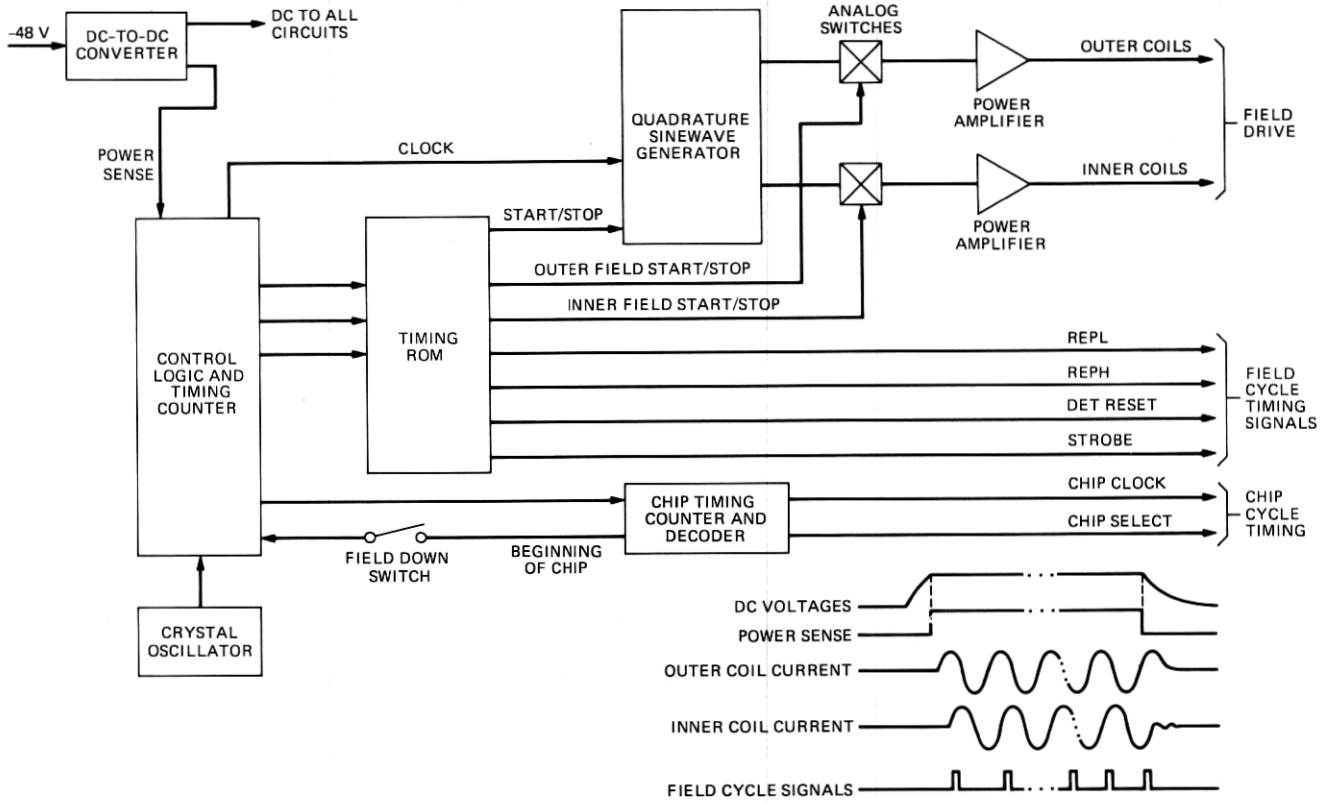


Fig. 12—Field and chip timing circuitry.

The resultant field vector lies within the ±45-degree sector necessary to maintain nonvolatility.

The final links in the chain for the inner and outer coil field drives are the associated power amplifiers. To maintain nonvolatile bubble memories during steady-state, transient, and variable-loading conditions, these amplifiers must be carefully designed. During steady-state operation, the amplifier must supply a sinusoidal signal whose amplitude must stay within ±5 percent and whose phase must not vary by more than ±1 degree for a load variation of 1 to 16 field coils. When the field drive signals are first turned on, the field drive loads appear capacitive. For this case, the power amplifiers must be capable of supplying up to 16 amperes at the sinusoidal peak voltage (12.57 volts). On turn-off, the power amplifiers must exhibit the transient response and low output impedances necessary to dampen the field coil energy. The power amplifiers also include circuitry to inhibit extraneous signals from reaching the field coils when the power supply voltages are below 13 volts. This is necessary to deal with transients occurring during low-voltage conditions when the 13A system is powered up or down.

VI. POWER CONSIDERATIONS

To ensure a nonvolatile system, the 13A must sense loss of power and turn the rotating fields and timing signals off before power supply voltages decay to the point that the control logic will no longer function. On power up, the system must hold the fields and timing signals off until power supply voltages are within normal limits. Figure 12 shows the functional circuitry and signals related to the 13A power start-up and shutdown operations.

When the dc voltages from the power supply are within 5 percent of their nominal value, the power sense signal is sent to the control logic. The power sense signal initializes all the logic and starts the sinewave generator via the timing ROM. Allowing sufficient time for the sinewave generator to stabilize, the field drive and field cycle timing signals are switched on.

If the -48 volt power is lost, or the power switched off, the power sense signal is switched low when the dc voltages have decayed by 5 percent. This signal, delayed by the control logic, switches off the field drive signals and associated field cycle timing signals at the proper time in the rotating field cycle. The maximum delay is one cycle of the rotating field, or 21 μs.

Although the previously described power-down sequence maintains 13A nonvolatility, it causes the messages to be stopped at a random point in the chip cycle. Message boards powered down in this manner cannot be interchanged between different 13A's without introducing

preambles at different relative positions. The ambiguous preambles would not permit proper synchronization of the 13A system. This, of course, would not be a problem for a single-channel 13A. To permit interchangeability of message modules for multichannel 13A's, the 13A can also be powered down by first employing the Field Down switch. Operating this switch (before switching the power off) turns the field drive signals off near the beginning of the chip cycle. This ensures that all message modules fielded down in this manner will have preambles in the same relative position. This feature cannot be ensured for emergency power down, or loss-of-power cases, because the control timing would have to delay the field down switching for up to one chip cycle (2.84 seconds) to reach the proper point in the chip cycle.

VII. RECORD AND PLAYBACK CONTROL

The record and playback operation of the 13A is controlled locally via circuit-card edge switches and light-emitting diodes (LEDs). The audio source can be either a telephone handset or a tape recording. Message modules can also be prerecorded at one site and installed in systems at other sites, provided the proper precautions are taken using the Field Down switch.

The record operation starts with the record-request signal generated from a card-edge push-button switch. This sets the record-request flip flop, which in turn lights a record-request LED on circuit pack UD3's card-edge. When the chip counter arrives at the appropriate point of the chip cycle, the record process is started by pulsing the z coil of all accessed message modules to clear the data recorded previously. Next, the preamble pattern is generated. The record-request LED is turned off and the record LED turned on as a signal to input the audio. At the end of each chip, the generated data is switched to the next chip until the last-chip signal occurs. The last-chip signal turns off the record LED, which signals the end of the record interval.

The playback operation can be controlled either locally or remotely. With the selected channel started remotely or accessed locally, the playback operation begins. This involves replication and detection of bubble signals, decoding the ADM data, and amplification for driving trunk circuits. At the end of each chip cycle, the replication process is switched to the next chip in the bubble module. If the playback involves two bubble memories, switching between them is not immediate. Owing to the delay between the replicator and the detector inside the 29A, switching of the detector from the first to the second module must follow switching of replication by 30 data cycles.

The setting of the thumb-wheel message-length switch determines which chip is the last chip in the message. At the end of the last-chip signal, the message ends and, if the start or access signals are present,

a 2.84-second silence interval begins, after which the message repeats. During the silence interval, several relay signals are given to signal the end of the message and the start of the next message repetition.

VIII. PREAMBLE SYNCHRONIZATION AND ERROR DETECTION

In the 13A system, the stored-message-synchronization and error-detection techniques were combined into common logic. The design requirements which prompted this approach were based on a need to provide synchronization of stored messages to the control counter and inexpensive means of logic fault detection. It was considered important that the fault-detection scheme be capable of detecting stuck-at-one(SA1) and stuck-at-zero(SA0) conditions in the data paths, and at the same time tolerate small or transient errors in the data. It was also considered desirable that the system be able to detect and recover from conditions when the control counter was out of synchronization with the messages.

Referring to Fig. 11, the data stream of the ADM encoded speech is first processed to inhibit preamble patterns and their complement from the data stream. A preamble of 15 1's is then first generated and stored in the bubble memory. When reading the data from the bubble memory, the data is first applied to the preamble detector noninverted. The output of the preamble detector, the match signal, is used to time synchronize the chip timing counter. Normally the first preamble match signal that occurs after powering up is employed to provide this synchronization. Following this operation, all 13A messages are chip-cycle synchronized to the control logic. All further occurrences of the match signal are compared with the chip-timing counter signal, TR. With a normal 13A system, match signals occur timed to TR. In this normal mode, every 60 seconds (enough time for two cycles of the longest 13A message) the data from the bubble store is inverted and applied to the preamble detector logic. During this cycle, the preamble detector in effect searches for 15 0's. Since this pattern was inhibited from the memory, any match signal generated in this cycle is interpreted as an error condition.

To make the system tolerant to transient errors, a threshold of two or more false preambles during a 60-second interval was established. If two or more false preamble errors are detected, the internal digital voice alarm (DVA) is set. To cover the possibility that the control counter has slipped out of sync with the stored messages, a sync retry cycle is initiated at this point. It starts by permitting the next preamble match signal to resync the chip timing counter. If another two or more false preambles occur, the external voice alarm test (VAT) signal is set. This same alarm is set for any case of a false preamble match signal during the data complement cycle. When an alarm is set during the

noncomplement data cycle, repeated attempts to resync the control counter to the preamble match signals are made. If a resync condition is achieved the alarm is reset and the system is returned to a normal state.

IX. PHYSICAL DESIGN AND CIRCUIT PACK DESCRIPTION

The five types of circuit packs used in the 13A are 8 by 11 inches. Except for circuit packs UD1 and UD2, all have three 963B-20 connectors for a total of 60 I/O pins per pack. UD1 and UD2 need only two connectors each. All packs are class 1 (25-mil paths and spaces) double-sided printed-circuit boards. All controls and indicators for operation of the 13A are mounted on the front edge of the circuit packs.

A major objective in the physical design of the 13A system was to eliminate hand wiring. This is accomplished by the backplane, shown in Fig. 13. This double-sided printed-wiring board interconnects all the circuit packs and the packs to the 123 I/O pins. Screw terminals are provided for -48V power and ground return. All other I/O terminals are 0.045-inch-square wire-wrap pins. Only four wires are needed to connect the handset and tape jacks located on the mounting strip at the front of the system.

Overall dimensions of the 13A system are 9.88 inches high by 12 inches deep by 23 inches wide. Compatibility with all the types of offices and frames in which the 13A is used is achieved by ordering different brackets to mount the system in the various frames. On the front of the unit there is a smoked plastic door, hinged at the bottom. All system indicators can be seen through the closed door at either the top or bottom. The strip across the center of the door is opaque. When

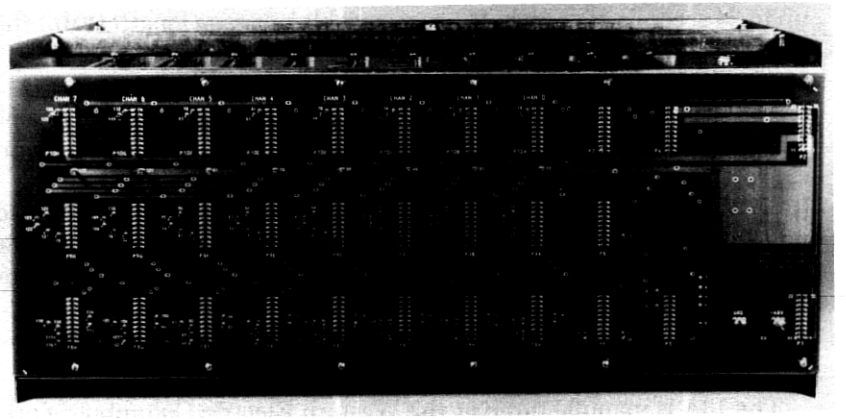


Fig. 13—The 13A Announcement System backplane.

the door is opened, the instructions on the inside of the door are visible. These instructions, shown in Fig. 2, contain a summary of the procedures for monitoring an existing message, recording a new message, and shutdown of power. All system indicators (LEDs) and control switches are also identified here.

The first circuit pack in the 13A is the power supply, which is coded UD1. It is a pulse-width-modulated dc-to-dc converter. It converts the -48 volt supply to +15.75V at 1.6A, -15.75V at 0.5A, and +5.2V at 3.2A. Also, two low-current supplies, -4V at 100 mA and -8V at 100 mA, are derived from the -15.75V. When supplying these currents, which are a maximum for a fully equipped 13A, UD1 draws 1.6A from the -48V supply. The voltage outputs have a tolerance of ±5 percent, except for the +5V supply. It has a tolerance of ±3.5 percent. Circuitry is also provided for electronic shutdown if the voltages exceed their tolerance or if currents exceed specified values. Each message board adds a resistor in parallel with the current-sense resistor on UD1, changing the current-sense limit in proportion to the number of message boards in the system. Also, the +5.2V and +15.75V outputs are monitored, and both must be higher than the minimum values to result in a high level on the PWR SENSE output.

The second common circuit pack is UD2, the encoder driver. It provides the circuitry for the input speech processing and encoding. This circuit pack also generates, amplifies, and provides analog switching of the field drive signals.

The other common circuit pack is UD3. This circuit pack contains the basic digital control and timing for the 13A. It controls the rotating field generation, provides bubble memory timing signals and chip sequencing, and placement of the recording of new messages. UD3 also provides the logic for message synchronization and error detection.

UD4 is a variable-length message module that stores and plays back up to 24 seconds of speech. It has a variable message length (VML) that can be adjusted from 3 to 24 seconds in 3-second increments. UD4 stores the digitally encoded speech in two 29A bubble memories. It converts the stored information back into analog speech, and it amplifies and buffers the output to drive up to 500 trunk circuits. Signaling closures are also provided by this circuit pack.

UD6 is a variable-length message module that stores and plays back up to 12 seconds of speech. It is similar to UD4. In fact, the two codes use the same printed-circuit board. A UD4 has the second 29A and associated components, a UD6 does not.

X. MANUFACTURING AND APPLICATION STATUS

The 13A is manufactured at the Western Electric Columbus Works. Manufacturing information was released on October 1, 1977. The first

13A was shipped to New York Telephone Company in February 1978. By the end of 1981, approximately 4188 13As had been shipped, and production should continue at the rate of about 110 systems per month. This requires 1670 29A memories per month. Each circuit pack must pass a circuit-pack test. Testing of UD3, UD4, and UD6 packs is automated, using computer-controlled test sets. The only adjustments during circuit-pack test are made on the message-module packs to match the detection threshold with the particular 29A device. In addition to circuit-pack tests, each 13A is given a system test before shipment.

The first 60 systems manufactured went to a special application in New York City. This is the Automatic Dial Coin Zone (ADCZ) System, which uses announcements to automate handling of two-message-unit coin phone calls in the New York City area. Each 13A is equipped with six UD6 message-module packs, for a total of 360 29A's in the 60 systems. All systems were placed in service on July 1, 1978.

At present 13A systems are also in service in Step-by-Step, No. 1 and No. 5 Crossbar, No. 1/1A ESS, No. 2/2B ESS, and No. 3 ESS offices. In No. 3 ESS applications, the 13A is installed and shipped with the office from the manufacturing facility. For No. 1/1A and No. 2/2B ESS the 13A's are installed and shipped as part of an announcement frame. In all other applications the 13A's are shipped directly to central offices for installation.

XI. CONCLUSION

The 13A is the first application of magnetic bubble memories in the Bell System. The 13A performance and modular design has permitted it to satisfy a very large percentage of the Bell System announcement market. It is being used in all types of central offices, and will be used in No. 5 ESS.

The 13A compares very favorably to the widely used electromechanical 7A system. The 13A is lower in cost for systems employing three or more channels, requires 77 watts for an eight-channel system versus 30 watts for a single 7A, and eliminates the need for costly periodic maintenance.

Magnetic bubble memory technology has proven to be an excellent match to the needs of the 13A Announcement System. By using magnetic bubble memories as the storage medium, the 13A offers nonvolatile storage of recorded announcements. The high storage density of magnetic bubble memories has enabled the 13A to occupy as little as one-eighth the space previously taken by eight 7As. The high density and low cost of magnetic bubble memories relative to other nonvolatile and writable storage devices enable the 13A to be very cost competitive with electromechanical systems.

In its fifth year of production and at its current manufacturing rate of 110 per month, the 13A has proven to be a successful product. This is true both in terms of the use of magnetic bubble memories and the 13A modular design.

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