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D4 Digital Channel Bank Family:

The Channel Bank

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The D4 channel bank is the most recent Western Electric product in an evolution of time-division multiplex terminals for digital transmission facilities. D4 incorporates many technical innovations relative to the earlier developed D1D, D2, and D3 channel banks but is fully compatible with these earlier banks. D4 banks may be operated in any of five different modes as required to connect to a particular digital carrier facility (T1, T1C, T2, or FT2). The D4 channel bank is partitioned into common equipment and channel units. The common equipment provides digital line interface, pulse code modulation coding and multiplexing, alarms, trunk processing power, power fusing, and distribution. Individual channel units provide the circuits that interface to external circuits. There are many different versions of channel units including standard interoffice voice-frequency trunk types and those supplying data and special services.

I. INTRODUCTION

The D4 channel bank was initially proposed as a complementary terminal development to the 3.152-Mb/s T1C line facility to enhance the cost-effectiveness of 48-channel applications.[1,2] As planning progressed, it became clear that because of the introduction of new technology in D4, and the inherent need for an end-to-end compatibility with the forerunner D1D, D2, and D3 channel banks,[3-9] the D4 architecture should be expanded to include 24- and 96-channel, as well as 48-channel, operations. Thus, the early objectives of the D4 were to

develop a more economical, flexible, digital terminal for T1C and T2 applications, as well as a smaller, lower priced, more reliable terminal for T1 applications. In addition, D4 was to have simplified maintenance and to incorporate technological advancements.

Each D4 bank is a completely self-contained, 48-channel terminal consisting of two 24-channel digroups, each with essentially separate common equipment sections and interchangeable digital line interface units. The predecessor 24-channel D3 design required 18 inches of vertical bay height plus space for an external fuse/alarm panel. Because of application of integrated circuit technology in the D4 design and incorporation of fusing into the channel bank frame, a size reduction of better than 2:1 was achieved. The result is that each D4 bank requires only about 19 inches of vertical height for the 48 channels. Electrical compatibility with earlier vintage banks has been realized through the use of the standard 7-5% bit, 15-segment, μ255 nonlinear coding characteristic, and the D3, D2, D1D basic frame and signaling format. D4 uses improved versions of the highly accurate and stable, D3 multiple-pole, resistor-capacitor (RC) active thin-film filters[10,11] to achieve transmission performance that meets toll-grade transmission objectives. The D4 bank can be universally used in direct, tandem, toll-connecting, and intertoll trunks. In addition, by giving each channel direct access to the digital bit stream, synchronous digital data or "dataport"[12,13] channels, for direct digital connectivity up to the 56-kb/s rate, is a reality. Like the D3 Unitized Bay (UTE), which includes Switched Maintenance Access System (SMAS)[14] relays for special services maintenance, versions of a D4 UTE are now available.

Additional features of the D4 bank include improved per-channel maintenance through increased access at the channel unit jack, per-channel trunk processing, and electronic features such as built-in 1000-Hz digital milliwatt for receiver checking and "signaling bit storage"[15] with extended carrier group alarm (CGA) timing. Formerly, CGA timing in digital systems would only allow a 0.3-second maximum out-of-frame condition to exist prior to bank shutdown, trunk conditioning, and office alarming. With the introduction of signaling storage, wherein past-state signaling information is stored and used to hold up the proper connection in the event of an out-of-frame condition, it became permissible to extend the CGA timing from 0.3 second to more than 2.0 seconds. This resulted in over a two-fold reduction of CGA outages and consequential reduction in the number of lost calls. Trunk processing that occurs during a CGA bank shutdown is handled by per-channel trunk processing relays under control of timing from the alarm control unit and the common relays in the trunk processing unit (TPU) plug-in. This has reduced the size, cost, and administration associated with trunk processing.

II. FUNCTIONAL OVERVIEW

2.1 General description

Figure 1 is a block diagram of the D4 bank. Channel units for two 24-channel digroups (designated *A* and *B*) are apparent, accompanied by common equipment that includes transmit, receive, alarm, trunk processing, and line interface units. Power is derived from the −48-volt office supply by means of a dc-to-dc converter unit. Two alarm units are used in all applications except for the special Mode 1, T1C application. Separate digital line interfaces and associated units, such as dual synchronizing/desynchronizing (syndes) units, are used to interface the digital line facilities. Since trunk processing relays are included within each channel unit, a simple dual control, common relay TPU is used. This unit houses one or two digital line equalizers (or line build-out networks) that plug into connectors on the TPU. Common equipment channel-counting options are administered on the TPU. This feature quickly restores a failed transmit or receive unit since there is no need to note and set the options on the new units before making the restoral. The power distribution unit provides a fused −48V distribution arrangement.

Channel units available for the D4 bank range from standard interoffice trunk types to data and special services. These units connect to common backplane signal busses that make all necessary connections to the common equipment, office equipment, and signaling systems.

2.2 Modes of operation

Figure 2 shows how the D4 banks interface with the digital hierarchy. Single D4 banks operating in Mode 2 or 3 have 48 voice-frequency (VF) channel interfaces to DS1C or DS1 rate facilities. Dual bank arrangements, where two D4 banks are connected together, have 96 VF channel interfaces to DS2 rate wire or FT2 lightwave facilities. These are designated Modes 4 and 5, respectively. Also provided is an additional DS1C rate interface (not compatible with the hierarchy), which is a low-cost D4-to-D4 connection designated as Mode 1.

D4 channel banks can be connected to any of four digital transmission facilities (T1, T1C, T2, or FT2). Configuration of the banks for interfacing a particular digital facility is accomplished by simply inserting an appropriate line interface unit (LIU), and in some cases, a snydes unit (SU) plug-in into the bank to set up a mode of operation. The mode configurations are illustrated in Figs. 3 and 4. In all but the FT2 facility connections, small plug-in equalizer or line build-out boards are installed to accommodate cable distances between the D4 channel banks and the office digital cross connect or office repeater bay. Table I summarizes the digital facility connections in terms of D4

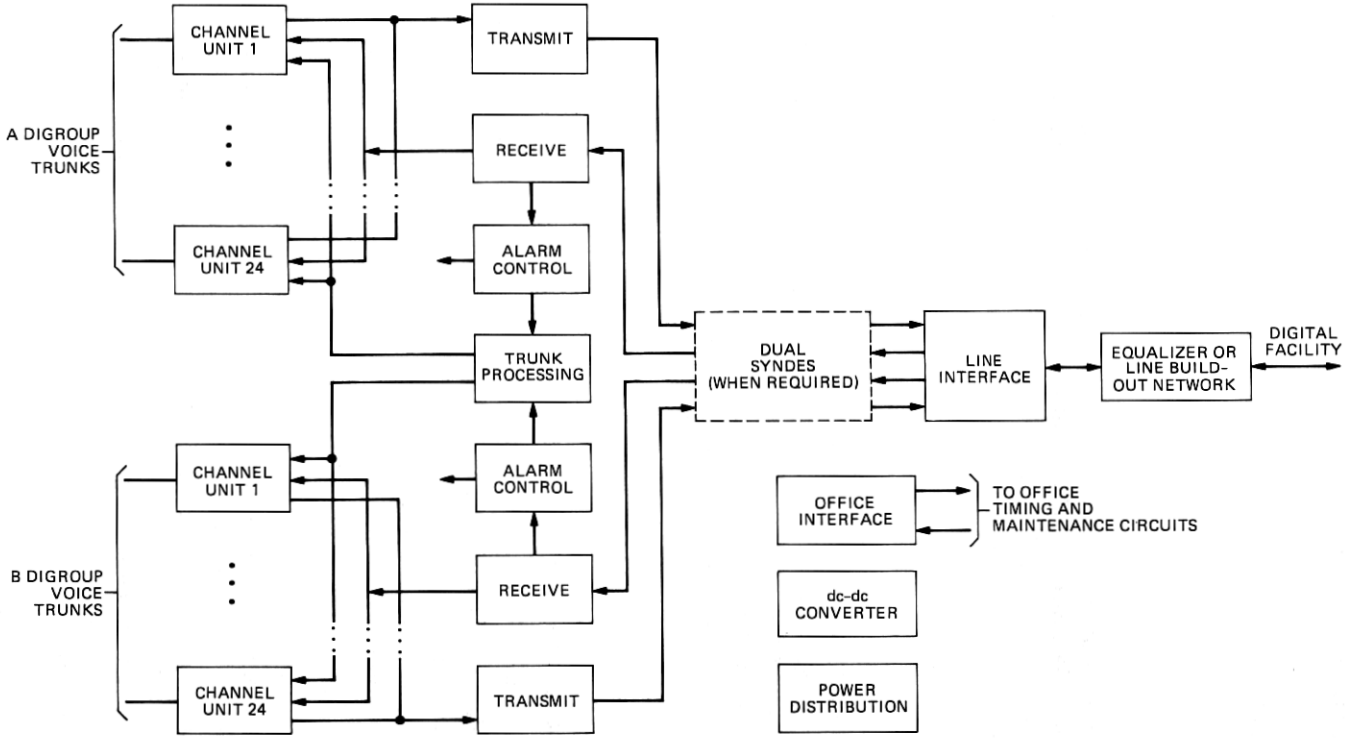

Fig. 1—The D4 channel bank.*

* Acronyms and abbreviations used in these figures are defined in the Glossary at the end of this paper.

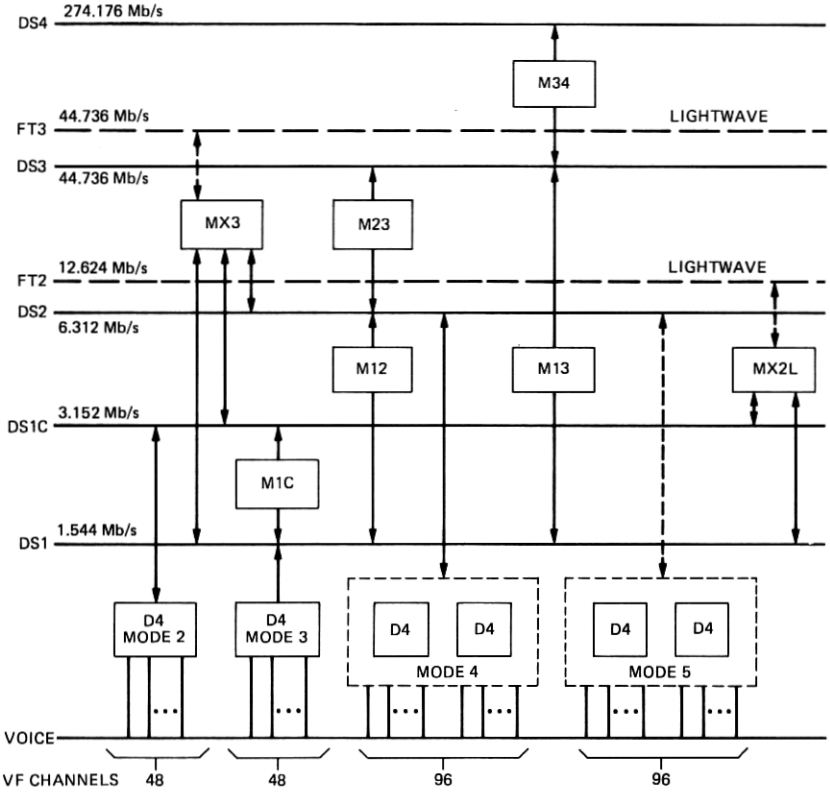

Fig. 2—D4 channel bank interfaces to the digital hierarchy.

Table I—Digital facility connections

D4 Mode	Digital Transmission Facility (System Bit Rate in Mb/s)		Number of Voice Channels	Number of Digroups	Compatible Digital Hierarchy Multiplexer
1	T1C	3.152	48	2	None
2	T1C	3.152	48	2	M1C
3	T1	1.544	24	1	—
4	T2	6.312	96	4	M12
5	FT2	12.624	96	4	MX2L

modes of operation, digital hierarchy multiplex compatibility, and number of voice channels and digroups.

There are two modes of operation over T1C digital facilities. Mode 1 (Fig. 3a) is a low-cost, dedicated D4-to-D4 connection that uses a single clock so that two digroups are synchronized and multiplexed by interleaving PCM bits from each digroup. Mode 2 (Fig. 3b) has a more flexible terminal capability because it uses a syndes unit and an M1C

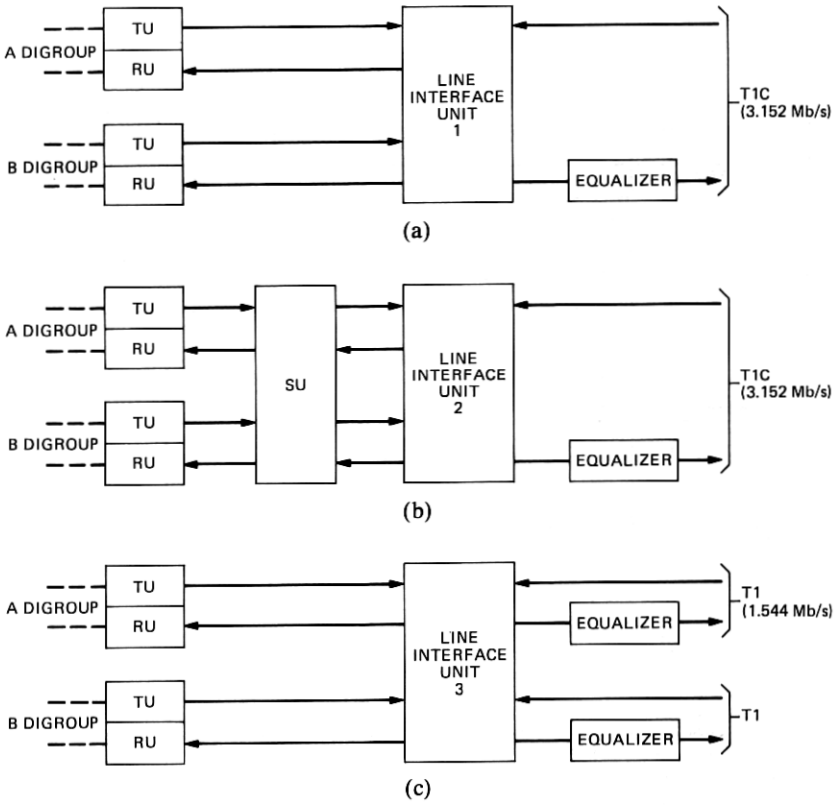

Fig. 3—D4 channel bank mode configurations. (a) Mode 1. (b) Mode 2. (c) Mode 3.

multiplex standard signal format. This mode connects the D4 bank to other digital terminals at the far end using the M1C Multiplexer. Mode 2 also provides alarm and M1C-compatible maintenance features. In addition, Modes 2, 4, and 5 have a unique in-service digroup test capability.

Mode 3 (Fig. 3c) electrically conditions the D4 bank for independent digroup transmission over separate T1 carrier digital lines. The two digroups are then compatible with a similarly configured D4 bank or with any arrangement of D3-, D2-, or D1D-type terminals. Alarming and trunk processing functions are provided on a per-digroup basis to allow for maintenance or restoral work to be done independently. In this mode, some common units such as the power converter, battery filter, and the LIU are shared between digroups.

Interface to T2 digital facilities is provided when two D4 banks are interconnected and each has line interface and syndes units to operate

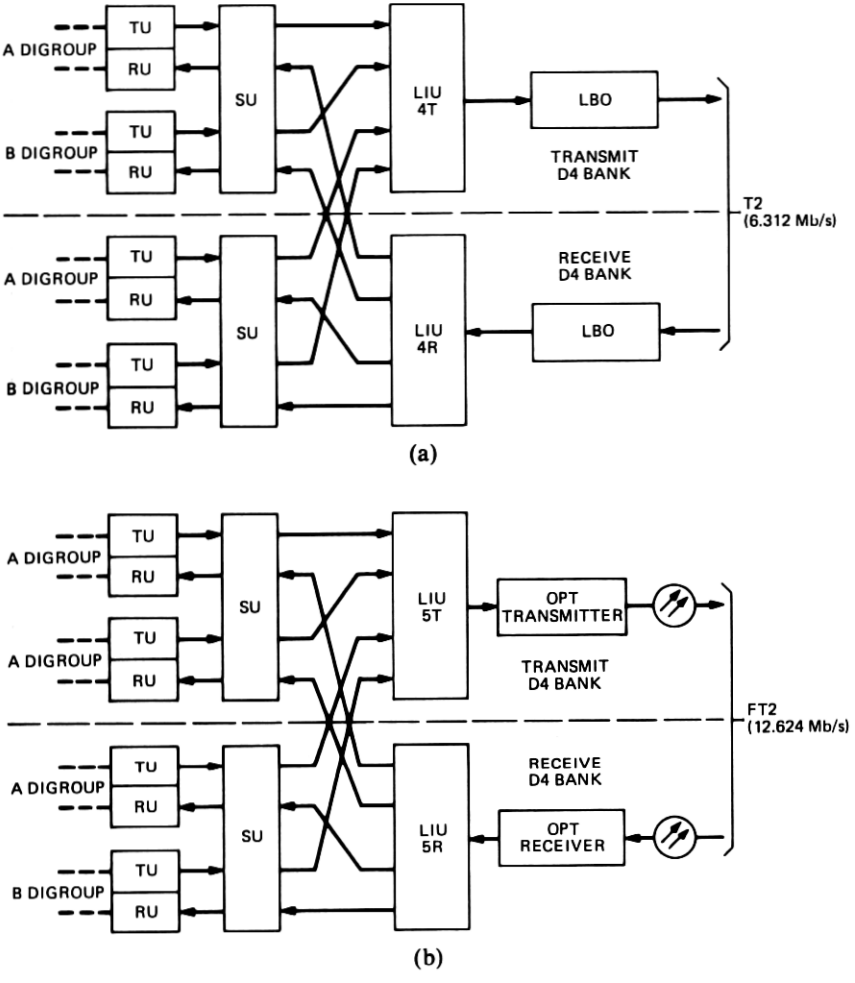

Fig. 4—D4 channel bank mode configurations. (a) Mode 4. (b) Mode 5.

in Mode 4 (Fig. 4a). In this mode, the banks provide an M12 Muldem-compatible signal format and alarm functions.

The most recent expansion of D4 digital facility interface capability is Mode 5 (Fig. 4b), which implements a lightwave system connection. This mode incorporates optical transducers and circuits in the channel banks, as well as multiplexing and coding circuits for optical transmission. The multiplexing circuits are similar to those used in Mode 4. A unique dipulse coding format is employed that takes advantage of the wide transmission bandwidth available and doubles the bit rate (compared to mode 4) to provide for bit-error detection equivalent to bipolar-violation detection employed with wire systems.

III. CHANNEL UNITS

D4 channel units make the D4 channel bank adaptable to a variety of application requirements. The channel unit designs have been responsive to the evolving electronics technology; the functionality and economy of the channel units have been important factors in the success of the D4 channel bank. This section describes conventional channel bank channel units. Other channel-unit designs meet special needs such as those of loop electronics and digital data transmission.

Channel units are the interface between the channel bank common equipment and the central office equipment. The common equipment interface is identical for all channel-unit circuits; the central office equipment interfaces change as a function of the type of service being supplied.

3.1 Generic functions

This section classifies the signals that flow through the channel units into general categories and describes the processing of these signals by the D4 channel unit.

The message signal is typically an analog voice-frequency signal with information flowing from each end of the connection to the other. The channel unit supplies level compensation and, in some cases, gain vs. frequency distortion compensation for each direction of transmission. The electronic processing of the message signal within the carrier system requires that each direction of transmission be separate. In some applications, the message signals for each direction of transmission are on separate pairs of wires at the voice frequency interface to the channel unit. Four-wire channel units are used for this class of application. In other cases, the voice-frequency interface is bi-directional, with the messages for each direction sharing a single pair of conductors for transmission. The appropriate channel unit for this application is called a two-wire channel unit. The circuitry of the two-wire channel unit interfaces between the external bi-directional two-wire interface and the internal four-wire unidirectional format.

All the above functions serve to interface between various external voice-frequency signals (with their associated degradations) and filtering and sampling circuits that reside on the channel unit but are identical for all applications. These circuits interface between a standard internal (to the channel unit) voice-frequency signal format and the pulse-amplitude-modulated and time-division multiplexed signals at the common equipment interface of the channel unit.

In most applications, the digital carrier system must transmit certain control signals in addition to the message signal. This control flow capability is used to oversee the dynamic nature of the traffic that may

be associated with the service. This process is called signaling and, for the purposes of this paper, the signals are subdivided as follows:

(*i*) *Supervisory* signals distinguish between the idle and busy states of a channel. These are typically dc signals that are applied either to the same conductors that carry the message signal or to separate conductors. Supervisory state transitions are used to

(*a*) Seize control of a circuit in response to a service initiation by a customer

(*b*) Oversee the flow of address information between originating and terminating switching machines

(*c*) Inform the originating switching machine when the called party answers or hangs up (control of billing and circuit availability).

Supervisory signals are two-state (busy/idle) signals and change infrequently relative to the digital carrier sampling rate. Robbed bit signaling, which results in 7-5/6 bit PCM encoding, is the technique typically used to transmit this information from one end of the carrier link to the other. The channel unit must detect the state from the central office equipment and reproduce the state to the central office equipment. Timing signals from the common equipment control the sample, hold, multiplex, and demultiplex functions that are performed in the channel unit to support the transmission of these signals.

(*ii*) *Address* signals transfer call routing information from the originating to the terminating office. These signals are most typically transmitted within the message frequency band and, therefore, require no special processing by the carrier system. For other applications, dc signals are used for addressing. Detection, transmission, and reproduction techniques are similar to those for supervisory signals. Addressing signals (dial pulses) change at a higher rate than do supervisory signals; and, therefore, dial pulse percent distortion performance becomes an important system characteristic.

(*iii*) *Alerting* is the process of indicating to the called party that a message is waiting. For most applications this function is controlled by the local office at the called-party end, which means that the carrier system is not involved. For some special services, the alerting is controlled from a remote office, and the carrier system must transmit information to control the low-frequency ringing signals. An additional dc two-state channel (similar to the supervisory channel) facilitates this function.

3.2 Channel-unit applications

The channel unit has the features necessary to meet the wide variety of applications of the D4 channel bank. There are numerous channel-

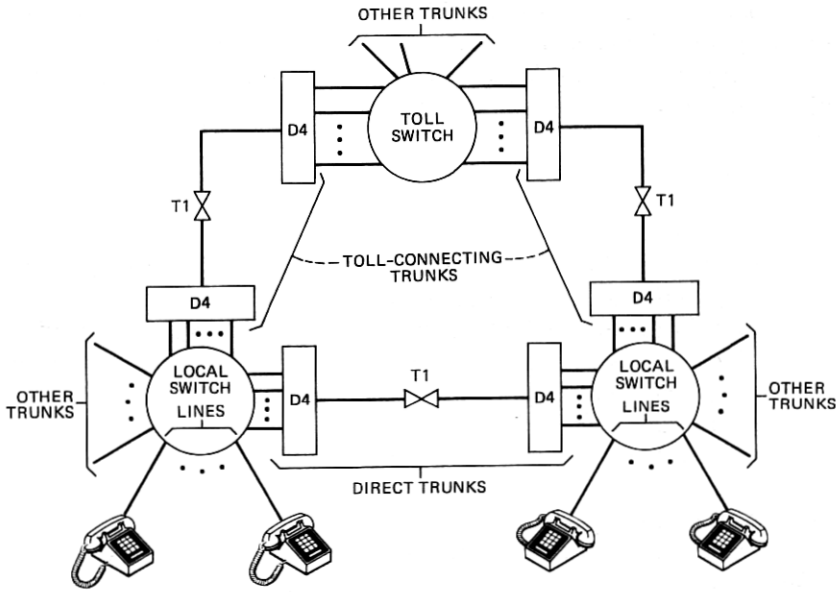

Fig. 5—D4 trunk application.

unit designs; each serves a particular subset of the application spectrum.

Message telephone services interconnect central office switching equipment that serves the switched telephone network. These connections between switching machines are called trunks. The predominant D4 trunk applications are in the local trunk network because of the quantity of trunks involved and because of the suitability of the D4 bank to short-distance applications. Figure 5 depicts these applications. Connections between two local class 5 (or end) offices are called direct trunks. This application represents a large portion of the present D4 applications. These are typically trunks between two-wire switches with superimposed dc signaling except for inband addressing. Toll connecting trunks connect the class 5 local switching machine and the toll switching network. Both two- and four-wire circuits are used for toll connecting trunks. For most applications, the conversion between the four-wire toll switching network and the two-wire local network is performed by the D4 channel unit at the local office end of the toll connecting trunk.

Special services represent a rapidly growing portion of the D4 application spectrum. Transmission equipment is dedicated to a specific customer on a full-time basis. A typical application is diagrammed in Fig. 6. This is a foreign exchange application where a customer is connected to a remote central office by interoffice circuits on a full-

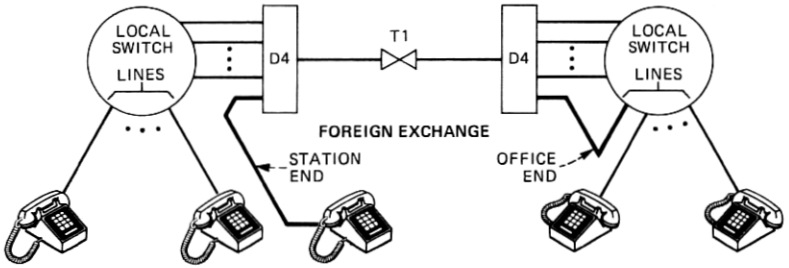

Fig. 6—D4 foreign exchange application.

time basis. The customer with this service is provided local service on the remote telephone exchange. This service is commonly used for a business with a large community of customers in a neighboring city. Other special service applications include trunk connections between the central office switch and a private branch exchange switch, as with a large business customer.

3.3 Functional description

Figure 7 shows the functional block diagram of a typical D4 channel unit. Many of the circuits are customized to the specific applications of each channel-unit type. Manual settings customize each channel unit to a particular application.

Translations between internal logic level signals and the various external signaling conditions from connecting equipment are performed by the signaling circuits. Signaling detectors differentiate among the signaling states from the central office equipment and generate the appropriate logic level signals as inputs to the control logic. Signaling generator circuits receive signals from the control logic and control the output signaling conditions to the central office equipment.

The trunk processing function controls the output signaling conditions when a carrier system fails; the channel unit translates control logic level signals from the D4 common circuits into output signaling conditions or specific conditions on separate wires. This function serves to minimize customer inconvenience and switching machine confusion that would otherwise result from the unpredictable signaling outputs from a failed carrier system.

The hybrid performs the two- to four-wire conversion within two-wire channel units. Internal four-wire operation is used for all channel-unit types. An important performance criteria of the hybrid is how well it isolates signals in the receive direction from signals in the transmit direction. Degradations in hybrid isolation in combination with signal delay, can result in poor echo performance. The degree to

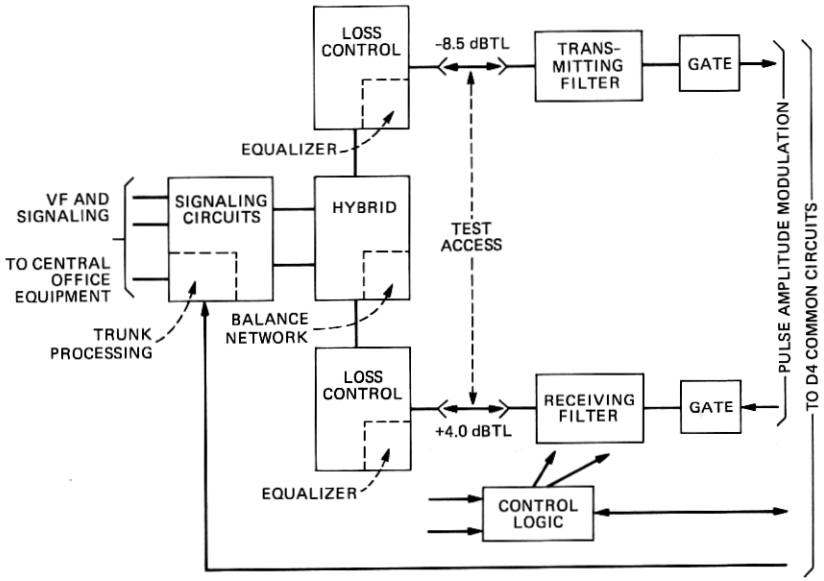

Fig. 7—D4 channel unit functional diagram.

which the balance network of the hybrid circuit matches the two-wire port impedance connected to the hybrid has direct impact on the isolation characteristics of the circuit. Another function of the hybrid (or other input circuit) is to isolate common mode input signals on the balanced input from the unbalanced internal signals. Induction at the fundamental and harmonics of 60 Hz from power lines is the most prevalent source of this interference.

Flat loss (or gain) adjustment is a channel-unit function that allows setting the nominal loss of the end-to-end carrier system and compensating for the transmission loss of the office wiring. Some D4 channel units equalize gain-vs-frequency distortion in external wiring. This is typically required where long lengths of cable interconnect the channel unit to a terminating circuit.

The filter and gate circuits condition the message signals. Thin-film active filters bandlimit the voice-frequency input signals in the transmit direction and reconstruct the continuous voice frequency signals from the PAM output in the receive direction. The input bandpass filter provides attenuation of undesired low-frequency interference and of signals above the 4-kHz Nyquist frequency. The receive reconstruction filter is a low-pass network. The transmission level is the same for all D4 channel units at the input to the transmit filter, [−8.5 decibels-transmission level (dBTL)], and the output of the receive filter (+4.0 dBTL). Each channel unit has a transmit and receive sampling gate.

The transmit gate samples the continuous bandlimited input signal. Under control of the D4 common circuits, the sampling interval is narrow and time sequenced among the channel units in a digroup, with the outputs of all the sampling gates in a digroup wired together to carry out the multiplexing function. The receive sampling gates select the PAM samples for a particular channel from a PAM bus. Timing for this process originates in the D4 common equipment. The function of the control logic on D4 channel units is to interface between the address and timing signals from the D4 common circuits and the sampling and signaling circuits on the channel units. During trouble conditions, trunk processing signals bypass and override the control logic so that proper trunk processing does not rely on the availability of power to the control logic.

3.4 Signaling storage

Signaling storage[15] is an important innovation of the D4 channel bank. In earlier digital bank designs, disturbances in the digital carrier system that cause the channel bank to go out-of-frame temporarily also cause disruption in the trunk and special services network. These short disturbances are a minor impairment for voice message transmission but can cause serious signaling disruptions. Improperly detected idle-to-busy transitions cause multiple false seizures; falsely decoded busy-to-idle transitions may cause disconnection and other difficulties. Predecessors to the D4 channel unit stored only the most recent signaling information as demultiplexed from the receiving common circuits. The D4 channel unit stores multiple successive signaling values. When an out-of-frame event occurs, the common equipment causes the channel unit to cease storing new values and present the oldest stored value to the central office equipment. Because the interval for detecting the disruption is shorter than the interval over which signaling values are stored, the disturbance is successfully bridged. The trunk processing function takes effect for long disturbances.

3.5 Circuit realizations

The signaling interfacing circuits must withstand high-energy signals. For cases where signaling is superimposed on transmission signals, circuit balance must not be seriously degraded by the signaling circuits. Achieving the necessary ruggedness and isolation has led to the predominant use of relay circuits for output signaling states and high-impedance resistive networks for detecting input states. Circuit elements are required to interface between the balanced external transmission circuits and the internal unbalanced circuits. In four-wire channel units this is accomplished by transformers at each interface.

The hybrid circuit provides this function in two-wire channel units. The hybrid function in two-wire D4 channel units is realized with the interconnection of the windings of two transformers to form the four-port network. A compromise network consisting of a series resistor and capacitor may be optionally connected to the network port of the hybrid to approximate the impedance at the switch. In addition, network build-out capacitors are set to compensate for the capacitance of the connecting office wiring. If a VF cable is permanently connected, there is capability for connecting an external precision balance network.

Thin-film resistor networks are used in both the receive and transmit direction to provide settable control of the transmission level of the channel unit. Four-wire channel units typically have lower input transmission levels and higher output transmission levels in contrast to two-wire channel units. The additional gain required is provided by integrated circuit operational amplifiers with resistive feedback gain control elements. The filter circuits consist of operational amplifiers with thin-film RC networks controlling the frequency shaping.[16] The sampling gates are discrete N-channel junction field effect transistors (JFETs). The receive JFET is physically mated to the receive filter so that trimming of the filter can compensate for unit-to-unit variations in the JFET. This results in improved performance. The logic circuit is a custom silicon integrated circuit and is fabricated using the standard buried collector (SBC) technology. The circuit contains about 30 logic gates. The signaling detector is a custom linear SBC integrated circuit. This circuit is a special-purpose comparator and interfaces between the high-impedance signaling interface circuits and the logic circuit. The relay drivers used in the channel units are general-purpose integrated circuits that translate low-energy control signals from the logic into drive signals for the signaling relays. The JFET driver is a custom silicon integrated circuit in the complimentary bipolar integrated circuit (CBIC) technology. High-speed and wide-output signal voltage excursions characterize this circuit that provides an interface between the logic and the JFETs.

3.6 Maintenance and provisioning interfaces

The operational requirements of D4 channel units encompass a wide spectrum. Mechanical options[17] allow each channel unit code to be custom tailored to the application. Increasing the application spectrum for an individual channel-unit type decreases the number of types required at the expense of increased channel-unit cost. The approach in D4 design has been to include only the options that offer significant channel-unit-type reduction with minimal cost penalty, particularly in high-production-volume channel units. One set of option settings con-

figures the channel unit to the type of service being supplied. Examples are the subclass of signaling interface and type of trunk processing. Settings are provided to compensate for external signal degradations and to achieve the desired nominal circuit performance. Gain, equalization, and hybrid balance are all involved. These options are prescription set based on records of the type of connecting equipment, cable gauge and length, and circuit loss requirements.

There is a connector on the faceplate of each channel unit. Test cords are available for interconnecting these connectors and test equipment. Voice-frequency access is provided at the standard internal channel-unit transmission-level point. Access is available in both directions, facilitating both line-side and drop-side testing. Test cords are also available for split-signaling lead access at the same connector. The signaling access point is at the interface between the central office circuits and the channel unit.

Channel units may be connected to a channel bank by a channel-unit extender. The extender splits the access to the transmission and signaling leads at the interface between the channel unit and the distribution frame in the central office. The field-settable options on the channel units are accessible while the channel unit is engaged in the extender.

A maintenance bank facilitates thorough testing of channel units at a centralized location within the central office on an out-of-service basis. Other maintenance functions are also performed; the maintenance bank is discussed in a companion article.[18]

IV. PCM CODING AND MULTIPLEXING

4.1 General overview of transmit and receive functions

The D4 bank is a dual digroup system with nearly independent operation per digroup. Operation is not completely independent because the transmit sections of the digroups share a common clock and both transmit and receive units share a common power converter.

The major functions performed by the transmit and receive units are: encoding, decoding, timing generation for channel units, multiplexing channel-unit signals, frame generation, transmission of data over signaling frame bits, and synchronization of multiple transmit units.

Because the D4 bank must be compatible with D1D, D2, and D3 channel banks, there are three channel-counting sequences. These sequences are electronically controlled by option plugs in the trunk processing unit. In addition, D4 has the option of voice or data channel units. Voice signals are encoded into PAM samples, which are then converted into 8-bit PCM words. Data-channel-unit signals are multiplexed directly into the PCM signal in 8-bit bytes. Special service 5-

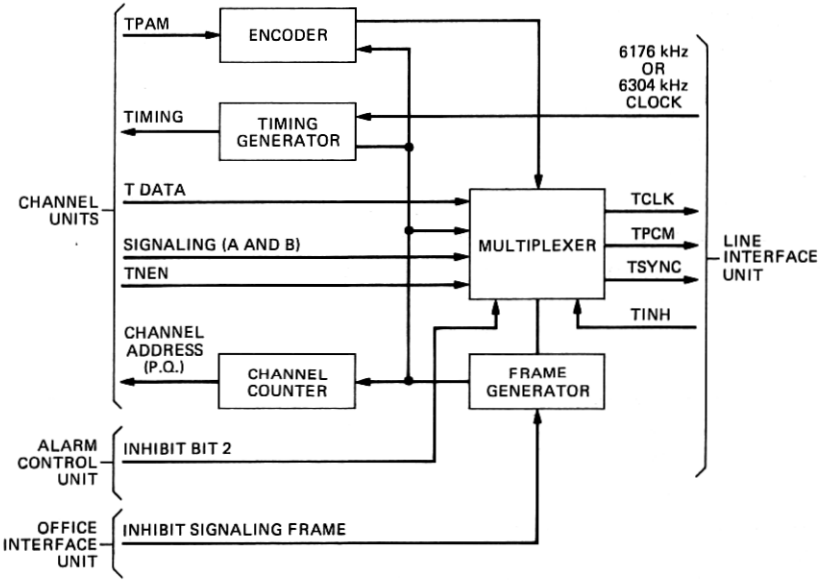

Fig. 8—The transmit unit.

kHz, 8-kHz, and 15-kHz program channel-unit signals are sampled like voice signals but displace one, two, and six voice channels, respectively, to increase the bandwidth. Because the D4 bank has built-in multiplexers, the transmitter and receiver have optionally selectable input clock rates and transmitter and receiver synchronization.

4.2 Transmit unit

The transmit unit (TU) (Fig. 8) provides address and timing signals to the channel units for sampling the voice or data signals, encodes voice PAM samples into 8-bit PCM words, multiplexes the PCM words, and inserts signaling and framing information to form the transmit PCM (TPCM) bit stream. It also provides zero code suppression, which substitutes a fixed word for PCM words having all zeros to meet digital line signal requirements. The signaling frame pattern of the TU can optionally be inhibited so that these frame bits can be used as a slow-speed (approximately 4-kb/s) data channel.

The TU logic is clocked at either 6176 or 6304 kHz by a crystal-controlled oscillator located on the line interface unit.

4.2.1 Timing

The transmit unit generates timing signals used by the channel units to construct time-division multiplexed voice samples on the transmit pulse amplitude modulated (TPAM) bus. These pulses are translated

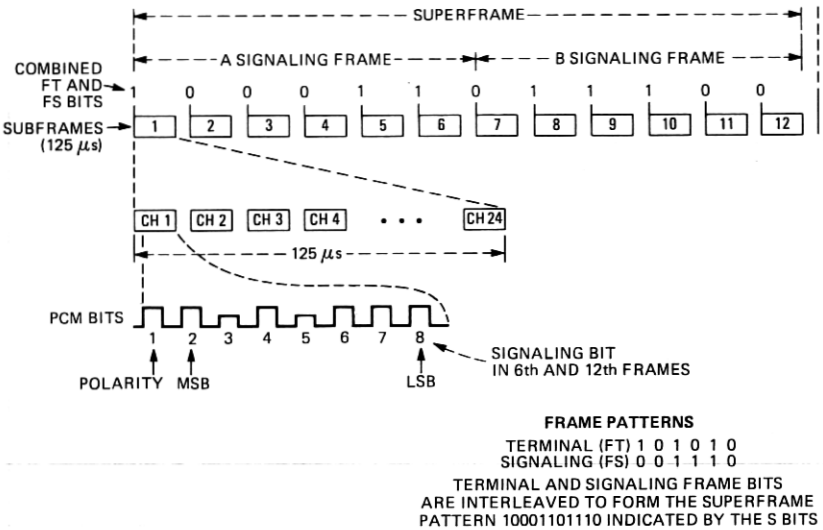

Fig. 9—D4 frame organization.

into 8-bit PCM words within the transmit unit by the encoder. Signaling from each channel unit is substituted for bit eight of these words during every sixth and twelfth frame. To help ensure proper T1 line performance, words with all zeros are substituted with a 00000010 word. This is referred to as zero code suppression. The channel unit has the option of having PAM samples translated in 8-bit PCM words or direct multiplexing of eight data bits. This option is controlled by a bus lead transmit, negated enable (TNEN). When the signal level of TNEN is made a logical zero, PAM samples are encoded into PCM by the transmit unit. When TNEN is a logical one, eight data bits are clocked into the transmit unit and inserted in the digroup bit stream.

The D4 frame organization is illustrated in Fig. 9. It is generated by multiplexing terminal frame (FT) and signaling frame (FS) signal patterns to form a composite superframe that includes 12 subframes. Each subframe includes one frame bit and 24 8-bit PCM words representing the voice samples or data bytes. As indicated in Fig. 9, the composite frame pattern is obtained by multiplexing two frame signals, the terminal frame 101010 pattern and the signaling frame 001110 pattern. The terminal frame pattern is used by the receiver for synchronization to decode the PCM words. The signaling frame pattern identifies the sixth and twelfth terminal frames, which contain the signaling information in bit 8 of each PCM word. The terminal frame must always be sent, but once frame synchronization is achieved, the signaling frame pattern can be replaced by data from some external source. When an external data pattern is substituted for the signaling frame pattern,

per-channel signaling in frames six and twelve is normally disabled although signaling can still be transmitted.

In Modes 2, 3, 4, and 5, each frame consists of 24 8-bit words plus one frame bit (193 bits). When the banks are operating in Mode 1, four additional stuff bits are added (one for each six channels) to form a 197-bit-per-frame signal and the two digroups are frame and bit synchronized.

As we learn in a subsequent section, alarm transmission to the far end terminal is accomplished by suppression of bit-2 (the most significant bit) in every channel time slot.

4.3 Receive unit

The receive unit (RU) decodes the 24-channel PCM unipolar line signal, received from the line interface unit, into PAM signals and necessary control signals for use in the channel units. It also provides signals and controls for maintenance and alarm functions. The functions normally performed by the D4 receive unit are summarized below:

(*i*) Synchronization to the 193-bit-per-frame or the 197-bit-per-frame FT

(*ii*) Synchronization to the FS

(*iii*) Control of signaling storage

(*iv*) Switching from 8-bit to 7-bit decoding during signaling frames

(*v*) Shifting from 7-⅝-bit decoding to 8-bit decoding when common-channel interoffice signaling (CCIS) is being used

(*vi*) Indication of FS and FT bit positions

(*vii*) Channel-unit timing

(*viii*) Provision of electronically controlled 3-mode channel counter

(*ix*) Provision 12-channel shift of the channel counter sequence for testing two-wire channel units

(*x*) Provision of 1-kHz, 0-dBm0 maintenance test code signal

(*xi*) Out-of-frame and loss-of-clock alarm detection

(*xii*) Bit-2 detection for the yellow alarm

(*xiii*) Provision of ac-coupled channel-unit enable pulse to protect channel-unit active filter.

Optional functions that can be performed by the receive unit include:

(*xiv*) Synchronization to the bank transmit frame pattern

(*xv*) Provision of a data channel by means of the signaling frame bits.

Figure 10 is a block diagram of the receive unit. It shows the major functional blocks and interconnections to the other bank circuits. Decoding is done by a shared nonlinear μ255, 15-segment decoder. The output of the decoder consists of received PAM (RPAM) samples, which are supplied to the channel units over a common bus.

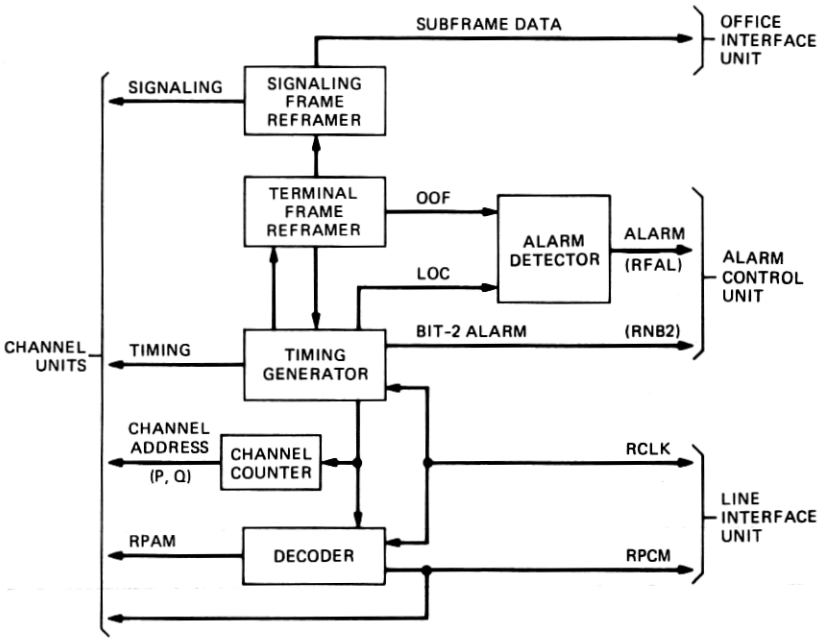

Fig. 10—The receive unit.

The terminal frame reframer synchronizes the timing generator to the incoming 101010 terminal frame bit pattern received from the PCM line. This reframer is an 8-bit-at-a-time reframer with a maximum average reframe time of 43.6 ms. The algorithm for terminal frame reframing is shown in Fig. 11. The signaling frame reframer locks onto the signaling frame pattern to identify the sixth and twelfth frames, which have the signaling information. An out-of-frame (OOF) or loss of clock (LOC) signal is detected by the alarm detector (ALM DET), which sends an alarm signal (ALM) to the alarm control unit. This quiets the voice-frequency noise in each channel unit during the reframe time.

A timing generator, synchronized to the clock recovered from the incoming PCM bit stream, provides timing for the reframers and the receive side of the channel units. This timing generator optionally divides the incoming recovered clock by 193 or 197 to form frame-length words. All frame lengths are 193 except when the bank is operating in Mode 1, which has a 197-bit frame, formed by adding a stuff bit after the frame bit in time slots for channels 6, 12, and 18. As we describe in a later section, when the channel bank is working in Mode 1, a signal derived by the two receive units is used by logic in the LIU to steer demultiplexed data to the proper receive units. This signal is derived from the frame signals of each receive unit, which are

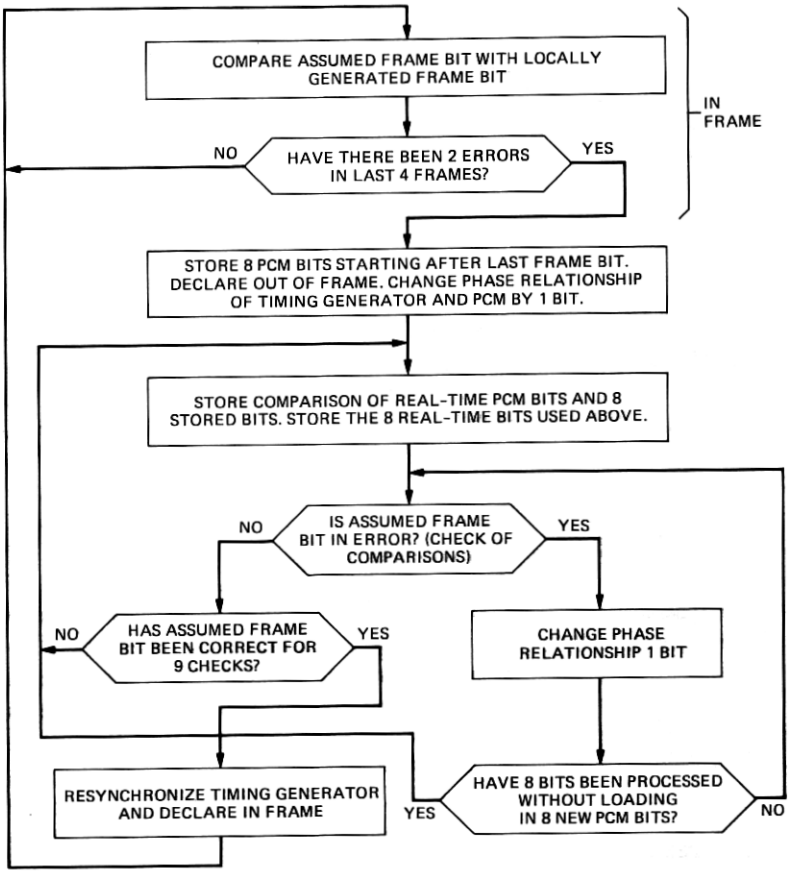

Fig. 11—Reframer flowchart.

algebraically added in receive unit A. The timing generator also extracts the PCM "bit 2" alarm signals for processing in the alarm control unit.

The channel counter derives channel address signals, which are routed over busses to the channel units to activate each channel circuit at the proper time. The signaling frame reframer synchronizes the receiver to the 001110 FS pattern and produces pulses that enable channel units to read the signaling bits into storage registers. The reframer also switches the decoder from 8-bit to 7-bit decoding during signaling frames to prevent the signaling bits from affecting the RPAM samples. The FS reframer is insensitive to errors in the FS bits. In fact, after the circuit has reframed properly on the FS pattern, the FS pattern can be removed, and the receiver will continue to indicate where the FS pattern should be. Insensitivity to FS bit errors provides noise

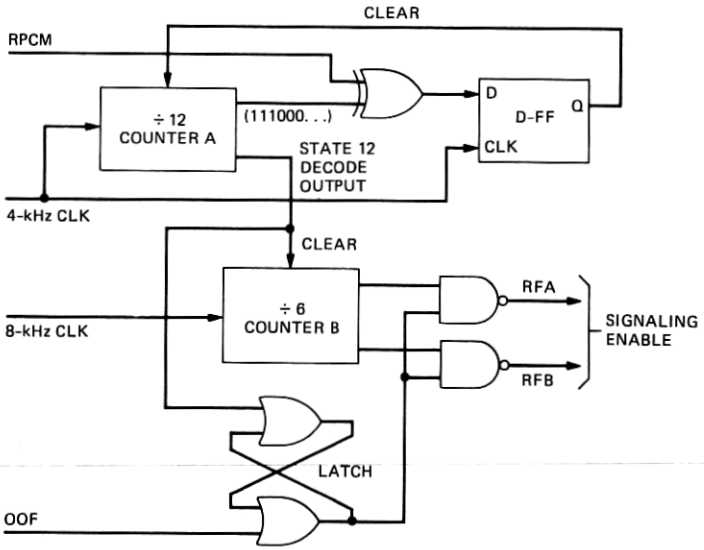

Fig. 12—Signaling frame reframer.

immunity and permits the transmission of data in the FS bit positions while maintaining normal signaling in bit 8 of the voice channels. Data transmission via the FS bit can approach a maximum rate of 4 kb/s. The *SLC**-96 Subscriber Loop Carrier, described in a companion article, uses this subframe data path to send alarm status, concentration, and maintenance information while maintaining full signaling capability.

Figure 12 shows the major portions of the signaling frame reframer. Counter A is a divide-by-twelve counter having an output the same as the 1100 FS pattern. FS bits from counter A are compared with the received FS bits by the exclusive-OR gate. If the FS bits do not match, counter A is cleared and another comparison begins; when the two patterns match over twelve consecutive pairs of FS bits, frame synchronization is recognized; and when counter A reaches state 12, a signal is sent to counter B and the latch circuit. Counter B is then reset and forced into synchronization with the superframe pattern generating the receive frame signal for A digroup (RFA) and the receive frame signal for B digroup (RFB). RFA and RFB are signaling enable outputs to logic in the channel units. If terminal frame synchronization is lost, an out-of-frame (OOF) signal resets the latch and forces RFA and RFB to logic one at the same time to save the stored signaling bits in

* *SLC* is a trademark of Western Electric.

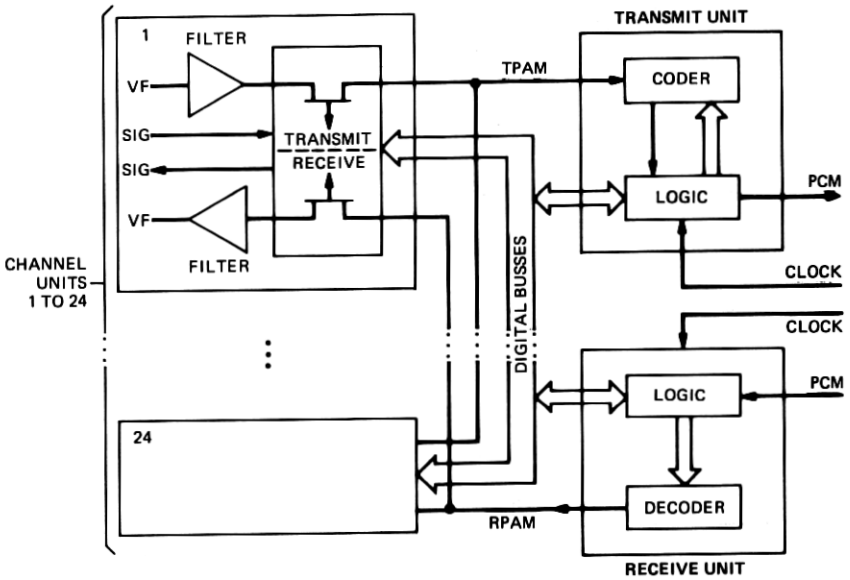

Fig. 13—The CODEC system.

the channel units. The signaling states are maintained until counter A has resynchronized to the signaling frame pattern.

A 1-kHz, 0-dBm0 "digital milliwatt" code generator circuit is provided in the receive logic. It causes the receive unit analog circuits to develop analog PAM samples that are applied to all 24 channel units for receive circuit-level testing. This code generator is activated by inserting a plug into a jack on the faceplate of the receive unit.

4.4 CODEC

The D4 PAM and coder-decoder (CODEC) system is partitioned as shown in Fig. 13. Each of 24 channel units contains a transmit active filter and a receive active filter, plus an integrated circuit that performs voice-frequency sampling and signaling functions for both transmit and receive directions. The remainder of the channel-unit circuitry, not shown in Fig. 13, comprises battery, overvoltage, ringing, signaling, hybrid, and related circuits.

Voice-frequency signals in the channel unit are filtered and then sampled at 8 kHz with a JFET sampling circuit. The PAM samples are time-division multiplexed onto the TPAM bus and sent to the transmit unit, where they are buffered, sampled, held, amplified, and encoded with the nonlinear μ255 successive approximation coder shown in Fig. 14. In the receive direction, serial PCM is formatted by logic in the receive unit into parallel words that are applied to the decoder shown

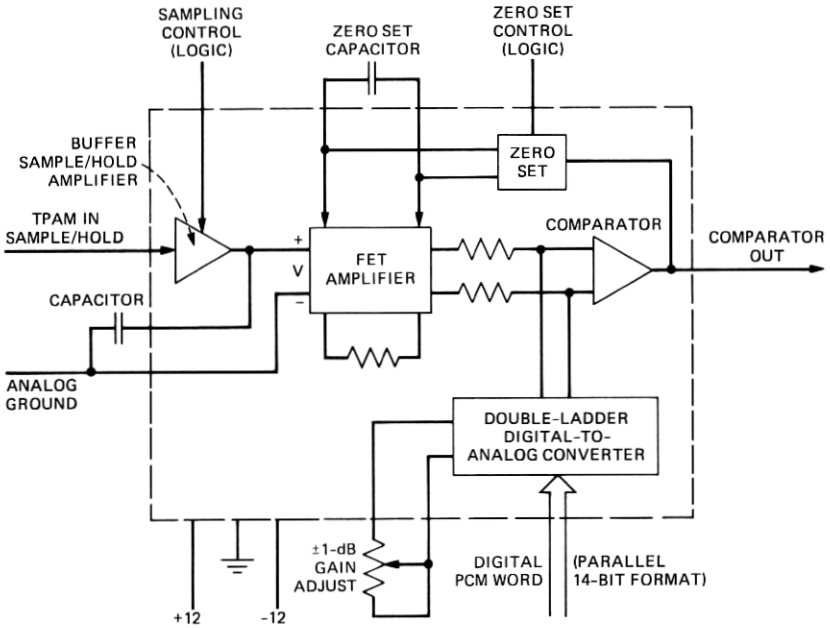

Fig. 14—The coder.

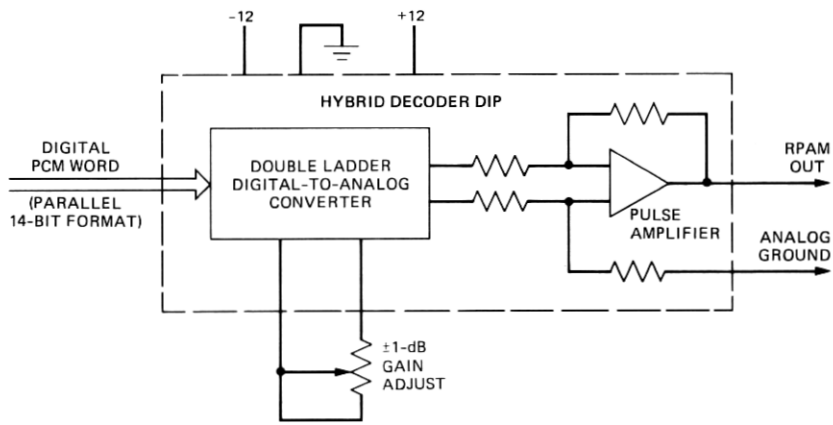

Fig. 15—The decoder.

in Fig. 15. Using the nonlinear $\mu 255$ characteristic, the decoder generates multiplexed PAM samples that are sent to the channel units via the RPAM bus. When each channel unit is addressed (see Fig. 10), a JFET gate applies the proper PAM samples to the receive filter, which reconstructs the voice-frequency signals. The CODEC processes samples

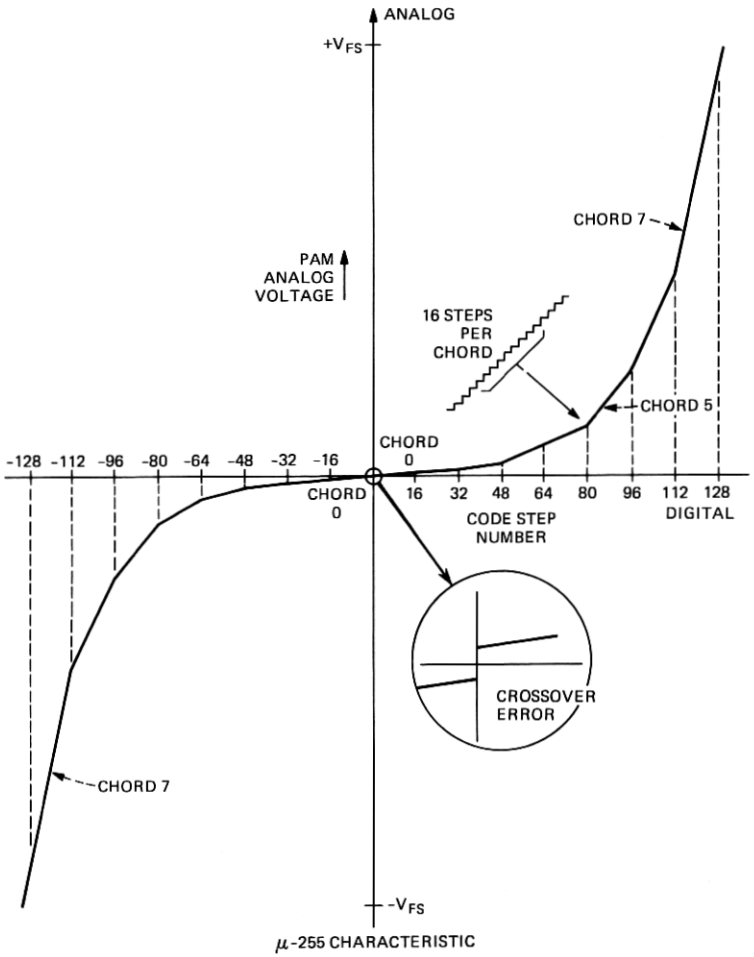

Fig. 16—Nonlinear μ255 companding characteristics of the decoder.

every 5.2 μs (192 kHz). TPAM samples are of approximately 970-ns duration, while RPAM samples are approximately 3.5 μs. The channel-unit operations are timed and controlled by digital busses from the transmit and receive units. The logic devices in these units also control the CODEC timing.

On both the coder and decoder, a digital-to-analog converter (DAC) develops precision voltages that produce the nonlinear μ255 companding characteristic shown in Fig. 16. This DAC consists of one custom silicon integrated circuit and 40 thin-film resistors. A simplified schematic of this DAC is shown in Fig. 17. Any one of the 255 output

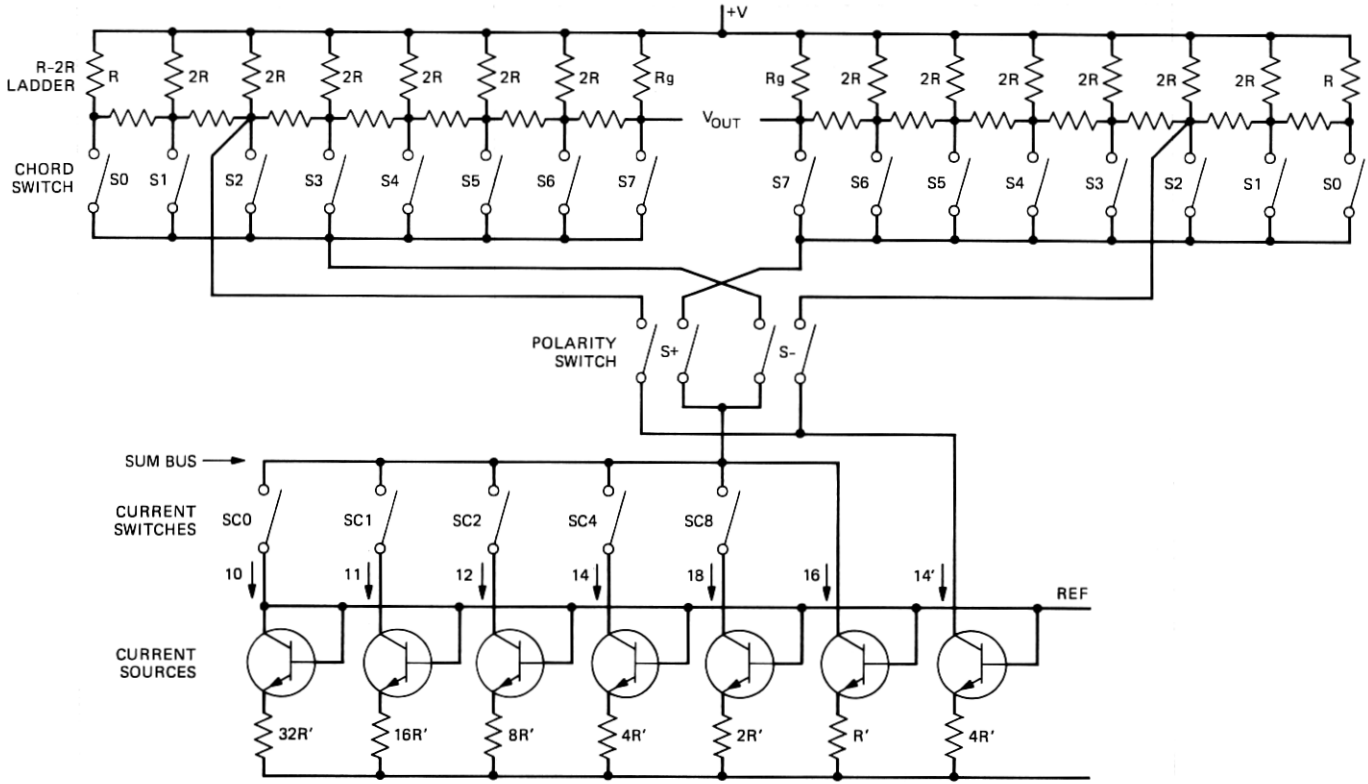

Fig. 17—The digital-to-analog converter.

voltages can be produced at VOUT by choosing an appropriate combination of switches SC8, SC4, SC2, SC1, S+, S−, and S0 through S7. Switches SC1, SC2, SC4, and SC8 can be set to any one of sixteen possible binary combinations, which represent the sixteen possible levels on any chord. Depending on this setting, a specific value of current is drawn from the summing bus (SUM BUS shown in Figure 17). This current is developed by binary-weighted current sources I16, I8, I4, and I1 from a voltage reference (V_{ref}). The polarity of the output voltage is determined by switching on either S+ or S−, thus routing the current to either the positive or negative ladder. Choosing one (but only one) of switches S0 through S7 allows the current to be drawn from the proper node of the R-2R ladder to develop the output voltage. These switches correspond to chords 0 through 7, respectively. At the same time, the polarity switch also routes current I4' (I4' = 14) to the third node of the opposite ladder. This produces a voltage equivalent to I16 through S0 to node 1. Hence, for zero code (either positive or negative) VOUT is ideally zero. In reality, however, a finite voltage difference between positive zero and negative zero exists and causes a nonlinearity, known as crossover distortion (Fig. 16), at the origin of the companding characteristic. This nonlinearity is a primary contributor to gain tracking and signal-to-distortion (S/D) degradation for lower level (≤ -40 dBm0) signals. In addition, crossover distortion can seriously impair the crosstalk and idle circuit noise performance of the terminal. To meet system objectives, a crossover error equal to or less than one-third the least significant bit (LSB) is necessary in the DAC. Switch SCO provides a switchable one-half LSB bias for two applications in the CODEC, as follows:

(*i*) One-half code step midtread bias at the origin of the coder, and

(*ii*) Conversion from 8-bit decoding to true 7-bit decoding in the decoder when the eighth bit is robbed for signaling.

To provide the rapid coding of PAM samples (one decision every 325 ns), the DAC settles to 0.1 percent of final value in less than 100 ns. On the decoder, the DAC drives a differential to single-ended pulse amplifier consisting of six thin-film resistors and a wideband operational amplifier. This pulse amplifier settles to 0.1 percent of final value in ≤ 2 μs. Additional circuits are required in the coder. These include a sample/hold amplifier, a FET amplifier, a high-gain comparator, and a zero set circuit. Also included, but not shown in Fig. 14, is a JFET switch driver, which drives a discrete N-channel JFET that clamps the TPAM bus to ground during encoding to prevent crosstalk between samples and to reduce coding noise. Some of the pertinent requirements for the circuit are as follows:

(*i*) Comparator gain $\geq$ 25,000,

(*ii*) Comparator delay $\leq$ 100 ns with ⅛ code step overdrive (code

step size depends on successive approximation algorithm and typically one transition dominates),

(*iii*) Coder dc offset ≤ 8 LSB,

(*iv*) Sample/hold-buffer amplifier settling time ≤ 900 ns to 0.1 percent of final value,

(*v*) Droop of held sample ≤ ⅛ code step (size depends on sample amplitude).

The basis for the D4 CODEC design objectives is the specification for end-to-end system performance. Because the CODEC is only part of the system, however, CODEC design objective allocations must be derived from these specifications. In deriving objectives, it is important to observe that any coder-decoder combination plus VF filters, sampling gates, etc., must meet end-of-life requirements for new facilities. This automatically allocates less than half of each system requirement to the DAC. How much less than half depends on the sensitivity of other system components to the requirement in question and, therefore, is subject to engineering judgment. Because of this, the objectives are somewhat arbitrary but, nevertheless, consistent with overall system requirements. CODEC and DAC objectives, along with the system requirements, are summarized in Table II. There are several points to note concerning these requirements and objectives. First, all requirements and objectives must reflect the D2/D3/D4 7-⅝-bit coding format, in which 7-bit coding is used every sixth sample to accommodate signaling information. Second, CODEC S/D requirements cannot be directly inferred from those of a single DAC because, for small DAC errors, most of the distortion power is due to theoretical quantizing noise. Last, idle channel noise and crosstalk are dominated more by physical constraints than by circuit design. Theoretically, the CODEC contributes a maximum 17-dBrnC0 idle channel noise and −71 dBm0 crosstalk power, assuming D4 system constraints of 7-⅝-bit coding and a +3 dBm0 virtual overload for the CODEC. The theoretical idle channel noise calculation assumes that low-power white noise perturbs a coder biased at a decision level one LSB. The crosstalk calculation is performed similarly, except that all the power is assumed concentrated in a square wave of peak amplitude one LSB at the crosstalk frequency. This assumption is justified only if the input crosstalk power is sufficiently larger than the input white noise to the CODEC.

DAC gain tracking and S/D performance as specified in Table I can be calculated and plotted by computer simulation, given each of the 255 DAC output voltage levels. However, this method is not practical during laboratory evaluation and production testing. An alternate method, though slightly more stringent, is to directly specify limits on certain output levels. These limits guarantee the aforementioned gain tracking and S/D requirements while simplifying the test procedure. It

Table II—CODEC and DAC objectives

	1-kHz Level (dBm0)	System Requirement (dB)	D4 CODEC Objective (dB)	DAC Objective (dB)
Signal-To-Distortion*	0	33	33	35
	−10	33	33	35
	−20	33	33	35
	−30	33	33	34
	−40	27	27	30
	−45	22	22	26
Gain Tracking*	+3	±0.5	±0.25	±0.08
	0 (Reference)	—	—	—
	−10	±0.5	±0.25	±0.08
	−20	±0.5	±0.25	±0.08
	−30	±0.5	±0.35	±0.12
	−40	±1.0	0.50	±0.23
	−45	±1.0	±0.75	±0.35
Harmonic Distortion	1-kHz Level 0 dBm0	−40	−50	−55
Gain Stability (0°C–50°C)	1-kHz Level 0 dBm0	±0.25	±0.20	±0.05 (150 ppm °C) (0°C–75°C)
Crosstalk Coupling Loss	Level 0 dBm0 200 to 3400 Hz	>65	>75	Not applicable
Idle Channel Noise		23 dBrnC0	20 dBrnC0	Not applicable

* Includes crossover error.

is sufficient to specify only the seven-chord endpoints, zero crossing, full-scale error ratio, and current source ratios to characterize the DAC. Harmonic distortion is calculated assuming a linear gain variation between the positive and negative portions of the coding characteristic. Although this is not absolutely true (different ladders and switches are used), nonlinearities are sufficiently small to make it a good assumption. Second-harmonic distortion is then given by

$$\text{2nd-harmonic distortion} = 20 \log_{10} \frac{2}{3\pi} [1 - R]$$

$$R = \left[\frac{+V_{FS}}{-V_{FS}}\right] (V_{FS} = \text{full-scale voltage}).$$

Therefore, for a second-harmonic better than 55 dB down, $0.992 \leq R \leq 1.008$, where R is the full-scale error ratio. The power supply rejection ratio is chosen based on available power supplies, associated supply noise, and the desired noise immunity and gain stability. Computer simulation, verified by experimental results, was employed to develop the tolerances on the DAC output levels by using the 255 nonideal DAC output levels as coder decision levels with perfect decoder reconstruction levels. The computer calculated and plotted S/D and gain tracking for sinewave inputs of various amplitudes that were then compared with the DAC objectives in Table II. A summary of the derived specifications for the D4 DAC is given in Table III. The specifications pertaining to the other coder and decoder silicon integrated circuits (SICs) that were stated earlier depend more on the implementation of the coding and decoding than on the system requirements. It is obvious, however, that the remaining circuitry must not significantly impair DAC performance, or system requirements will

Table III—DAC requirements

Chord/ Segment	Lower Endpoint Error	Step Size	Step Size Error (Note 1)
7	0 (Note 2)	128 LSB	±2 LSB
6	±4 LSB	64 LSB	±14 LSB
5	±2½ LSB	32 LSB	±½ LSB
4	±1½ LSB	16 LSB	±¼ LSB
3	±1 LSB	8 LSB	±⅛ LSB
2	±½ LSB	4 LSB	±1/16 LSB
1	±¼ LSB	2 LSB	±1/32 LSB
0	±⅛ LSB (Note 3)	1 LSB	±1/64 LSB

Crossover Error: ≤⅛ LSB
Operating Temperature: −40°C to 85°C
Full-Scale Error Ratio (R): 0.8 percent
Power Supply Rejection Ratio: 1mv/V

Note 1: Because current sources are summed to generate chord steps, error may accumulate for each step on the chord, e.g., the maximum error of the top level of chord 5 would be (2 − ½ LSB + 15 × ½ LSB) = 10 LSB.
Note 2: Normalized as the reference.
Note 3: Neglecting dc offset, which is ≤⅛ LSB.

not be met. Operating temperature range, power supply rejection, and gain stability are implicitly assumed in all specifications.

V. DIGITAL FACILITY INTERFACES

The D4 line interface unit functions include unipolar/bipolar digital conversions, transmit timing, clock recovery, maintenance signal looping, coding, and multiplexing/demultiplexing. All modes except 1 and 3 require syndes units, which work closely with the multiplex/demultiplex circuits. PCM signal synchronization, coding, and multiplexing/demultiplexing are not required for Mode 3 operation, which provides independent digroup transmission over two T1 lines. Also, Mode 5 does not require unipolar/bipolar conversion since unipolar logic signals connect to the optical transducers.

The line interface units provide voltage-controlled crystal oscillator (VCXO) circuits, which function as clock generators for timing the transmit units in the bank. The VCXO oscillator is illustrated in Fig. 18. Depending upon the system arrangement, the oscillator may either be free-running or phase-locked to either an external clock (D4 bank externally timed) or to the clock extracted from the incoming PCM (D4 bank loop timed). In the free-running mode, the VCXO is switched to a stable voltage reference to establish the operating frequency. In the externally and looped timed modes the VCXO output is connected to a quadrature phase detector, which forms part of the phase-locked loop (PLL) to control the oscillator. The VCXO specifications are summarized in Table V. The oscillator frequencies are divided by four to obtain the clock signals for the transmit units. The oscillator frequency is higher for Mode 1 because in this synchronous digroup, D4-to-D4 mode, the bank transmit units are operated at 1.576 MHz instead of 1.544 MHz as in the other modes. This allows the oscillator to drive the T1C digital line as well as the bank transmit units. When operated

Table IV—Typical D4 CODEC performance

1-kHz Level (dBm0)	Signal to Distortion (dB)	Gain Tracking (dB)
+3	37.0	±0.1
0	37.5	0 (Reference)
−10	39.0	±0.05
−20	36.5	±0.05
−30	36.0	±0.10
−40	31.5	±0.15
−45	27.5	±0.20

Harmonic Distortion: −52 dB
Gain Stability: ±0.12 dB
Crosstalk Coupling Loss: >80 dB
Idle Channel Noise: 14 dBrnC0 Average

* 7-%-bit coding: *C*-message weighted noise.

Table IV summarizes typical CODEC performance of production units, which is considerably better than the objectives in Table II.

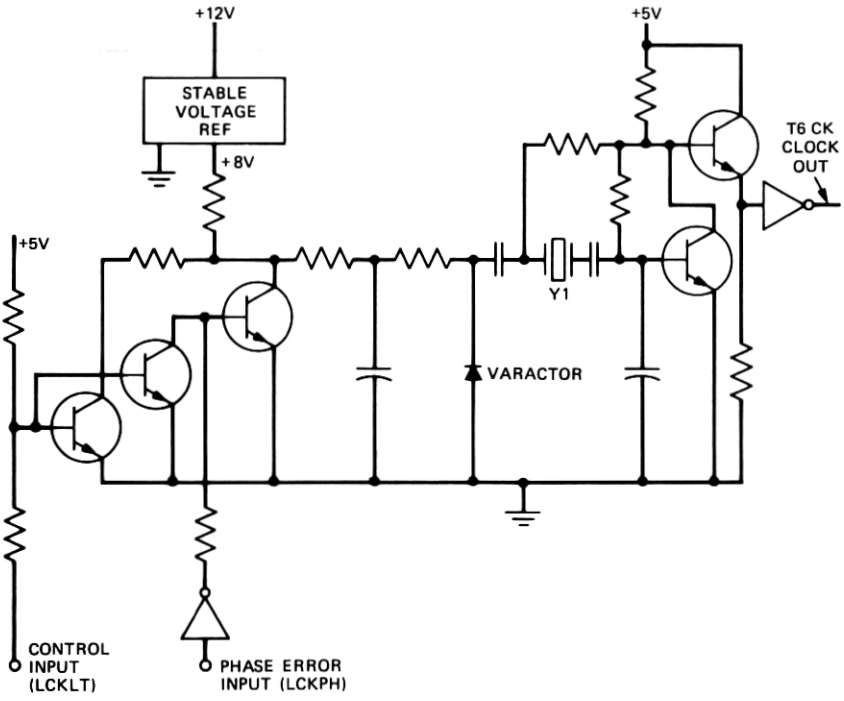

Fig. 18—Voltage-controlled crystal oscillator.

Table V—VCXO specifications

	Specification	
Mode	Frequency (ppm)	Pull Range (Hz)
1	6.304 MHz ± 30	±500
2 to 5	6.176 MHz ± 32	±500

in this mode, the transmit units generate 197-bit frame patterns (instead of 193 bits) by inserting four extra bits per terminal frame, one after every sixth channel. On the receive side, these extra bits are ignored during decoding of the PCM.

5.1 Unipolar-to bipolar conversion

Wire-type digital transmission facilities require balanced bipolar signals. The D4 line interface units provide balanced bipolar signal outputs meeting the requirements depending on the type of facility and far-end terminal to be used in the system.

Figure 19 shows the transmit converter circuit for LIU-1 and -2, along with the associated timing diagram. The unipolar input (TPCM) is converted to bipolar at the output of transformer, T1. The flip-flop

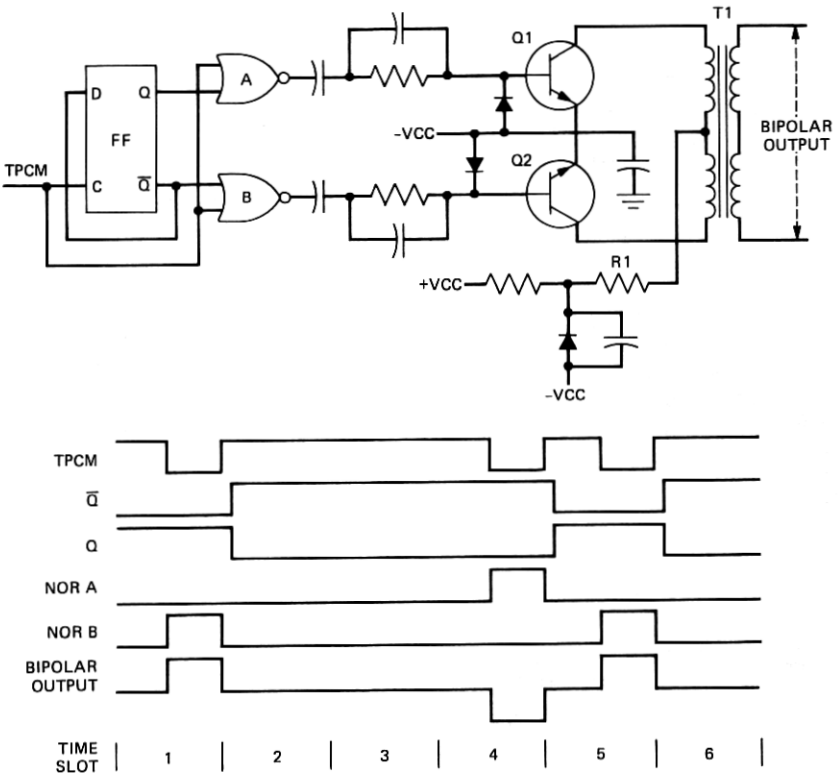

Fig. 19—The transmit converter.

(FF) divides the TPCM input by two, alternately steering the bits through NOR gates to turn ON transistors Q1 or Q2. The outputs of the NOR gates are capacitively coupled to the transistor bases so that, in the absence of the TPCM input, both transistors are OFF. Collector voltage is supplied to Q1 and Q2 by the center tap on T1. Resistor R1 is selected to set the peak pulse amplitude to six volts.

The transmit converter for LIU-3 is a variation of that used for LIU-1 and LIU-2. In LIU-4T the unipolar-to-bipolar conversion circuit is the same as that used in the M12 multiplexer-demultiplexer.

5.2 Clock extraction

Timing of the D4 receive units is derived from the received PCM bit stream. The received clock is extracted from the PCM either by traditional inductor-capacitator, or crystal tank circuits. In the case of the T1 and T1C interfaces, clock is extracted by means of a receive converter circuit,[19] which includes a phase-locked loop. Since the receive converter is embodied in an integrated circuit, this latter

approach has resulted in a significant circuit size reduction for the Modes 2 and 3 line interface units.

Figure 20 shows a block diagram of the receive converter. The circuit accepts the bipolar PCM line signals at the input, extracts the clock by means of the PLL, and provides regenerated PCM data and clock at the output. In addition, the circuit provides unipolar clock and PCM inputs—loop PCM (LPCM) and loop clock (LCLK)—with associated loop control inputs for bank maintenance looping. It also features an automatic output shutdown option to turn off the clock and data outputs in the event of loss of incoming bipolar PCM. This function is provided because when a PLL is used for clock recovery, loss of input signal does not result in loss of clock since the voltage-controlled oscillator continues to operate. Because in some systems a free-running clock is preferred over loss of clock, the circuit provides output shutdown on an optional basis selected by external pin connections. The receive converter, which is implemented in the (CBIC) technology, is described in a companion article describing D4 channel bank integrated circuits.[20]

An important consideration when using the PLL for clock extraction is that the phase comparator must be able to work with a PCM bit stream as an input. This implies that the loop will have the ability to accommodate intervals when timing information is not present. In other words, the output of the clock recovery circuit should ideally remain at its previous phase-locked frequency during the time phase comparisons are not possible (i.e., when a data bit is a logic zero). Since for T1 (1.544-Mb/s) and T1C (3.152-Mb/s) bipolar PCM signals the maximum number of consecutive zeros is restricted to 15, this interval is approximately 9.5 and 4.7 microseconds, respectively.

In the receive converter, these gaps in timing information are spanned by a tristate gate that acts as the phase comparator in the loop. The tristate gate has three output states (logical one, zero, and

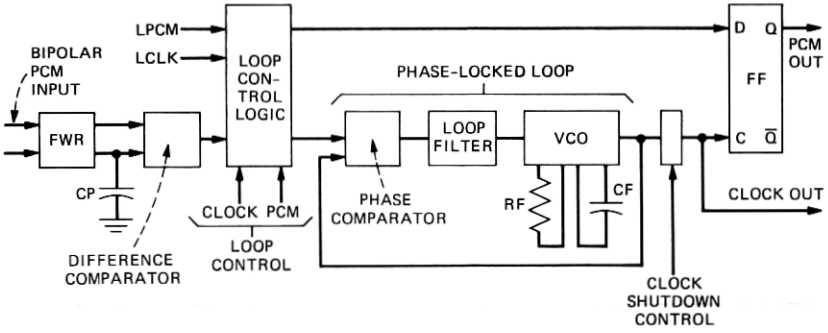

Fig. 20—The receive converter.

high impedance). The gate is forced to the high-impedance state when valid phase comparisons cannot be made because the bipolar PCM input bits are logical zeros. The voltage-controlled oscillator (VCO) frequency is then held by the dc voltage on the loop filter capacitor.

5.3 Maintenance capability

The line interface and syndes unit(s) (SU) provide maintenance capability by means of switchable loop transmission paths so that the transmitted PCM bit stream is looped back to the receiver. If the receiver is able to frame on the looped signal, the bank is judged good. The loop is made as close as is feasible to the digital facility connection in the line interface units to test as much of the bank circuitry as possible.

Because in D4 banks two or four digroups may be multiplexed together, a maintenance loop at the LIU output would disrupt service on any normally operating digroups, as well as those experiencing failures. For this reason, Modes 2, 4, and 5, which have independent digroup operation except for multiplexing, have two levels of looping capability, one in the syndes for individual digroups and another in the line interface unit for the multiplexed output.

The line interface loop capability is unique because it permits an in-service loop test that interrupts the incoming bit stream and bridges the multiplexed output to the input for a period of time long enough to allow frame lock of each receive unit to occur. If any receive units do not achieve frame lock, the logic stores and displays a test fail indication that isolates the cause of failure to the SU synchronizer, or the multiplexer/demultiplexer (MUX/DEMUX).

Whenever a single digroup is looped, an all ones signal is substituted for the PCM and transmitted to the distant terminal. This keeps the digital line repeaters operating and, as discussed in a succeeding section, enables the alarm control unit within the far end terminal to give indication that the near-end digroup has been looped.

The maintenance loop control is derived from the bank alarm control units, which have logic to ensure a normally operating bank cannot be inadvertently looped and interrupt transmission. The LIUs have a special pin-jack option, however, which will override the logic and force loop transmission under out-of-service standby maintenance conditions.

5.4 Equalizers

As we mentioned previously, cable equalizers are installed between the D4 line interface transmit converter and the office digital cross connect or repeater bay. The same set of equalizers is used for the T1 and T1C applications (Modes 1 through 3). There are five equalizer

networks for these applications, each of which is designed to compensate for a range of cable lengths. The equalizers are passive bridged-T-network configurations mounted on small plug-in cards that are installed in the D4 trunk processing unit (TPU).

The Mode 4, T2 interface requires line build-out networks (LBOs) for both directions of transmission. These networks are electrically of the same design as used for the M12 Muldem but have been physically redesigned to fit into the D4 TPU. There are seven different (LBO) codes.

5.5 Multiplexing— Modes 2, 4, and 5

Large-scale integrated multiplex and demultiplex circuits are used in the LIUs for Modes 2, 4, and 5. These custom-designed logic devices are described in a companion article.[20] The same devices are used to optionally multiplex two or four digroups into M1C- and M12-compatible signal formats. The multiplexer, working closely with the syndes unit(s), combines the bit streams of two or four digroups. It also generates and adds a control bit pattern. The control bit pattern is used by the demultiplexer for framing, destuffing, and alarm status indication. The demultiplexer frames on the incoming signal and separates the data into two or four digroup signals along with destuffed clock signals. It also decodes alarm information to indicate a remote terminal alarm status.

The M1C- and M12-compatible multiplexed data formats are presented in Figs. 21 and 22.

5.6 Line interface units

The line interface units supply the circuits and signal connections to other bank common units to set up a particular mode of operation. In addition to line interface units, Modes 2, 4, and 5 require SUs for synchronization of the digroup signals. In this section, the line interface circuits required for each D4 mode of operation will be described.

MODE 2 M1C COMPATIBLE FORMAT:

M1 (52)	C11 (52)	F0 (52)	C12 (52)	C13 (4)	(I1/STUFF) (47)	F1 (52)
M2 (52)	C21 (52)	F0 (52)	C22 (52)	C23 (5)	(I2/STUFF) (47)	F1 (52)
M3 (52)	C11 (52)	F0 (52)	C12 (52)	C13 (4)	(I1/STUFF) (46)	F1 (52)
M4 (52)	C21 (52)	F0 (52)	C22 (52)	C23 (5)	(I2/STUFF) (47)	F1 (52)

- THE FRAME ALIGNMENT SIGNAL IS F0, F1, WHERE F0 = 0 AND F1 = 1.
- THE MULTIFRAME ALIGNMENT SIGNAL IS M1, M2, M3, M4 AND IS 011X, RESPECTIVELY, WHERE X IS AN ALARM SERVICE DIGIT.
- THE STUFFING INDICATOR WORDS ARE Ci1, Ci2, WHERE i = DIGROUP CHANNEL.
- ( ) = NUMBER ENCLOSED REPRESENTS NUMBER OF INFORMATION BITS.
- INFORMATION BIT FORMED BY INVERTING DIGROUP CHANNEL 2 FOLLOWED BY MODULO TWO SUMMATION WITH CHANNEL 1.

Fig. 21—Format of the Mode 2 multiplexed data stream.

MODE 4 M12 COMPATIBLE FORMAT:

M1 (49)	C11 (49)	F0 (49)	C12 (49)	C13 (49)	F1 (I1/STUFF) (48)
M2 (49)	C21 (49)	F0 (49)	C22 (49)	C23 (49)	F1 (1) (I2/STUFF) (47)
M3 (49)	C11 (49)	F0 (49)	C32 (49)	C33 (49)	F1 (2) (I3/STUFF) (46)
M4 (49)	C41 (49)	F0 (49)	C42 (49)	C43 (49)	F1 (3) (I4/STUFF) (45)

- THE FRAME ALIGNMENT SIGNAL IS F0, F1, WHERE F0 = 0 AND F1 = 1.
- THE MULTIFRAME ALIGNMENT SIGNAL IS M1, M2, M3, M4 AND IS 011X, RESPECTIVELY, WHERE X IS AN ALARM SERVICE DIGIT.
- THE STUFFING INDICATOR WORDS ARE Ci1, Ci2, Ci3, WHERE i = DIGROUP CHANNEL.
- ( ) = NUMBER ENCLOSED REPRESENTS NUMBER OF INFORMATION BITS.
- INFORMATION BIT MULTIPLEXING IS I1 I2 I3 I4 I1 I2 . . . (I2 AND I4 ARE INVERTED).

Fig. 22—Format of the Mode 4 multiplexed data stream.

5.6.1 Mode 1

Mode 1 provides a unique dual digroup operation over the T1C digital lines. In this mode, full advantage is taken of the inherent synchronization properties of two commonly clocked digroups for an economical D4-to-D4 connection. Both multiplexing and alarm functions are integrally related for the pair of digroups.

A single alarm circuit is provided that responds to failures in either digroup and removes all 48 VF channels from service if either receive unit loses frame synchronization. Only one alarm unit is used because circuits associated with the individual digroups, as well as those shared, must be working normally for proper Mode 1 operation.

Figure 23 is a block diagram of the line interface for Mode 1 bank operation. This unit is designated LIU-1. The circuit multiplexes the two 24-channel digroups (ATPCM and BTPCM) with a bit rate of 1.576 Mb/s into a composite signal at the T1C line rate of 3.152 Mb/s. Multiplexing is done with the two digroups synchronized such that a bit from the A digroup is alternated with a corresponding bit from the B digroup, as shown in Fig. 24. The multiplexed signals are then scrambled in a one-bit scrambler to randomize the bit stream. The transmit converter changes the unipolar format into bipolar to drive the T1C line.

On the receive side, the receive converter accepts the bipolar input from the T1C line, converts it to unipolar, extracts clock, and produces the regenerated, scrambled PCM and clock. After descrambling, demultiplexing is done by alternately clocking two D-type flip-flops. Since demultiplexing in this manner can result in arbitrary steering of the A and B digroup bit streams at start-up, there is equal probability of steering the A digroup bit stream to the B receive unit. Knowledge of A-bit followed by B-bit multiplexing scheme and signals from the A and B receive units provide the means to automatically correct the data steering if it is incorrect. The logic in essence requires that the A frame bit occur before the B frame bit. If the B frame bit precedes the

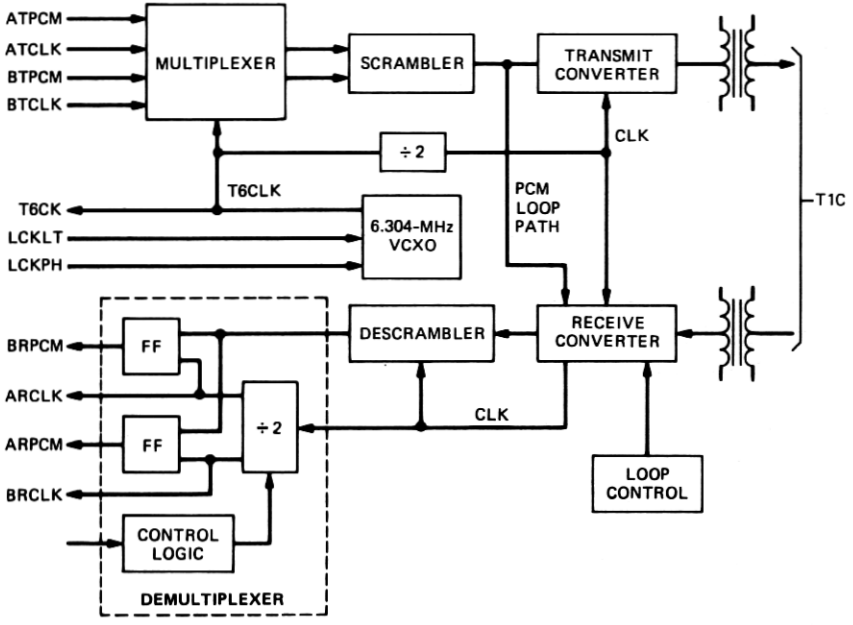

Fig. 23—Line interface unit-1.

MODE 1 MULTIPLEXED DATA FORMAT:

S_A S_B $F1_A$ $F1_B$ (96) $F1_A$ $F1_B$ (96) $F0_A$ $F0_B$ (96) $F0_A$ $F0_B$ (96) ....

CH 1-6 CH 7-12 CH 13-18 CH 19-24

- SUFFIXES A, B REFER TO A AND B DIGROUPS, RESPECTIVELY.
- SUPERFRAME BITS: F1 = LOGICAL ONE, F0 = LOGICAL ZERO.
- S_A, S_B ARE S BITS OF A AND B DIGROUPS, RESPECTIVELY.
- (96) = REPRESENTS 96 PCM BITS, 8 BITS PER CHANNEL, 6 CHANNELS FROM DIGROUP A AND 6 FROM DIGROUP B. PCM INTERLEAVED, I.E. –

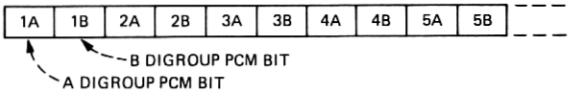

Fig. 24—Mode 1 multiplexed data format.

A frame bit, the logic inverts the phases of ACLK and BCLK to the flip-flops such that the receive units do not go out of frame and the data is properly strobed.[21]

The clock generator has a 6.304-MHz clock (T6CLK), which controls timing for the LIU multiplexer, transmit converter, and the two transmit units.

Maintenance looping to test bank operation is provided through the

receive converter circuit, which is controlled by the bank alarm unit. When the maintenance loop is activated, the receive converter switches from the normal PCM input to the loop path and the transmit converter supplies an all-ones code to the distant terminal.

5.6.2 Mode 2

A block diagram of LIU-2 is shown in Fig. 25. As mentioned previously, Mode 2 is M1C multiplex compatible, requiring that the asynchronous digroups be synchronized for multiplexing. The multiplex/demultiplex circuits work with the syndes circuit (Fig. 26) to synchronize the digroup signals on the transmit side (TPCM) and perform a desynchronizing and smoothing of the digroup signals on the received, negated PCM (RNPCM). There are two identical but independently operating syndes circuits on the SU, one for each digroup. In each syndes 8-bit, elastic store circuits provide temporary storage for both the synchronizing and desynchronizing functions. The elastic store in the synchronizer has data sequentially written in by the transmit clock (TCLK) and data read out by the multiplexer clock (MCK). The multiplexer inserts stuff bits (Fig. 21) when the elastic store stuff request (SR) is activated. Desynchronizer input data is DCH, which is written in by the destuffed clock (DCLK). The read clock (RCLK) is generated by a VCO, which is phase-locked to the write clock. The bandwidth of the phase-locked loop is set to greatly reduce the jitter introduced by bit stuffing and control bit multiplexing.

The multiplexer and demultiplexer circuits (Fig. 25) are complementary metal oxide semiconductor (CMOS) large-scale integration (LSI)

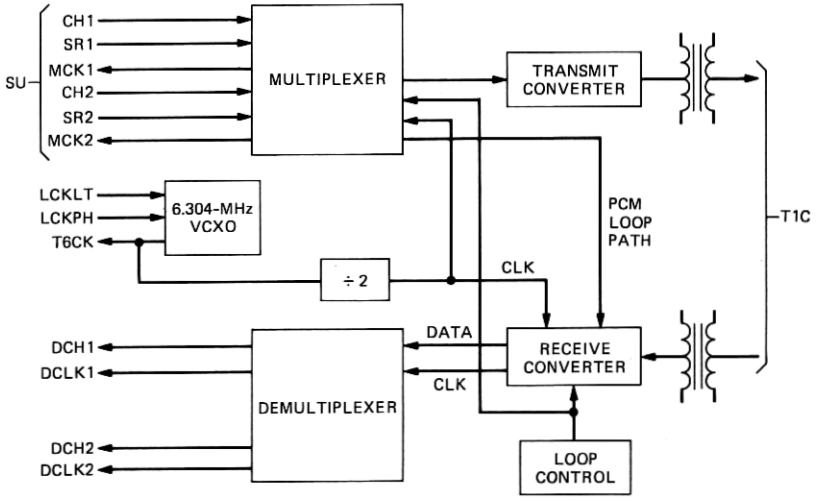

Fig. 25—Line interface unit-2.

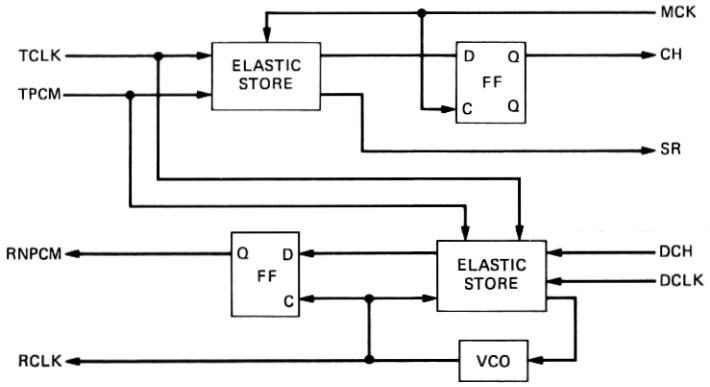

Fig. 26—The syndes circuit.

devices that supply the M1C-compatible format, and the transmit and receive converters provide the line interface functions, both of which we described earlier.

The loop control logic activates the loop path for maintenance. As we noted previously, there are two modes of looping: one is the fast loop, and the other is a maintenance loop, which loops the transmitted data and transmits all ones on the T2 line.

5.6.3 Mode 3

As we see in Fig. 27, the line interface unit for Mode 3 is an essentially independent digroup operation over T1 lines. It consists primarily of transmit and receive converter circuits for each digroup, which interface with the T1 lines. A common 6.176-MHz VCXO provides transmit timing for both digroups. There are independent digroup alarm and maintenance loop functions in this mode.

5.6.4 Mode 4

Mode 4 is a dual D4 bank configuration that multiplexes four digroups into an M12-compatible DS2-level signal. Because two D4 banks must be interconnected to combine the signals, wires must be added between one backplane connector on each of the banks. In addition, a transmit line interface unit (LIU-4T) is inserted in one bank and a receive line interface unit (LIU-4R) in the other. The transmit LIU multiplexes four digroup signals from both banks, and the receive LIU demultiplexes the four digroup signals. Figure 28 illustrates the line interface units and major interconnections between banks.

As with Mode 2, the banks have syndes units installed for the synchronization/desynchronization of the digroup signals. In effect,

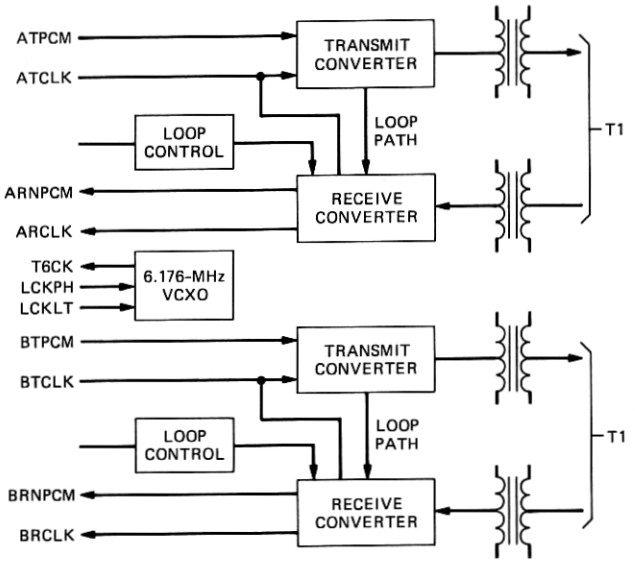

Fig. 27—Line interface unit-3.

Mode 4 incorporates an M12 multiplexer within the banks. This has been made physically possible by the LSI multiplex devices.

The code translator establishes the binary six zero substitution (B6ZS) coding to meet the T2 and M12 compatibility requirements.

Both the in-service fast loop and maintenance loops are included in the LIU circuits. The 6.312-MHz crystal oscillator (XO) provides the timing for both the multiplexer and the T2 line. The 6.176-MHz VCXO oscillators generate transmit clock signals for the bank transmit units.

A variation of Mode 4 is also available that is an M12-compatible interface to T2 facilities at intermediate power stations for add/drop capability. This mode, termed Mode 4A, requires LIU-4TA and LIU-4RA, which are similar to those shown for Mode 4 except that it has lightning protection, since the LIUs interface to T2 lines without intervening T2 office repeaters.

5.6.5 Mode 5

The recent addition of a lightwave system interface capability to the D4 banks illustrates the flexibility of both the electrical and physical architecture of the D4 design. The information-carrying capacity of Mode 5, as well as much of the line interface circuitry, is the same as for Mode 4. In Mode 5, two banks are interconnected, and the four digroups are multiplexed using the same devices as in Mode 4.

Figure 29 is a block diagram of the line interface units for Mode 5. The optical transducer circuits are not physically located in the LIUs

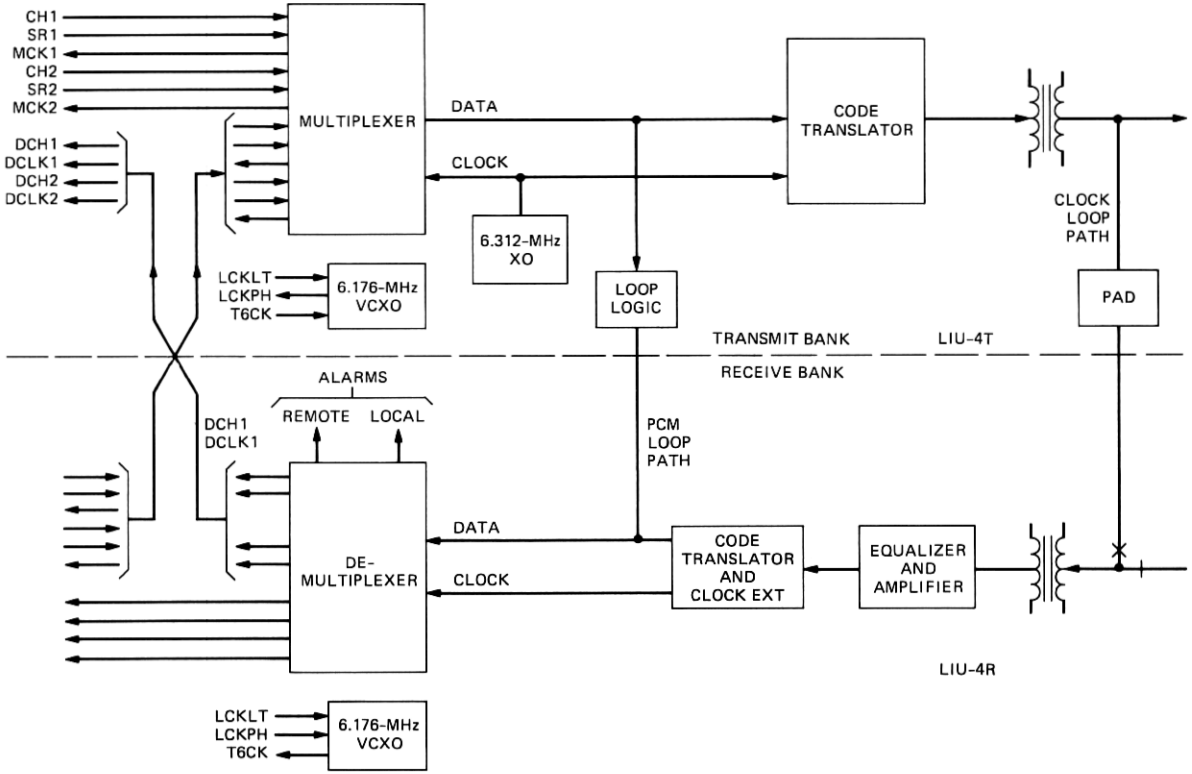

Fig. 28—Line interface units-4T and -4R.

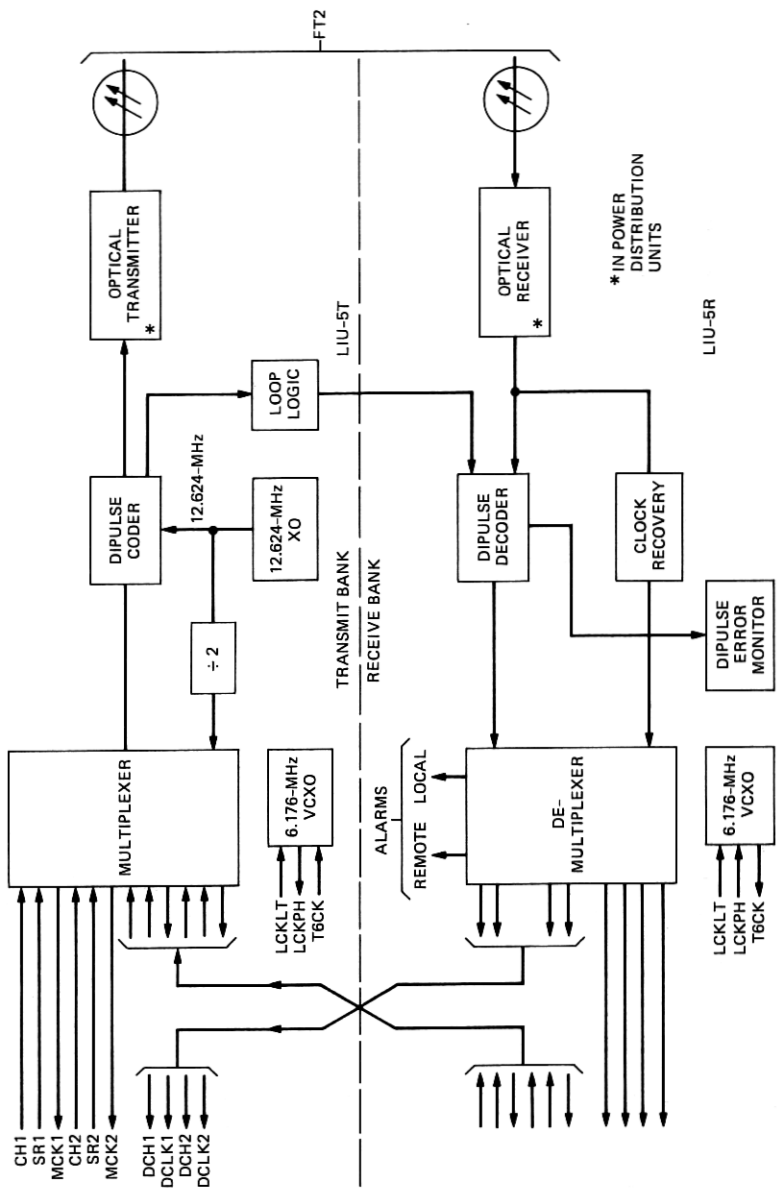

Fig. 29—Line interface units-5T and -5R.

but in special power distribution units where the optical fibers are connected.

Because the lightwave system components have much greater bandwidth available than necessary for the 6.312-Mb/s multiplexed data, the data is dipulse coded. The dipulse code format has several advantages for the lightwave application. It has two levels, avoiding nonlinearity problems with the laser, which would result from a three-level code; there are no long strings of zeros, thus making timing recovery easy; and redundancy is included for error detection.

The dipulse coding scheme uses only two levels to achieve analogous capability to three-level bipolar coding used with the wire systems. Correspondence of the two coding schemes is illustrated in Table VI below. Use of the dipulse code doubles the lightwave system bit rate to 12.624 Mb/s. The dipulse coded signal drives an injection laser transmitter. On the receive side, an avalanche photo diode (APD) detects the lightwave pulses, which are processed by an optical receive circuit. The APD receiver has automatic gain control with a dynamic range of approximately 85 dB.

The dipulse decoder converts the bit stream back to 6.312 Mb/s for demultiplexing. It also detects dipulse code errors that accumulate in the error monitor and turn on an LED indicator if the bit error rate exceeds 10^{-6}. Alarm control units initiate trunk processing to remove the banks from service if the digroup error rates exceed approximately 10^{-3}.

Present lightwave component technology allows this Mode 5, FT2-level signal to transverse lightguide distances of up to 4.5 miles without optical repeaters. This corresponds to maximum optical loss of 48 dB.

Connection to the lightguide cable is made through protected single fibers that connect at the rear of the power distribution units on one end and at the lightguide cable interconnection equipment (LCIE) at the other. The LCIE provides the terminations for the incoming lightguide cable. The lightguide ribbons (12 fibers per ribbon) are connected to a fan-out assembly, which provides separate connectorized fibers. The lightguide fiber is a low-loss graded-index type with a 55-μm diameter core.

Table VI—
Correspondence of bipolar and dipulse coding schemes

Bipolar Code	Dipulse Code
+1	11
0	10
−1	00

D4 Mode 5 and the other FT2 system components utilize modified versions of the optical circuits developed for the FT3 Lightwave Digital Transmission System, as well as the same lightguide cable, LCIE, and hardware. The optical transmit circuit uses a GaAlAs injection laser diode operating at a wavelength of 825 nm. In the optical receiver, the APD circuit current gain ranges from approximately 6 to 120. Bias for the APD is supplied by a ±5 to −575 volt dc-to-dc converter and a high-voltage regulator circuit.

5.7 Office interface

D4 office interface units (Fig. 1) are optionally used as a common access point for connecting the D4 bank to external timing sources. They also are used as circuits for loop timing of the transmitted PCM with the received clock. Loop and external timing of the banks is required by electronic switching system (ESS) switches and digital data system (DDS) applications.

VI. ALARMS AND TRUNK PROCESSING

6.1 ACU functions

The D4 alarm control unit (ACU) is the alarm center for the D4 channel bank. In all modes except Mode 1 ACUs are required for each digroup to monitor alarm status and facilitate location of transmission failures.

As Fig. 30 shows, the ACU monitors outputs from the receive unit to

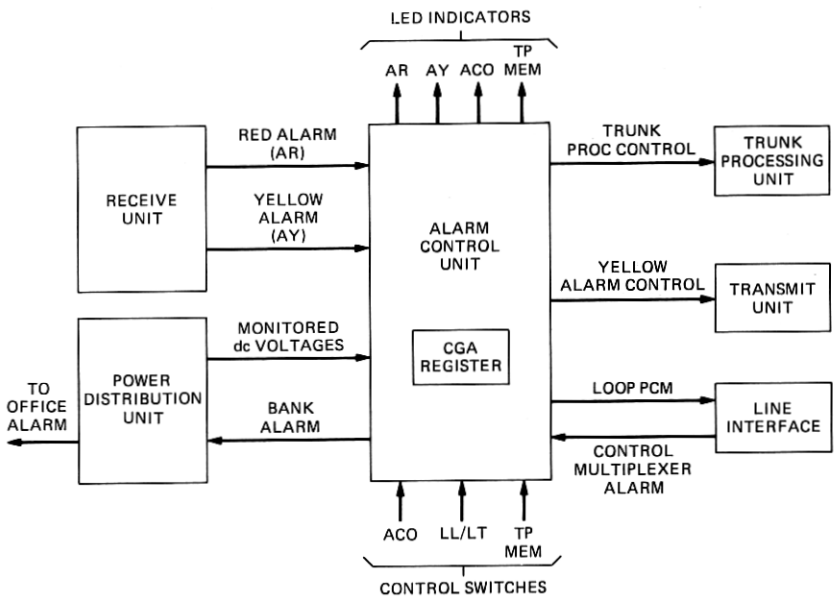

Fig. 30—Bank alarm and maintenance.

detect incoming alarms and control trunk processing, local office alarms, and transmission of alarm signals to banks at distant offices. In addition, it initiates alarms in response to dc power failure. The ACU controls trunk processing to remove trunks from service when a failure occurs (carrier group alarms) and totals the number of times service is lost by an electromechanical register.

Features of the D4 design include a minimum 2.0-second delay before bank and office alarms are turned on and trunk processing is initiated (versus 0.3 second for earlier banks). In addition, the features include hit integration, which reduces sensitivity to sporadic alarm signals while maintaining capability to alarm when intermittent alarm signals persist. The ACU timing circuits utilize current sources to drive capacitors connected to the input of comparators obtaining nearly linear voltage changes. Hysteresis enables positive comparator output switching to occur at the timing threshold voltages. The active circuit portions of the timers comprise two 16-pin dual in-line package (DIP) integrated circuits, and the ACU logic is contained in two custom transistor-transistor logic (TTL) gate array devices. Figure 31 is a functional block diagram of the alarm control unit.

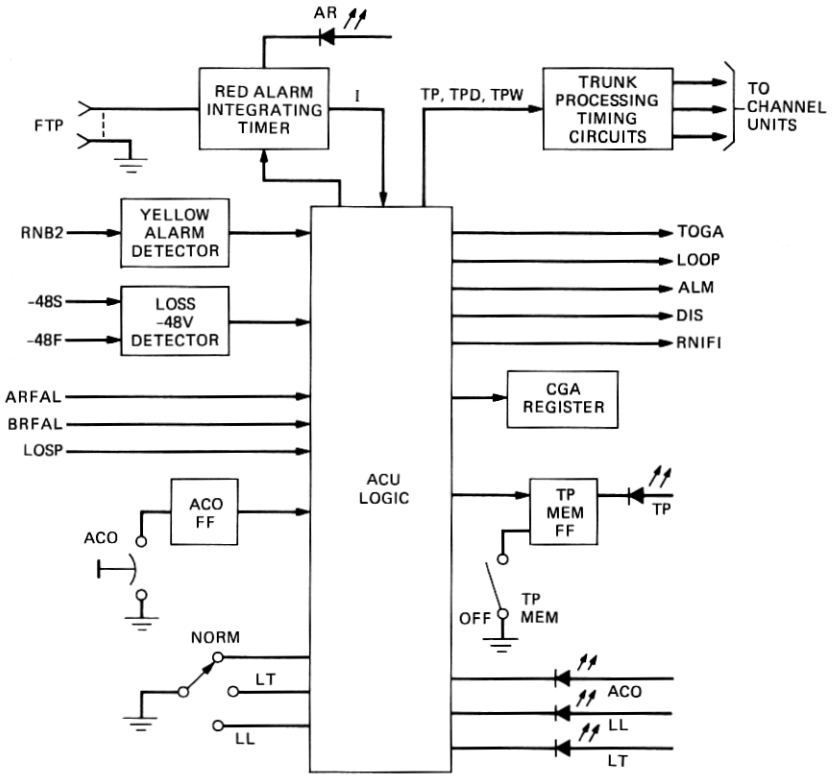

Fig. 31—Functional diagram of the alarm control unit.

6.2 General description of operation

6.2.1 Red and yellow alarms

The ACU responds to several types of alarm conditions that indicate digital line or bank failure. They are designated as red alarm (AR) when locally detected and yellow alarm (AY) when detected at the distant terminal. Red and yellow light-emitting diode (LED) indicators are mounted on the ACU faceplate. The AR indicator is ON whenever an alarm signal is present; however, trunk processing is not started, and bank and office alarms are not turned on until after the 2-second delay interval. In the case of a yellow alarm the indicator turns ON, trunk processing is initiated, and bank and office alarms are triggered simultaneously after the alarm is detected (approximately 450 ms).

A red alarm occurs as a result of loss of incoming digital information, either because of digital line or local bank receive side failure or a bank power failure. A yellow alarm occurs as a result of transmitting line or transmitting side local bank, or receiving side at the distant terminal failure. The yellow alarm is transmitted by the distant bank when it indicates a red alarm. Another alarm situation is presented as simultaneous red and yellow alarms. This happens when a yellow alarm is followed by a red alarm and occurs if the far end detects a red alarm and is looped to determine if the failure is within that bank.

6.2.2 Trunk processing

After initial timing requirements are met, a red or yellow alarm causes the ACU to initiate trunk processing to remove the trunks from service. Circuits within the ACU signal to operate relays located in the trunk processing unit. Contacts on these relays are connected to the channel units to control trunk processing. A yellow LED (TP), located on the ACU faceplate, is turned ON to indicate the bank is out of service. After the alarm has been cleared and a nominal delay interval of 15 seconds has elapsed, the bank is returned to service and the TP indicator is turned OFF. In the case of the yellow alarm, the restoral delay is controlled by the bank transmitting the yellow alarm. This results in a coordinated restoral of the system into service.

6.2.3 Alarm cutoff

The ACU has a pushbutton alarm cutoff (ACO) to turn off bank and office alarms. Depressing the ACO pushbutton will cause the ACO LED to be locked ON and the bank and office alarms to be turned OFF. The ACU panel alarm indicators (AR and AY) are not extinguished, however, until the trouble is cleared. If an alarm occurs as a result of a fuse operation or power converter failure, the ACO pushbutton is

prevented from clearing the bank and office alarms. In these cases, the ACO LED will not turn ON, and the fuse must be replaced, or the power converter turned OFF to silence the alarms.

6.2.4 DC power monitoring

The ACU monitors particular −48-volt office battery leads and the output voltages of the bank dc-to-dc converter and performs the following functions:

(*i*) Loss of −48 volts: Immediately turns on AR indicator, and after approximately 2.5 seconds, it turns on bank and office alarms and initiates trunk processing.

(*ii*) Loss of dc-to-dc converter outputs: Immediately initiates bank and office alarms and causes trunk to be removed from service.

6.2.5 Troubleshooting

The ACU provides a switch (LT/LL) that conditions the bank to aid in locating troubles. The switch is only functional when the trunks are removed from service by the TPU (normally as a result of an AR or AY alarm and ACO operation). With the switch set to the LT position, the maintenance loop is activated. This causes the digital output of the bank to be looped to the input in the line interface unit to determine whether the bank is operating normally. In the LL position, the yellow alarm is transmitted to hold the bank out of service to allow trouble-shooting of digital line problems by transmission loop patches at repeater locations. When the patch provides good transmission, the red alarm at the bank clears but the yellow alarm is looped to hold the bank out of service. Proper operation of the LL feature requires that *both* bank LL switches be thrown to avoid inadvertent restoral of one or both terminals under "noisy line" conditions.

6.3 Circuit overview

Refer to the functional block diagram of the ACU as presented in Fig. 31. The ACU logic is implemented in two custom TTL gate array devices. There are five timing circuits in the ACU; two are illustrated explicitly in Fig. 31 as the red alarm integrating timer and yellow alarm detector. The three remaining timing circuits are incorporated in the trunk processing timing circuits and ACU logic. All of the switches and LED indicators are located on the ACU faceplate.

The red alarm inputs are loss of PCM (LOSP), A digroup of frame alarm (ARFAL), and B digroup frame alarm (BRFAL). The −48F and −48S inputs are monitored by the loss −48-volt detector, which also initiates the red alarm if any of these voltages fail. The receive, negated

bit 2 (RNB2) input is digit (or bit) two of the PCM word, which indicates the yellow alarm when fixed at logic one.

The ACU outputs include TU, TP, trunk processing delayed, and trunk processing wink outputs control relays in the TPU. Transmit outgoing alarm (TOGA) is an output to the TU to control the transmission of the yellow alarm in the PCM output. RNIFI is logic output that controls signaling storage. DIS is a logic output that controls the sampling gates in the channel units. LOOP is a relay drive output signal to operate the looping relay in the line interface unit. Output ALM controls the bank alarm relay.

The purpose of each of the main functional components of the ACU circuit is described in the following paragraphs.

6.3.1 Red integrating alarm timer

The red integrating alarm timer performs the following functions:

(*i*) It provides a nominal 2.5-second delay between receipt of a red alarm signal and initiation of trunk processing.

(*ii*) It integrates intermittent red alarm inputs with a nominal 6 to 1 ratio (i.e., it times out towards the alarm state at a rate six times faster than it recovers toward nonalarm state).

(*iii*) When trunks are processed, it provides a nominal 15-second delay after the last alarm before the service is restored.

(*iv*) It provides a means to force trunk processing without an alarm by shorting a special jack (FTP).

6.3.2 Yellow alarm detector

The yellow alarm detector performs the following functions:

(*i*) It provides a nominal 450-ms delay between receipt of the last PCM bit two pulse (RNB2) and initiation of the yellow alarm and trunk processing.

(*ii*) It provides immunity to noisy lines by integrating the RNB2 pulses.

(*iii*) It provides a nominal 30-ms delay before clearing a yellow alarm to reduce sensitivity to a noisy line.

6.3.3 TP memory flip-flop

The TP memory flip-flop (FF) optionally allows the occurrence of a single trunk processing event to be held indefinitely, as indicated by the TP LED remaining ON after the trunks have been processed and returned to service. The TP LED is placed in this mode by setting the OFF/MEM switch to the memory mode position MEM. This is useful to bring attention to banks that experience intermittent failures. With

the switch in the OFF position, the TP LED is only ON during the time the trunks are out of service and turns OFF when service is restored.

6.3.4 CGA register

The CGA register is an electromechanical register that records the number of times the bank trunks are taken out of service. Each time trunk processing occurs, the register is incremented.

6.3.5 Trunk processing timing circuits

When trunk processing is initiated by a red or yellow power alarm or by forcing the FTP input, a simple sequence of relay drive signals is initiated to operate the relays located in the TPU. The trunk processing timing circuit provides the required sequence of relay drive signals.

6.3.6 ACO flip-flop

The ACO pushbutton switch turns off bank and office alarms when depressed following a red or yellow alarm. The ACO FF holds the alarm OFF. It also serves to enable the LL/LT switch after an alarm has occurred and been cut off. The LL/LT switch is disabled if alarm and ACO have not occurred. This prevents inadvertent looping of the banks while they are in service.

6.3.7 ACU logic

The logic gates interconnecting the functional ACU blocks provide the required digital logic to control the various output signals and status and alarm LEDs. The logic gates are included in two integrated gate array devices.

6.4 Summary of ACU timing

Table VII summarizes the timing functions for the ACU.

Table VII—ACU timing

Red Alarm (AR)	
Initiation	2.5 ± 0.5 seconds*
Integration Ratio	6/1 ± 20%
Time to return trunk to service after alarm clears	15 ± 4 seconds
Yellow Alarm (AY)	
Initiation	450 ± 100 milliseconds
Time to return trunks to service after alarm clears	30 ± 6 milliseconds

* The AR LED is ON whenever an alarm signal occurs, but alarm status and trunk processing is not initiated until this time has elapsed. For intermittent alarms, the initiation time is longer because of the alarm integration.

VII. DC POWER

Power is supplied to the D4 bank circuits by means of an efficient, low cost, dc-to-dc power converter unit (PCU) that operates from the office −48 volt supply. The output voltages for the D4 circuits are +5 and ±12 volts. The power unit consists of an input filter, switching power amplifier, power transformer, output rectifiers filters, and control circuits.

The PCU voltage outputs have ripple voltages of less than 30 mv rms over a 0- to 20-MHz frequency band. Tolerance on the output voltages is ±5 percent for the ±12 volt outputs and ±10 percent for the +5 volt output. The converter has over-voltage protection and low-voltage alarm indication.

The power unit provides an input switch with a mechanical interlock that automatically turns the power off when the unit is being removed from the D4 bank. The faceplate has alarm and alarm cutoff LED indicators and test points for measurement access to the ±12 and +5 output voltages.

A power distribution unit (PDU) furnishes a fused −48-volt distribution arrangement for the bank PCU and other circuits. Office alarms and a local PDU alarm are activated by any fuse or bank failure. The PDU also has a filtered talk battery and 20-Hz ringing supply outputs.

VIII. SUMMARY

The D4 channel bank is a versatile, cost-effective addition to the digital telephone plant. Circuits designed for D4 have been incorporated into many other parts of the digital plant. The most prominent additional applications of the D4 circuits (and some of the D4 hardware) include the *SLC*-96 subscriber loop terminals, and the LT-1 connector.

Many of the D4 LSI integrated circuits have been incorporated into other parts of the digital network, such as the digital interface frame (DIF) for No. 4 ESS, and maintenance systems, such as the digital access and cross-connect system DACS and DATS.

The success of the D4 bank and D4 technology is the result of close and extensive cooperation among many Bell Laboratories organizations.

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GLOSSARY

ACO	alarm cutoff
ACU	alarm control unit
ALM	alarm
ALM DET	alarm detector
APD	avalanche photo diode
AR	red alarm
ARFAL	A digroup receive frame alarm
ARNPCM	A digroup inverted PCM
ARCLK	A digroup receive clock
ATCLK	A digroup transmit clock
ATPCM	A digroup transmit PCM
AY	yellow alarm
B6ZS	binary six zero substitution
BRCLK	B digroup receive clock
BRFAL	B digroup receive frame alarm
BRNPCM	B digroup receive PCM
BTCLK	B digroup transmit clock
BTPCM	B digroup transmit PCM
CBIC	complementary bipolar integrated circuit
CCIS	common-channel interoffice signaling
CGA	carrier group alarm
CH	channel
CMOS	complementary metal oxide semiconductor
CODEC	coder-decoder
CU	channel unit
DAC	digital-to-analog converter
DACS	digital access and cross-connect system
dBTL	decibels-transmission level
dBrnCO	dB above reference noise, measured with C-message weighing at 0 transmission level point
DCH	destuffed channel (PCM)
DCLK	destuffed clock
DDS	digital data system
DEMUX	demultiplexer
DIF	digital interface frame
DIFF COMP	differential comparator
DIP	dual in-line package
EQL	equalizer
ESS	electronic switching system
EXT	external
FET	field effect transistor
FF	flip-flop

FS	signaling, frame signal pattern
FT	terminal frame signal pattern
JFET	junction field-effect transistor
LBO	line build-out network
LCIE	lightguide cable interconnection equipment
LCKLT	line interface unit clock loop time
LCKPH	line interface unit clock phase control
LCLK	loop clock
LED	light-emitting diode
LIU	line interface unit
LL	line loop
LOSP	loss of pulse code modulation
LPCM	loop pulse code modulation
LSB	least significant bit
LT	loop terminal
MCK	multiplexer clock
MEM	memory
MUX	multiplexer
OOF	out-of-frame
OPT RCVR	optical receiver
OPT TRMTR	optical transmitter
PAM	pulse amplitude modulation
PCM	pulse code modulation
PCU	power converter unit
PDU	power distribution unit
PLL	phase-locked loop
RC	resistor-capacitor
RCLK	read clock
RCLK	receive clock
RFA	receive frame signal for A digroup
RFB	receive frame signal for B digroup
RNB2	receive, negated bit 2
RNIFI	logic output that controls signaling storage
RNPCM	receive, negated pulse code modulation
RPAM	receive pulse amplitude modulation
RPCM	receive pulse code modulation
RU	receive unit
S/D	signal-to-distortion
SBC	standard buried collector
SIC	silicon integrated circuit
SMAS	switched maintenance access system
SR	stuff request
SU	synchronizing-desynchronizing unit
SUM	summing

syndes	synchronizing-desynchronizing
T6CK	transmit 6 megahertz clock
TCLK	transmit clock
TINH	transmit inhibit
TNEN	transmit, negated enable
TOGA	transmit outgoing alarm
TP	trunk processing
TPAM	transmit pulse amplitude modulation
TPCM	transmit pulse code modulation
TPD	trunk processing delayed
TPM	trunk processed memory
TPU	trunk processing unit
TPW	trunk processing wink
TSYNC	transmit synchronization
TTL	transistor-transitor logic
TU	transmit unit
VCO	voltage-controlled oscillator
VCXO	voltage-controlled crystal oscillator
VF	voice frequency
XO	crystal oscillator