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D4 Digital Channel Bank Family:

Dataport—Channel Units for Digital Data System Subrates

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The single-channel dataports are a series of D4 channel units that convert the digital signal derived from one T-facility time slot by the D4 common circuits to an appropriate format at speeds of 64, 9.6, 4.8, or 2.4 kb/s for use in the Digital Data System (DDS). They come in two formats, the first being the DDS bipolar format for 64 kb/s and the second, for the remaining three speeds, being an EIA RS-449 format. Their error-correction feature ensures 10^{-8} error-rate performance for a 10^{-3} error-rate transmission channel. Advances in large-scale integration (LSI) technology have allowed the packaging of all the digital circuit functions needed into the space of a single channel unit. An on-board power converter unit generates the additional current required by the dataports over that needed by regular analog channel units. The local loop side of each channel unit uses integrated technology to achieve signal equalization and timing recovery. Standard DDS remote maintenance features are provided. The dataport channel units are easily installed and removed; they supply economical digital transmission.

I. INTRODUCTION

The D4 channel bank can be equipped with over forty different channel units, each one designed as a customized transmission and signaling interface between the T-carrier transmission facility and the central office switch or local wire loop. These channel units are used for diverse applications, such as regular telephone grade voice band and radio program wide band, dial-pulse signaling and nonsignaling transmission only, switched service and private line, and analog and

digital loop service. Dataports are the series of D4 channel units that allow a direct digital interface into the T-facility from the customer loop, bypassing the regular analog-to-digital conversion of voice channel units.

As Ref. 1 describes, some dataports connect to the customer's location, while others link inside a telephone office. For each of the above two applications, two kinds of dataports exist, those that serve a customer using one T-facility time slot and those that use two time slots. This article describes the hardware implementation of the class of dataports that serves a customer at a data rate of 2.4, 4.8, or 9.6 kb/s, the so-called "subrate" dataports. A companion article details the designs for the class of dataports that serves a customer at 56 kb/s.[2] The basic D4 bank functions are described in Ref. 3, while the system issues of dataport are fully treated in Ref. 1.

This article briefly reviews the various applications and system issues of dataports. The basic hub office unit, the digital signal zero (DS0) dataport, is then described, as well as the basic end office dataport, known as the Office Channel Unit (OCU) dataport. The last variety of dataport discussed is the Data Service Unit (DSU) dataport. Finally, the subrate error-correction algorithm and the on-board power converter are detailed. Field evaluations show that dataports are reliable, quick to install and remove, and are easy to maintain. Dataport has allowed the Digital Data System (DDS) to expand at low cost to serve the increasing needs of the *Dataphone** Digital Service.

II. GENERAL FUNCTIONS

2.1 Dataport applications

Figure 1 shows the typical dataport configurations.[1,4] The DDS network offers data transmission service to every major metropolitan area in the United States.[5,6] If a customer network requires a termination in a serving area not now covered by regular DDS equipment, a dataport extension can be made. An existing DDS hub office serves as a focal point for gathering various DDS signals and multiplexing them together for transmission across the country. The hub office sends one customer signal in a format of 64 kb/s, the DS0A format, to a DS0 dataport. The DS0 dataport inserts, through the D4 bank interface, the 64 kb/s signal onto the T-facility channel time slot. The T-facility carries the signal to a D4 bank at the local end office that serves the customer location. Each local office has an OCU dataport, which receives the single time slots, corrects errors in the receiver data, and sends out data to the customer at the baseband rate over the local distribution

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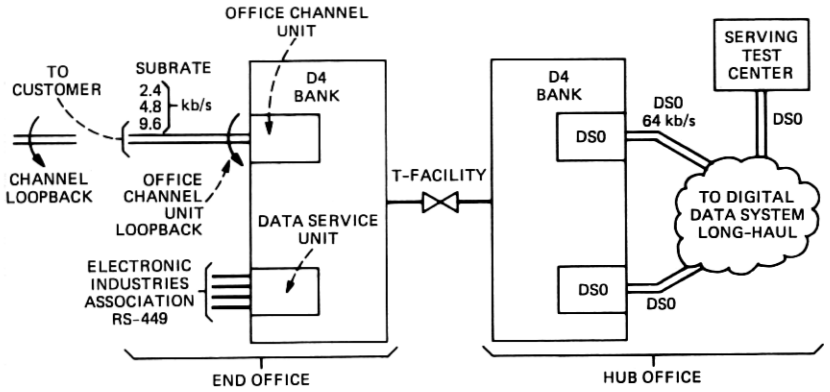

Fig. 1—Dataport applications.

cable. At the customer premises, the local cable pairs terminate either on a DSU or Channel Service Unit (CSU).[7] This DS0, T-facility, and OCU link allows DDS to grow from an existing hub office out to a new serving central office of the *Dataphone* Digital Service. The dataport is designed to handle small numbers of DDS channels economically. Combining voice and data services in the same digital bank lowers capital costs and efficiently uses the T-carrier plant. Offices with many customers could still be served by the separate, dedicated DDS equipments.[8]

For special applications, the DSU dataport has a DDS-type link between two telephone central offices for internal use.[9] In effect, the miles of cable pairs that connect the OCU with the customer-located equipment are shrunk to a few millimeters of printed wiring board path. The DSU dataport has a direct Electronic Industries Association (EIA) connection and does not need a separately mounted DSU. If the two end offices of the point-to-point link are directly connected by one T-system, then a DSU dataport may be used in each terminating D4 channel bank and no OCU dataports are required. The 10A Remote Switching System uses the DSU dataport in precisely this fashion.[10]

2.2 D4 channel bank and channel multiplexing

The D4 channel bank using a digital signal one (DS1) facility has twenty-four time slots of 64 kb/s each. All subrate dataport channel units occupy one physical mounting position in the D4 bank and use one time slot, just as regular analog channel units do. This allows dataports to be installed in any of the channel-unit positions of the D4 bank. One common D4 circuit pack, the Office Interface Unit (OIU), and a connection at the hub office to the DDS network timing system are required to convert a standard D4 bank to a dataport-capable

bank.[1] This simple procedure allows the D4 bank to mix conventional analog and dataport DDS services.

The single customer DS0A signal is handled in the network in bytes of eight bits. Each byte contains a leading multiplexing bit, which for subrate DS0A signals is always a logic zero, six customer data bits, and a control mode bit. In each 8-bit byte only six bits carry data, thus the effective data speed is 6/8ths of 64, or 48 kb/s. The basic subrate DS0 signal contains repeated information. The highest speed signal has five repeated bytes; therefore, the true customer information rate is one-fifth of 48 kb/s, or 9.6 kb/s. The DS0A signals for 4.8 and 2.4 kb/s service similarly have repeated bytes of ten and twenty times. It is the repeated byte pattern that allows dataport to carry out error correction of the local T-facility transmission plant. An additional format exists that allows standard DDS equipment to multiplex subrate data signals for efficient transmission in the national long-haul network.

2.3 Maintenance plan

The maintenance strategy for testing DDS is described in Refs. 11 and 12. The individual customer channels of a dataport circuit are analyzed for trouble conditions in the same manner as a conventional DDS channel. When a trouble is reported by the customer to the DDS Serving Test Center (STC), the customer channel is first monitored in both directions on an in-service basis. The STC checks the data signals for the occurrence of specific repeated control signals, which would automatically replace the customer data in cases of equipment failures. If no indication of a network failure is detected by this monitoring, then the local cable pair is removed from service and checked by loopback tests. There are three dataport loopbacks from the DS0 channel and hub office. The STC can cause a loopback to occur at the output of the OCU dataport, at the end of the loop plant in the customer premises DSU or CSU, and at the output of the DSU. The "OCU loopback" tests out all the network from the STC to the OCU output circuits that drive the local cable pairs. The loopback at the input of the customer-located equipment, called the "channel loopback," tests the local distribution cable from the end office to the customer site. The final "DSU loopback" guarantees the integrity of the data service unit located on the customer premises. Thus, the loopbacks are used to isolate the trouble to the internal telephone company network, the outside cable plant, or the customer-located equipment. To obtain an error-rate performance measure, the STC starts a loopback by sending out a fixed-control-code byte to lock the distant circuit into the loopback state. Next, an alternating pattern of the fixed-control-code byte and a pseudo-random message sequence is sent to the distant circuit. At the loopback point the fixed-control code maintains the

loopback state of the equipment while the message sequence is reflected back to the STC. The received pseudo-random sequence is examined at the STC, and the error-rate performance of the circuit is measured.

If the OCU loopback test fails, then the problem lies in the internal DDS network. To isolate the problem further, a local craftsperson can manually activate dataport loopbacks. Each OCU and DS0 dataport channel unit has a jack access that alllows a looping plug to be inserted, which causes the DDS signal to be looped back for comparison at the STC. In addition, the looping plug also supplies a jack access for use with portable test equipment.

The DSU dataport has all the normal DDS remotely controlled loopback features. In addition, the customer-controlled loopbacks specified in the EIA RS-449 document are included. Maintenance of the DSU dataport is described in Section 5.3.

III. DS0 DATAPORT HARDWARE

The DS0 dataport converts DDS bytes in bursts of eight bits at a DS1, 1.544-Mb/s rate to and from a continuous DS0, 64-kb/s rate. The unit operation is frequency synchronous but allows arbitrary phase difference between the DS1 and the DS0 signals. In this article, relative to the local D4 channel bank, the transmit direction defines signals toward the T-carrier facility and the receive direction defines signals toward the customer.

3.1 Transmit and receive circuitry

A simplified block diagram of the DS0 dataport is shown in Fig. 2. In the receive direction, the 1.544-Mb/s pulse code modulation (PCM) stream is available to the channel unit from the receive PCM bus.[1] The rate converter picks off the 8-bit DDS byte from the PCM stream and in normal operation outputs the same eight bits at the 64-kb/s rate. Since there are 24 8-bit bytes on each frame of the DS1 stream, receive select information from the D4 common circuitry is required to select the proper byte. In Fig. 2, the output of the rate converter is sent to the code insertion function (Section 3.2), and that output is then connected to the input of a 3-out-of-5 error-correction circuit. For subrate data, this circuit allows DDS error-rate objectives to be met without special testing and selection of T-line facilities. A discussion of the operation of this circuit is given in Section VI. The output of the error-correction circuit feeds a buffer that converts the logic signal into a bipolar nonreturn-to-zero (NRZ) signal.

In the transmit direction a similar but reverse process takes place. This path contains no error correction, and the transmit PCM backplane

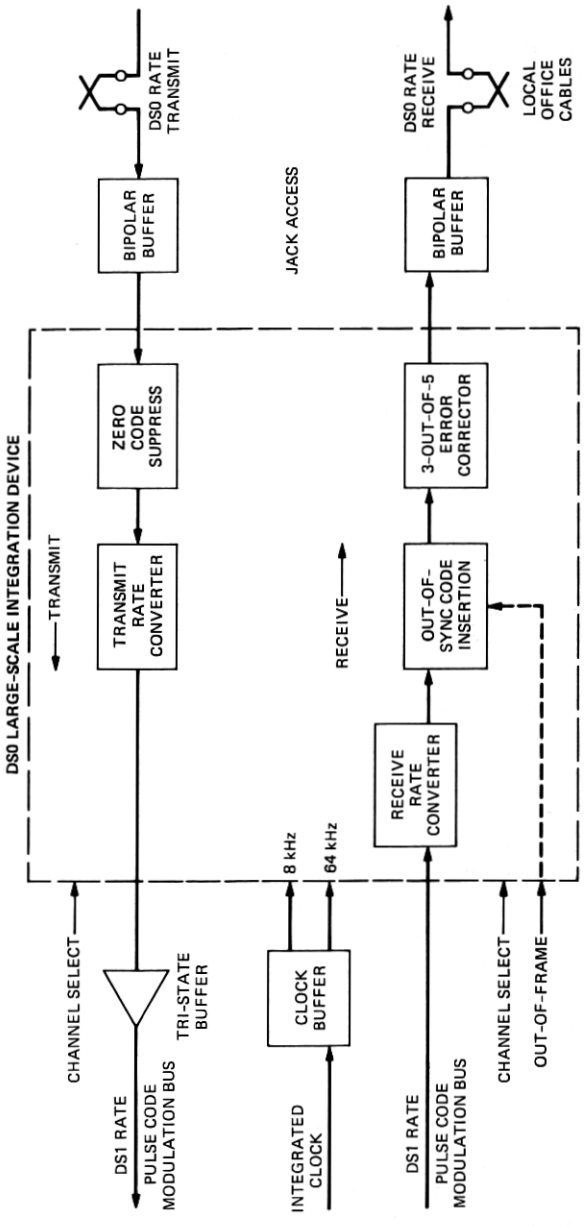

Fig. 2—DS0 dataport channel unit.

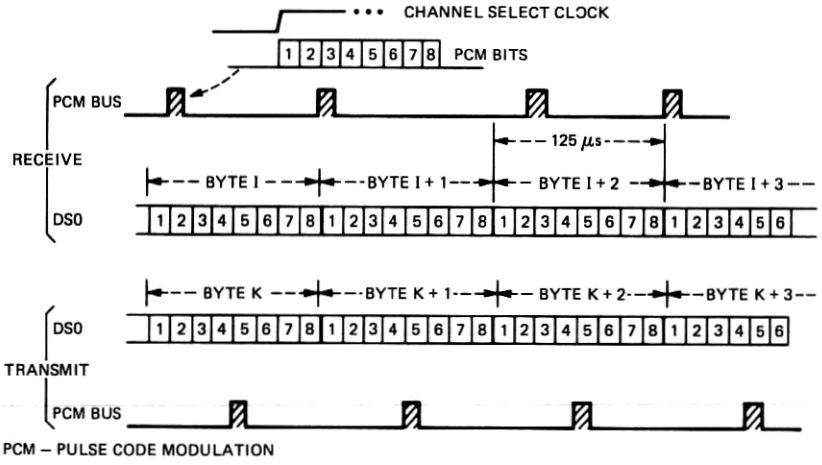

Fig. 3—DS0 input/output signals.

bus that connects all 24 channel units is driven by a tri-state buffer (logic zero, one, or open circuit outputs).

The input and output signals described above are shown in Fig. 3. Only the appropriate dataport PCM bus signals are shown. The DS0 receive and transmit signals are in byte and bit synchronization with the DDS clock. Also, while the receive and transmit D4 bus signals are frequency-synchronized, they are not phase-synchronized with each other or with the DS0 signals.

Circuitry within the dotted lines in Fig. 2 is contained in an N-channel metal-oxide semiconductor (NMOS) LSI chip in a 40-pin dual in-line package (DIP). Since this chip forms almost the entire circuit of the DS0 dataport channel unit, it has been appropriately named the DS0 chip. Further information on the realization of the chip can be found in a companion article.[13]

The integrated clock timing is shown in relation to the D4 bank composite clock and to the 8- and 64-kHz clocks used by the DS0 chip in Fig. 4. The clock buffer circuit shown in Fig. 2 provides level-detector circuitry needed to separate the 64-kHz bit clock and 8-kHz byte clock. It also has a high-input impedance to prevent loading down the clock bus.

3.2 DS0 control code substitution

As we saw in Fig. 2, whenever the near-end or far-end D4 bank is not framed[3] (the near-end bank in red or yellow carrier group alarm), an out-of-frame signal is presented to the DS0 chip. In this mode the receive rate converter outputs, irrespective of the input signal, a special DDS "multiplex out of synchronization" byte code. This informs local customer equipment of a transmission equipment malfunction.

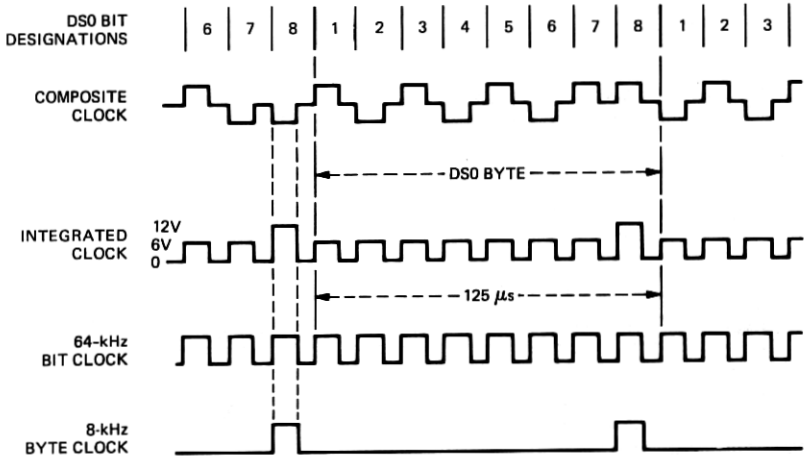

Fig. 4—DDS clock signals.

Similarly, when the transmit rate converter receives an unallowed byte code of all zeros in bits two through eight, the output byte is modified automatically to force bits three and four to logic ones. The receipt of such an unallowed code suggests that a malfunction in the equipment on the customer side of the DS0 dataport has occurred. For example, this code would result if the wire pair carrying the DS0 signal to the dataport were cut.

3.3 Phase synchronization circuit

Figure 5 is a block diagram of the transmit rate converter, which shows three 8-bit byte shift registers. Each register is loaded at 64 kb/s and unloaded at 1.544 Mb/s. Three shift registers are required to synchronize the DS0 byte to the DS1 rate, allowing arbitrary phase difference between input and output. This phase shift can be caused by channel unit placement within the 24 time slots of the bank and by T-facility phase jitter.

The normal operation of the three registers is depicted in Fig. 6. Register A loads byte K at 64 kb/s and then unloads it at the start of bit 5 of byte K+1 at 1.544 Mb/s; it loads and unloads every third byte in the same manner. The loading/unloading sequence is load A, unload C, load B, unload A, load C, unload B, load A, unload C, etc.

If there is a phase shift of the 1.544-MHz transmit clock, a sequence correction may be required to prevent data destruction. The phasing algorithm checks to see if a register is being concurrently loaded and unloaded, and if so, then the same information in the register is unloaded twice. This process will always break the overlap; an example is shown in Fig. 7. The unloading pulse advances a total of three-quarters of a bit (at the 64-kb/s rate). The first overlap occurs in

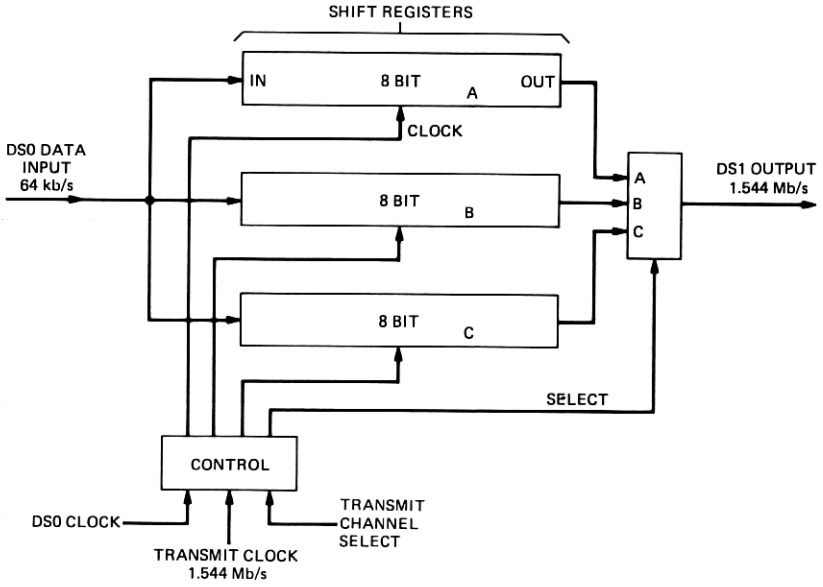

Fig. 5—Transmit rate converter.

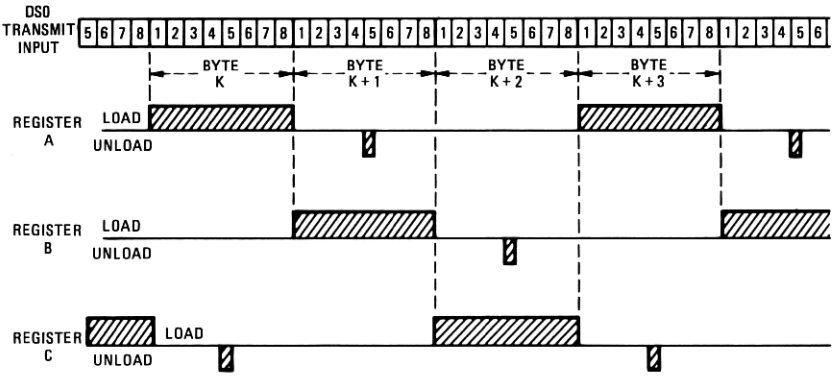

Fig. 6—Transmit rate converter load/unload sequence.

register B, so register B is unloaded twice. An overlap will not take place again as long as the input and output phase difference stays within plus or minus eight bits at the 64-kb/s rate. The receive rate converter is equivalent to the transmit rate converter except for the interchange of input and output bit rates.

3.4 DS0 dataport maintenance

Figure 2 shows two jacks on the office wiring side of the channel unit that can be used for maintenance of the DS0 dataport. By

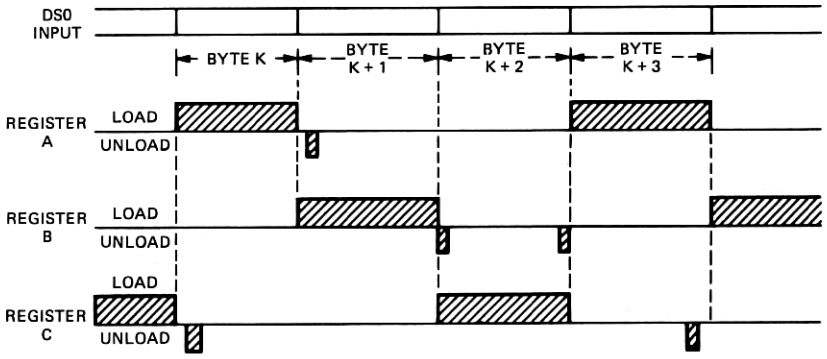

Fig. 7—Transmit rate converter overlap correction.

manually inserting a special plug into the faceplate of the dataport channel unit (accessible from the front of the bank), a loopback is made that connects the bipolar DS0 receive signal back to the DS0 transmit input. This ability makes it easier to locate faulty equipment. The maintenance plug and the DS0 dataport, as well as the OCU and DSU dataports, are shown in Fig. 8. The two jack connectors on the plug can be used to access the channel, in either direction, with portable DDS signal-generation test equipment.

IV. OCU DATAPORT HARDWARE

The OCU dataport contains all the digital circuitry of a DS0 dataport, and it includes the additional circuits to convert the DS0 signal to and from the local loop format used for communication with the customer premises. Figure 9 is a block digram of the office channel unit section of the OCU dataport. The major functions include a synchronous-timing-generation circuit, a rate-matching section, control-code recognition, analog signal conditioning, and a local cable interface.

4.1 OCU signal formats

The DS0 signal, as described in Section 2.2, has a 64-kb/s, byte-oriented format. The signal to the customer over the local cable pairs is at the customer data-bit rate, with a logic one represented by a bipolar pulse and a logic zero represented by no pulse. The six data bits of the 8-bit byte at the DS0 level are sent to the customer in a bit-by-bit, non-aligned fashion. For example, at the 4.8-kb/s service rate, the customer will get the six data bits that are repeated ten times in the DS0 byte at the 64-kb/s rate. This yields six new data bits every ten times 125 μs, or 4800 b/s.

The receive DS0 signal may be pre-empted by the STC during maintenance operations. The control-mode bit is set to a logic zero,

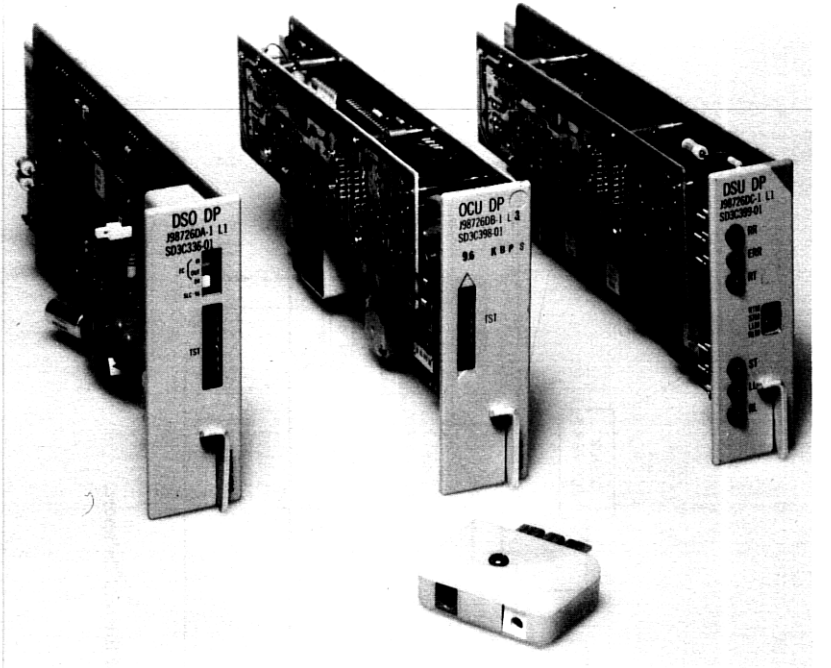

Fig. 8—DS0, OCU, and DSU dataports.

and the six normally allocated customer bits are now used to define a maintenance code, which can be used to start loopbacks or to signify transmission difficulties. Monitoring circuits in the OCU section are designed to recognize the codes for maintenance testing.

No clock signals are separately sent to the customer site; the customer-located DSU must recover the clock frequency from the received OCU data signal. This requires that enough energy always be sent to the CSU or DSU in the signal, which in turn forbids transmission of long strings of zeros (no bipolar pulses) in the customer data. To maintain bit transparency, a zero-code substitution is employed by the OCU, where any DS0 byte containing six data bits as all zeros is replaced on the local cable pair by a bipolar violation sequence. In addition, several control codes are also transmitted to the customer site as coded bipolar violations. Reference 7 describes the code translation from the byte format to the bipolar violation format.

4.2 Digital hardware realization

The digital circuitry for the office channel unit portion of the OCU dataport is contained in the previously mentioned DS0 device and in two smaller LSI devices. These "rate-matching" devices convert the

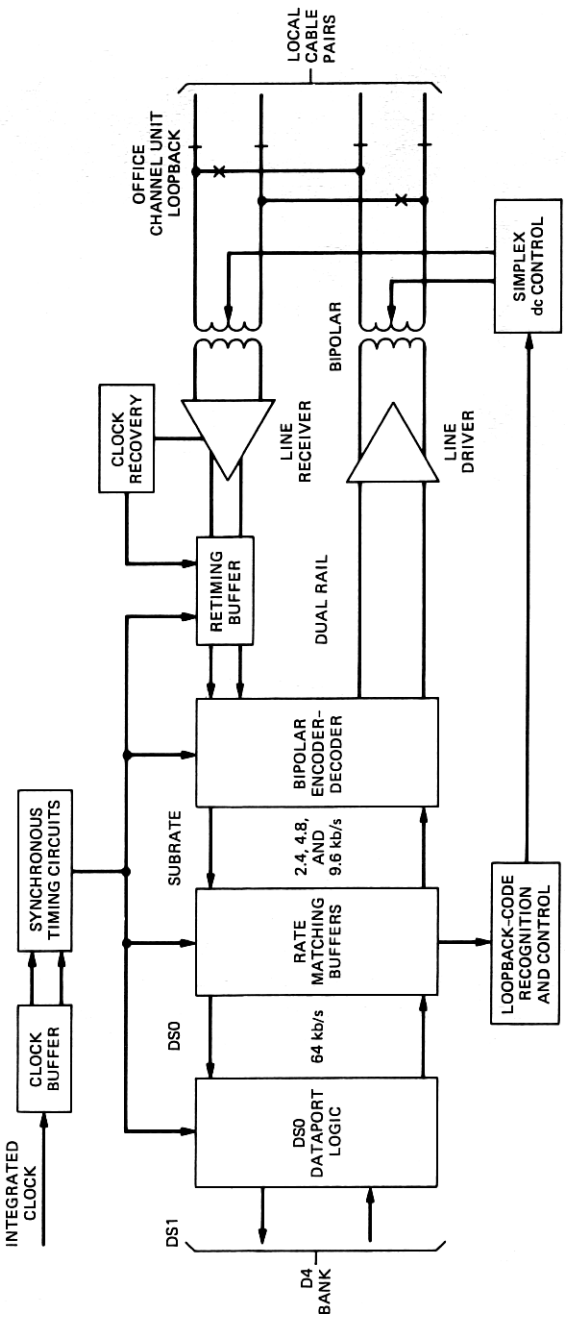

Fig. 9—Block diagram of the OCU dataport.

signal at the DS0 rate to the customer rate, monitor for the presence of control codes, and convert bipolar violations to control codes. The DS0 device has the additional OCU function of providing a high-speed clock and strobe signal to the rate-matching devices. The rate-matching devices use the high-speed clock at 1344 kHz, the least common multiple of 64, 56, and 9.6 kHz, to generate customer bit rates. The OCU loopback command, which causes a relay to connect the output of the OCU back to the input at the local cable pairs interface, is detected in the rate-matching devices.

There are two logic-level outputs from the bipolar encoding logic that together form a dual-rail signal that creates a bipolar loop-line signal. In this scheme, one logic rail supplies the bits for the positive voltage signal, and the other rail supplies the bits for the negative voltage signal. On the loop line during normal data transmission, a logic 1 is transmitted as either a positive or negative pulse with successive pulses alternating in polarity; a logic zero is transmitted as no pulse. Control-code information is transmitted between the OCU dataport and customer premises unit by bipolar violation sequences, i.e., successive bipolar pulses with the same polarity.[7]

4.3 Analog line circuits

In the direction from the T-facility toward the local cable pair, the analog line-drive circuitry transforms the logic signals into bipolar pulses suitable for transmission on the cable pairs to the customer. It contains a level shifter, band elimination filter, line-drive amplifier, transformer, lighting protection circuitry, and two low-pass filters.

A Butterworth filter, with a pole at 1.3 times the signaling rate, limits the high-frequency signal energy on the line. Also, a 28-kHz band elimination filter is implemented to eliminate 28-kHz energy from interfering with other services that may be in the same loop cable.

The line-driver circuitry buffers the filters from the varying impedances of the transmission line. It also converts the dual-rail signal, by means of a transformer, to the bipolar signal for transmission over the cable pair.

In the direction towards the T-facility from the local cable pair, the loop signal passes through the line-receiver circuitry that consists of lighting protection, line transformer, input buffer amplifier, low-pass filter, and line equalizer. It also contains a second-order filter that, when combined with the first filter, forms a third-order Butterworth low-pass filter with a cutoff frequency equal to 1.3 times the signaling rate. The filters in this circuitry are used to increase noise immunity and provide pulse shaping for the following OCU logic circuits.

The local loop plant consist of 19-, 22-, 24-, and 26-gauge metallic

pairs; the insertion loss of these cables is a function of both frequency and length. To compensate for the variously shaped loop losses an adaptive equalizer is required in the line receiver that terminates the cable pair from the customer. The equalizer has variable gain and a movable real zero, both controlled by a single variable resistor, to compensate for the varying loop characteristic. The equalizer output signal drives a slicer circuit, the outputs of which form a dual-rail digital signal that serves as the input to the conversion logic.

The analog portion of the OCU dataport was developed using existing and ongoing designs. The real effort was to realize those designs with much lower power drain and in a much reduced area. To this end, Standard Tantalum Active Resonator (STAR) DIPs[14] were used in the design of the low-pass filters. The gain-zero equalizer was implemented by using the STAR-DIP along with a multiple operational amplifier DIP.

The level shifter and line-driver circuitry are contained in a 12-pin Transmission Equipment DIP (TED).[15] A second 24-pin TED is used for the active circuitry in the transmit side and contains the line terminator, equalizer, and slicers.

V. DSU DATAPORT HARDWARE

The DSU dataport contains all the digital circuitry of the OCU dataport, and it includes the additional circuits to convert the OCU dual-rail local-loop format signal to an EIA-compatible multi-pin interface signal. Figure 10 is a block diagram that shows how the functions of the data service unit are added to the basic OCU dataport. The major functions include a timing synchronization circuit, a control-code-to-

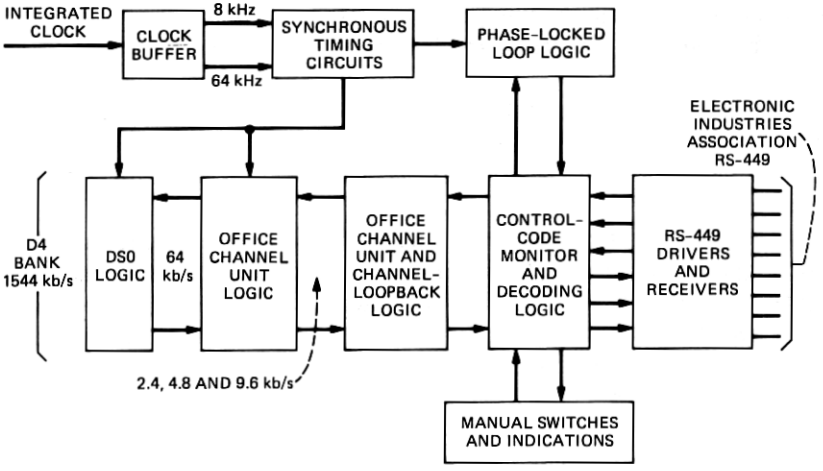

Fig. 10—Block diagram of the DSU dataport.

control-signal section, an EIA RS-449 interface,[16] and maintenance controls and indications.

5.1 Hardware realization

The digital outputs of the OCU section are fed into an LSI device and not into the normal analog OCU circuits. In this application, the normal cable loop pairs to the Data Service Unit do not exist; the customer-located DSU is incorporated directly into the D4 bank channel unit. The equalizers, relays, and analog filters are not needed. The workhorse DS0 LSI device is again used to provide functions needed for the DSU dataport application. The timing synchronization is obtained directly from the clock feeding the OCU section, and it is not recovered from the OCU data stream as would normally be done by a remote DSU. While the frequency is easily obtained, strobe signals used in the DSU LSI device require phase alignment with the data produced by the OCU devices. A phase-locked circuit slips the clock feeding the DSU section until the DSU strobe signal is aligned properly with the OCU data. At this point, the circuits are synchronized and will remain synchronized until power interruption or unit removal. The digital alignment circuit eliminates the need of the regular DSU clock-recovery circuit and crystal oscillator.

The DSU logic monitors the incoming data from the OCU section for control codes, indicated by bipolar violations, which here must be decoded from the dual-rail logic signals. These control signals and other status signals are decoded as individual logic-level leads. These signals, indicating loopbacks, idle conditions, and line errors, are used as maintenance aids and are also presented to the user interface.

5.2 User data interface

The signals to the user from the DSU dataport are in accordance with the EIA RS-449 standard.[16] The D4 bank has provision for only ten leads to be brought out from each channel-unit position, so the full 37-pin format of RS-449 could not be accommodated. Since the dataport is used as a point-to-point, private-line, nondial-up connection, many of the "mandatory" EIA signals are provided with the use of the EIA-termed "dummy" signal generators by simply tying a lead to a dc source voltage through a resistor. The active signals used are transmit clock and data, receive clock and data, signal quality (generated by the D4 bank's out-of-frame detector), local and remote loop commands, and the needed RS-423 common-signal reference leads.

5.3 Maintenance capabilities

Maintenance features, suggested in RS-449, have been implemented in the DSU dataport in addition to all the normal DDS features. The

OCU and channel loopbacks, described above, are provided in the DSU dataport even though there is no real local cable pair connecting an OCU and DSU. The loopbacks are carried out in logic in the center of the DSU dataport function, so that from any remote DDS test facility, the DSU dataport responds in the identical way that a standard OCU and customer-located DSU would respond. The DSU dataport has many additional on-board maintenance features. Internal looping and error-detection circuits rapidly detect faults. The user can initiate, through the electrical RS-449 interface, the "Local" and "Remote" loopbacks of RS-449. This allows automatic fault isolation under user control, without the need of intervention by the regular DDS maintenance craft. An array of light-emitting diodes and toggle switches allows local manual-fault detection and isolation.

VI. ERROR CORRECTION

T-carrier facilities were initially designed for voice quality transmission; as such, the T1 and T1C lines are engineered so that 95 percent of the systems have a probability of line error, p, being $\leq 10^{-6}$. Studies by Brilliant[17] show that a significant number of T-facilities might not, therefore, meet the DDS specification on error-free seconds.[18,19] The DDS solves this problem by selecting only those lines that pass an acceptance test.

If dataport were to require T-facility line selection, the goal of quickly installing a channel unit to meet new customer data needs would be severely impaired; thus, error correction was incorporated as a standard feature for dataport.

To ensure proper service quality, the common equipment of the D4 bank declares the facility out of service and issues a "carrier group alarm" when the short-term error rate is worse than 10^{-3}. Hence, $p = 10^{-3}$ was chosen as the worst-case operating error rate. An error-correction strategy was required to decrease the error rate from 10^{-3} to 10^{-8} or lower, assuming a binary symmetric channel model.

6.1 Encoding and decoding

As we saw earlier, in the transmit direction a 9.6-kb/s OCU dataport takes six customer data bits, and adds both a leading zero and the network control bit to form an 8-bit byte. Next, the OCU repeats the byte five times to build up the data rate to 64 kb/s. For 2.4 and 4.8 kb/s, the 8-bit bytes are repeated 20 and 10 times, respectively. Since a repeat of 10 can be regarded simply as two repeats of five and a repeat of 20 as four repeats of five, the OCU can be regarded as a repeat-of-five encoder.

At the receiver, the five repeated bytes are decoded into the correct message byte one bit at a time. If no errors have occurred, each of the

received five repeats of each bit in the byte will be the same. When they are not received correctly, it can be shown[20] that taking a majority vote on the five bits is the maximum likelihood method of making the correct decision. This majority vote scheme is implemented in the subrate dataports and is performed on each of the bit positions in the received byte. While more efficient coding schemes can be devised, this method is a natural outgrowth of the DDS subrate nonmultiplexed signal format. For multiplexed OCU channels on one time slot, the methods described in Ref. 2 may be used.

Since the rule for recovering each information bit is to take a majority vote of the five received bits, a decoding error is made only if three or more line errors are made. Hence, the probability of bit error after decoding is given by:

$$P_r = \sum_{i=3}^{5} \binom{5}{i} p^i (1-p)^{5-i}, \tag{1}$$

where p is the bit-error probability of the channel and satisfies $p \leq 10^{-3}$, as explained earlier.

Equation 1 is approximately equal to:

$$P_r \approx 10\,p^3 \text{ for } p \ll 1 \tag{2}$$

$$\leq 10^{-8} \text{ for } p \leq 10^{-3}. \tag{3}$$

Thus, for a line error rate of 10^{-3}, the dataport error rate is reduced to less than 10^{-8}.

6.2 Word synchronization

At the receiver, no clock signal is available to mark the start of the five repeated bytes. A word marker must be formed from the statistics of the data. As we see in Fig. 11, the word marker is synchronized when the six data bits of the first byte and the six of the fifth byte are the same. When not synchronized, the first and fifth bytes represent different data bytes from the customer and should be different with high probability. The synchronization algorithm loads in five bytes T_1 times and compares the six data bits of the first byte with the six data bits of the fifth byte. If the number of times the first and fifth byte patterns are different exceeds a threshold T_2, then a mis-synchronization is declared, and a byte slip of the word marker is made as corrective action. A slip in the same direction will be introduced every T_1 trials until synchronization is achieved.

6.3 Probability of false mis-synchronization

Mis-synchronization is declared whenever more than T_2 cases of mismatch occur between the first and fifth byte in T_1 trials. Since the probability p_1 that a bit of the first and fifth byte is the same is the

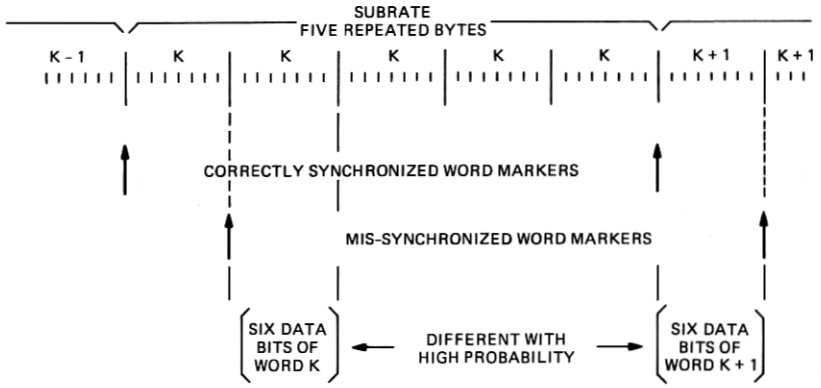

Fig. 11—Error-correction synchronization.

sum of the probabilities of no error either time and an error both times,

$$p_1 = (1-p)^2 + p^2 = 1 - 2p + 2p^2, \tag{4}$$

where p is the probability of a bit error on the T-facility. The probability, p^*, that when properly synchronized the six data bits of the first byte will not match the six data bits of the fifth byte, is given by:

$$p^* = 1 - p_1^6 \approx 12p \text{ for } p \leq 10^{-3}. \tag{5}$$

Hence, the probability, P_F, of false mis-synchronization for this Bernoulli experiment is:

$$P_F = \sum_{i=T_2}^{T_1} \binom{T_1}{i} (p^*)^i (1-p^*)^{T_1-i}. \tag{6}$$

6.4 Probability of failure to recognize mis-synchronization

A failure to recognize mis-synchronization occurs whenever in T_1 trials fewer than T_2 mismatches occur between the assumed first and fifth bytes of the repeating pattern. If we assume two 6-bit customer bytes, a similar Bernoulli experiment can be conducted. Hence, the probability, P_M, of failure to recognize mis-synchronization is given by:

$$P_M = \sum_{i=0}^{T_2-1} \binom{T_1}{i} \left(\frac{63}{64}\right)^i \left(\frac{1}{64}\right)^{T_1-i}. \tag{7}$$

For the error-correcting circuit of the subrate dataports, $T_1 = 160$, and $T_2 = 20$. This results in $P_F = 10^{-12}$ while $P_M = 10^{-195}$. Keeping the probability of failing to recognize a mis-synchronization so low with respect to falsely declaring a mis-synchronization was done to guard against customer data that was not independent. An expanded discussion of the above algorithms can be found in Ref. 21.

VII. ON-BOARD POWER CONVERTER

The dataport units have much more logic circuitry than do normal D4 channel units. The standard D4 bank power converter supplies +5V, +12V, and −12V to each channel,[3] but has a limited current drain allocation. The dataport units require hundreds of milliamperes to run the NMOS LSI devices. To avoid changing the standard bank converter, an on-board dc-to-dc converter was designed onto each dataport to supply the current. This converter uses power from the ample −48V office battery used in regular channel units to power the customer voice loop.

The dc-to-dc converter develops a reference voltage from the −48V office supply and regulates a series pass transistor. The output of the transistor is chopped and fed to a transformer, where two sets of taps are used to obtain +5V, +12V, and −12V. An output filter on each voltage supply keeps the noise down to a few tenths of a volt. The total maximum output power of the converter is over six watts.

VIII. CONCLUSION

Dataport has been designed as an easy, inexpensive way to expand the area served by the Digital Data System. It can be quickly installed into a properly conditioned D4 bank and has all the normal DDS maintenance features. The error-correction ability of the dataport removes the need to select T-carrier facilities to achieve error objectives. Dataport is lower in cost for small numbers of customers than is conventional DDS equipment, and it allows economical voice and data sharing of digital terminals, achieving efficient T-facility usage.

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