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D4 Digital Channel Bank Family:

Dataport—Channel Units for Digital Data System 56-kb/s Rate

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Increasing demand for high-speed data services makes it desirable to give more customers access to the Digital Data System (DDS). To provide service at 56 kb/s, the highest DDS rate, "dataport" channel units have been developed to extend DDS network channels over T-carrier lines, using D4 terminals. These 56-kb/s dataport units offer a flexible and economical arrangement for serving smaller cross sections of data subscribers, and make use of a coding scheme for error correction that makes special selection of lines (for error rate) unnecessary. We describe the design of 56-kb/s dataport units, while articles referenced herein discuss dataport system questions and the design of lower speed dataport units.

I. INTRODUCTION

Consider the use of existing T-carrier facilities to extend the Digital Data System (DDS) serving area. "Dataport" channel units are needed for the carrier terminals (such as D4 channel banks) to insert customer data bit streams into the carrier pulse code modulation (PCM) bits tream. Special problems must be addressed with 56-kb/s service; hence, dataports for this speed are treated separately from those for subrate speeds.

Field studies of the performance achieved by T-carrier facilities[1] indicate that a significant number of them , if used to carry DDS channels, will fail to meet an *overall* quality objective of 99.5-percent error-free seconds. T-carrier lines are designed and engineered for a

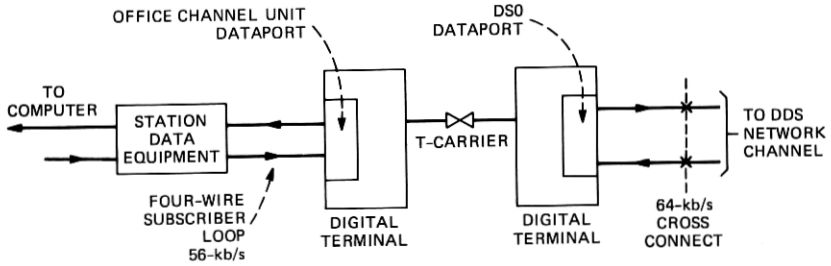

Fig. 1—Basic dataport application.

bit error rate of around 10^{-6} for 95 percent of the systems. This is more than adequate for voice grade services. Major alarms do not appear until the error rate has increased to approximately 10^{-3}. A much lower error rate must hold to support DDS channels for data transmission; Ref. 2 states that the T-carrier line should appear to have at least 99.6-percent error-free seconds (EFS), and an error rate closer to 10^{-8} is needed to insure this. The 56-kb/s dataports use an error-correcting code that translates an error rate of 10^{-3} to an effective error rate on the order of 10^{-8}. Thus, even a barely functioning T-carrier facility should perform adequately as part of a DDS channel, using dataport channel units with error correcting features. In general, the penalty paid for using of error-correcting codes is the need for additional bandwidth. In the case of 56-kb/s DDS transmission, the data and control information[3] occupies the full usable capacity (64 kb/s) associated with the PCM channel time slot. To gain capacity for error correction, a full extra time slot must be used, since borrowing partial capacity would make that carrier channel unusable for normal service in any case. This dictates that the code will have a rate of one-half (the ratio of information bits to total transmitted bits).[4]

With these considerations in mind, let us look at what a dataport for the 56-kb/s rate must be able to do. It must provide those functions which DDS hardware would perform, while ensuring that the carrier facility will meet error-rate requirements. Consider the simplest dataport application, shown in Fig. 1.[5] The DDS network furnishes a channel, working at 64 kb/s ("DS0" rate) to a D4 terminal. A "56-kb/s digital signal zero (DS0) Dataport" conditions this signal for insertion into the digital signal one (DS1) bit stream, which is transmitted over the digital line to the far terminal. At this point, the "56-kb/s Office Channel Unit (OCU) Dataport" removes the signal from the DS1 stream and performs the rate conversions necessary for transmission to the station at the subscriber bit rate. (Reference 6 discusses synchronization to the DDS network clock.) There are several "building block" functions to be implemented (see Fig. 2). Working

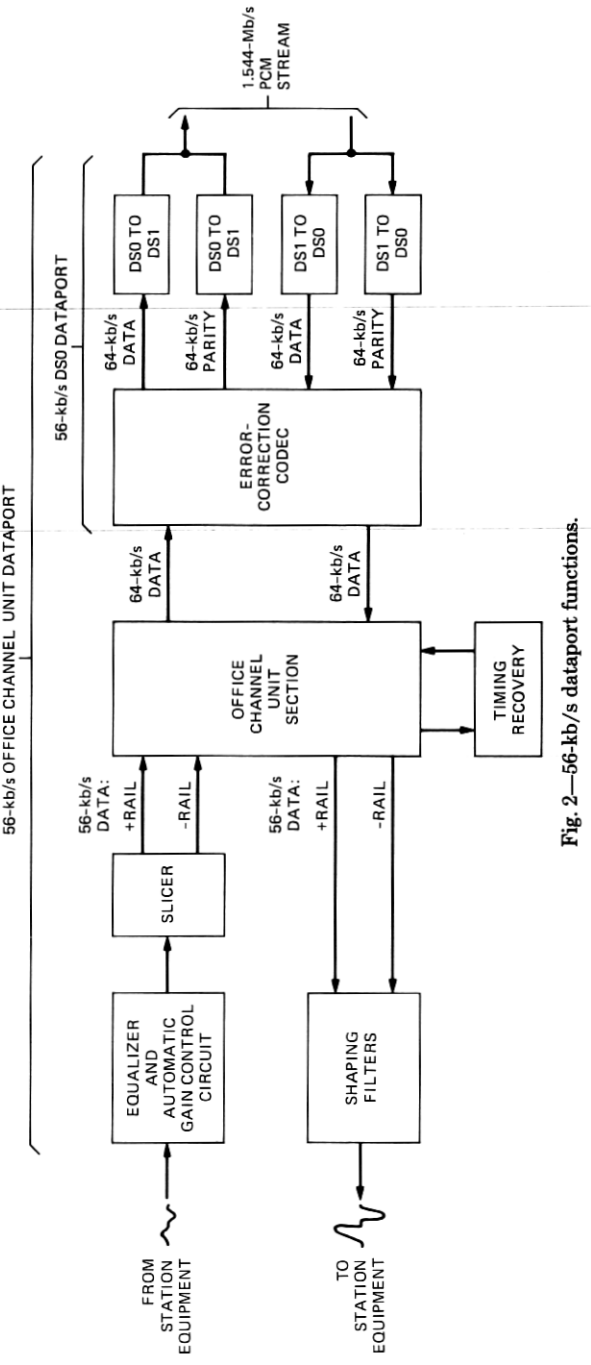

Fig. 2—56-kb/s dataport functions.

from the station toward the network, the pulses arriving from the customer premises equipment must be equalized and amplified to compensate for the loss and dispersion of the cable. The slicer returns the pulses to digital-logic-level signals, and the timing recovery circuit samples the bits and retimes the data. The "office channel unit" section (terminology from DDS[7]) builds the 56-kb/s data signal into the 64-kb/s network signal format. The coding logic processes this signal to obtain the wideband, redundant signal (128 kb/s) for transmission over the carrier. The DS0-to-DS1 interface places this signal into two channel time slots on the 1.544 −Mb/s PCM stream. Transmission from network to station reverses the sense of these functions, except that in this direction filters merely shape the 56-kb/s pulses as they come from the OCU section (since timing recovery is not needed).

Thus, the "56-kb/s DS0 dataport" is implemented with only the error correction and "DS0-to-DS1" blocks, while the "56-kb/s OCU dataport" requires all of the Fig. 2 blocks. Designs for these basic building blocks involve techniques from many fields. Linear and nonlinear "analog" circuits are needed, as well as sequential and combinational digital functions; information theory must be called in as well to implement the error-correction code. Let us look at the building blocks in more detail, progressing from the station equipment toward the DDS network.

II. SUBSCRIBER LOOP INTERFACE

The station uses standard DDS equipment, such as the channel service unit (CSU) or the data service unit (DSU).[7] Figure 3 depicts the dataport line circuits for station-to-network transmission. This circuitry processes pulses arriving from the subscriber loop at 56 kb/s. The second-order filter is in series with a first-order low-pass filter in the network-to-station link, forming a third-order Butterworth low-pass filter with a cutoff frequency 1.3 times the signaling rate. These filters are used to increase noise immunity and to provide pulse shaping.

The local loops are metallic wire pairs of various gauges; their insertion loss is a function of frequency, length, and environmental conditions. An adaptive equalizer compensates for the resultant shaping; it has a variable flat gain and a movable real zero, controlled by the variable resistance of a junction field-effect transistor (FET). Feedback keeps the peak amplitude of the equalized signal at a fixed level at the input to the slicer, this being the ±1.5V pulse amplitude transmitted from network to station.[7] The slicer acts as a comparator with a reference at one half the pulse amplitude, hard-limiting the rectified signal to logic "one" or "zero". This makes it suitable for digital processing. Logic ones retain their identity as having been

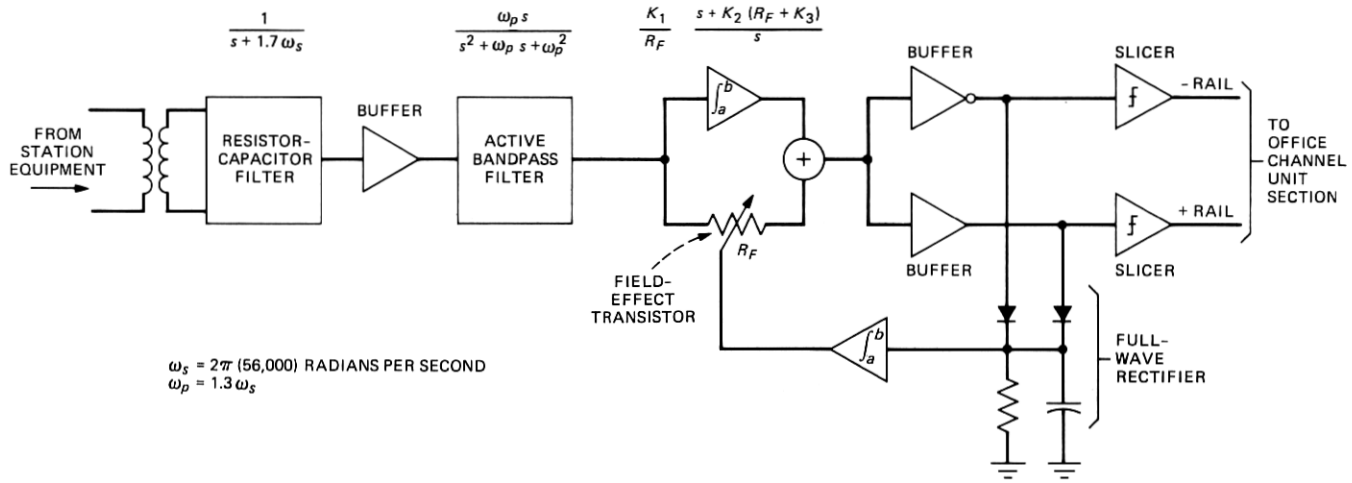

Fig. 3—Station-to-network equalizer and slicer.

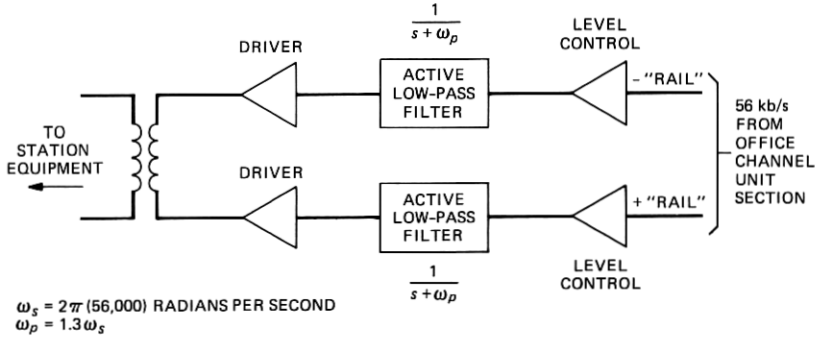

Fig. 4—Network-to-station shaping circuit.

positive or negative pulses by the use of two separate "rails" or leads. In this way, violations of the bipolar encoding rule can be detected.

In the network-to-station direction, data arrives at 56 kb/s from the OCU section, having the aforementioned dual-rail format. Figure 4 shows this circuitry. The level shifter converts the transistor-transistor logic (TTL) signal to a fixed voltage level, appearing as a voltage source to the filters. The line drivers isolate the filters from the variable line impedance and drive the dual-rail signal into the transformer, producing the bipolar signal for transmission over the cable pairs.

Parts of the filter and equalizer circuitry are combined within transmission equipment dual in-line packages (DIPS), known as TEDS.[8] The use of TEDS reduces in large measure circuit size and cost, owing to simpler testing and assembly procedures.

III. TIMING RECOVERY

The DDS network and subscriber loop signals are synchronized in frequency, that is, the 56-kb/s loop pulses occur at exactly seven-eighths the rate of the 64-kb/s network signal. However, since the loop has a variable propagation delay, bits arriving from the station data equipment have unknown "*phase*." This timing must be recovered to ensure that the sampling instants occur at the center of each bit interval.

The 56-kb/s dataport has a 5.376-MHz clock that is phase-locked to the 64-kHz network bit clock. This frequency divides by 96 to yield 56 kHz. By momentarily adjusting the divisor to 95 or 97, the phase of the 56 kHz is advanced or retarded by (1/5.376 MHz)/(1/56 kHz) = 1.04 percent (3.75°). A phase comparator views the data relative to the assumed 56-kHz recovered clock to determine when to change the divisor. The comparator translates this phase difference into a voltage, which is applied to a pair of threshold detectors having a reference

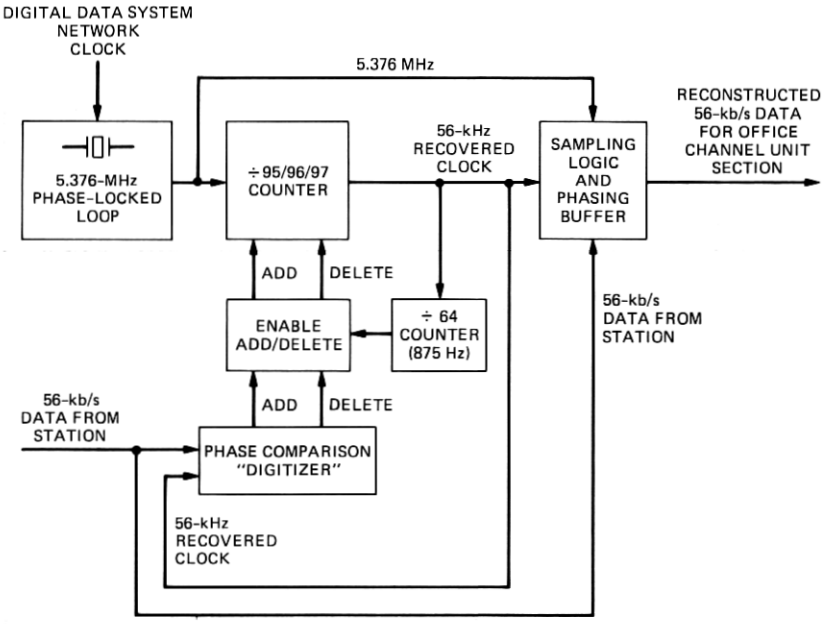

Fig. 5—Timing recovery.

corresponding to approximately four degrees of phase difference. A digital command to add or delete a 5.376-MHz cycle from the present "56-kHz" recovered clock is generated if there are more than eight degrees of phase error. To limit its responsiveness to noise, the system can make only one phase correction for every 64 recovered clock periods (875-Hz maximum correction frequency). Figure 5 summarizes this function. This timing recovery section is, in effect, a "digital" phase-locked loop.

IV. OFFICE CHANNEL UNIT SECTION

The Office Channel Unit (OCU) section provides bidirectional rate conversion between the 56-kb/s subscriber loop signal and the DS0 (64-kb/s) signal and monitors the data stream for control information.[7] The OCU circuitry processes the serial data stream on a byte-by-byte basis, using the DDS bit and byte clocks. This byte structure remains transparent to the customer.

Data on the subscriber loop appears as shaped pulses in a bipolar format. Bipolar encoding ensures that successive data "ones" appear as alternate positive and negative pulses, and "zeros" appear as the absence of pulses during the signaling time interval. Control information is indicated by bipolar "violations", that is, two successive pulses of the same polarity.

Table I—OCU XOV codes in the DS0 to local loop direction

Control DS0 Codes		Name	Definition	Local Loop Code	
*b0**	*b1b2b3b4b5b6b7*			*d0*	*d1d2d3d4d5d6*
Ø	0000001	ZS	Zero Suppression	*b0*	000*X*0*V*
Ø	0011ØØ0	OS	Out of Service	*b0*	001*X*0*V*
0	0101100	LB	Loopback Code	0	010*X*0*V*
Ø	0111ØØ0	TIFP	T1DM Framing Pattern	*b0*	011*X*0*V*
Ø	1001010	—	Reserved	*b0*	100*X*0*V*
Ø	1011010	—	Reserved	*b0*	101*X*0*V*
Ø	1101010	—	Reserved	*b0*	110*X*0*V*
Ø	1111ØØ0	IDLE	IDLE	*b0*	111*X*0*V*
Ø	0101010	OCU	LB	0	010*X*0*V*
Ø	0101000	Channel	LB	0	010100†
Ø	0101100	DSU	LB (DSU on cust. prem.)	0	010*X*0*V*
Ø	0101100	DSU	LB (CSU on cust. prem.)	0	010110†

* The Ø is a "don't care" symbol. The DS0 and loop bits are given the names *b*0, *b*1, *b*2, · · · , *b*7, and *d*0, *d*1, *d*2, · · · , *d*6, respectively.
† dc sealing current is reversed.

The transmit (station-to-network) circuitry collects seven data bits at a time and appends a "one" in the eighth bit position (to indicate a data byte). The resultant eight-bit byte is clocked out at 64 kb/s, the eighth bit being marked by the DDS byte clock.

Detection of bipolar violations causes a mapping of the loop form of a control code to its appropriate DS0 code (see mapping, Table 1), identifiable by a "zero" in the eighth, or control bit position. Loop-side control codes, containing the violations, are seven bits in length.[7] These seven-bit groups may not correspond with the groups being stuffed into DS0 bytes (that is, byte boundaries may not "align" in time). For continuous data, this is of no consequence, but unknown alignment is important when switching between data and control modes. The OCU section assures the transmission of the last bits of customer data, at the expense of loss of the first few (up to six) bits following a control code.

The receive (network-to-station) logic circuitry retimes and reformats the DS0 data stream to 56 kb/s for the loop. Bytes collected are checked for valid control codes. Non-zero data and invalid control codes are encoded into a bipolar pulse sequence. All-zeros data and valid control codes are mapped into their appropriate prefix and a suffix (designated by *X*0*V*),* which will generate a bipolar violation (see Table II).

* This suffix represents three bits; '*V*' is a logic one transmitted in violation of the alternating sign (bipolar) rule; '0' is a logic zero; '*X*' is a bit transmitted according to the normal bipolar rule, chosen to be logic 'one' or 'zero' to ensure that consecutive '*V*' bits occur with alternating signs.

Table II—OCU code map in the local loop to DS0 direction

Label	Loop Code		Second Generation OCU DS0 Code	
	$d0$*	$d1d2d3d4d5d6$	$b0$	$b1b2b3b4b5b6b7$
ZS	∅	$000X0V$	$d0$	0000001
CA	∅	$001X0V$	β†	0010010
LB	0	$010X0V$	0	0100001‡
CB	∅	$011X0V$	β	0110010
—	∅	$100X0V$	β	1000010
—	∅	$101X0V$	β	1111010
—	∅	$110X0V$	β	1101010
IDLE	∅	$111X0V$	β	1111110
No Local Loop Signal§			β	0011110

* The ∅ is a "don't care" symbol.

† The β symbol indicates a "1" for 56-kb/s service. The $b0$ bit is the $d0$ bit if a customer multiplex option is used, and the network and loop byte boundries align.

‡ The 1 in $b7$ is fixed, but the other 1 can appear anywhere in $b0 \rightarrow b6$, depending on relative alignment of loop and network bytes. If a customer remote test option is used and we are *not* already in a network-commanded loopback, then the $0010X0V$ code will be mapped into 00101100 (DSU loopback) to cause a loop on the far-end station equipment.

§ If the OCU receives no signal from the local loop during an interval of time (approximately two seconds), then the indicated code is placed on DS0.

The OCU section interprets certain loopback codes for standard DDS maintenance features. Receipt of "OCU loopback" connects the transmit and receive directions on the loop side, sending the bit stream back toward the network. The "Channel loopback" reverses the polarity of the dc loop sealing current (which is normally circulated through the cable pairs to reduce splice resistance), resulting in a loopback at the loop interface of the station equipment. The "Data Service Unit (DSU) loopback" sends a code recognized by the station equipment and initiates a loop on the side remote from the network (i.e., at the customer interface). Reference 7 discusses in more detail the subscriber loop signal formats, standard DDS loopback commands, and violation coding.

V. ERROR CORRECTION

It has been mentioned that field studies show a need for some form of error correction in the 56-kb/s dataport to ensure that objectives for error performance will be met using any working T-carrier facility. Since voice quality service over T-carrier is reasonably adequate up to error rates near 10^{-3}, major alarms do not appear until the error rate has gone above this threshold. For data transmission, an error rate approaching 10^{-8} is desired. This is a conservative result, based on the error-free second requirements for DDS channels. In the 56-kb/s data-

ports, the error-correcting code allows one to translate a "raw" facility error rate around 10^{-3} to an effective error rate closer to 10^{-8}. Thus, channels of any T-carrier facility that is not in a major alarm condition should, using dataports with error correction, perform adequately as part of a data circuit. The next paragraphs give an overview of the encoding and decoding algorithms used to implement error correction using two 64-kb/s channels. Some background in coding has been assumed.

5.1 Encoding

The (17,9) BCH* code generated by the polynomial

$$g(x) = 1 + x^3 + x^4 + x^5 + x^8, \tag{1}$$

is chosen. Forcing the ninth data bit of the (17,9) code to a zero and not transmitting it shortens the code to a (16,8) code.

If the eight data bits to be encoded are given by

$$\{a_0, a_1, \text{———}, a_7\},$$

define the polynomial $a(x)$ as,

$$a(x) = a_0 + a_1x + \text{——} + a_7x^7. \tag{2}$$

Then, define the parity polynomial $p(x)$ as:

$$p(x) = x^8a(x) \bmod g(x), \tag{3}$$

the right-hand side of which means the remainder left when $x^8a(x)$ is divided by $g(x)$. Since there are eight parity bits for eight data bits, the parity rate is also 64 kb/s, enough to fit into a channel time slot.

It can be shown that the natural length[4] of the polynomial $g(x)$ is 17, i.e., 17 is the smallest integer i such that

$$x^i \bmod g(x) = 1. \tag{4}$$

Hence, it can be shown[4] that the code word

$$c(x) = p(x) + x^8\, a(x) \tag{5}$$

is an element of a cyclic code. For this particular $g(x)$, the cyclic code is a 2-QP (Quasi-Perfect)[4] BCH code and is, hence, optimum for the numbers (17, 9).

In general, $p(x)$ can be generated by feedback shift registers,[4] but can also be generated by a combinational network using the following result:

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* Bose-Chaudhuri-Hocquenghem (BCH) codes are a class of cyclic codes discovered in 1959–60. The designation (n, k) for a binary code indicates that an n bit codeword is transmitted for every k data bits encoded.[4]

$$p(x) = x^8 a(x) \bmod g(x)$$
$$= \sum_{i=0}^{8} a_i x^{8+i} \bmod g(x). \tag{6}$$

Noting that $a_8 = 0$ in this case, and expanding $x^j \bmod g(x)$, for $j = 8, 9, \cdots, 16$, after suitable manipulation,[9] eq. (6) becomes

$$\begin{aligned} p(x) = {} & (a_0 \oplus a_3 \oplus a_4 \oplus a_5 \oplus a_6) && + \\ & (a_1 \oplus a_4 \oplus a_5 \oplus a_6 \oplus a_7)x && + \\ & (a_2 \oplus a_5 \oplus a_6 \oplus a_7)x^2 && + \\ & (a_0 \oplus a_4 \oplus a_5 \oplus a_7)x^3 && + \\ & (a_0 \oplus a_1 \oplus a_3 \oplus a_4)x^4 && + \\ & (a_0 \oplus a_1 \oplus a_2 \oplus a_3 \oplus a_6)x^5 && + \\ & (a_1 \oplus a_2 \oplus a_3 \oplus a_4 \oplus a_7)x^6 && + \\ & (a_2 \oplus a_3 \oplus a_4 \oplus a_5)x^7, \end{aligned} \tag{7}$$

where $\oplus$ denotes binary addition (EXCLUSIVE OR).

Finally, the data sequence $\{a_0, a_1, \cdots, a_7\}$ has the standard DDS zero code suppression performed upon it, if desired, prior to encoding. The parity sequence, $p(x)$, never needs zero code suppression, as the only data sequence that can result in an all-zero parity sequence is the all-zero data sequence, which is not allowed to occur.

5.2 Decoding

When the code word $c(x)$ of (5) is transmitted, suppose one receives

$$r(x) = c(x) \oplus e(x), \tag{8}$$

where $e(x)$ is the error polynomial. Then error correction essentially consists of making a maximum likelihood decision on $e(x)$. This operation, called decoding, is generally the most difficult aspect of error correction. To begin decoding, $r(x)$ is used to form a remainder polynomial $s(x)$, the "syndrome" of $r(x)$:

$$s(x) = r(x) \bmod g(x). \tag{9}$$

Reference 9 develops a simple technique for decoding the (17,9) BCH code using memoryless decoding and "chains" of syndromes. Figures 6 and 7 define a decoder structure that is shown to be maximum likelihood.[9] In our context, notice that the sixteen received bits (eight data and eight parity) form a code word in the (16,8) shortened cyclic code described earlier. A zero is added as the ninth data bit, and the decoder of Fig. 6 decodes the received word as if it were a code word in the (17,9) BCH code described earlier. It should be noted that when the D4 bank framer recognizes a misframe situation or when a major alarm is raised, the decoder creates an "Out of Service" control code for the subscriber loop.

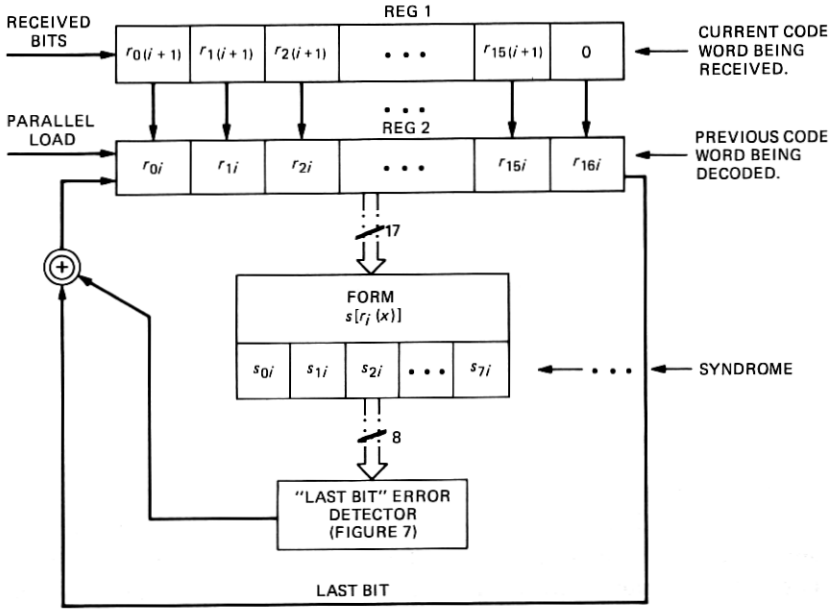

Fig. 6—An implementation of memoryless coding.

5.3 Performance

Given that the (17,9) BCH code is 2-QP and using the decoding strategy outlined in the previous section, the reader can verify that for the (16,8) shortened code the correctable subset consists of the:

(*i*) All-zero pattern

(*ii*) 16 single-error patterns,

(*iii*) $\binom{16}{2} = 120$ double-error patterns

(*iv*) $2^8 - 1 - 16 - \binom{16}{2} = 119$ triple-error patterns.

Thus, the probability of "word" error after error correction is given by

$$P_{we} = \left\{\binom{16}{3} - 119\right\} p^3(1-p)^{13} + \sum_{i=4}^{16} \binom{16}{i} p^i (1-p)^{16-i}, \quad (10)$$

where p is the raw error rate of the T-carrier facility, treating it as a binary symmetric channel.

For $p \leq 10^{-3}$ one finds that

$$P_{we} \doteq 441p^3. \quad (11)$$

Now, words occur at the rate of 8000 per second; and hence the

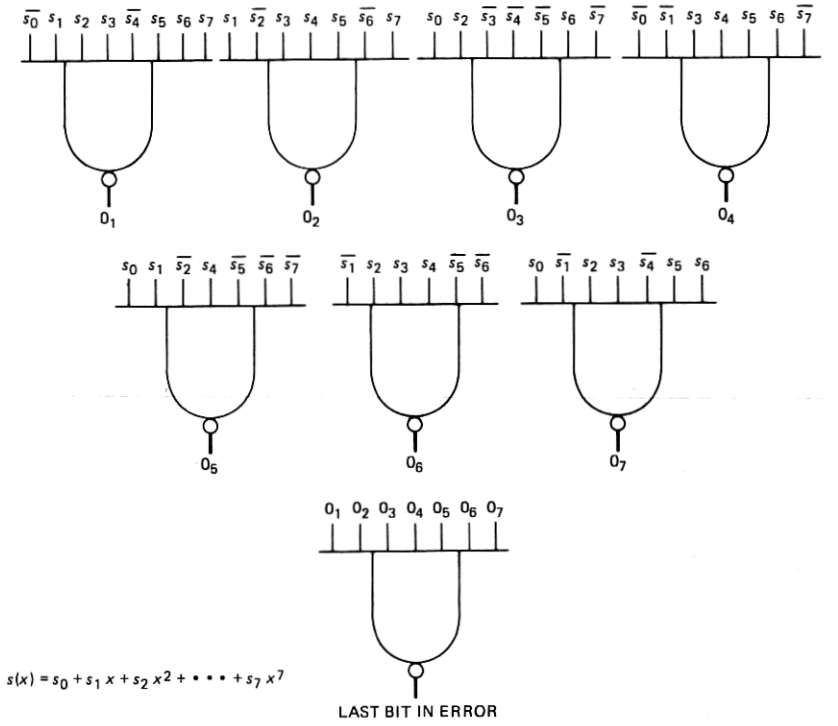

Fig. 7—A realization of the "last bit" error detector.

probability of an error-free second (EFS) is given by

$$P[\text{EFS}] = (1 - P_{we})^{8000}. \tag{12}$$

To compute the effective *bit* error probability, P_e, that will yield the same error-free second count, realize that since data bits occur at 64 kb/s,

$$P[\text{EFS}] = (1 - P_e)^{64000}. \tag{13}$$

Finally, from eqs. (11) through (13),

$$P[\text{EFS}] \doteq (1 - 441p^3)^{8000} = (1 - P_e)^{64000}$$
$$P_e \doteq 56p^3 \quad \text{for} \quad p \leq 10^{-3}. \tag{14}$$

Thus, an error rate of 10^{-3} gets translated to an effective error rate of 5.6×10^{-8}. Substituting this result into (13) yields $P[\text{EFS}] = 0.9964$, or 99.64-percent error-free seconds.

VI. DS0 to DS1 INTERFACE

The DS0 to DS1 interface accepts the two eight-bit words from the coder at 64 kb/s. Each of these words is loaded into a three-register elastic store arrangement identical to the subrate case.[5] The circuitry utilizes the channel sequencing information by which the terminal accepts pulse amplitude modulation (PAM) samples from each voice channel. When the sampling time for the dataport occurs, the unit inserts the longest held eight-bit word from the elastic store into the PCM stream at 1.544 Mb/s. The second eight-bit word (parity) is inserted into a subsequent channel. A counter, using the 1.544-MHz bit clock, determines when the parity word will be inserted, thus allowing that only the first physical channel need be occupied by the dataport unit. The channel position associated with the parity time slot need merely be left unoccupied (or filled with a dummy channel unit). Since each pair of eight-bit words is clocked simultaneously into the elastic store registers from the coder section, each sequential pair that is put within a given DS1 frame corresponds to a 16-bit word from the (16,8) code book. Receiving the data and parity channel from the PCM stream reverses the techniques used when transmitting. Clearly, the time slots used for data and parity must be the same as those selected at the far-end terminal.

VII. PLUG-IN CHANNEL UNITS

Figure 2 groups the functional blocks into two different plug-in channel units for the D4 terminals. The 56-kb/s DS0 dataport includes the two-channel DS0-to-DS1 interface and the algebraic coder for error correction. As such, it serves to place a single DS0 data source into the DS1 stream as one channel or two channels (when the encoding for error correction is used). This interfaces the DDS-format DS0 signals with standard T-carrier. Since the code acts over the entire 64-kb/s time slot, it should be noted that the input data could be multiplexed subrates, the DS0-B signal described in Ref. 3. The 56-kb/s DS0 dataport could be used to provide error correction in this case. The four-wire DS0 input passes through an access point on a faceplate jack, so that testing or loopback is possible at the channel unit, if needed. Driving circuitry for the DS0 office cabling is identical to that used in the subrate DS0 dataport.[5]

The 56-kb/s OCU dataport is more complex and includes all of the Fig. 2 functions; thus, it includes an entire 56-kb/s DS0 dataport as a subset. The 56-kb/s OCU dataport serves a DDS engineered loop,[7] interfacing the loop format with the DS0 format and then with the standard T-carrier. The DS0 signal passes through an access point on the channel unit, enabling access to the midpoint of the circuitry. It is possible to test toward the loop, or near end, or toward the carrier, or

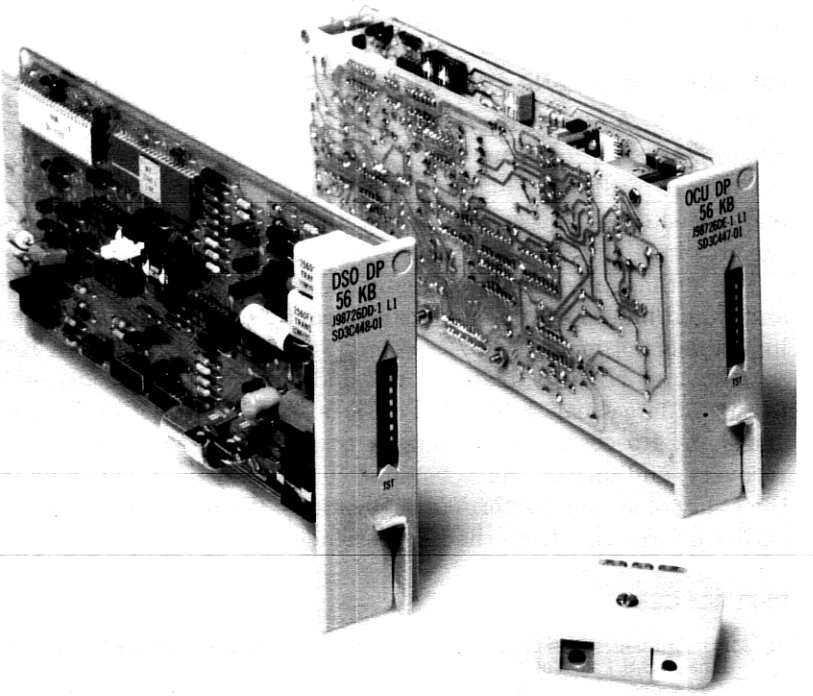

Fig. 8—The 56-kb/s DS0 and 56-kb/s OCU dataports, shown with a test/loopback plug.

far end. A DDS hub office test board[10] may also initiate network loopbacks.

The current available from the channel bank power converter is not sufficient to supply a full bank of dataport channel units or a full mix of dataports and voice units. Consequently, each dataport unit has a dc power supply, fed by the -48 volt office battery. This dc supply is identical to the one used in the subrate dataports.[5]

The units are physically interchangeable with other voice channel units (see Fig. 8, which also shows the test/loopback plug[5]). Two large-scale integrated circuit devices encompass the OCU section (with part of timing recovery) and a conjoint error-correction/DS0-DS1 section, allowing dataport functions to reside within the volume of a D4 channel unit. To serve a data customer, then, the plug-in unit is merely placed in an existing D4 terminal that has been conditioned for network synchronization using the office interface unit (OIU-2).[6] This permits the dataport approach to enjoy economic advantages.[11] Notice

that two 56-kb/s OCU dataports could also provide a *stand-alone* data link over a T-carrier system, independent of the DDS network.

VIII. CONCLUSION AND ACKNOWLEDGMENTS

The 56-kb/s dataports extend the serving area for DDS, and also create opportunities for point-to-point digital data services over existing digital facilities. This is an economical method of transmitting high-speed data over such facilities; it effects ways to keep pace with the growing market for higher bit-rate services.

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