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D4 Digital Channel Bank Family:

Custom-Integrated Circuits for Digital Terminals

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This article describes the design steps for generating custom and semi-custom integrated circuits for digital terminals. The design styles and processing techniques are discussed with special emphasis on the interaction of the device organization with the system organization. Metal-oxide-semiconductor technology makes possible high-packing-density custom integration. Logic conversion is verified by simulation, layout is performed automatically, and timing is verified by using layout information as input to the timing simulator. Gate arrays facilitate semi-custom designing at low cost for modest scales of integration. The same design automation tools are used for both custom and semi-custom integration. Complementary bipolar integrated circuit technology realizes high-performance analog circuitry and can be combined with buried injector logic to integrate both analog and digital circuitry on the same chip. The combination of these technologies offers cost-effective system integration for digital terminals.

I. INTRODUCTION

Custom-integrated circuits offer significant cost savings for system applications. These savings are achieved by using fewer printed-circuit boards, connectors, and less hand wiring, thereby leaving fewer components to test and assemble and requiring less physical space. This article describes three types of custom-integrated circuits: (1) Custom metal-oxide-semiconductor (MOS) very large-scale integration (VLSI), (2) bipolar gate array, and (3) custom-analog complementary bipolar

integrated circuit (CBIC) combined with analog-digital buried injector logic (BIL) bipolar.

The technology for the digital terminals described in this article was determined by the following considerations. MOS technology offers the advantages of a high packing density for a large number of gates. In addition, the complementary MOS (CMOS) option permits chip power dissipation to be very low. Bipolar gate arrays are especially attractive for the use of minimum work force when gate counts are fewer than 1000 and when the volume is low. Both MOS polycells and bipolar gate array layouts permit quick turnaround for design changes. The CBIC is the best means for realizing high-performance analog functions. The CBIC-BIL combination allows digital logic to be put on the same chip with the analog functions, thereby achieving high packing densities. Whatever the technology choice, the effective support of the system organizations by the device organization has led to a rapid growth of custom large-scale integration (LSI) in the Bell System. Close mutual cooperation between system and device organizations is essential for successful integrated-circuit design and manufacture.

This article is divided into three sections. In the first section custom MOS VLSI chips designed for the D4 channel bank, *SLC**-96, and dataport digital terminals are discussed. The design steps from logic design through manufacture are described. In the second section, gate array technology and design techniques are described. This section includes an introduction to the gate array approach and the motivation for using it. The design steps from logic to manufacture are described, along with the various custom chips for the D4 system. The last section describes the complementary bipolar integrated circuit and the buried injector logic bipolar technologies. Examples described include circuits used both in the channel units and the common equipment of several versions of digital banks.

II. CUSTOM MOS VLSI INTEGRATED CIRCUITS

2.1 Introduction to VLSI custom logic

Over the last six years, custom MOS logic integrated circuits at Bell Laboratories have evolved from 1000-transistor LSI chips to VLSI chips containing tens of thousands of transistors. This evolution has been made possible by two major factors—process technology and design aids. Processing advances have resulted in the reduction of the design rules for custom logic chips from 7.5 μm to the current 3.5 μm. Thus, a chip today has approximately one-quarter the area of the corresponding chip six years ago that had the same logic complexity. In addition,

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Table I—Chip statistics

Code Name	Technology	Number of Gates	Number of Transistors		Operating Frequency (kHz)	Nominal Power (mW)
			Polycell	Memory		
257A	7.5-μm NMOS	250	850	—	3150	350
257B	7.5-μm NMOS	230	730	—	6300	250
229AC	7.5-μm NMOS	500	1580	—	1544/1576	425
229AA	5.0-μm NMOS	1300	4380	—	2048	450
229AB	5.0-μm NMOS	2300	8500	—	1544	445
229AD	5.0-μm NMOS	1960	6000	—	1544	650
257D	5.0-μm NMOS	850	2980	—	56	410
257B	5.0-μm CMOS	2000	7000	—	1544	8
229AG	5.0-μm NMOS	760	2900	—	1544	310
229AR	3.5-μm NMOS	1000	3330	—	4	150
229W	5.0-μm NMOS	600	3020	7200	1544	580

the change from P-channel MOS (PMOS) to depletion N-channel MOS (NMOS) or CMOS has improved the speed performance and reduced the chip power dissipation dramatically. Accordingly, system designers working with transistor-transistor logic (TTL) chips have found it particularly advantageous to cost-reduce their systems by replacing TTL dips and PC boards with a single custom integrated circuit (IC). Besides the obvious reduction of parts, cost savings are achieved by reduced labor costs, increased reliability, decreased system power dissipation, and reduced assembly facilities. Nowhere at Bell Laboratories has this cost reduction been more in evidence than for digital terminals. Eleven custom MOS chips have been designed and manufactured for the D4 channel bank, dataports, and the *SLC*-96 systems (see Table I).

Custom NMOS logic (enhancement and depletion) development at Bell Laboratories has followed NMOS memory development. This strategy has allowed custom NMOS logic chip designs to have the benefit of memory development and fabrication experience; the result is minimal difficulty in achieving high chip yields and high reliability of the custom-designed logic chips with advancing technologies. Both in 5-μm enhancement NMOS and 3.5-μm depletion NMOS, the first logic chips designed in the technology became fully operational without requiring process modifications. Recently, CMOS technology also has become available for custom logic VLSI chips. Currently, 5-μm CMOS custom chips are designed routinely, with 3.5-μm CMOS designs beginning in the second half of 1981.

Custom MOS logic chips at Bell Labs use the polycell design approach. Polycells are predesigned and pre-characterized logic elements (e.g., inverters, flip-flops) that are used to build a function. They all have the same layout height but vary in width, depending on logic complexity. All cell inputs and outputs occur along the cell boundary

at fixed distances called grids. Polycells are laid out according to the appropriate design rules—via interactive layout software in the case of NMOS or by an automatic program in the case of CMOS. The automatic program for CMOS uses symbolic coding to yield polycells that are free of design rule violations. In the case of NMOS, the polycells are thoroughly checked automatically for design rule violations by use of a layout characterization and verification program. For both technologies, programs exist so that all appropriate transistor sizes and capacitances are automatically calculated and put in the appropriate format for circuit timing simulations. In the chip layout phase, the polycells are placed in rows and the layout software optimally connects the appropriate polycell inputs and outputs, leaving a chip pattern of polycell rows and routing interconnections between the rows. Protection input devices, pull-up resistors, and output buffers are placed between chip pads. An example of a polycell chip is shown in Fig. 1. The integrity of the chip design is maintained by having a common connectivity description language, called logic simulation language (LSL),[1] for the design aids (simulation and layout) that describe the logic gates and their interconnections. The result of the polycell approach to chip design is a quick design cycle that is error free and highly flexible for last-minute logic changes.

Logic designs that employ synchronous clocked circuits, minimal gate delays between clocked memory elements (flip-flops and shift registers), RAMs or ROMs, and dynamic logic lend themselves optimally to VLSI chip design. Optimally means race-free, low-power dissipation and smallest chip size. Synchronous design permits various programs to be used to determine large propagation paths before actual timing simulations are run.

2.2 System organization—device organization interface

There are two types of custom MOS design modes—fast turnaround and full custom. In the fast-turnaround mode the system designer does the conversion into MOS polycells and stipulates design validity by simulating it with sequences of vectors. (Vectors are input/output patterns of logic ones and zeros.) After timing simulations are complete, the device organization takes the verified LSL description from the system organization and does the layout, processing, and testing.

In the full-custom mode, the device organization does the conversion to MOS polycells from logic schematics suppled by the system organization. The device organization then proceeds to complete the job in the same way as for the fast-turnaround mode. In either mode, the device designer is available to the system designer for consultation during the front-end system design and conversion to polycells. Also in either mode, a TTL breadboard that is input/output compatible with

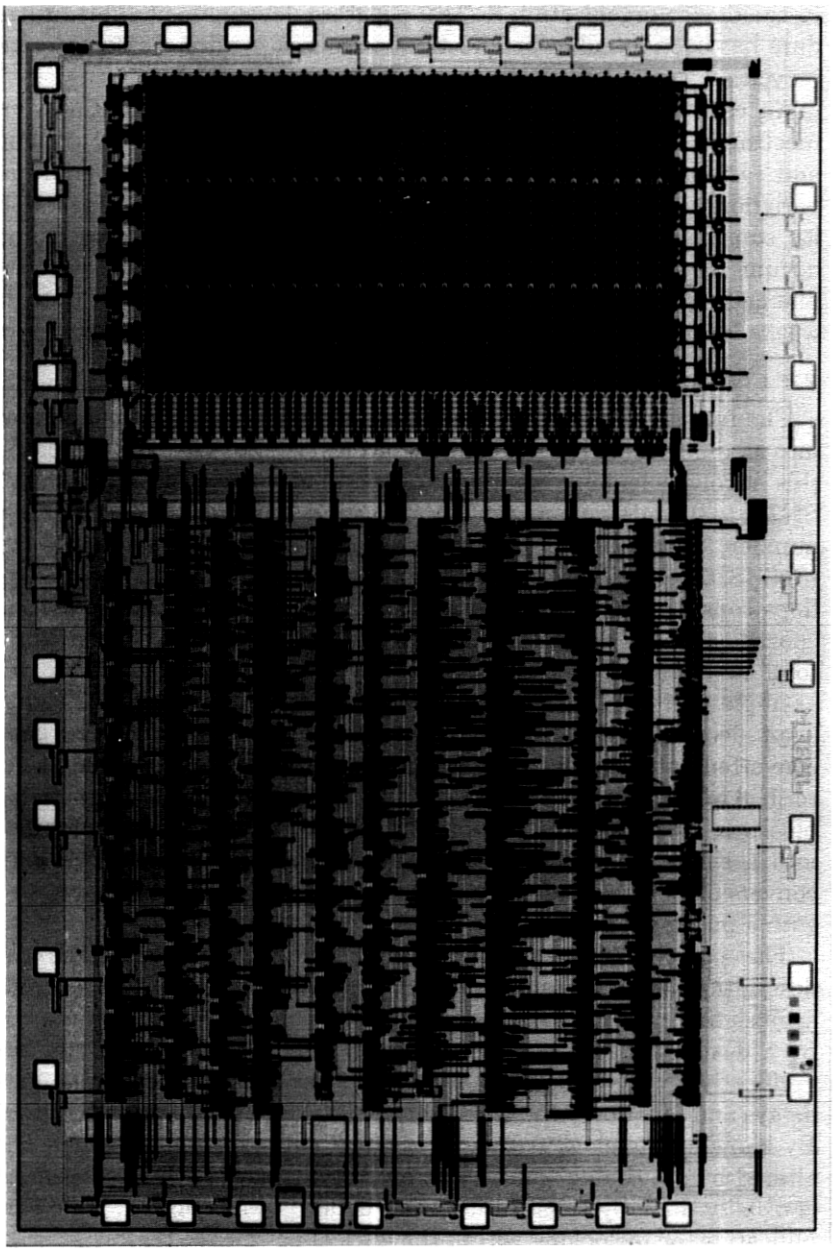


Fig. 1—Typical polycell chip.

the MOS chip and, in some cases, gate-to-gate compatible with the MOS chip, is first verified in the system environment and then transferred to the device organization for test program development. This procedure has been found to be effective in eliminating unnecessary design recycles.

An essential aspect to any custom chip design is an initial joint meeting between the system and device organizations in which chip and system specifications (e.g., frequency, voltage, and temperature variations), functional description of the system, package and testability considerations, and work force and schedule are discussed and documented. Typical current schedule times for first-model dual in-line packages (DIPs) are 8 to 12 weeks for fast turnaround and 12 to 24 weeks for full-custom DIPs.

2.3 Chip design

The first step in chip design is the conversion of the logic diagrams into MOS polycells. If the diagrams are in TTL (as is usually the case), this involves looking up the part number in a TTL catalog (e.g., SN74S163) and implementing the desired function with a minimal number of gates. For example, a divide-by-13 counter in TTL (SN74S163) consists of about 30 combinatorial gates and four D flip-flops consisting of six gates each. The equivalent MOS representation consists of four combinatorial gates and four dynamic registers, for a total of 12 MOS gates and seven polycells. It is evident from this example that the MOS representation of TTL usually involves a significant decrease in gate count. After the logic diagrams have been converted to MOS polycells, the connectivity of the polycells is described in LSL, usually according to functional blocks. These functional blocks are considered as subnetworks of LSL coding that are combined into a single network describing the entire logic design. The logic conversion is given additional logic to ensure that the chip is testable with a minimum number of test vectors.

The polycell conversion is then verified by simulating the LSL description with vector sequences and checking the MOS outputs against the known TTL outputs. This checking is done automatically by a design aid that compares the TTL and MOS vectors. After the verification, other programs are run on the LSL that determine gate delays and fanouts of the gates between clocked flip-flops or registers. By knowing the clock frequency, critical paths can be identified and altered before timing simulations are run. Critical-path improvement is usually done by substitution of a higher power polycell, logic simplification, or reclocking within the critical path.

Timing simulations are done by three types of simulators: (*i*) detailed timing, (*ii*) multiple delay, and (*iii*) mixed mode. Detailed timing takes into account all capacitance, voltage, and temperature effects and is

simulated on a user-selected time step. The multiple-delay simulator ascribes a rise and fall time delay parameter (in ns/pF) for different gate types. The determination of a gate's input and output capacitances then yields appropriate delay in ns. This permits an accurate yet much faster simulation than the detailed-time simulator. The mixed-mode simulator permits a design to be simulated before all of it is converted to MOS. Thus, MOS devices, logic gates (e.g., NAND, NOR), and functional elements (e.g., memory) can be simulated simultaneously. Options under the mixed-mode simulator include a unit delay (no capacitances or voltage or temperature effects) and detailed timing (all capacitance, voltage, and temperature effects). Hence, critical paths can be simulated in the design phase with timing while other paths can use unit delay. Chips containing thousands of MOS gates and tens of thousands of transistors are routinely simulated en masse.

The layout of the chip usually begins after the MOS LSL is unit-delay-verified. Functional block sizes are calculated, tentative input/output pad positions are determined, clock, data bus and power bus distributions, and critical paths are considered in an initial polycell placement. The design aids determine the final position of each polycell by reflecting and exchanging the cells in each row to reduce the routing area between polycell rows. All routing capacitances are then automatically calculated and the designer compares each signal loading to the values estimated in the pre-layout simulation. Post-layout simulations may be judged necessary, depending on the results of this comparison. The layout is completed on an interactive layout system by connecting input and output buffers to pads, adding pull-up resistors, and finishing power bus routing. A final design rule check of the entire layout is made with a design aid before masks are made by EBES,[2] an Electron-Beam Exposure System.

Custom MOS logic chips are fabricated at Western Electric in Allentown, Pennsylvania. Typical processing time for MOS wafers is less than six weeks. Several wafers are returned to the chip designer for testing on the SENTRY test sets. The program to test the chip is written by a test engineer who has a TTL breadboard. The *same vectors that simulated the chip* are applied to the breadboard to ensure validity of the logic design and permit debugging of the test program. Assuming that the chip passes the sequences on the SENTRY test set, packaged models (DIPS) can be delivered to the system organization within a few days for evaluation. Once the system organization approves the chip operation, Western Electric begins production.

2.4 Digital integrated circuits: statistics and system impact

2.4.1 D4 channel bank

Three custom MOS chips have been made for the D4 channel bank. They are referred to by Western Electric code name as the 257A, 257B,

and 229AC. The 257A and 257B replace six digital logic transmission equipment DIPs (TEDs) in the TTL version of the D4 transmit unit. In particular, the 257A provides all of the digital processing necessary to sample and encode each voice channel into 8-bit pulse code modulation (PCM) words. The 257B multiplexes the 8-bit PCM words together with framing bits into a single 1.544 Mb/s digital bit stream. The 229AC replaces four logic TEDs in the TTL version of the D4 receive unit. The 229AC in conjunction with a divide-by-24 counter decodes a 24-bit stream into signals that are used by a digital/analog (D/A) converter. The 229AC also provides signals for use in the receive side of the D4 bank for signaling and alarm functions. The wide usage of these chips has made necessary a design for foreign systems, referred to by Western Electric code name 229AA.

2.4.2 Dataport

Four custom MOS chips have been designed for dataport application. One, the 229AB, consists of a transmit portion, which inputs 8-bit bytes at the DS0 rate (64 kb/s) and outputs the same 8-bit bytes at the DS1 rate (1.544 kb/s), and a receive portion, which inputs 8-bit bytes at the DS1 rate and sequentially outputs the 8-bit bytes at the DS0 rate. A feature of the receive portion is a 3-out-of-5 majority gate error correction circuit, which substantially reduces the effect of facility line errors.

The 229AB is analogous to the 229AD. This chip is used for 56 kb/s data and requires its own error-correcting scheme. (The DS0 function for the subrate dataports has to be modified for 56 kb/s.) Also available is a recent CMOS version of the 229AB, designated as 257F.

The 229AB, together with two other chips, the 140H and 140J, combine to form a 64-kb/s Office Channel Unit Dataport (OCUDP). This dataport permits data from the T-line at 1.544 Mb/s to be converted to and from data at the Digital Data System (DDS) subrate speeds (2.4, 4.8, or 9.6 kb/s). The 257D contains all the digital logic and control functions for a 56-kb/s Office Channel Unit (OCU). In particular, it performs bidirectional rate conversion between the user's rate (56 kb/s) and the DS0 rate (64 kb/s) and monitors the data for control information. This chip, combined with the 229AD, yields a 56-kb/s OCU dataport.

2.4.3 Subscriber loop carrier (SLC-96) system

Three custom codes have been designed for the *SLC*-96 system. The 229AG data link chip replaces the transmit and receive sections of the Data Link Unit (DLU) of the *SLC*-96 system. The transmit section generates control signals and clocks to multiplex data bit streams from the Alarm Control Unit (ACU), the Line Switch Unit (LSU), the Channel

Test Unit (CTU) and the Time Assignment Unit (TAU). The receive section demultiplexes the incoming datastream to these four units. The 229AR data link multiplex chip enables line switch, alarm, channel maintenance, and concentrated information to be transmitted to each of two 48-channel remote *SLC* terminals. The 229W, Time-Slot Interchange (TSI) chip for the TAU digitally concentrates two standard 1.544-Mb/s PCM bit streams into a single stream with a full-access time-slot interchange function. In the transmit mode, any one of the incoming 48 channels can go out on any of the 24 outgoing trunks. In the receive mode, any one of the incoming 24 trunks can go out on any of the 48 outgoing channels. The on-chip scratch pad memory, which sets up the desired trunk connections and busy-word assignments, is written and updated through microprocessor-compatible address and data ports.

III. GATE ARRAYS

3.1 Gate array technology

If more circuitry is placed on an integrated circuit chip, fewer and simpler circuit boards are required. This results in a lower cost, better performing system that enters the marketplace sooner. The scale of integration has an impact in two ways. First, board space is saved over small- or medium-scale catalog logic parts. Second, and more important, if the system can be designed the first time to take full advantage of LSI, it results in a more nearly optimal design. Moreover, significant performance advantages accrue from the use of larger scales of integration. Approximately 80 percent of total system delays are associated with board and connector capacitance. By moving more of the interconnect wiring onto the silicon chip, these delays are greatly decreased, as is the power required to drive these on-chip lines. Higher scales of integration can be used when there is sufficient production volume to amortize the development cost. The alternative is the use of general-purpose small- and medium-scale-integrated catalog parts having a small amount of circuitry. There are relatively few general-purpose catalog parts at high levels of integration, owing largely to the difficulty of defining suitable LSI parts. Gate arrays provide a low-cost, fast-development-time alternative to LSI.

The emphasis in gate array design is on fast turnaround and low user risk. These objectives are accomplished by flexible and conservative generic chip design and an extensive computer-aided design (CAD) support package.

3.1.1 What is a gate array?

A gate array chip consists of digital circuit elements prefabricated on a silicon wafer. The circuit elements are logic primitives, typically

NAND gates, interconnected to accomplish the desired logic function. The processing steps prior to the interconnection levels are the most difficult and time consuming, while the metal wiring deposition is performed quickly. Bell Laboratories has designed a number of gate array generics (basic prefabricated wafer) for various types of applications. These range in size from 22 gates to 1000 gates and in speeds up to more than 40 MHz.

3.1.2 An I^2L gate array

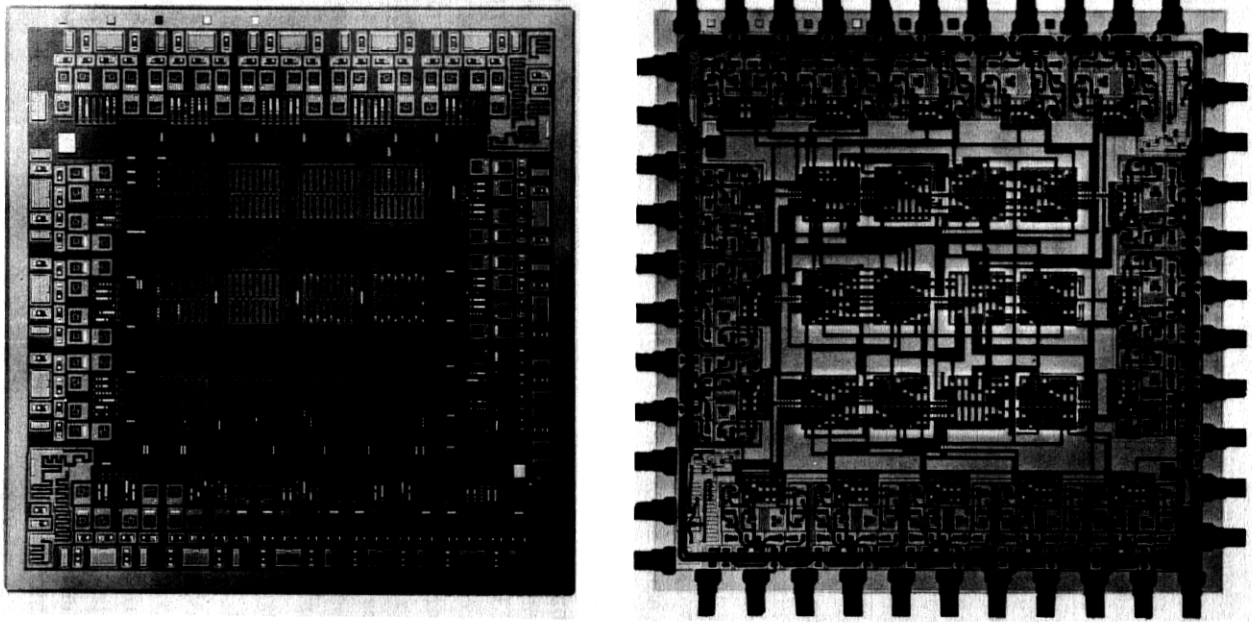
The D4 gate array before and after customization is shown in Fig. 2. It consists of 192 Integrated Injection Logic (IIL or I^2L) gates in an internal array and 32 input-output buffers on the periphery. It is fabricated in standard buried-collector, single-level metal technology. Since the array was designed for low-speed application, n+ crossunders are used at lower cost than two levels of metal. Moreover, customizing the emitter diffusion gives added routing flexibility over the cell.

The buffers translate the relatively large voltages and currents required to provide ample system noise margins to the much smaller power levels internal to the chip. Thus, the majority of logic can be done at low power levels (for this array, about 50 μW/gate) while 10-mA line driving capability is maintained. The buffers consist of a collection of npn and pnp devices, which can themselves be programmed to perform different functions at various power levels. Two voltage regulators provide the capability of driving different portions of the array at different powers, providing speed where necessary and saving power elsewhere.

The internal gates on this particular array are divided into 12 groups of 16 gates. This arrangement is advantageous because of the use of n+ crossunders. Connections between rows are made in predefined vertical channels, since the gate diffusions do not allow crossunders in gate areas. Two-level metal arrays are arranged in continuous rows. The array in Fig. 2 superficially resembles a polycell chip, except that a significant amount of interconnect is located on the gates themselves, rather than connecting at top and bottom. In addition, there are relatively large areas of the chip, and many gates, that are unused. This reflects the emphasis of fast turnaround and design simplicity over packing density.

3.2 Array design techniques

The emphasis on fast turnaround, low risk, and large volume of codes requires a heavy dependence on design aids for design and design verification. The chip shown in Fig. 2 reflects this dependence in its structured appearance. The design process for arrays is discussed below. It is emphasized that the same aids are used for all generic



BEFORE
A GATE-ARRAY CHIP CONTAINS
A STANDARD ARRANGEMENT OF LOGIC CIRCUITS

AFTER
CONDUCTIVE PATHS ARE APPLIED TO PRODUCE
A CUSTOM-DESIGNED DIGITAL LOGIC CHIP

Fig. 2—Typical gate array chip.

arrays. Indeed, some of the aids are shared by both custom MOS and bipolar gate arrays.

3.2.1 Functional description and simulation

The system designer provides a logic diagram and a logic description, the latter in Bell Laboratories' common LSL[1] language. The logic is in the form of gate array primitives (NAND) and a hierarchy of functional blocks such as flip-flops and multiplexers. The input-output buffers are also cited in the logic description. The designer also provides a set of test vectors (a truth table), which is a sequence of binary inputs and outputs designed to test for proper chip operation. The vectors are exercised to ensure information transmittal and to generate the test programs as described below.

3.2.2 Layout

Chip layout is accomplished either semiautomatically or manually. On those jobs on which there is high assurance of first-time success, the layout aids perform gate assignment and channel routing. These are accomplished quickly, since for a given generic the domains, the input-output locations, etc., are predefined and much of the time-consuming work is done once, ahead of time. The layout routine for arrays is the same as for custom NMOS polycell.

In many cases there are special layout requirements and the gate assignment and routing are done semiautomatically on an interactive system. A connectivity audit aid examines the mask description for the interconnect levels and compares it directly with the logic description supplied by the customer. It also ensures that inputs and outputs are in the correct locations, and that the power and ground are connected correctly. Only erroneous or missing connections are reported. The connectivity audit aid is central to the manual layout system. It has resulted in almost 100-percent layout confidence, since the comparison is against logic supplied by customer, with no logic translation or transformation.

3.2.3 Testing

The LSL logic description and the truth table supplied by the customer serve as input to a test program generator aid. This aid writes a program for a commercial test set, providing both functional and parametric testing. The former is specified by the truth table, the latter by a table-driven association of input-output buffer generic names and parametric tests. Thus, each buffer is always tested the same way, which gives assured manufacturing yield.

3.2.4 Introduction of manufacture

The design aids are integrated with aids to generate the manufacturing information transmitted to Western Electric, i.e., logic and mask

descriptions, test program, and specifications. In this way manufacture and design are consistent, and information flow is rapid and accurate.

3.3 Gate arrays for digital terminals

A total of 36 codes were designed for digital terminals, 19 of which were for *SLC*-96 systems and 10 for D4 channel bank export market. In both cases system cost and physical space requirements, together with the need for rapid introduction to manufacture, necessitated the use of gate arrays. The experience of D4 is typical of those systems using gate arrays. Eight codes were begun in about one month, using shared resources, with models derived for all in about nine weeks. Change in system requirements led to a delay in starting the last two codes until the time the first eight were delivered. However, during the interval when the last two were being fabricated, system prove-in could be accomplished on the bulk of the system. Two of the codes were modified as a result of the prove-in. All ten codes worked in the system five months after the first was started.

IV. CUSTOM ANALOG AND ANALOG–DIGITAL BIPOLAR INTEGRATED CIRCUITS

4.1 Bipolar IC technology

4.1.1 Introduction

The analog functions in the early D-channel banks were realized first by using discrete devices and later by using small-scale integrated circuits. Although overall performance objectives were met, it was recognized that integration on a larger scale was needed to resolve physical design and interconnection problems. However, it was also obvious that the usual analog integrated circuit process, Standard Buried Collector (SBC), would not be adequate. Two major improvements were required:

(*i*) A pnp transistor comparable in performance to the npn transistor of the SBC process was needed to implement many of the proposed circuits.

(*ii*) A high-density digital technology fully compatible with analog technology would alleviate the interconnection difficulties encountered with separate analog and digital chips.

These objectives could only be met by the development of a new IC process technology. The high-quality pnp transistor was realized by the development of the complementary bipolar integrated circuit technology. This CBIC structure is illustrated in Figs. 3a and 3b. The fabrication process is given in the appendix. The analog/digital capability was realized with the development of buried injector logic, a new device structure available from the CBIC process. Although these new technologies were not developed specifically for digital banks alone,

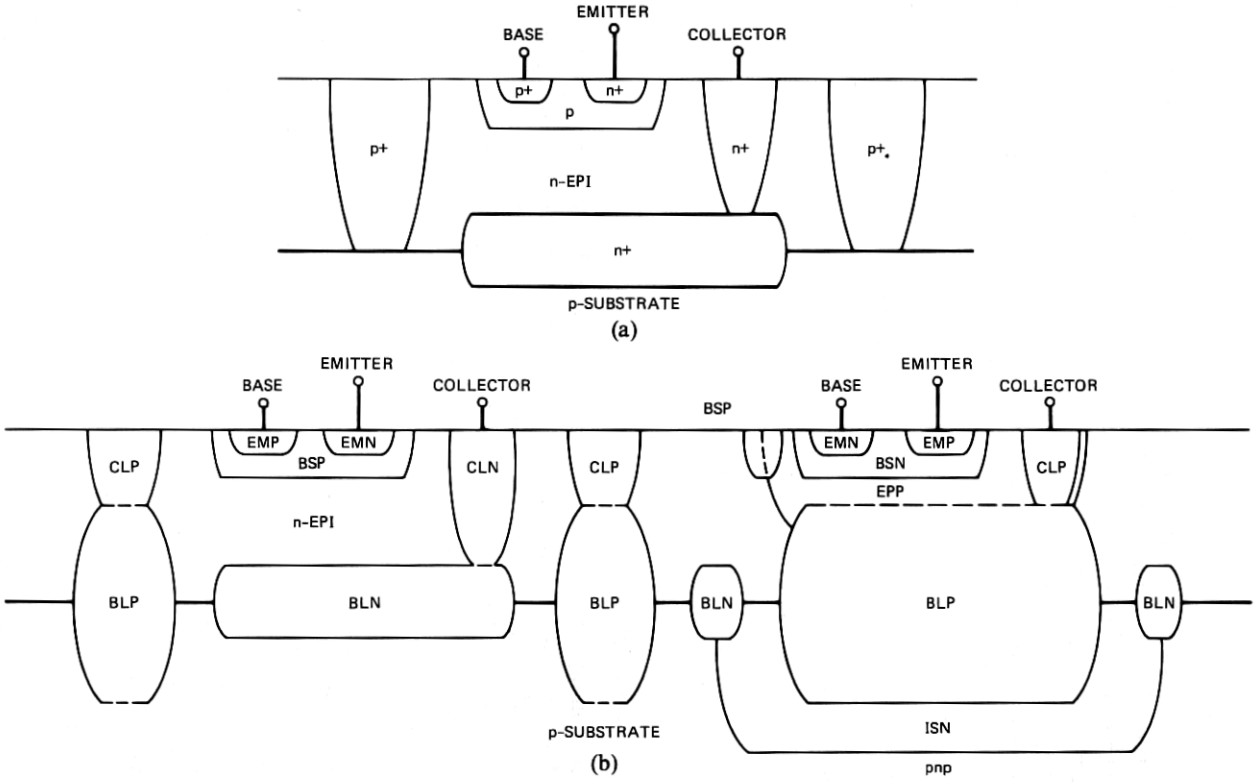


Fig. 3—Transistor cross sections. (a) SBC npn transistor. (b) CBIC npn and pnp transistors.

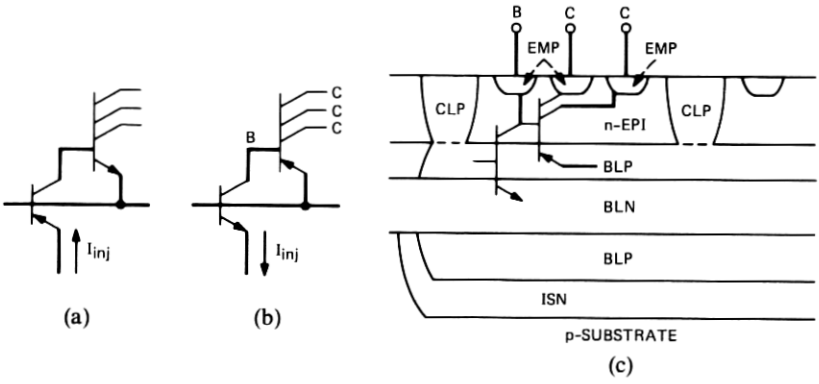


Fig. 4—Injection logic configurations. (a) Schematic representation of integrated injection logic. (b) Schematic representation of buried injection logic. (c) Cross section of buried injection logic.

D4 was one of the first systems to take full advantage of their capability.

4.1.2 Buried injector logic

With the development of Integrated Injection Logic (IIL or I^2L) in the early 1970s, it was hoped that a means for integrating high-performance analog functions and high-density digital circuits on the same chip had been obtained. Unfortunately, the process requirements, particularly epitaxial layer requirements, for I^2L and the analog functions were not readily compatible. However, A. A. Yiannoulos[3] showed that the CBIC process could also be used to obtain a novel form of I^2L. Whereas normal I^2L uses an inverted multi-collector npn switching transistor and a lateral pnp injector, as shown in Fig. 4a, Yiannoulos proposed using a pnp switching transistor and a vertical npn injector (Fig. 4b). The structure is illustrated in Fig. 4c. The n- and p-buried layers and the n-epitaxial layer form a vertical npn injector transistor. The p-buried layer, the n-epitaxial layer, and several diffused pnp emitters form the multi-collector switching transistor. Since the injector transistor is "buried," this type of logic was called buried injector logic (BIL). A major advantage of BIL is that, since the injector is buried, only the signal path interconnections are on the surface, the power being supplied by two buried layers. Thus, gate size, shape, and alignment are essentially unrestricted by power-supply considerations, which lead to very high wiring efficiency. This is illustrated in Figure 5, which shows the layout of a D-type flip-flop. It is interesting to note the variations in gate size, shape, and orientation. The high wiring efficiency compensates for the relatively large size of the BIL gate (compared with I^2L), which is due to the use of the relatively deep

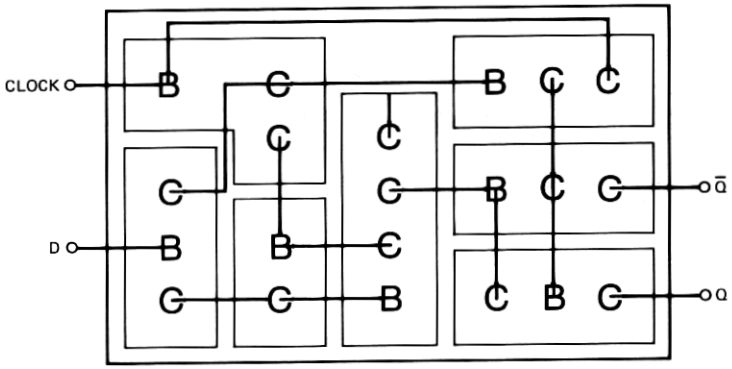


Fig. 5—Layout of edge-triggered D-type flip-flop in BIL illustrating high wiring efficiency.

diffusions associated with CBIC, basically an analog process. CBIC-BIL chips having more than a thousand gates, as well as the usual analog functions, are feasible.

It should be noted that BIL has many of the performance characteristics of I^2L. It is a low-power logic, with a delay power product of less than 1 pJ. However, it is also relatively slow, as is I^2L. Fortunately, many telecommunications applications require large amounts of logic operating slowly—sub-audio rate signaling, for example.

4.1.3 Miscellaneous components

Several other active and passive components normally are provided by the CBIC process. For example, a p-channel junction field-effect transistor (JFET) is obtained by using the pnp collector epitaxial-conversion layer, EPP, for the channel and the n-base for the gate. Two types of resistors are commonly employed—a 200-ohm/square p-base resistor, and an ion-implanted 2000-ohm/square resistor. NMOS capacitors using SiO_2 and the passivation Si_3N_4 as a dielectric are also commonly used.

4.2 Custom integrated circuits for digital banks

In the following sections, three circuits designed specifically for the D4 bank will be described briefly. In each case, realization of the required performance depended on the availability of CBIC technology.

4.2.1 555N Receive Converter

The D4 bank receive converter circuit, designed by C. Crue and H. G. Ansell, derives a clock from the DS1 bipolar-coded bit stream of data and regenerates the data. Deriving a clock from data has previously been accomplished in DS1 and DS1C digital terminal equipment

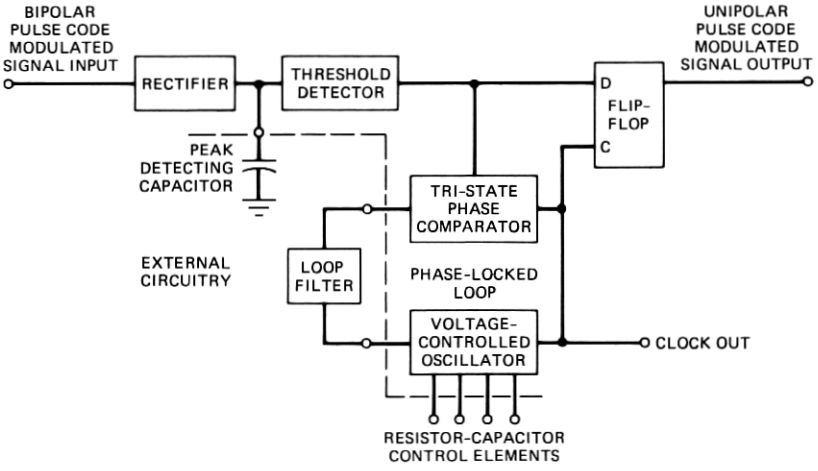


Fig. 6—Simplified block diagram of 555N Receive Converter.

using tuned inductor-capacitor (LC) or crystal circuits. The implementation of such circuits often resulted in awkward physical designs.

To improve the physical design by taking advantage of integrated circuit technology, an RC-tuned phase-locked loop (PLL) approach to clock extraction was taken. The main problem concerned the functioning of the PLL during intervals of logic zeros at the input, intervals that contain no timing information using standard bipolar coding. Reconciling competing requirements on the effective Q of the PLL was another problem, i.e., how to make the Q sufficiently large to suppress jitter, yet sufficiently small to capture the signal.

To solve the first problem, a tristate gate was used as a phase comparator in the PLL. The second problem led to a compromise in the selection of the effective Q of the loop. Figure 6 shows a block diagram of the silicon integrated circuit (SIC) realization of this circuit, the 555N Receive Converter. The loop filter and the indicated RC elements are external to the IC. The PLL consists of the voltage-controlled oscillator (VCO), the phase comparator, and the loop filter. When the input to the receive converter is a logic zero, the tristate-phase comparator ideally has zero output current, the loop filter capacitor holds its charge, and the VCO continues at its previous frequency. The PLL design includes temperature compensation for both the free-running frequency and the loop gain. In addition, this circuit also includes maintenance circuitry and an option allowing automatic shutdown of the output for no input. It operates at 5 volts and 35 mA.

The 555N Receive Converter is fabricated on a 2.8 x 2.8 mm chip using CBIC technology.

4.2.2 608D Sample-and-Hold / Comparator

The successive approximation analog-to-digital converter used in the D4 bank requires several component parts: a sample-and-hold circuit, a digital-to-analog converter, a comparator, and logic to generate the successive approximations. The 608D Sample-and-Hold/Comparator, designed by F. W. Crigler, J. J. Nahas, and D. A. Spires, performs two of these four functions along with an additional function, automatic zero adjustment.

Figure 7 is a block diagram of the 608D. The circuit is designed to operate with a dual R-2R ladder D/A converter. The comparator connects to the main legs of both the positive and negative ladders. The zero adjustment is performed using the zero adjust block and the field-effect transistor (FET) driver. The remainder of the circuit performs the sample-and-hold function.

The comparator consists of multiple stages of npn and pnp emitter-coupled pairs, resulting in a gain in excess of 84 dB and a delay of less than 75 ns.

The sample-and-hold circuit has both input and output amplifiers. The input amplifier is a sequence of npn and pnp emitter followers. The output amplifier uses a high-input-impedance source-follower followed by a Darlington-connected emitter follower. This amplifier is a single-ended voltage to double-ended current converter. The sample-and-hold switch is a diode bridge driven by positive and negative current sources directed by npn and pnp emitter-coupled pairs, respectively. The switch has a transition time of less than 80 ns.

During the automatic zero adjustment, the FET driver is used to turn on a JFET switch connecting the pulse amplitude modulation (PAM) bus to the analog ground. The zero-voltage input signal is sampled onto the hold capacitor. The zero adjustment system then adjusts the voltage on a second capacitor in such a fashion as to balance the comparator. The voltage on the second capacitor controls the current in the right-hand leg of the hold amplifier and thus adjusts the gate-to-source voltage on the right-hand source follower.

The 2.32- by 2.32-mm circuit is fabricated using CBIC technology with p-channel JFETs.

4.2.3 668A Detector / Sampler Family

The 668A Detector/Sampler integrated circuit family, designed by J. H. Green, S. F. Moyer, P. C. Davis, and J. J. Nahas, controls the timing of both the audio sampling and the sub-audio signaling on D4-bank channel units. A block diagram of the circuit is shown in Fig. 8. The receive and transmit audio sample from and to their respective PAM busses is handled with low-resistance (approximately 80 ohms) on-chip JFETs. The JFETs are switched using a fast, efficient driver that

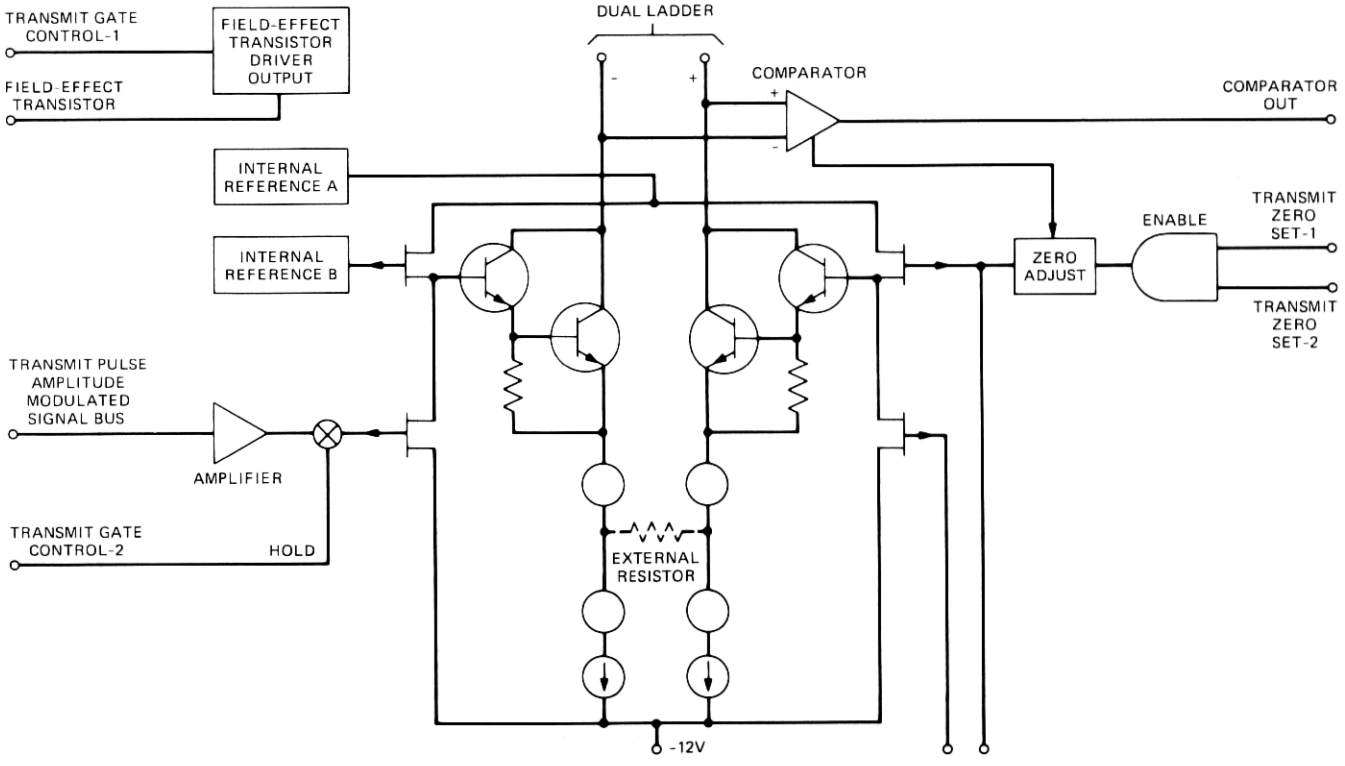


Fig. 7—Simplified block diagram of 608D Sample- and Hold/Comparator.

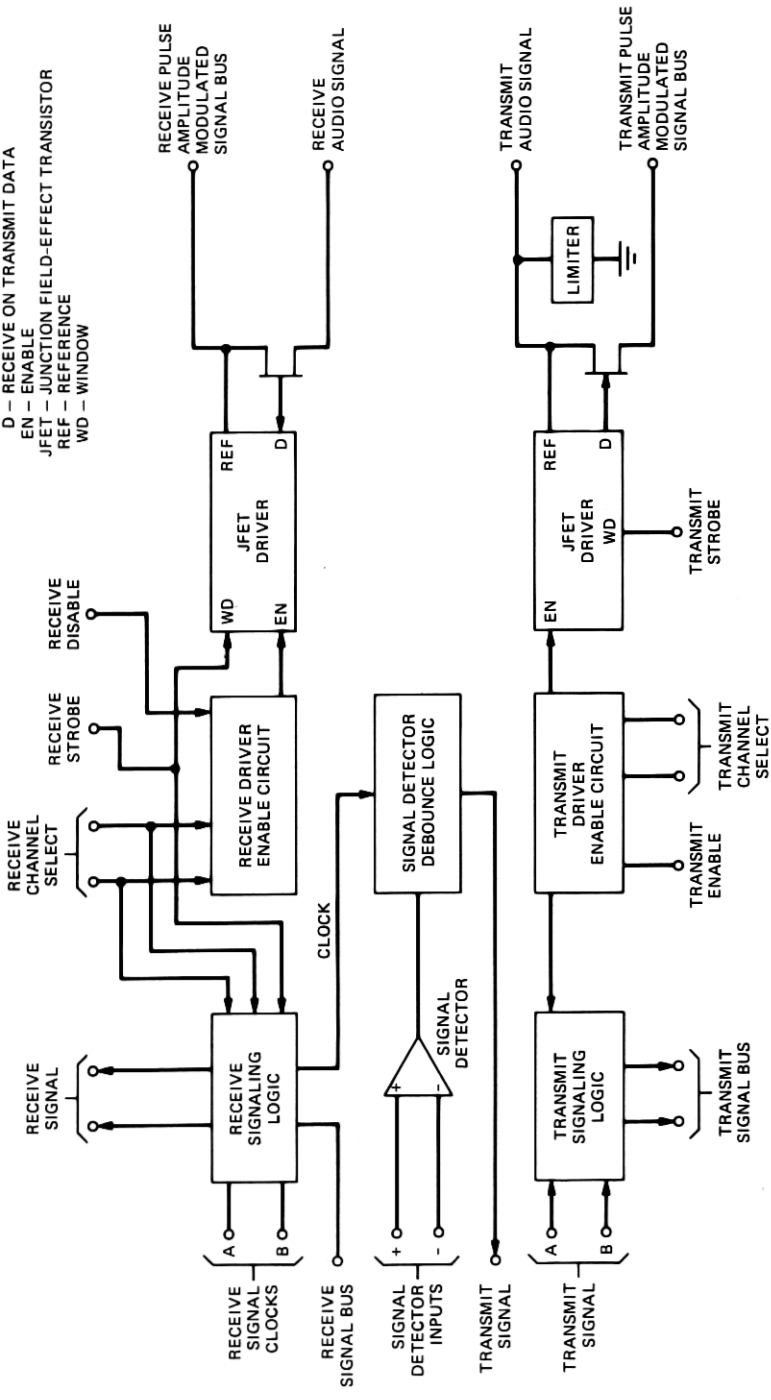


Fig. 8—Simplified block diagram of 668A Detector/Sampler.

can switch the large JFETs either on or off in less than 100 ns using only 1 mA. The JFET drivers have both select and window logic input signals. The high-speed requirements in this portion of the circuit were met using both npn and pnp emitter-coupled logic. In a typical application, the drivers are only enabled for about 4-percent of the time using channel unit selection signals, thus considerably reducing the average power required for the drivers. The sampling window signal occurs within this 4-percent time period.

The channel unit selection and sampling signals clock the receive signaling information into D-type latches. In the case of the primary or A signal, the signal is delayed using two edge-triggered D flip-flops as a shift register to prevent signaling information loss during T-carrier faults. The signaling information is transmitted to a separate off-chip line-reversal circuit.

The transmit signaling is detected using an off-chip resistor network and a simple comparator. The signal from the comparator is debounced, using a digital circuit, to prevent erroneous status signals from being transmitted over the T-carrier system. Simple open-collector outputs are used to connect the transmit signaling information to the transmit signaling bus.

The detector/sampler is a 2.56- by 2.56-mm beam-leaded silicon integrated circuit fabricated using CBIC technology. The relatively slow receive and transmit signaling logic was realized using BIL (approximately 100 gates). A number of variants of the basic detector/sampler have been developed for use in many D4 applications.

V. SUMMARY

Approximately fifty custom-integrated circuits were made for digital terminals by MOS polycells, bipolar gate arrays, or CBIC-BIL techniques. In each case, the circuitry was designed in the technology and design style that was the best match for the particular function requirements. In this manner, the choice of technologies provided a cost-effective system integration capability for digital terminals.

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APPENDIX

CBIC Technology

The structure of a typical npn transistor fabricated using SBC technology is illustrated in Fig. 3a. To fabricate a comparable pnp transistor, a similar structure with a reversal of doping type, n-to-p type, p-to-n type, is required. Thus, to obtain both npn and pnp transistors on the same chip, the CBIC process requires roughly twice as many diffusion steps as does SBC for the npn alone. Using the CBIC npn and pnp structures shown in Fig. 3b as guides, the CBIC process can be briefly described as follows:

(*i*) Buried layers: The npn requires the usual highly doped, n-type buried layer, BLN, which forms the internal collector contact. The pnp requires two buried layers. The first, a lightly doped, deep n-layer, ISN, isolates the pnp collector from the p-substrate. The second is a highly doped p-layer, BLP, which forms the pnp internal collector contact. Notice that the p-buried layer also forms the lower portion of the npn isolation ring.

(*ii*) Surface-to-buried layer diffusions: To make low-resistance connections to the buried collectors, deep, heavy diffusions, CLN and CLP, are used. The p-diffusion of this step, CLP, provides the remainder of the npn isolation ring.

(*iii*) Epi-conversion: The collector region of the pnp is obtained using a light p-ion implant and diffusion, EPP.

(*iv*) Bases: Both the n- and p-bases, BSN and BSP, of the pnp and npn, respectively, are ion-implanted and diffused. Note that the p-base is used to provide a "channel-stop" around the pnp transistor.

(*v*) Emitters: Highly doped, shallow n- and p-type diffusions, EMN and EMP, are used for the emitters and the contacts to the bases.

(*vi*) Contact windows and metalization: Silicon nitride, Si_3N_4, passivation is used with Ti-Pt-Au metallization. All CBIC devices developed for D4 use beam leads to connect to metallized ceramics.

The transistors obtained by this process provide $f_t \sim 300\ MHz$. The current-carrying capabilities of the npn and pnp transistors are comparable, and they are similar in area. It should be noted that since the p-isolation around the npn transistor is obtained from up- and down-diffusions, BLP and CLP, each moving part-way through the n-epi layer, the total lateral diffusion is significantly less than in the case of the single deep diffusion used in the SBC process. Thus, for a given breakdown capability, the base-to-isolation spacing is significantly less with the CBIC process. The CBIC npn transistor area is therefore approximately 25 percent less than its SBC counterpart; i.e., the increase in process complexity is partially offset by a reduction in chip area needs.